CHAMP™-XD2

High Performance Multi-Core HPEC Module based on the Intel Xeon Processor D

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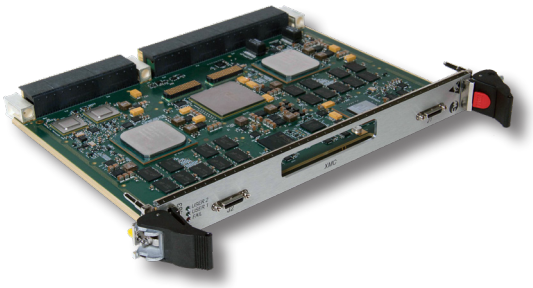

Key Features

- Dual processor Xeon D 8-core (820 GFLOPS @ 1.6 GHz total) or 12-core (1152 GFLOPS @ 1.5 GHz total)
- Extended operating temperature Intel eTEMP SKUs
- PCH integrated in Xeon D SoC
- Four ports of 40G/10G Ethernet or DDR/QDR/FDR10 InfiniBand on OpenVPX data plane
- Native dual KX 1 GigE or KR 10 GigE ports on OpenVPX control plane
- 16 to 32 GB DDR4 @ 2133 mega-transfers per second per Xeon D socket (68 GB/s aggregate)
- XMC PCIe up to Gen3, designed for up to 25W thermal dissipation
- Dual x16 PCIe Gen3 on OpenVPX expansion plane with switch
- Core Function FPGA and IPMI
- Air and conduction-cooled
  - + Contact Curtiss-Wright for Air-Flow Through (AFT) or Liquid-Flow Through (LFT) options
- TrustedCOTS

Applications

- Multi-mode Radar
- Synthetic Aperture Radar (SAR)
- Signal Intelligence (SIGINT)
- Electro-Optical/Infrared (EO/IR)
- Electronic warfare (EW)
- Mission computing
- Industrial server applications

Overview

The 6U OpenVPX™ CHAMP-XD2 rugged digital signal processor (DSP) engine module is designed for use in very compute-intensive Industrial, Aerospace and Defense applications, enabling developers of High Performance Embedded Computing (HPEC) systems to take full advantage of the unmatched performance of today's leading-edge Xeon processor D architecture.

The CHAMP-XD2 combines the high core count and floating-point performance of the latest Intel Xeon D processors with the substantial bandwidth and system-enabling features of the VITA 6U OpenVPX form-factor. Providing a pair of extended temperature Intel Xeon D processors with 8 or 12 core processors each, the CHAMP-XD2 has a peak performance of >800 GFLOPS or >1100 GFLOPS respectively. This is coupled with 32 GB of high capacity DDR4-2133 per processor, with a bandwidth of >17 GBps per channel with two channels per processor.

Supports constant 'no-throttle' operation without XMC up to maximum operating temperature within supported thermal envelope.

For high speed data transport, the CHAMP-XD2 supports 1 Gigabit (Gb) or 10 Gigabit Ethernet (GbE) interfaces along the OpenVPX control plane in addition to 40G/10G Ethernet or InfiniBand® on the data plane. The CHAMP-XD2's XMC mezzanine site (designed for up to 25W of thermal dissipation) adds even more configuration flexibility, with a myriad of mezzanine cards available from both Curtiss-Wright and other industry vendors.

The CHAMP-XD2 is available in a range of ruggedized configurations to deliver optimal performance in the harshest deployed environments, including air-cooled and conduction cooled variants. There is also resident a Core Function field programmable gate array (FPGA) used for Trusted COTS™ security and general purpose I/O in addition to a dedicated Intelligent Platform Management Interface (IPMI) FPGA used for system monitoring and health.

The CHAMP-XD2 is supported by a suite of firmware, Operating Systems (OS), communication Application Programming Interfaces (APIs) and signal processing libraries. In particular, the OpenHPEC™ Accelerator Suite is Curtiss-Wright's software environment of integrated OS with board specific drivers, optimized messaging and data movement middleware, and high performance computational libraries. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright.

Leveraging Curtiss-Wright's extensive 6U OpenVPX ecosystem, the CHAMP-XD2 forms the centerpiece of high core count HPEC system architectures. Other Curtiss-Wright 6U OpenVPX modules available for HPEC configurations include Single Board Computers, Ethernet/InfiniBand Switches and Routers, Graphics Processors, and FPGA-based ADC/DAC modules.

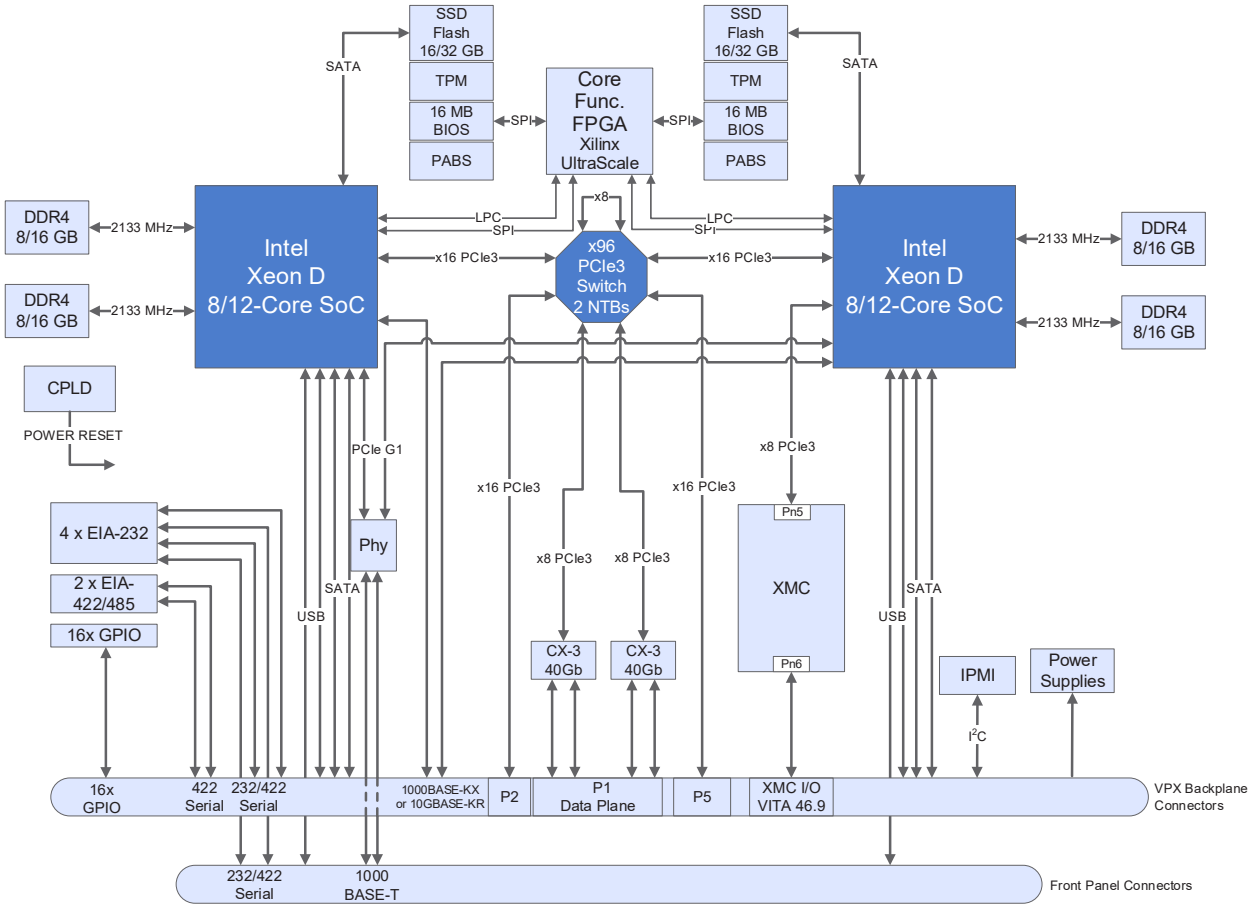

Figure 1: CHAMP-XD2 block diagram

Specifications

Dual processors

- Intel Xeon D SOC Processor with integrated Platform Controller Hub (PCH)
- Extended temp SKUs ranging from 8 (D-1539) to 12 (D-1559) cores and higher (410 to 576 GFLOPS)
- 64-bit
- 45W TDP and 35W TDP packages supported
- 14 nm process technology
- 1.5 MB max last level cache per core
- 2-channel DDR4 memory controller with transfer rates up to 2133 MT/s
- 16-lane PCI Express® (PCIe) Gen3 Interface from each processor to PCIe switch
- Serial ATA (SATA) controller – up to 6 ports, 6 Gb/s support
- Low Pin Count (LPC) Interface between processor and Core Function FPGA
- 4 x USB EHCI host controllers – up to 4 ports, USB 2.0/ USB 3.0
- Serial Peripheral Interface (SPI) – Up to 50 MHz
- SMBus 2.0 up to 100 Kbps
- Enhanced DMA controller – supports LPC DMA
- Integrated GbE LAN controller
- 2 x 10G Ethernet interfaces
- JTAG 1149.1

Volatile memory per processor

- 2 x channels DDR4 SDRAM, 2133 MT/s, 17 MBytes/sec per channel, 2 channels per processor
- Single rank (SDP) and dual rank (DDP) supported
- 8 or 16 GB per channel based on SDP/DDP build option, 32 to 64 GB total per module
- ECC

Non-volatile memory

- SSD – SATA Gen2, NAND Flash, 16 or 32 GB, one per processor node
- SPI Flash for BIOS (16 MB), x 2 including PABS, per processor node
- NVRAM (512 KBytes)

On-board interconnects

- LPC, PCH to Core FPGA, one per processor node
- SPI, PCH to Core FPGA, one per processor node
- TPM, BIOS and PABS route through Core FPGA
- PCH SMBus 2.0/I2C to PCIe switch for field update, node A only
- IPMC FPGA to SMLink (SMBus) interface of PCH for temperature data
- SATA Gen3 to backplane, two ports per each processor node
- PCIe Gen3, processor to PCIe switch, one x16 connection per processor node
- PCIe Gen2, PCH to i210 Ethernet NIC (Gen1 only) and Core FPGA, one per processor node
- PCIe Gen3, two ConnectX3 devices to PCIe switch

Mezzanine site

- One XMC with PCIe Gen2/Gen3 with direct connection to the node B processor
  - VITA 46.9 X38s+X8d+X12d

Peripherals

- 10 GbE
  - 2 x 10GBASE-KR / 1000BASE-KX (backplane, one per node)
- GbE
  - 2 x 10/100/1000BASE-T (one per node, front panel or backplane through build option)
- PCIe
  - 96-lane, 24-port switch
  - 1 x16 PCIe Gen3 ports from each processor to the switch
  - 1 x8 non-transparent port on each processor
  - Up to 2 NTB port supported on PCIe switch
  - x16 from Switch to P2
  - x16 from Switch to P5
  - One x8 from Switch to XMC
- SATA 2.0
  - Solid Disk Drive Flash, one per node
- SATA 3.0
  - Up to 4 to backplane, 2 per processor node

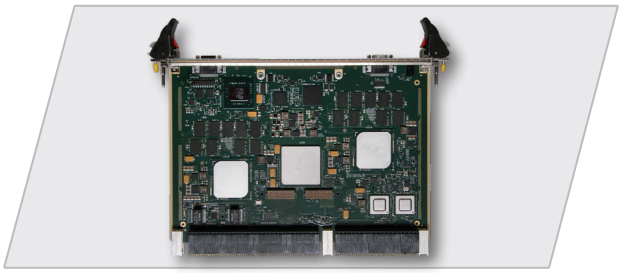

Figure 2: CHAMP-XD2, air-cooled top view

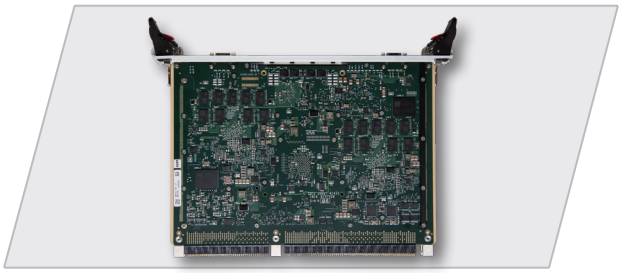

Figure 3: CHAMP-XD2, air-cooled bottom view

Figure 4: CHAMP-XD2, air-cooled metal on, top view

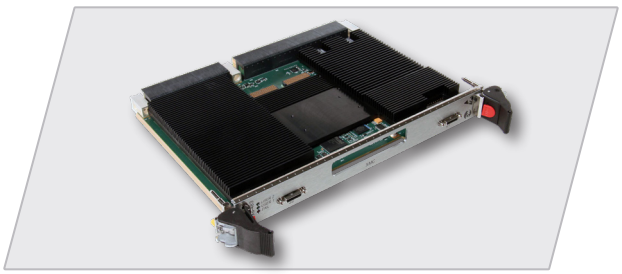

Figure 5: CHAMP-XD2, air-cooled metal on, front view

- USB 2.0
  - 2 x USB 2.0 ports to the front panel, one per processor node
  - 2 x USB 2.0 ports to the backplane, one per processor node
- USB 3.0
  - 2 x USB 3.0 ports to the backplane, one per processor node
- Digital I/O (DIO)
  - Up to 8 x interrupt-capable DIO
  - Up to 2 x differential I/O
- Serial ports
  - 4 x RS-232, 2 x per processor node connected to both the front panel and backplane
  - 4 x RS-422/485, 2 x per processor node

Test headers

- JTAG – available on RTM for programming
- Intel XDP header – for debug only

I2C/SMBus devices

- Temperature and voltage sense integrated into IPMI solution
- Fully compliant VITA 46.11 solution available (contact factory for details)

Core Function FPGA (Xilinx KU035)

- Provides logical hardware services for VPX6-483
- Interfaces to Intel Processor through LPC bus
- Uses Curtiss-Wright common hardware reuse blocks
- Interrupt controller supports serial IRQ protocol
- 4 x 16550-compatible UART serial ports (2 x RS-232 and 2 x RS-422/485) per node
- 1 x internal dedicated 16550-compatible UART serial port (for IPMC comm)
- 1 x watchdog timer per node
- 6 x general-purpose timers per node
- Port 80 registers
- Internal low-latency, high-performance bus switch between processor complex and target
- SPI interface to external TPM/main Flash/PABS
- SPI interface to external NVRAM (accessed through LPC)
- Multi-Board Synchronous Counter (MBSC) using backplane sync/clock signals
- Board configuration/status registers
- Jumper status registers
- 8 channels of Discrete LVTTL I/O (DIO) and 2 channels of Differential Discrete RS-422 I/O (DDIO)
- JTAG I/O port for IPMI FPGA configuration programming
- Reset control (in conjunction with reset CPLD)
- Reset cause registers
- 16 x semaphore registers

IPMC FPGA

- Proven FPGA fabric
- Complete ARM® Cortex™-M3 MCU subsystem
- Flash-based device
- 2 x status LED outputs
- 1 x fail LED output
- XMC status registers
- VPX geographical address status registers
- Field Upgradable Unit (FRU) information storage
- 4 x voltage and 4 x temperature sensors (programmable ADCs)
- UART interface to Core FPGA

CPLD

- Power-up and reset support

Trusted Platform Module (TPM)

- SPI based Atmel AT97SC3205

Mechanical

- Air-cooled Level 0/Level 100
  - >29 CFM airflow recommended to support maximum temperature at maximum power
- Conduction-cooled Level 200

Power

- Max thermal power (max temp, max activity): 160W (12c) / 150W (8c) no XMC
- Typical power @ 25°C:
  - Minimal activity: 75W
  - Moderate activity: 100W
  - Stress: 135W
- Max supported XMC: 25W
- Max current (does not include XMC):
  - 12V = <15 A
  - 3.3V = <0.5A

Software

- Operating system support: CentOS Linux®, Red Hat® Enterprise Linux®, Wind River® VxWorks® 7 (SR0600)
- Additional OS and RTOS support contact Curtiss-Wright for more information
- Communications support via MPI/OFED
- VISPL and Vector Math/DSP libraries
- OpenHPEC Accelerator Suite (includes one module BSP)

Unparalleled PCI Express Flexibility

The CHAMP-XD2 incorporates a massive PEX8796 96 lane/24 port PCIe Gen3 Switch, which contains two Non-Transparent Bridges (NTBs) essential for complex PCIe system-wide interconnect. Sixteen PCIe lanes from each of the Xeon D sockets, 32 lanes from the OpenVPX expansion plane, and 16 lanes from the Ethernet/InfiniBand based data plane all aggregate to the switch. A wide array of partitioning schemes is possible with the PEX8796 providing developers with excellent flexibility in system design.

Superior XMC Mezzanine Support

Considerable attention has been applied to the XMC site on the CHAMP-XD2, which has been thermally designed to handle substantial XMC payloads of up to 25W of thermal dissipation. The Curtiss-Wright XF07-516 XMC for instance contains a Xilinx Kintex-7 in addition to 4 channels of 16-bit, 250 MS/s ADC converters and is quite capable of higher power draw figures. The CHAMP-XD2 can accommodate the XF07-516, which equates to a two Xeon D octal core (or more) processors, Xilinx Kintex FPGA, and 4 ADC channels all in a single 3U OpenVPX slot. This represents just one of hundreds of possible single-slot SWaP-optimized combinations.

Ordering Information

TABLE 1 CHAMP-XD2 VPX6-483-tuvwxyz Ordering Information

PART NUMBER	AVAILABLE OPTIONS
6U form factor	VPX6
Model number	483
t: Cooling method	› **A: air-cooled** › **C: conduction-cooled** › F: air-flow-through (AFT) cooled
u: Temperature range	› 0: 0 to 50°C › **1: -40 to 71°C** › **2: -40 to 85°C** › 5: -20 to 65°C › 9: customized range
v: Mechnical format	› **4: 1.0” pitch, no 2-level maintenance support** › 5: 1.0” pitch, 2-level maintenance support › 6-7: Reserved
w: Backplane I/O	› **A: 4 x 40Gb (Ethernet or Infiniband) to P1)** › **C: 40 GbE Mellanox device not populated** › D-H: reserved › Z: custom configuration
x: Processors	› **0: 8-core Xeon D BGA 35W** › **1: 12-core Xeon D BGA 45W** › 2-9: reserved
y: Memory per CPU	Memory is divided between four banks › 0: reserved › **1: 16 GB** › **2: 32 GB** › 3-8: reserved
z: Ethernet routing	› **0: Base-T Ethernet to the front panel** › **1: Base-T Ethernet to the rear panel** › 2-9: reserved

Note: Bold text indicates available option. Contact factory for specific combinations.

Contact Curtiss-Wright for additional product configurations.

TABLE 2	CHAMP-XD2 Peripherals and Software
PART NUMBER	AVAILABLE OPTIONS
RTM6-483-0000	Rear Transition Module (RTM) for the VPX6-483 board
CBL-483-0000	› I/O break out cable for front panel or RTM of VPX6-483 air-cooled Level 0/Level 100 board, single node › Two cables needed to access both processor nodes"
DSW-483-001-LNX	Red Hat Linux board support package and driver suite for the Curtiss-Wright CHAMP-XD2 (VPX6-483) dual Intel Xeon D 6U OpenVPX board
DSW-483-002-LNX	CentOS Linux board support package and driver suite for the Curtiss-Wright CHAMP-XD2 (VPX6-483) dual Intel Xeon D 6U OpenVPX board
DSW-483-003-VXW	Wind River VxWorks board support package and driver suite for the Curtiss-Wright CHAMP-XD® (VPX6-483) dual Intel Xeon D 6U OpenVPX board
MNT-483-###-xxx	Annual Maintenance for BSP (xxx=LNX or VXW)
DSW-HPEC01-LX-000	OpenHPEC LX Development Suite. Includes BSP, Alinea DDT/MAP, MPI, DataFlow, System Bit (other options available)
DPK-483-SI-000	S-Parameter Toolkit for CHAMP-XD2 high speed backplane signals