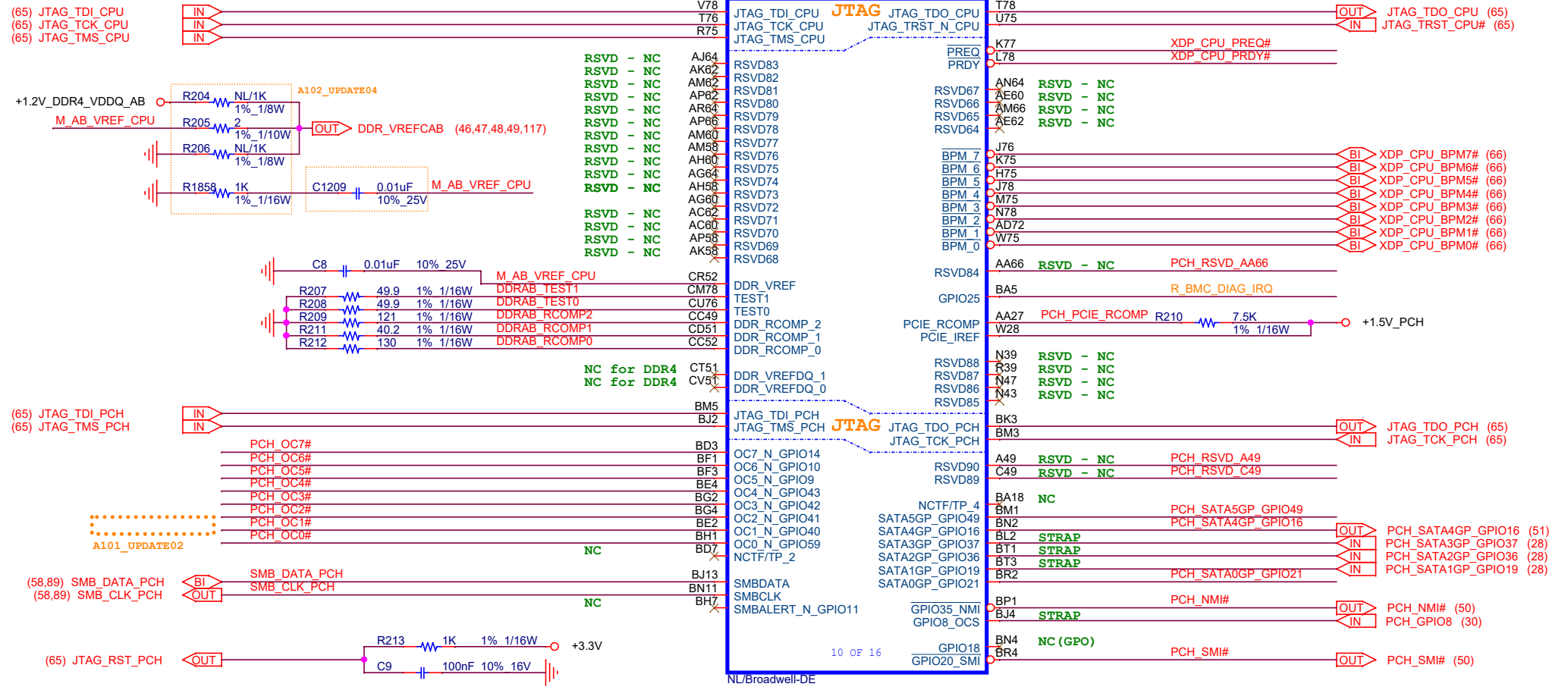


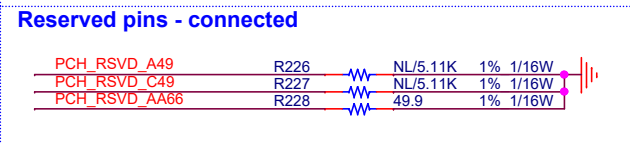
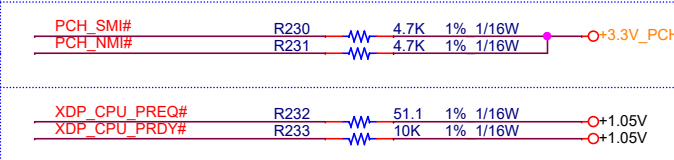
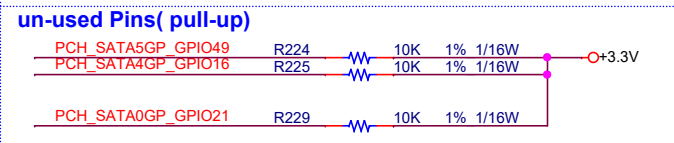
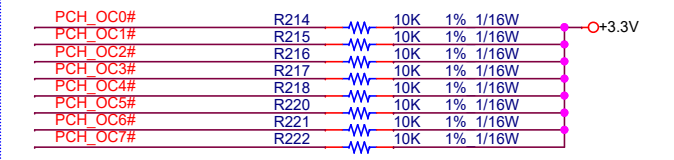
BDX-DE0[JTAG/SMB/GPIOS]



RSVD Reserved pins - no connect

A49	C49	N47	Y33	AE60	AK58	AP58	BP37
A55	C55	N54	Y35	AE62	AK62	AP60	BP56
A66	F69	R39	Y37	AG56	AM55	AP62	BP58
	H64	R44	Y60	AG58	AM56	AP66	BR60
	H71	T40	Y62	AG60	AM58	AP66	BT37
A76		T42	Y64	AG64	AM60	AR64	BT62
B54	J69	T44	AC56	AM62	AR71	BU60	
	K64	V37	AC60	AH58	AM66	BJ62	BW37
	K71	V39	AC62	AH60	AN64	AN78	CA37
C66	L54	V40	AL64	AJ64	BL37	CB39	
D54	N39	W66	AE56	AP55	BL60	CB43	
D71	N43	Y32	AE58	AK56	AP56	BM62	
F20	J20	P11	T37	AD9	BA14	BE32	
H11	K11	T35	AC11	AN7	BA18	BD7	BF33
CU76	CM78		E72	AK66			

Note : USB OC# Pins
 OC# pins must be shared between ports:
 OC#[3:0] can only be used for USB port 0-7
 OC#[4:7] can only be used for USB port 8-13
 Note : NCTF_TP[16:1] Leave as no connect



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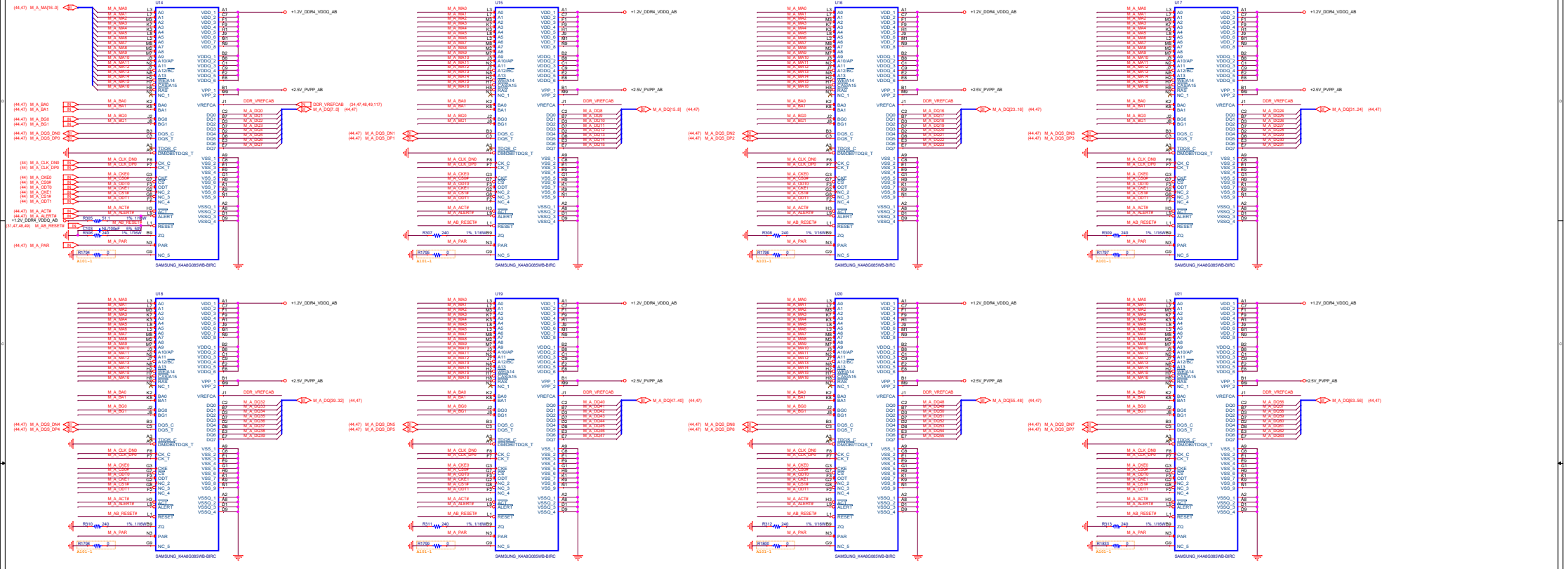
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Title: **BDX-DE0[JTAG/SMB/GPIOS]**

Size: Document Number **MIC-6315** Rev **A102-1**

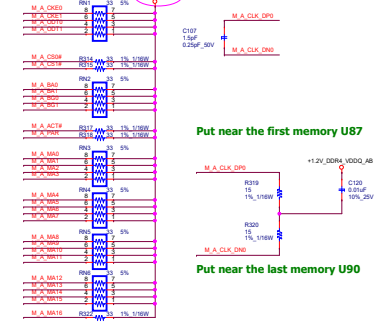
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[DDR4 DIMMA0 w/ECC]



Termination for DIMMA0

Increase "+0.6V VTT" Shape



Put near the termination resistors (For CHA Only)

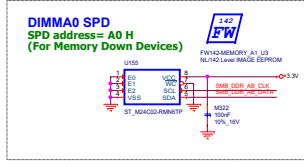
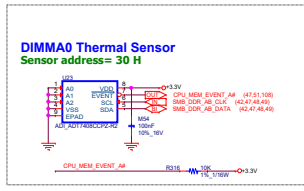
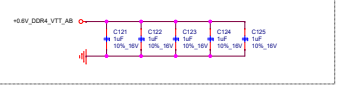


Table 6-18. R / U / DIMM socket SPD address configurations

Channel	DIMM Slot	SPD Address	TS0D Address	SA[2:0]
0	DIMM0	0x40	0x30	000
	DIMM1	0xA2	0x32	001
	DIMM0	0xA4	0x34	010
1	DIMM1	0xA6	0x36	011

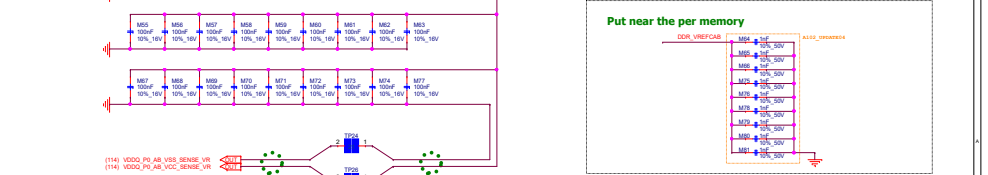
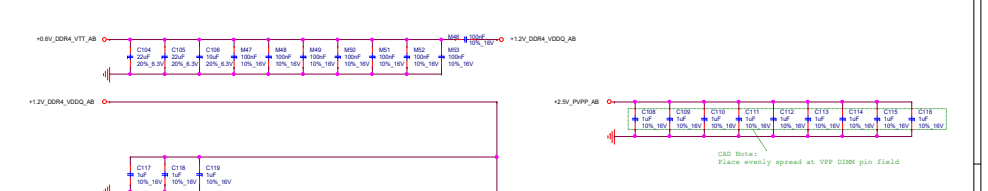
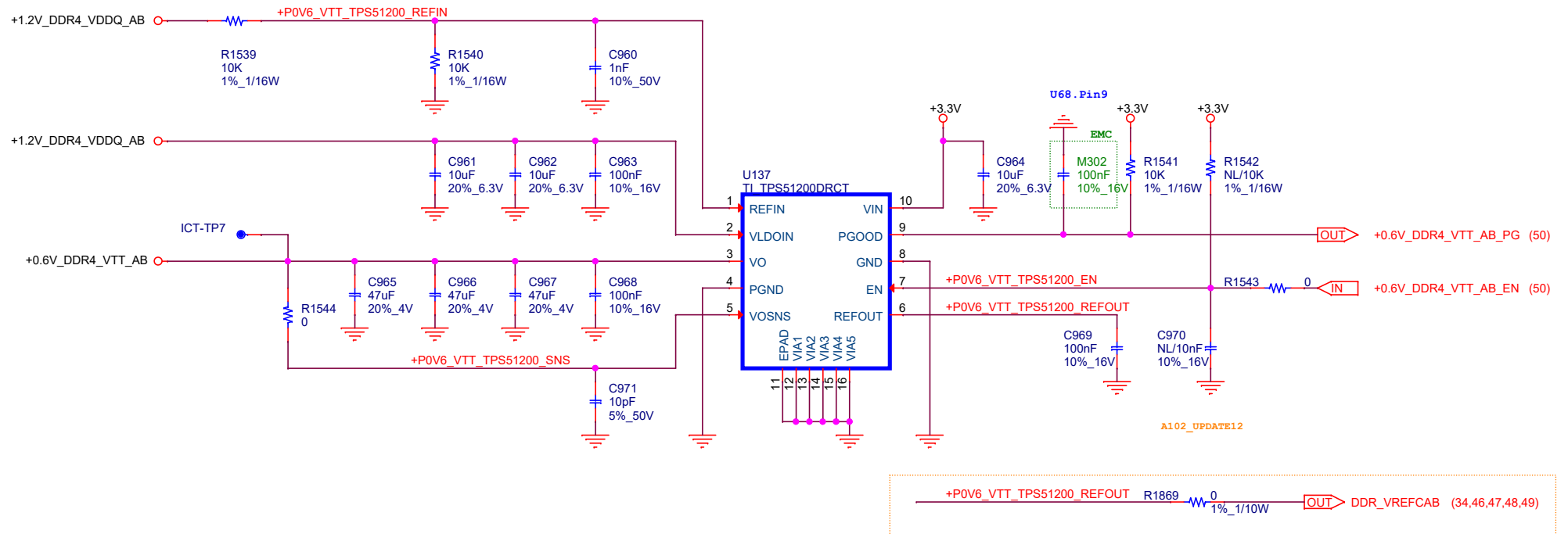


Table 6-19. R / U / DIMM socket VTT address configurations

+0.6V_DDR4_VTT_AB



Iout (TDC)	0.823A
OCP	xxxxxxx
Vout (TDC)	+0.6V_DDR4_VTT
OVP	
UVP	

VIN:1.2V
 VOUT:0.6V
 Pd:0.498w
 Rja:52.06 c/w
 Ta: 40 degree C
 Tj:65.925 degree C
 Storgae Temp: -55~150

Cap Description	Min Quantity	Notes
10.0 μF / 6.3V / 20% / X5R / 0603	3	place evenly spread at VTT DIMM pin field
22.0 μF/ 6.3V / 20% / X5R / 0805	4	place evenly spread at VTT DIMM pin field
	1	Placed close to VR controller

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Title: **PWR [CPU0_DDR4_VTT]**

Size: Document Number **MIC-6315** Rev **A102-1**

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