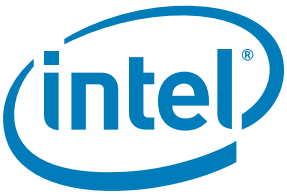

1000BASE-T/100BASE-TX/10BASE-T Physical Layer Compliance Tests Manual

June 2006

Revision History

Date	Revision	Description
May 2006	4.3	Revised document with new Intel branding documentation templates.
Oct. 2005	4.2	Replaced references to PhyConf tool with LANConf tool.
June 2005	4.1	Replaced references to GigConf tool with LANConf tool.
Feb. 2005	4.0	Updated the BER formula. Added a note to step 4 of Section 3.5 explaining how to measure droop across points F/G or H/J. Removed “100 Ohm Resistive Load” from Text Fixture 40-32 in Section 7.5.
Sep. 2004	3.9	Removed references to “BER Test User’s Guide.” This document does not exist.
Nov. 2003	3.8	Minor edits.
Oct. 2003	3.7	Minor edits.
Sep. 2003	3.5	More updates for IEEE Gigabit Ethernet testing.
Aug. 2003	3.0	General updates for IEEE Gigabit Ethernet testing.
Aug. 2002	2.0	General edits and additional information included in Appendix C.
Dec. 2001	1.2	Listed required versus recommended tests in Sections 1.1.1 and 1.1.2. Added new section for alien crosstalk noise rejection test. Included diagrams for test fixtures in Appendix A. Changed Appendix C from “Calculations for Worst-Case Gigabit Cable” to “Worst-Case Cable for Gigabit Jitter.”
Aug. 2001	1.1	Changed GT.exe software name to GigConf.exe.
June 2001	1.0	First release.

Contents

1 Introduction

Networking is complex and involves a combination of advanced analog and digital technologies. To insure interoperability of networking solutions from various manufacturers, it is imperative that standard compliance testing is performed.

This document describes procedures for basic 1000BASE-T, 100BASE-TX, and 10BASE-T PHY compliance testing on Intel-based networking solutions. It does not include the complete set of tests required for TP-PMD conformance. However, it does include a recommended subset of these tests. After completing the test procedures described in this manual, the user should be able to identify and understand how to correct areas where the Unit Under Test (UUT) fails to conform to the standards listed in Section 1.1.

The procedures in this document are not intended to be specific to a particular manufacturer's test equipment. Moreover, they do not encompass all methods that a test may be performed. The tester is assumed to have a basic knowledge of oscilloscopes, network analyzers, signal generators, etc. Advice for success in obtaining accurate measurements are included throughout the document in shaded boxes.

The test methods described in this document have been customized to test Intel networking silicon only. Results may vary if these procedures are used on other manufacturers' networking devices.

1.1 Reference Documents

IEEE Standard 802.3-2000, *Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*:

  - — Sections 40.6 - 4.8 for 1000BASE-T
  - — Section 14.3 for 10BASE-T)
- ANSI X3.263-1995, Section 9 for 100BASE-TX
- ANSI Standard 802.3-25.4-2002

1.2 Basic Concepts

Recommended equipment settings are provided for each test procedure. These settings provide a good starting point for measurement. Variations in equipment can effect the resolution and accuracy of a signal. User experience manipulating equipment trigger and display can also effect the perception and interpretation of the waveform. In addition, probe polarity and trigger polarity can effect the interpretation of the signals. The settings provided are based on the test equipment used and may vary depending on equipment.

1.2.1 Calibration

Due to the precise measurements required for compliance testing, accurate measurement instruments are required. All equipment used during the testing process must be properly calibrated. Oscilloscopes must have a signal path compensation and probe calibration completed prior to testing.

1.2.2 Triggering

Determining the appropriate trigger point can mean the difference between passing and failing the physical layer conformance tests. Triggering guidelines are provided throughout this document and provide a good starting point for measurement. Fine tuning adjustments may be necessary in order to achieve the best display.

1.2.2.1 Signal with an Ambiguous Trigger Level

An ambiguous trigger level (either width or height) can prevent a stable display.

1. Try to reduce the delta between the minimum and maximum pulse widths as much as possible.
2. Determine where the trigger level falls on the waveform.

If the line passes through more than one point on the rising edge of the waveform, raise or lower the trigger until a point is found that is unambiguous as illustrated in Figure 1-1.

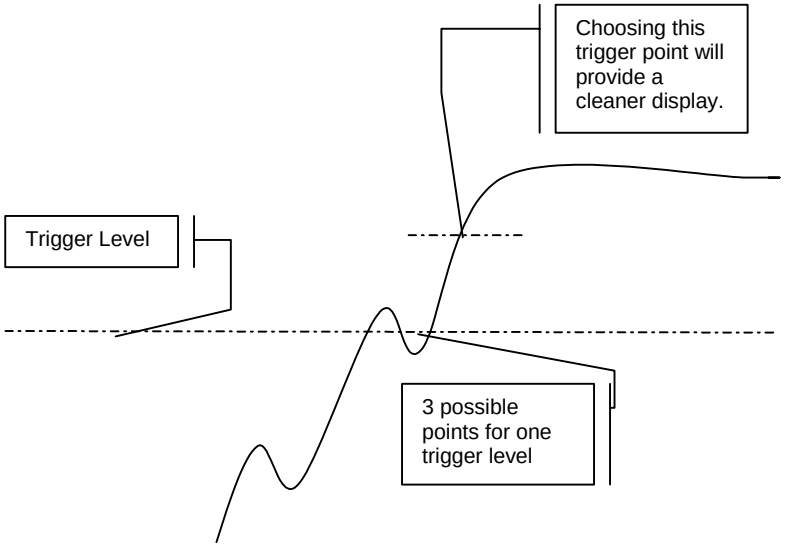

Figure 1-1. Ambiguous Trigger Level

1.2.2.2 Signal Does Not Appear

If the signal does not appear or appears only for an instant, the trigger level may be too high. Reducing the trigger level should cause the signal to appear (or re-appear).

1.2.3 Displaying Waveforms

When observing waveforms on the scope display, it is important to understand the purpose of the measurement being performed. If the purpose is simply to see a complete waveform, then the horizontal and vertical scales only need to be small enough to fit the waveform on the screen and the display does not need to be set to average or infinite persistence. However, if the purpose is to obtain the most accurate measurements, more care is needed. The recommended scope settings listed

throughout the procedures should allow the desired waveform to be displayed on the screen. For the best resolution, zoom in as much as possible on the waveform as observed in the following three screen shots.

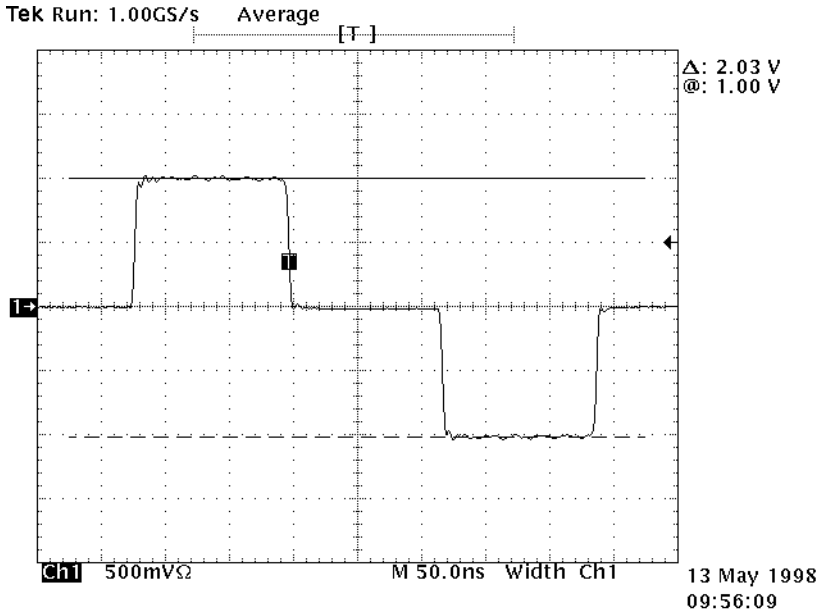

Figure 1-2. Poor Resolution (Wide View)

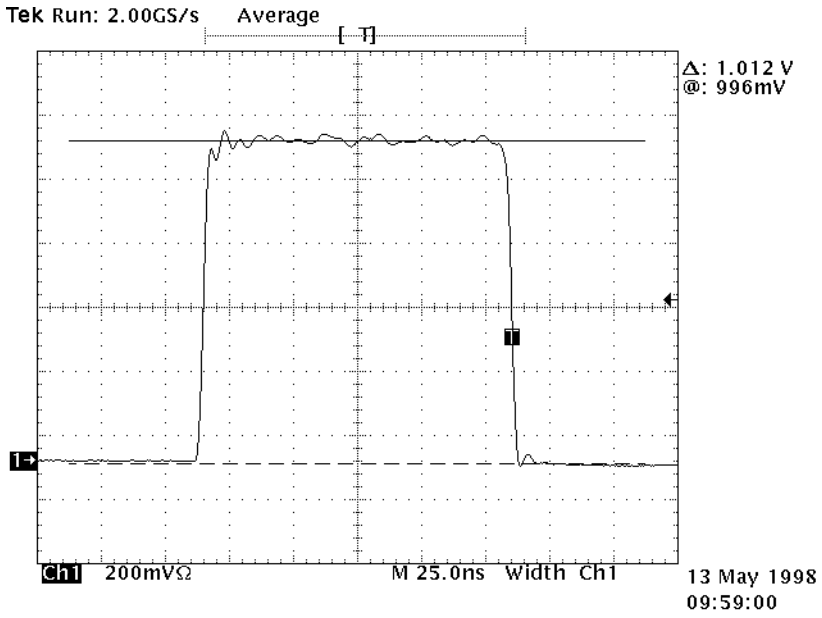

Figure 1-3. Good Resolution with Room for Improvement

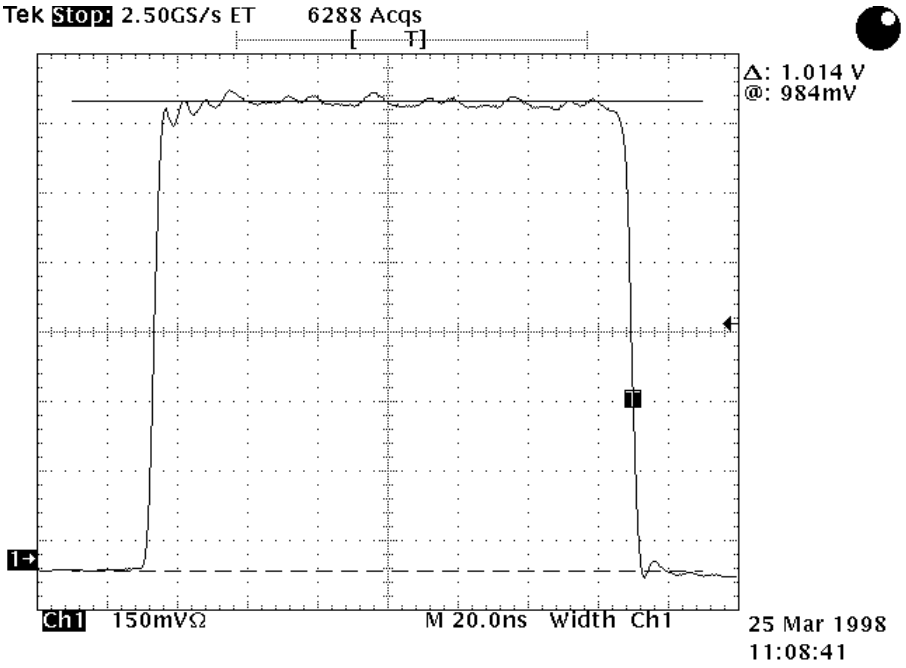

Figure 1-4. Best Resolution for Measurement

Note: The above three screen shots were not necessarily taken during the same session.

Note: The waveform in Figure 1-4 is displayed across the entire screen, showing enough of the edge of the pulse to allow the zero point to be approximated and providing the best resolution possible for measurement.

In the example above, the “Average” setting was used on the scope to produce a sharper image. This is the best (and easiest) way to measure the amplitude, period, overshoot, and rise/fall time of a waveform. Each time a new trigger signal arrives, the scope repaints the screen with a new signal. This causes the signal to appear unstable because each successive signal is not exactly the same as the previous one. By averaging the waveforms together, random noise will be filtered from the display, and a more representative signal will appear.

Some measurements require the scope display to be set to “Infinite Persistence.” In this case it is important that each successive waveform falls within specified boundary conditions. In infinite persistence mode, an adequate sample is obtained from data accumulated between a one to ten minute time period.

1.3 Required Test Equipment

This section describes the minimum equipment needed to complete the test.

- Digitizing oscilloscope with at least 1 GHz bandwidth (for example, Tektronix® 784).
- Two high bandwidth differential probes (for example, Tektronix® P6247) with capacitance less than or equal to 1 pF and a bandwidth greater than or equal to 1 GHz. Using lower bandwidth/higher capacitance probes may cause false failures of conformance tests.

- Two computers with open PCI slots and LANConf.exe installed.
- One Intel® 82543 controller-based 1000BASE-T adapter to generate Ethernet traffic.
- Network/spectrum analyzer (50 KHz to 500 MHz range) with S-parameter test set.
- BNC cable with 50-ohm impedance (approximately three feet long).
- Additional test equipment may be required for 100BASE-TX and 10BASE-T testing (refer to the appropriate test procedure for a list of needed equipment).

1.4 Required Test Fixtures

- 100 Ω load resistors—all four channels have 100 ohms (± 0.2 ohms preferred)
- Category 5 UTP cable (~2 inches long)
- Balun test fixture (100-ohm balanced to 50-ohm unbalanced)
- Network analyzer calibration loads:
- Short-circuit calibration standard
- Open-circuit calibration standard
- 100-ohm calibration load
- 50-ohm calibration load
- Common-mode output voltage test fixture (IEEE 802.3, fixture 40-32)
- 0.5 meter Category 5 cable, with female pins on 0.1 inch centers at one end
- Length of Category 5 cable that conforms to the following:
  - For 1000BASE-T, Section 40.7 of the IEEE 802.3 specification. The parameters that have the greatest impact on cable length are insertion loss and propagation delay.
  - For 100BASE-TX, Section 25.4.6 of the IEEE 802.3 specification.
  - For 10BASE-T, Section 14.4 of the IEEE 802.3 specificationAlien crosstalk noise injection cable.
- LAN adapter that can be forced into 100BASE-TX mode
- Alien crosstalk test fixture with male and female square pins and a circuit of three resistors (two 2 KW and one 100 Ω)
- Additional test fixtures are required for 100BASE-TX and 10BASE-T testing.

Appendices A through D provide test fixture illustrations and construction information.

1.5 Required Software and Data Patterns

Many of the tests in this procedure require the UUT to behave in a specified way. Intel's proprietary test utility, LANConf.exe, allows the UUT to be configured into the desired state and to transmit and receive specific test patterns. Contact your local Intel sales office for more details and to obtain a copy of LANConf.exe.

1.6 PHY Conformance Tests

There are several different ways to group the tests in this procedure, depending on the intent of the tester. The following minimum subset of tests necessary to catch the most problematic bugs in board design and implementation are listed in the three tables below.

- Pre-Test - minimal initial design validation requirements. These are the first tests that should be completed.
- IEEE Compliance Test - tests needed for basic IEEE testing. This test subset identifies most board design and implementation issues.

Note: Recommended tests are for higher design and implementation confidence. These tests are not required, but if completed will ensure a higher quality design.

Table 1-1.

1000Base-T PHY Conformance Tests	Pre-Test	IEEE Compliance Test
40.6.1.2.1 Peak Differential Output Voltage and Level Accuracy	X	X
40.6.1.2.2 Maximum Output Droop	X	X
40.6.1.3.2 Receiver Differential Input Signals (Receive Bit Error Rate)	X	X
40.8.3.1 MDI Return Loss		X
40.6.1.3.4 Alien Crosstalk Noise Rejection (Differential Noise Rejection)		Recommended
40.8.3.3 MDI Common-Mode Output Voltage		Recommended

100Base-TX PHY Conformance Tests	Pre-Test	IEEE Compliance Test
100Base-TX Differential Output Voltage (UTP)	X	X
100Base-TX Transmit Jitter	X	X
100Base-TX Differential Input Signals (BER)	X	X
100Base-TX Signal Amplitude Symmetry	X	X
100Base-TX Rise and Fall Times	X	X
100Base-TX Duty Cycle Distortion (DCD)	X	X
100Base-TX Receiver Return Loss		X
100Base-TX Transmitter Return Loss		X

10Base-T PHY Conformance Tests	Pre-Test	IEEE Compliance Test
• 10Base-T Peak Differential Output Voltage on TD Circuit	X	X
• 10Base-T Transmitter Output Timing Jitter without Cable Model	X	X
• 10Base-T TD Circuit Impedance (Transmitter Return Loss)		X
• 10Base-T TD Circuit Common-Mode Output Voltage		X
• 10Base-T Transmitter Output Timing Jitter with Cable Model		X
• 10Base-T RD Receiver Circuit Signal Acceptance Test (BER)		X
• 10Base-T RD Circuit Differential Input Impedance (Receiver Return Loss)		X
• 10Base-T Harmonic Content		Recommended

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2 1000BASE-T Peak Differential Output Voltage and Level Accuracy

IEEE STANDARD 40.6.1.2.1

2.1 Test Purpose

To measure the peak differential output voltage on all four channels and examine the linearity of each channel. This test uses "Test Mode 1" as defined by the IEEE 802.3 Specification, Section 40.6.1.1.2. An example of the test mode 1 waveform is shown below.

2.2 Specification

- Points A & B = ±(0.67 to 0.82)Vpk
- Amplitude Symmetry: < 1% delta between A and B
- Points C & D = ±(0.5*A or B) ±2%
- The above is true for all four MDI channels.

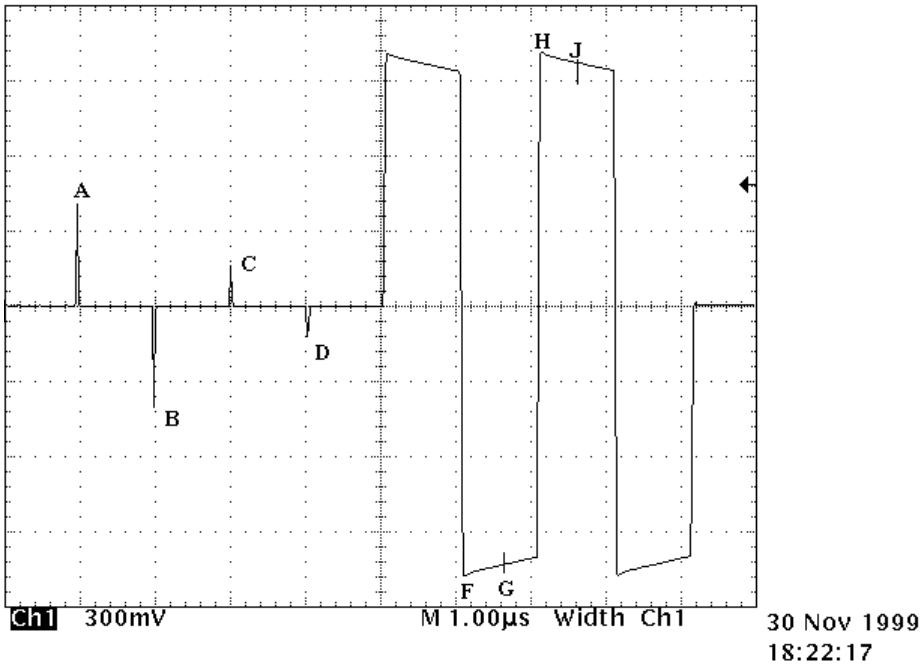


Figure 2-1. Example of Test Mode 1 Waveform

2.3 Test Equipment

- Digitizing oscilloscope with at least 1 GHz bandwidth
- Differential probe with 1 GHz or greater bandwidth

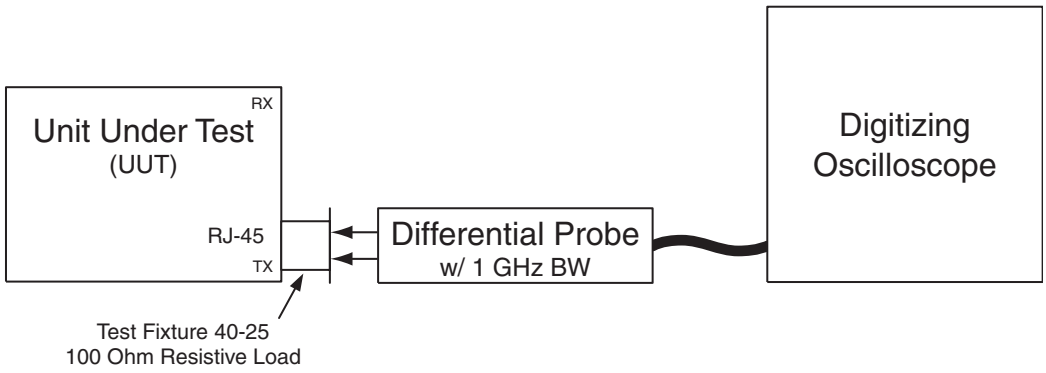
- UUT with LANConf.exe test software

2.4 Test Fixtures

- 100 Ω UTP test load (Appendix A).

2.5 Test Procedure

1. Connect the test equipment as shown in the figure below.



2. Set the probe to divide by 10 and to full bandwidth.
3. Select the Amplitude and Level Accuracy: 40.6.1.2.1 Test from the 1000BASE-T PHY Configuration Tests menu in LANConf.exe.
4. Measure the output voltage with a differential probe connected across the 100-ohm test load for each channel.
5. Adjust oscilloscope to the settings for Point A as shown in the following table and figure:

Table 2-1. Point A Peak Voltage

Trigger Settings	Trigger Type	Polarity	Limits	Level
	Pulse width	Positive	7 ns to 9 ns	+500 mV
Scaling	Vertical Scale	Vertical Position	Horizontal Scale	
	150 mV / division	-3.0 division	5 ns / division	
Cursors	Display Mode	Acquisition Mode		
Horizontal bars	Vectors	Average on		

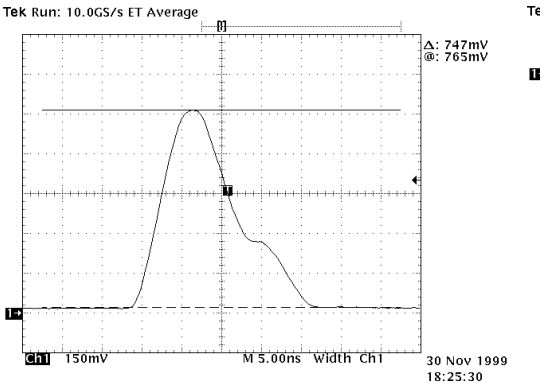


Figure 2-2. Example Point A Measurement

6. Repeat Step 5. for Point B:

Table 2-2. Point B Peak Voltage

Trigger Settings	Trigger Type	Polarity	Limits	Level
	Pulse width	Negative	5.6 ns to 8.6 ns	-500 mV
Scaling	Vertical Scale	Vertical Position	Horizontal Scale	
	150 mV / division	+3.0 division	5 ns / division	
Cursors	Display Mode	Acquisition Mode		
Horizontal bars	Vectors	Average on		

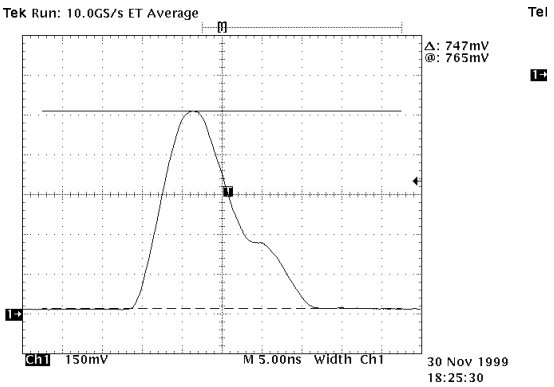


Figure 2-3. Example Point B Measurement

7. Repeat Step 5. for Point C:

Table 2-3. Point C Peak Voltage

Trigger Settings	Trigger Type	Polarity	Limits	Level
	Pulse width	Positive	7 ns to 9 ns	251 mV
Scaling	Vertical Scale	Vertical Position	Horizontal Scale	
	75 mV / division	-3.0 division	5 ns / division	
Cursors	Display Mode	Acquisition Mode		
Horizontal bars	Vectors	Average on		

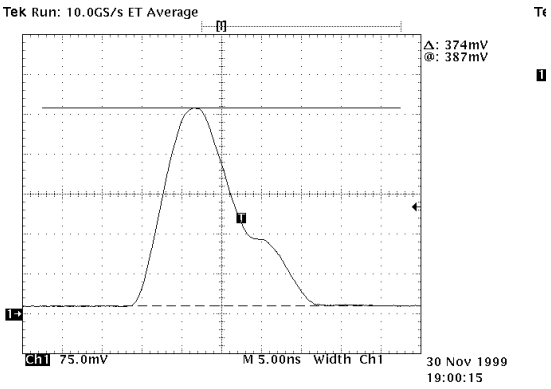
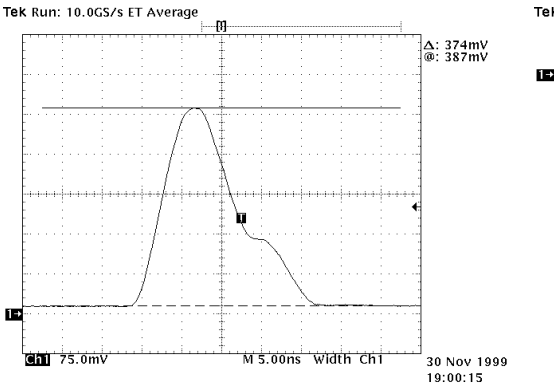


Figure 2-4. Example Point C Measurement

8. Repeat Step 5. for Point D:

Table 2-4. Point D Peak Voltage



Trigger Settings	Trigger Type	Polarity	Limits	Level
	Pulse width	Negative	5.6 ns to 8.6 ns	-278 mV
Scaling	Vertical Scale	Vertical Position	Horizontal Scale	
	75 mV / division	+3.0 division	5 ns / division	
Cursors	Display Mode	Acquisition Mode		
Horizontal bars	Vectors	Average on		

Figure 2-5. Example Point D Measurement

9. Verify that the measurements meet specifications for all four points

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3 1000BASE-T Maximum Output Droop

IEEE STANDARD 40.6.1.2.2

3.1 Test Purpose

To ensure that the LAN analog front end (AFE) is capable of handling DC bias. This test uses “Test Mode 1" as defined by the IEEE 802.3 Specification, Section 40.6.1.1.2. An example of the test mode 1 waveform is shown below.

3.2 Specification

- Point G amplitude > 73.1% of point F amplitude; point G is exactly 500 ns after F.
- Point J amplitude > 73.1% of point H amplitude; point J is exactly 500 ns after H.
- The above is true for all four MDI channels.

If the LAN design does not meet the output droop requirement, the open circuit inductance (OCL) for all four channels of the magnetics module should be verified and equal at least 350 µH with an 8 mA DC bias. (The OCL requirement is explained in more detail in the ANSI TP-PMD, 100BASE-TX physical layer specification.)

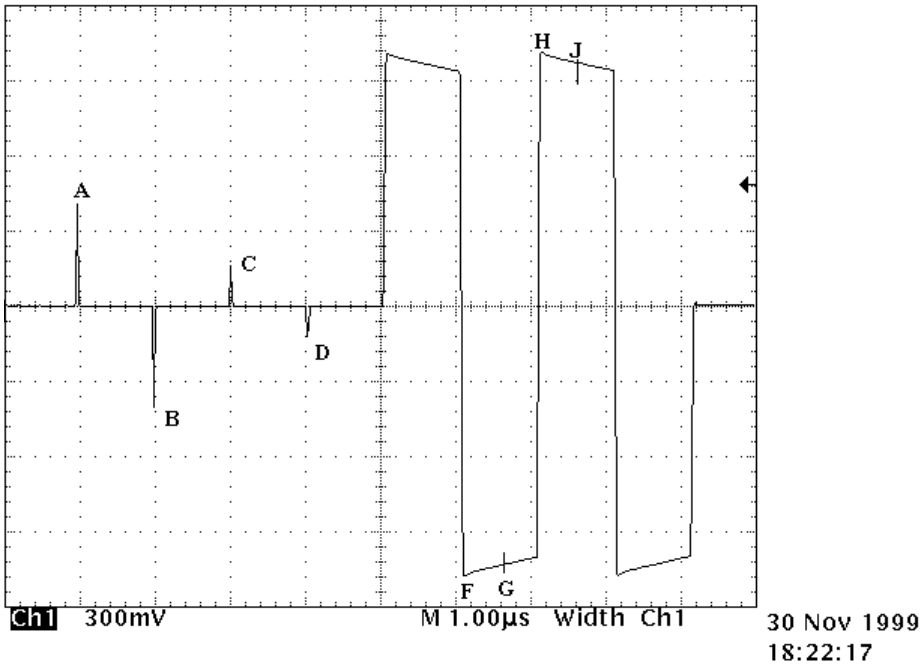


Figure 3-1. Example of Test Mode 1 Waveform

3.3 Test Equipment

- Oscilloscope with 1GHz or greater bandwidth
- Differential probe with 1 GHz or greater bandwidth

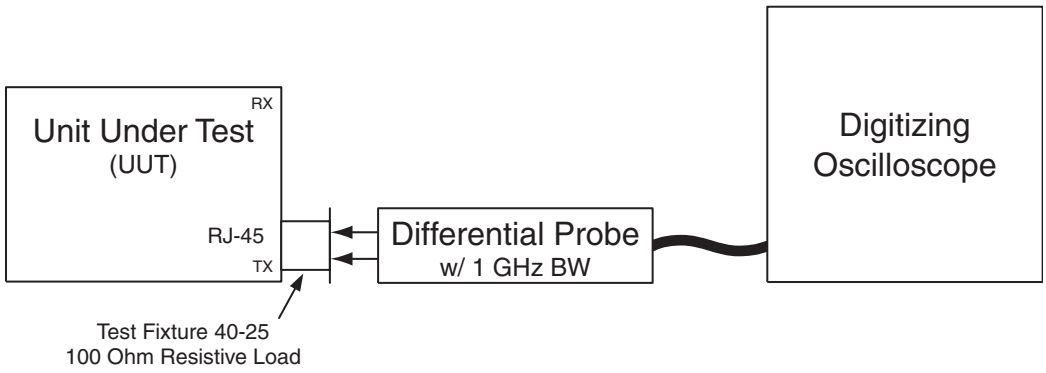
- UUT with LANConf.exe test software

3.4 Test Fixtures

- 100 Ω UTP test load (Appendix A.1).

3.5 Test Procedure

1. Connect the test equipment as shown in the figure below.



2. Set the probe to divide by 10 and to full bandwidth.
3. Select the Droop: 40.6.1.2.2 Test from the 1000BASE-T PHY Configuration Tests menu in LANConf.exe.
4. Adjust the oscilloscope to the settings for Points F and G.

Note: When measuring points F/G or H/J for droop, trigger the oscilloscope on point B to measure points F/G and point A to measure points H/J. Use a long record length and scroll over to the points to be measured.

Table 3-1.

Point F and G: Pulse Droop				
Trigger Settings	**Trigger Type**	**Polarity**	**Limits**	**Level**
	Pulse width	Negative	5.6 ns to 8.6 ns	-500 mV
Scaling	**Vertical Scale**	**Vertical Position**	**Horizontal Scale**	
	150 mV / division	+3.0 division	200 ns / division	
Cursors	**Display Mode**	**Acquisition Mode**		
Horizontal bars for F; Crosshairs for F and G	Vectors	Average on		

5. Measure the output voltage with a differential probe connected across the 100-ohm test load for each channel.
6. Adjust the oscilloscope to the settings for Points H and J as shown below.

Point H and J: Pulse Droop				
Trigger Settings	**Trigger Type**	**Polarity**	**Limits**	**Level**
	Pulse width	Positive	7 ns to 9 ns	+500 mV
Scaling	**Vertical Scale**	**Vertical Position**	**Horizontal Scale**	
	150 mV / division	-3.0 division	200 ns / division	
Cursors	**Display Mode**	**Acquisition Mode**		
Horizontal bars for H; Crosshairs for H and J	**Vectors**	**Average on**		

Note: Points F and G are like H and J, except they are negative polarity.

7. Measure the output voltage with a differential probe connected across the 100-ohm test load for each channel.
8. Compute the ratios as shown in the example below.

Channel	Point F	Point G	Ratio	Point H	Point J	Ratio
A	-1.024	-0.982	95.898%	1.020	0.984	96.471%
B	-1.022	-0.985	96.380%	1.022	0.985	96.380%
C	-1.019	-0.985	96.663%	1.018	0.985	96.853%
D	-1.019	-0.982	96.369%	1.012	0.983	97.134%

Point H peak = 1.020 Volts:

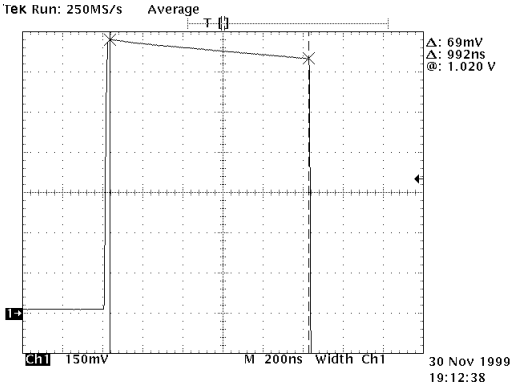


Figure 3-2. Example Maximum Output Droop Measurement, Point H

Point J, 500 ns after H = 0.984 Volts:

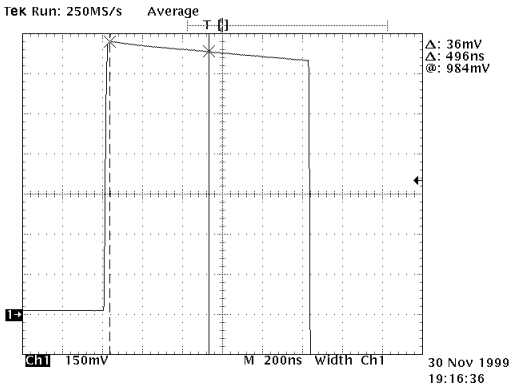


Figure 3-3. Example Maximum Output Droop Measurement, Point J

9. Verify the measurements meet specifications

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4 1000BASE-T Receiver Differential Input Signals (Bit Error Rate)

IEEE STANDARD 40.6.1.3.1

4.1 Test Purpose

To determine the UUT receiver sensitivity at various cable lengths.

This requirement can be accomplished by performing receive bit error rate tests with specification compliant Category 5 cables across a range of lengths from approximately 1 meter to greater than 100 meters (maximum specification). Insertion loss measurements and propagation delay measurements have shown high-quality Category 5 cable ranging from 115 m to 130 m may be equal to a maximum specification cable (depending on the vendor and the cable manufacturing lot). Appendix E contains details on constructing LAN cables.

4.2 Specification

The receiver shall have a frame error rate of less than 10^7 for 125 octet frames. A frame error rate of 10^7 for 125 octet frames is equivalent to a bit error rate (BER) of 10^{10} for any size of frame.

4.3 Test Equipment

- UUT with LANConf.exe software
- Second system running LANConf.exe with either a 1000BASE-T network interface card (NIC) or LAN on Motherboard (LOM) for the link partner
- Various lengths of Category 5 cable between 1 and 100 meters
  One of the cable lengths should be equivalent to the maximum cable length described in the IEEE 802.3 standard, Section 40.7.

4.4 Test Fixtures

Various lengths of Category 5 cable between 1 and 100 meters (Appendix A).

4.5 Test Procedure

1. Connect the UUT and the link partner using the desired Category 5 cable length and verify that a gigabit link has been established.
2. On the receiving system, go to the Transmit and Receive menu, and select the Receive option.
3. On the UUT, go to the Transmit and Receive menu, and select the Transmit option.
4. Allow the proper number of frames to be sent (see Section 4.6).
5. After transmissions is complete, press the <Esc> key on the receiver first and then the transmitter to stop the test and record the following results:
   a. Link partner: Transmit Good Packets and Transmit Total Packets. Both of these statistics should equal each other.
   b. UUT: Receive Good Packets and Missed Packets.
6. Calculate the bit error rate (BER).

7. Repeat steps 1 through 7 for each cable length.
8. Verify the measurements meet specifications

4.6 Calculating Bit Error Rate (BER)

The basic BER equation is as follows:

$$BER = \frac{TGP - MP - RGP}{TGP \times BF \times BB}$$

where:

- TGP = number of good frames transmitted (#_Transmit_Good_Packets)
- MP = number of missed packets (#_Missed_Packets)
- RGP = number of good frames received (#_Receive_Good_Packets)
- BF = number of bytes/frame
- BB = 8 (number of bits/byte)

Note: Conditions where the transmit link partner overwhelms the receive unit should be avoided. When this happens, the receive statistics counters may show "RX No Resources", "RX No Buffers", or a large number of missed packets. This complicates the BER calculation and the equations for the calculations will not yield accurate BER numbers. The TX transmit speed (frames per second) can be decreased to prevent this condition. Alternatively, the test operator can try to make sure the receive unit is always in a faster PC than the transmit unit.

Example 4-1 BER Calculation Example

If 4,249,995 good frames were received and 4,250,000 good frames were transmitted, then for 1,024 byte frames and zero missed packets the BER would be as follows:

BER = ((4,250,000 - 0) - 4,210,000)/(4,250,000*1,024*8) = 1.43 x 10^-10

This example fails because the resulting BER is greater than 1 x 10-10, which is the maximum specification.

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5 1000BASE-T Alien Crosstalk Noise Rejection

IEEE STANDARD 40.6.1.3.4

5.1 Test Purpose

To verify if the receiver can tolerate the specified injected differential noise signal without excessive errors.

5.2 Specification

The receive BER shall be less than 10^{10} with crosstalk voltage from a 100BASE-TX scrambled idles transmitter injected onto one MDI receive channel. This is required for all channels using a worst-case (max insertion loss and propagation delay) test cable as defined in the IEEE 802.3 specification, Section 40.7.

5.3 Test Equipment

- UUT with LANConf.exe software
- Second PC with Ethernet network interface card (NIC) that can be forced to transmit 100BASE-TX scrambled idle signals
- Third PC with LANConf.exe software with either a 1000BASE-T NIC or LAN on Motherboard (LOM) for a link partner

5.4 Test Fixtures

- Fixture 40-28A (Appendix A).
- Fixture 40-28B (Appendix A).
- Male-to-male RJ-45 coupler (Appendix A).
- Fixture 40.6.1.1.1.A (Appendix A).

5.5 Test Procedure

1. Using the maximum cable length and Fixture 40.6.1.1.1A in place on the UUT, perform a baseline BER according to the procedure defined in Chapter 4. The BER should equal zero.
2. Connect the equipment as shown in the figure below.

Figure 5-1.

3. Adjust the 100BASE-TX unit to send scrambled idles onto one channel of the UUT. Verify the injected signal is nominally 25mV pk-pk.
4. Verify Scrambled Idle Amplitude & record. Note: Signal amplitude may vary across various units.
5. Use the UUT and the 1000BASE-T unit to perform a BER test using the maximum cable length according to the procedure defined in Chapter 4.
6. Perform a warm reboot of the UUT after the test is complete.
7. Move the 100BASE-TX unit to send scrambled idles on to another channel of the UUT.

8. Repeat steps 5 to 7 for each remaining channel. Four sets of receive BER data should exist when the test is completed.
9. Verify the measurements meet specifications

Note: Before injecting the differential 100BASE-TX scrambled idles, a baseline receive BER test should be performed. Without the injected noise signal, the receive BER should equal 0 (zero).

Table 5-1. Example Data

MDI Channel	Frame Size (bytes)	Transmit Good Frames	Receive Good Frames	Total Receive Errors	BER
A	1024	6,513,468	6,509,797	0	0
B	1024	6,337,425	6,334,005	0	0
C	1024	7,691,347	7,687,308	0	0
D	1024	6,382,373	6,378,962	0	0

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6 1000BASE-T MDI Return Loss

IEEE STANDARD 40.8.3.1

6.1 Test Purpose

To measure the return loss on all four channels at the MDI.

6.2 Specification

The return loss for each transmit/receive channel shall be:

≥ 16 dB from 1 MHz to 40 MHz, and

≥ 10 – 20LOG(f/80)dB from 40 MHz to 100 MHz, where f is in MHz.

6.3 Test Equipment

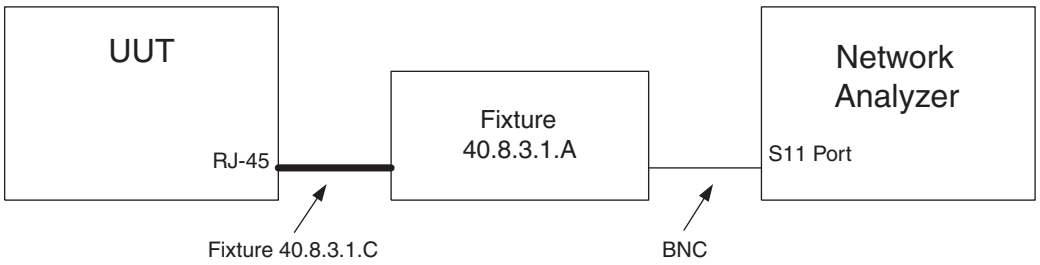
- Vector network analyzer
- BNC cable with 50-ohm characteristic impedance
- UUT with LANConf.exe test software.

6.4 Test Fixtures

- Fixture 40.8.3.1.A, Balun test fixture (Appendix A)
- Fixture 40.8.3.1.B, calibration standards (Appendix A)
- Fixture 40.8.3.1.C, square pin fixture (Appendix A)

6.5 Test Procedure

1. Connect the equipment as shown in the figure below. Note: do not connect test fixture 40.8.3.1.C to the UUT's RJ-45 at this time. See Appendix A for more details.



2. Select the Return Loss: 40.8.3.1 Test on the UUT from the 1000BASE-T PHY Configuration Tests menu in LANConf.exe.
3. Set the network analyzer to the settings as described below.

Table 6-1. Network Analyzer Settings

Setting	Value
Analyzer Type	Network
Measurement Format	S11
Start Frequency	1 MHz
Stop Frequency	101 MHz
Number of Points	401 point (or 801 points)
IF Bandwidth (Resolution Bandwidth)	100 Hz
Reference Position	10
Reference Level	0 dB
Scale	5 dB per division
Limit Lines and Pass/Fail Functions	On (if available)
Markers	1 MHz, 16 MHz, 30 MHz, 40 MHz, 60 MHz, 80 MHz, and 100 MHz

The Markers should be based on taken measurements. The sample points are recommended and convenient markers and are not absolutes.

4. Select the calibration menu and perform an S11 calibration using test fixture 40.8.3.1.B connected to the RJ-45 of fixture 40.8.3.1.C.

   At the appropriate prompts choose the open circuit standard, the short circuit standard, and the 100-ohm calibration load. After calibration is completed, ensure that correction is turned on. Note: once the S11 calibration has been completed, care should be taken to not move the test setup more than necessary. Changes in the layout of the test setup can change the electrical characteristics of the setup and lead to erroneous results.

5. Measure a 50-ohm resistor standard when the calibration is completed. Its return loss should be 9.54 dB ±0.05 dB. If the 50-ohm standard measures outside of that tolerance, check the cable, connection points and other calibration standards, and repeat the calibration process.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$ Balanced output impedance of the balun (for example, 100 Ω).

Z_{load} The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{\left|Z_{transmitter} + Z_{load}\right|}{\left|Z_{transmitter} - Z_{load}\right|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{\left|100\Omega + Z_{load}\right|}{\left|100\Omega - Z_{load}\right|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

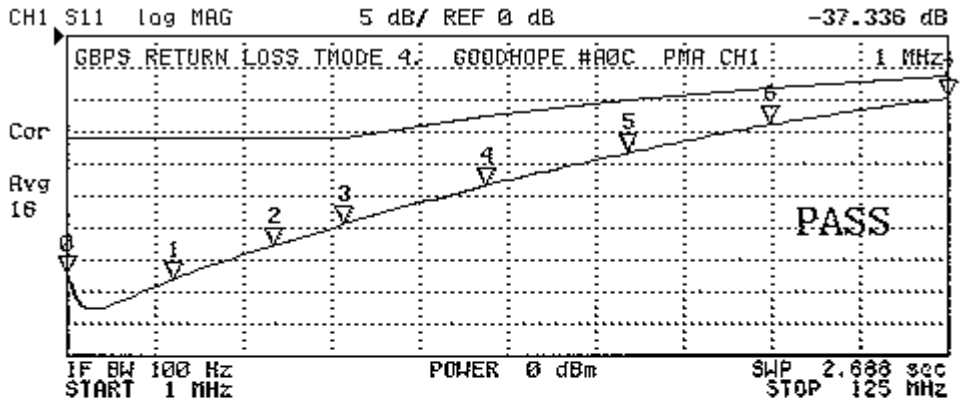
$$RL\_in\_dB = 20\log\frac{\left|100\Omega + 50\Omega\right|}{\left|100\Omega - 50\Omega\right|}$$

which simplifies to:

$$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54\ dB$$

6. Connect fixture 40.8.3.1.C to the UUT's RJ-45 and measure the LAN interface's return loss on channel A.
7. Repeat the calibration and measurement process for the remaining three channels.

If data is being plotted, there should be one graph for each channel. An example graph is shown below.



N	SWP PARAM	VAL
0	1 MHz	-37.336 dB
1	16 MHz	-38.013 dB
2	30 MHz	-32.729 dB
3	40 MHz	-29.422 dB
4	60 MHz	-23.337 dB
5	80 MHz	-18.267 dB
6	100 MHz	-13.848 dB
7	125 MHz	-9.7181 dB

Figure 6-1. Example Measurement

Note: Not all return loss measurements will look exactly like the example above. The most important part of the return loss measurement is to ensure that every point on the return loss line is below the limit specified by the IEEE 802.3 specification.

8. Verify the measurements meet specifications

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7 1000BASE-T MDI Common-Mode Output

IEEE STANDARD 40.8.3.3

7.1 Test Purpose

To measure and record the common-mode output voltage of the transmitter.

7.2 Specification

When transmitting data and using the test fixture shown in IEEE 802.3, Figure 40-32, the common-mode output voltage, Ecm_out, on any transmit pair shall be less than 50 mV peak-to-peak.

7.3 Test Equipment

- Digitizing oscilloscope with 1 GHz or greater bandwidth
- Differential probes with 1 GHz or greater bandwidth

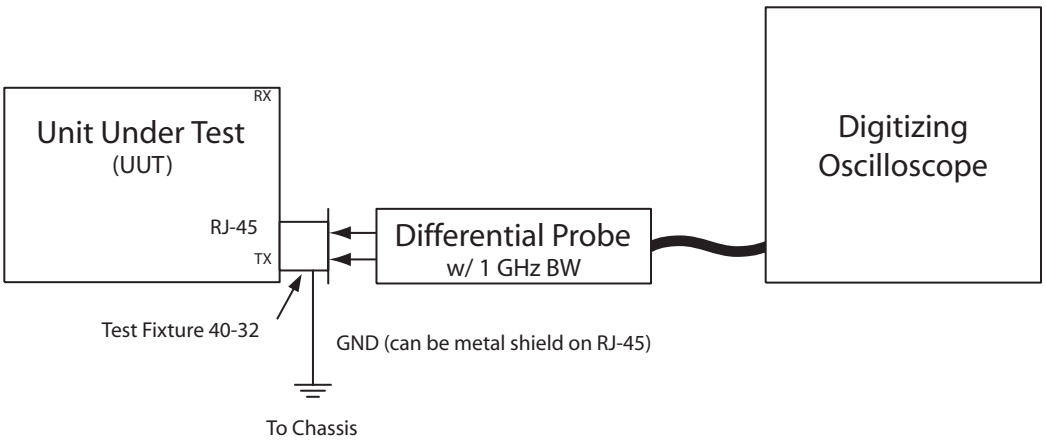
7.4 Test Fixtures

- Test Fixture 40-32 (Appendix A)

7.5 Test Procedure

1. Connect the test equipment as shown in the figure below.

Note: It is important to pay close attention to the grounding of test fixture 40-32. Inadequate grounding may lead to erroneous results. All ground connections should be as short as possible and continuous. Is is important to ensure that the ground on test fixture 40-32 is connected to a stable (not floating) ground through the RJ-45 of the UUT. Appendix A contains more details relating to test fixtures.



2. Adjust the probe settings to:
   — DC reject = on

— Bandwidth = full

— Attenuation = set to divide by one

3. Select the Common-Mode Output: 40.8.3.3 Test on the UUT from the 1000BASE-T PHY Configuration Tests menu in LANConf.exe.
4. Set the scope settings for positive common-mode measurement.

Table 7-1.

Scope Parameter	Setting
Horizontal Scale	2 ns / division
Vertical Range	-25 mV to +25 mV (at 10 vertical divisions, this equals 5 mV / division
Trigger Type	Level and positive or negative edge
Trigger Level	Adjust from 0 V to +25 mV to find peak voltage
Trigger Mode	Normal
Display Persistence	Infinite persistence or vectors (in other words, dots connected)

5. Adjust trigger level, in the positive direction, until trigger is lost and place cursor on the maximum or peak voltage.
6. Record maximum or peak amplitude value(s).
7. Set scope settings for negative common-mode measurement.

Scope Parameter	Setting
Horizontal Scale	2 ns / division
Vertical Range	-25 mV to +25 mV (at 10 vertical divisions, this equals 5 mV / division
Trigger Type	Level and positive or negative edge
Trigger Level	Adjust from 0 V to -25 mV to find peak voltage
Trigger Mode	Normal
Display Persistence	Infinite persistence or vectors (in other words, dots connected)

8. Adjust trigger level, in the negative direction, until trigger is lost and place cursor on the maximum or peak voltage.
9. Record maximum or peak amplitude value(s).

If data is being plotted, there should be at least two graphs for each channel (positive peak and negative peak)

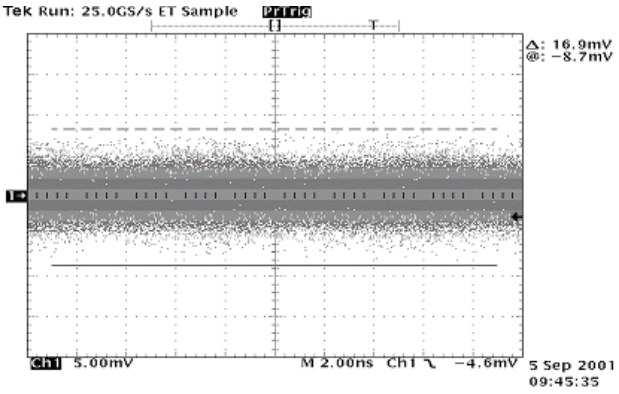


Figure 7-1. Common Mode Output Voltage: Negative Peak

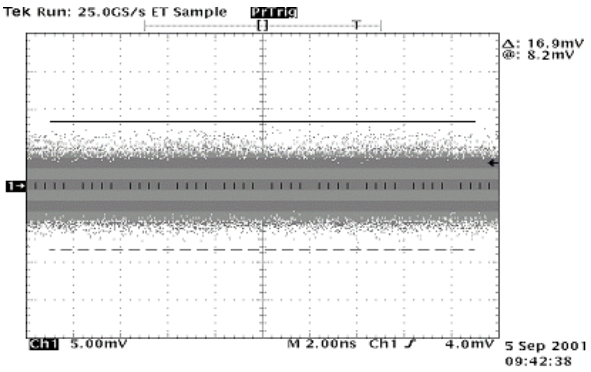


Figure 7-2. Common Mode Output Voltage: Positive Peak

MDI Channel	Ecm Output (mV pk-pk)
A	14.70
B	14.30
C	16.90
D	13.10

10. Verify the measurements meet specifications

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8 100BASE-TX Differential Output Voltage (UTP)

ANSI Section 9.1.2.2

8.1 Test Purpose

To measure the peak differential output voltage, Vout, at the transmit pins of the UTP connector (also known as the Active Output Interface or AOI).

8.2 Specification

For UTP, the differential output voltage, V_{OUT}, as defined in Specification 9.1.3 and Figure 8-1 shall be: 950 mV ≤ V_{OUT} ≤ 1050 mV.[1]

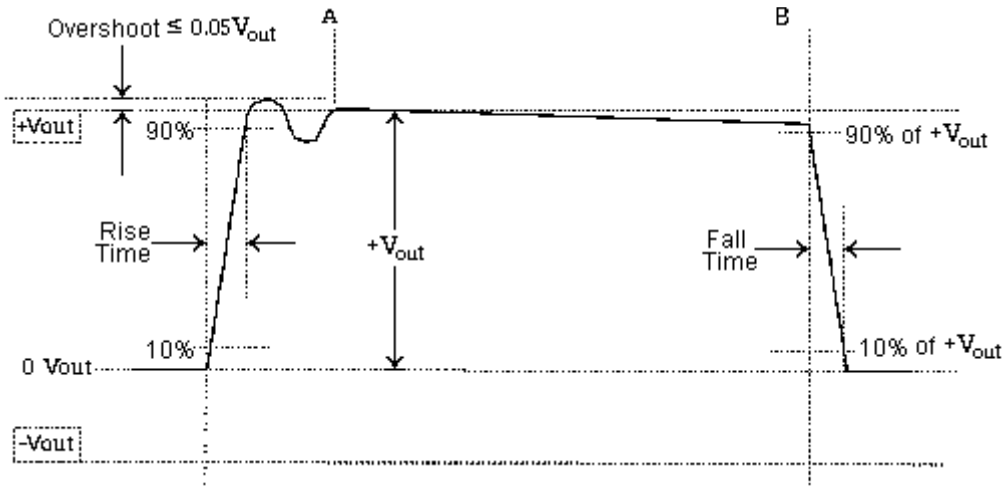

Figure 8-1. Waveform at Active Output Interface[2]

8.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

8.4 Test Fixtures

100 Ω UTP test load (Figure A-1)

8.5 Test Procedure

1. Connect the test equipment and UUT as shown below.

1. ANSI X3.263-1995, p 28.
2. Based on ANSI X3.263-1995, p 29, Figure 12.

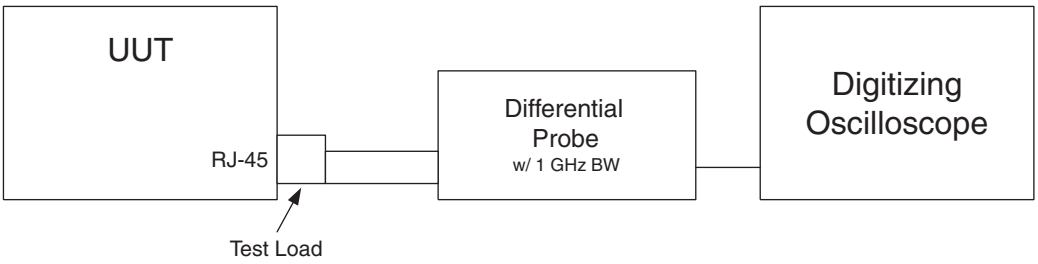

Figure 8-2. Test Setup for 100BASE-TX Differential Output Voltage

2. From the 100BASE-TX PHY Configuration Tests menu in LANConf.exe, select the Amplitude: 9.1.2.2 test.
3. Configure the oscilloscope according to Table 8-1.

Table 8-1. Setting for Positive Differential Output Voltage (UTP)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-150 mV to +1050 mV (1200 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Table 8-2. Setting for Negative Differential Output Voltage (UTP)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-1125 mV to +75 mV (1200 mV over the full vertical scale)
Trigger Type	Negative pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	-500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

4. Select the horizontal cursors. Move one cursor to +Vout and the other to the zero crossing of the waveform. Figure 8-3 can be used as a reference. The differential output voltage is the difference between the two cursors. Vout is defined as the intersection of the straight line best fit for amplitude with the vertical line indicating the start of the transition from 0 V to Vout. This does not include overshoot.

Measuring Peak Voltages

When measuring positive and negative peak voltages, do not use the absolute values on the screen. Often it will appear as thought the start and finish of the MLT-3 waveform do not go through zero. This is caused by the oscilloscope or probes adding in a small DC offset. To record the correct peak values, run one horizontal cursor through the middle of the “zero” of the waveform as shown in Figure 8-3 and Figure 8-4, and use the other cursor to measure the peak by running it though the average final value of the waveform. Record the average value between the two cursors.

5. Record actual values.
6. Repeat steps 4 through 5 on the negative going waveform. Configure the oscilloscope using Table 8-2.
7. Confirm +Vout and -Vout fall within specification.

Note: +Vout should be between 950 mV and 1050 mV. Although it is not specifically mentioned in specification 9.1.2.2, -Vout should also be between -950 mV and -1050 mV.

Figure 8-3 and Figure 8-4 provide examples of data for the differential output voltage measurement.

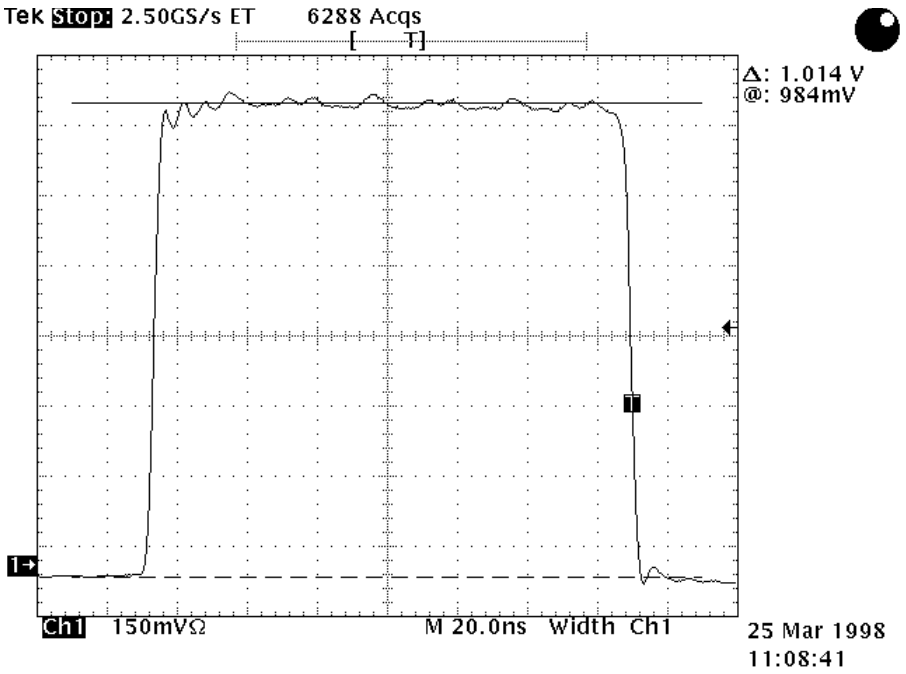

Figure 8-3. Positive Peak Differential Output Voltage (+Vpeak = 1.014 V)

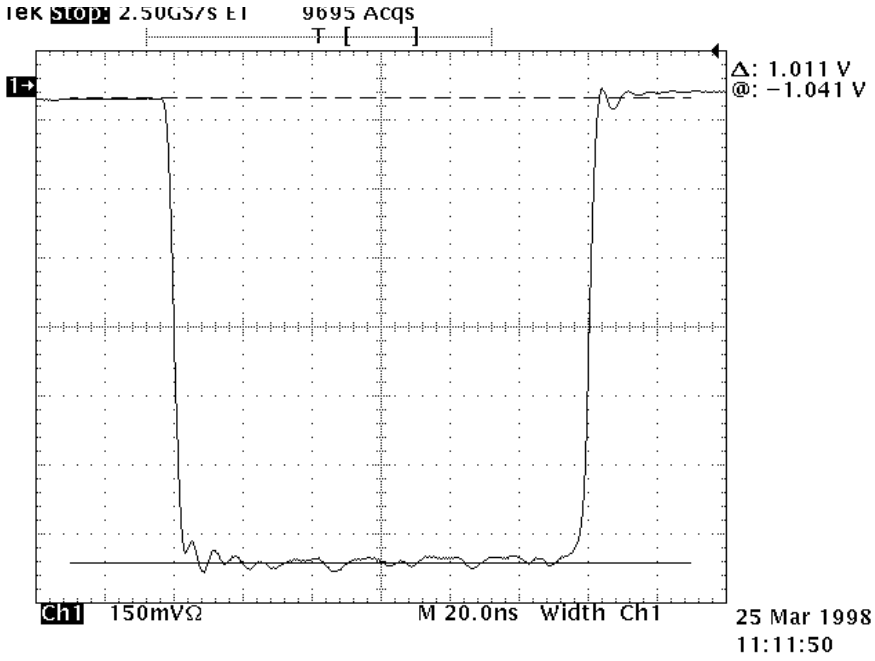

Figure 8-4. Negative Peak Differential Output Voltage (-Vpeak = 1.011 V)

8. Verify the measurements meet specifications

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9 100BASE-TX Waveform Overshoot

ANSI SECTION 9.1.3

9.1 Test Purpose

To measure the overshoot of the differential waveform.

9.2 Specification

"For the purposes of 9.1, overshoot is defined as the percentage excursion of the differential signal transition beyond its final adjusted value, Vout, during the symbol interval following the signal transition. The adjusted value is obtained by performing a straight line best fit to an output waveform consisting of 14 bit times of no transition preceded by a transition from zero to either plus or minus Vout as shown in Figure 9-1.

Vout is defined to be the intersection of the straight line best fit for amplitude with the vertical line indicating the start of the transition from 0 V to Vout.

The differential signal overshoot shall not exceed 5%. Any overshoot or undershoot transient shall have decayed to within 1% of the steady state voltage within [8.0] ns following the beginning of the differential signal transition.[1]

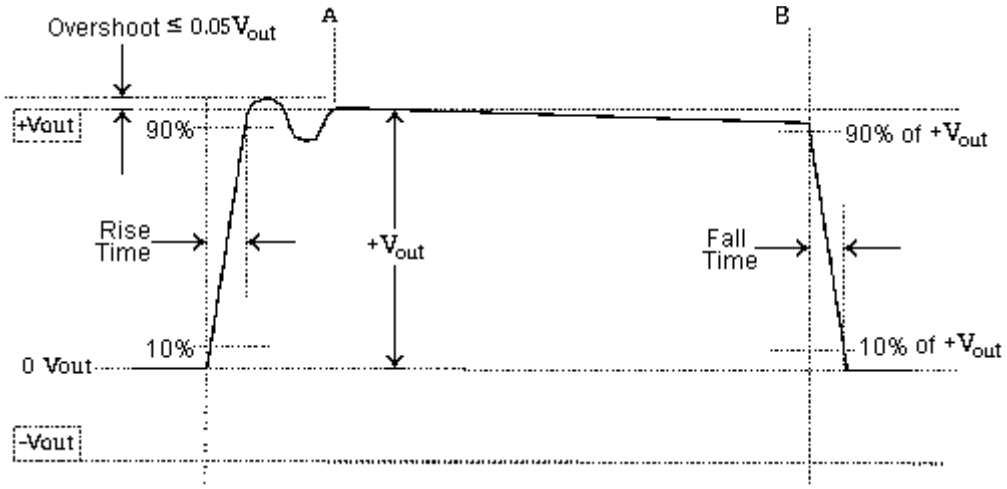

Figure 9-1. Waveform Overshoot at Active Output Interface[2]

1. ANSI X3.263-1995, p 28.
2. Based on ANSI X3.263-1995, p 29, Figure 12.

9.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

9.4 Test Fixtures

100 Ω UTP test load (Appendix A.1)

9.5 Test Procedure

1. Connect the test equipment and UUT as shown below.

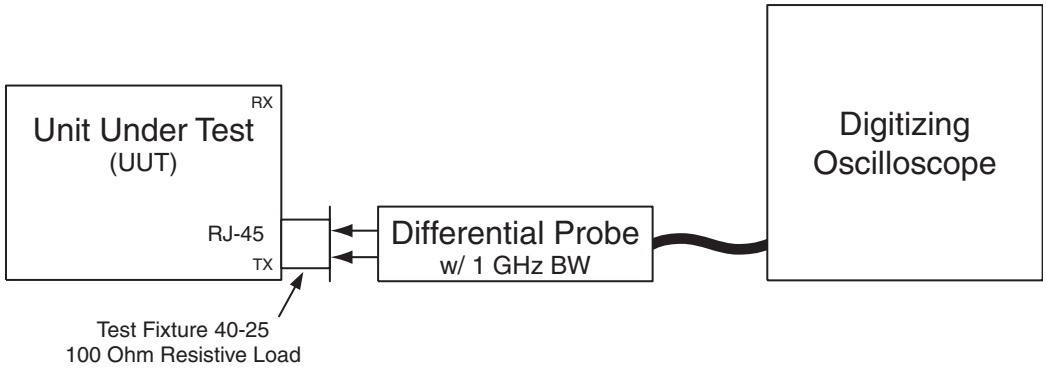

Figure 9-2. Test Setup 1

2. From the 100 BASE-TX PHY Configuration Tests menu in LANConf.exe, select the Amplitude Symmetry: 9.1.2.2 test.
3. Configure the oscilloscope according to Table 9-1.

Table 9-1. Setting for Positive Waveform Overshoot

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-150 mV to +1050 mV (1200 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Table 9-2. Setting for Negative Waveform Overshoot

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-1125 mV to +75 mV (1200 mV over the full vertical scale)
Trigger Type	Negative pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	-500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

4. Select the horizontal cursors. Move one cursor to +Vout and the other cursoro the maximum overshoot voltage.

Note: Overshoot is defined as the difference in voltage between the average peak voltage measured in Section 8 and the peak of the first ripple.

If there is no overshoot visible in step 4, then overshoot settling time is not applicable. The tester should record “not applicable” for overshoot settling time, and testing for “100BASE-TX Waveform Overshoot” is completed (make sure to check for both positive and negative waveform overshoot). An example of a 100BASE-TX waveform without overshoot is shown in Figure 9-3. However, if overshoot is present, the test should proceed to the next step (step 5).

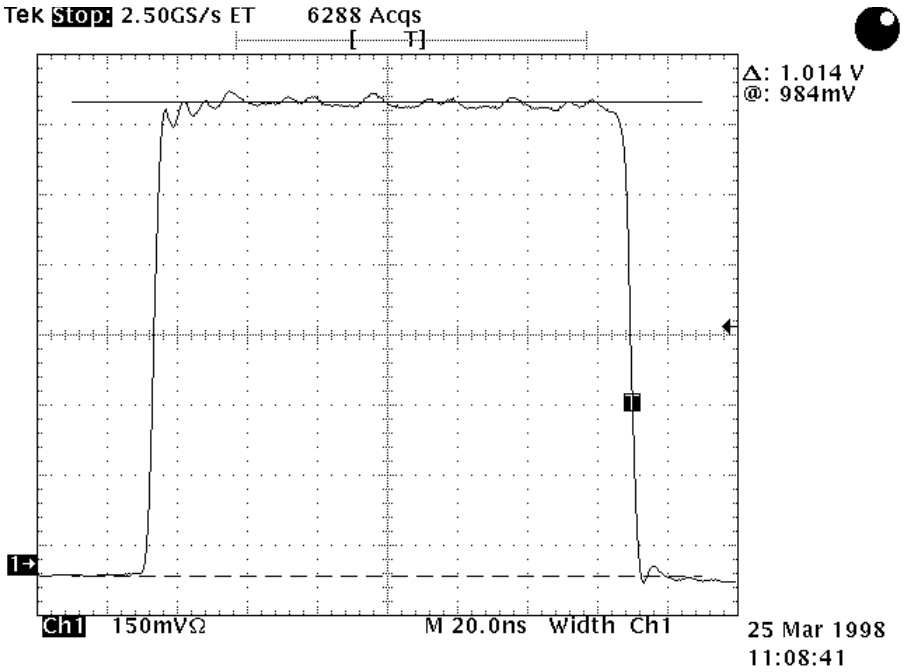

Figure 9-3. Positive Peak Waveform with No Overshoot on the Rising Edge

5. Calculate the overshoot by measuring the number of millivolts that the rising edge exceeds the positive or negative peak voltage (measured in Section 8) and dividing the measured overshoot voltage by the corresponding peak voltage. Multiply the result by 100 to obtain the percentage.
6. Record the results.
7. Select the paired-dot cursors. Move one cursor to the zero voltage crossing and the other cursor to 8 ns beyond the first cursor position.

   The overshoot voltage shall have decayed to within 1% of the steady state voltage within 8 ns following the beginning of the differential signal transition.
8. Repeat steps 3 through 7 using Table 9-2 to measure negative overshoot.

If the negative peak voltage (the voltage delta between the MLT-3 mid-level and the negative pulse top) is -1000 mV and the overshoot voltage is 35 mV, then the percentage overshoot is:

$$\frac{35\text{mV}}{1000\text{mV}} \times 100 = 3.5\,\%$$

Figure 9-4. Calculating Overshoot

9. Verify the measurements meet specifications

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10 100Base-TX Signal Amplitude Symmetry

ANSI SECTION 9.1.4

10.1 Test Purpose

To measure the voltage symmetry of the positive and negative waveforms.

10.2 Specification

"The ratio of the +Vout magnitude to -Vout magnitude shall be between the following limits:

$$0.98 \leq \frac{\left|V_{OUT}\right|}{\left|-V_{OUT}\right|} \leq 1.02 \text{."}$$ [1]

10.3 Test Procedure

1. Perform test described in Section 9 if it has not already been done.
2. Calculate the ratio of +Vout to -Vout using the values from the results of Section 9.
3. Record the results.
4. Verify the measurements meet specifications.

Table 10-1. Calculating the Ratio of +Vout to -Vout

From the plots in Chapter 8: $\frac{1.014V}{1.011V} = 1.003$ $0.98 \leq 1.003 \leq 1.02.$ *Note:* $+V_{OUT}$ and $-V_{OUT}$ have the same units (V).

1. ANSI X3.263-1995, p 29.

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11 100Base-TX Transmitter Return Loss

ANSI SECTION 9.1.5

11.1 Test Purpose

To measure the transmitter return loss.

11.2 Specification

The UTP... Active Output Interface shall be implemented such that the following return loss characteristics are satisfied for each of the specified line impedances.

Greater than 16 dB from 2 MHz to 30 mHz

Greater than (16 - 20log(f/30 MHz)) dB from 30 MHz to 60 MHz [where f = frequency]

Greater than 10 dB from 60 MHz to 80 MHz

The impedance environment for the measurement of the UTP AOI return loss shall be 100 ± 15 Ω. The impedance [environment] shall be nominally resistive, with a magnitude of phase angle less than 3° over the specified measurement frequency range.[1]

11.3 Test Equipment

- Network analyzer (50 KHz to 500 MHz range)
- S-parameter test set (or transmission/reflection test set)
- Host computer running LANConf.exe

11.4 Test Fixtures

- 100Base-TX balun test fixture (Appendix D.2)
- BNC cable, with 50 Ω characteristic impedance (Appendix E)
- Network analyzer calibration fixture (Appendix A.5)
- CAT5 twisted pair cable (under 6 inches in length)

11.5 Test Procedure

1. Connect the test equipment and UUT as shown in Figure 11-1.

1. ANSI X3.263-1995, p 29-30.

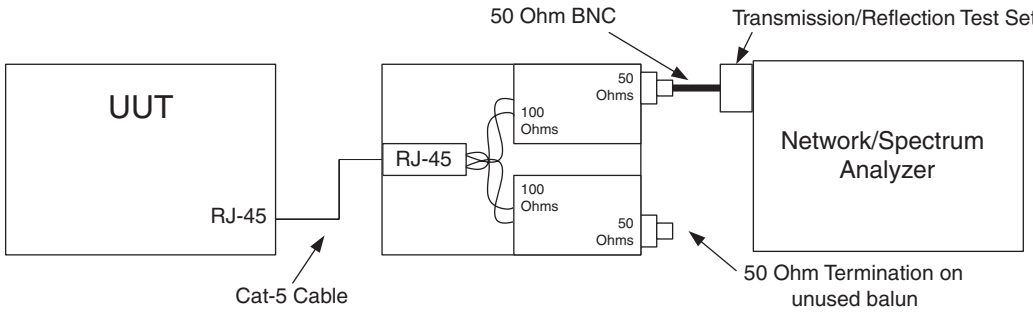

Figure 11-1. Test Setup for 100BASE-TX Transmitter Return Loss

2. Turn on the network analyzer and let it warm up for five to ten minutes.
3. Reset network analyzer to factory default settings.
4. Select the S11 measurement parameter (if necessary).
5. Configure the network analyzer as shown in Table 11-1.

Table 11-1. Network Analyzer Settings for Transmitter Return Loss

Analyzer Parameter	Setting
Start Frequency	1 MHz
Stop Frequency	101 MHz
Display Scale	5 dB/division
IF or Resolution Bandwidth	100 Hz
Triggering	Continuous
Display Points	401 (or as high as possible)

6. Disconnect the test fixture, but keep it close to the UUT.
7. Perform a 1-port, full calibration with an open, short, and 100 Ω load by connecting the calibration fixture to the RJ-45 connection in place of the UUT.

Note: It is important to try to keep the test setup as close as possible to its original position to achieve the best calibration.

8. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$
Balanced output impedance of the balun (for example, 100 Ω).

Z_{load}
The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{|Z_{transmitter} + Z_{load}|}{|Z_{transmitter} - Z_{load}|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{|100\Omega + Z_{load}|}{|100\Omega - Z_{load}|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

$$RL\_in\_dB = 20\log\frac{|100\Omega + 50\Omega|}{|100\Omega - 50\Omega|}$$

which simplifies to:

$$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54\ dB$$

9. From the 100 BASE-TX PHY Configuration Tests menu in LANConf.exe, select the TX Return Loss: 9.1.5 test.

   The resulting display should be similar to Figure 11-2.

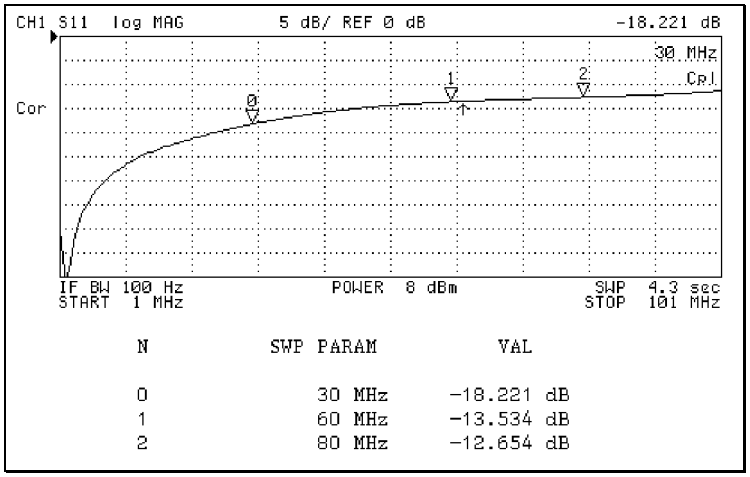

Figure 11-2. Transmitter Return Loss

10. Set the marker to the worst case return loss between 2 MHz and 30 MHz. Record the amplitude (dB of return loss).Repeat step 10 from 30 MHz to 60 MHz and from 60 MHz to 80 MHz.
11. Verify the measurements meet specifications.

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12 100Base-TX Rise and Fall Times

ANSI SECTION 9.1.6

12.1 Test Purpose

To measure the rise and fall times of a non-scrambled bit pattern (both positive and negative waveforms need to be measured).

12.2 Specification

For the purposes of 9.1, the AOI signal rise is defined as a transition from the baseline voltage (nominally zero) to either +Vout or -Vout. Signal fall is conversely defined as a transition from the +Vout or -Vout to the baseline voltage.

The rise and fall times of the waveform shall be determined as the time difference between the 10% and the 90% voltage levels of the signal transition, where 100% is represented by Vout in Figure 12-1.

Measured rise and fall times shall be between the limits: $3.0\ ns \leq t_{rise/fall} \leq 5.0\ ns$.

The difference between the maximum and minimum of all measured rise and fall times shall be ≤ 0.5 ns."[1]

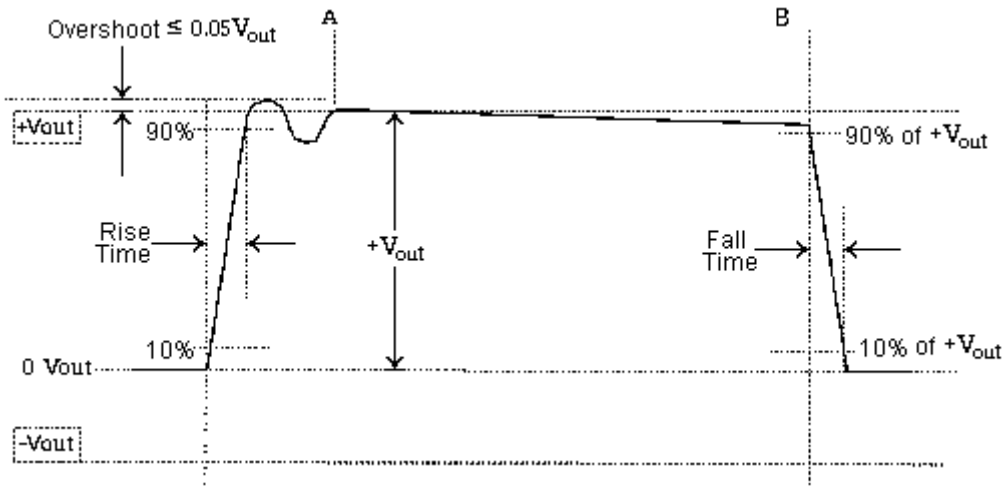


Figure 12-1. Waveform Rise and Fall Times[2]

1. ANSI X3.263-1995, p 30.
2. Based on ANSI X3.263-1995, p 29, Figure 12.

12.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

12.4 Test Fixtures

100 Ω UTP test load (Appendix A.1)

12.5 Test Procedure

1. Connect the test equipment and UUT as shown below.

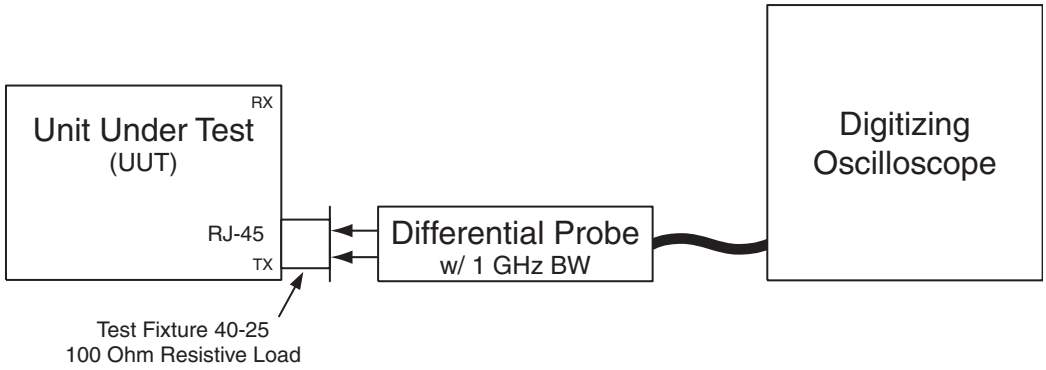


Figure 12-2. Test Setup 1[2]

2. From the 100 BASE-TX PHY Configuration Tests menu in LANConf.exe, select the Rise Fall Times: 9.1.6 test.
3. Configure the oscilloscope according to Table 12-1.

Table 12-1. Setting for Positive Rise and Fall Times

Scope Parameter	Setting
Horizontal Scale	1 ns/division or 0.5 ns/division
Vertical Range	-150 mV to +1050 mV (1200 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Table 12-2. Setting for Negative Rise and Fall Times

Scope Parameter	Setting
Horizontal Scale	1 ns/division or 0.5 ns/division
Vertical Range	-1125 mV to +75 mV (1200 mV over the full vertical scale)
Trigger Type	Negative pulse width triggering: 116 ns lower bound, 128 ns upper bound
Trigger Level	-500 mV
Record Length	Large enough to enable viewing of one complete MLT-3 (3-level) waveform by scrolling horizontally
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

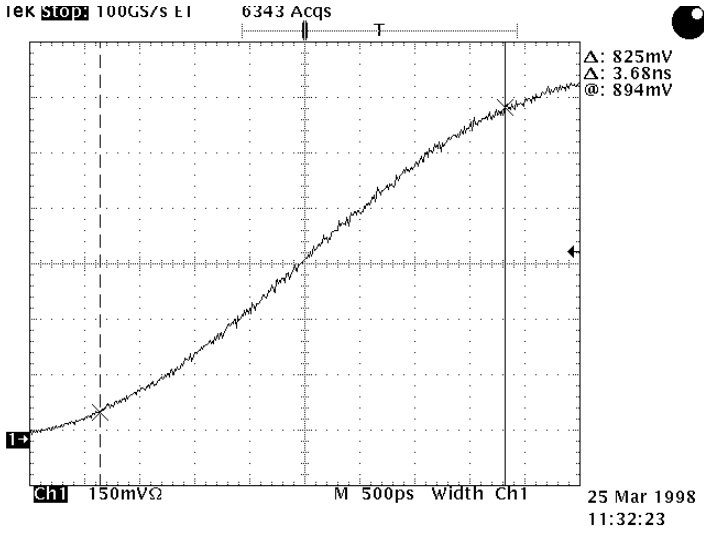
1. Set the trigger level to approximately 500 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 200 ns and the lower bound parameter to approximately 116 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

4. Locate the actual position of the peak voltage and the zero. Use the measurements from Section 9 plus the actual zero and peak voltage measurements to calculate the 10% and 90% voltage levels.
5. Zoom in on the positive waveform, expanding the rising edge of the wave so that it occupies as much of the screen as possible. See example measurement in Figure 12-3.
6. Select the split-dot (vertical pair) cursors. Move one cursor to 10% of +Vout on the rising edge of the waveform and the other cursor to 90% of +Vout on the rising edge as illustrated in Figure 12-3 and Figure 12-4.

Note: The rise time is the difference in time (Dt) between the two markers.

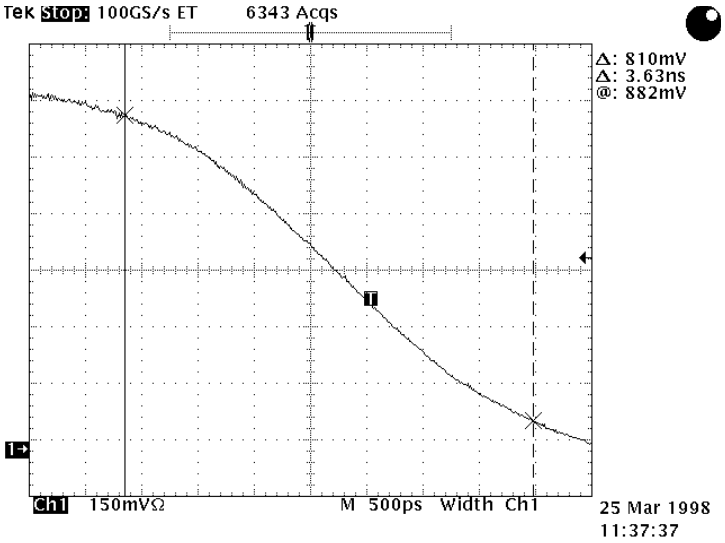
7. Repeat steps 6 and 7 for positive fall time.

8. Record the results. Confirm that the rise and fall times are between $3.0\ ns \leq t_{rise/fall} \leq 5.0\ ns$.
9. Repeat steps 3 through 9 for the negative-going waveform (Figure 12-5 and Figure 12-6) using Table 12-2 to setup the oscilloscope.
10. Confirm that the difference between the maximum and minimum of all measured rise and fall times is less than or equal to 0.5 ns.
11. Verify the measurements meet specifications.



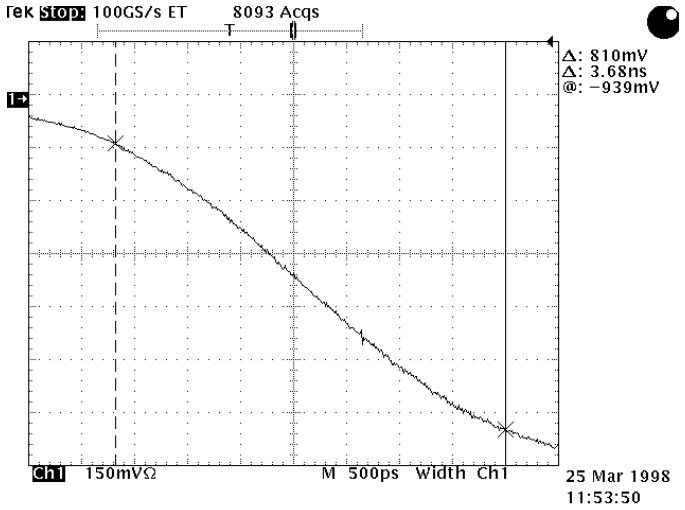
1 = The rise time (Δt) in Figure 12-3 is measured to be 3.68 ns.

Figure 12-3. Positive Rise Time Measurement



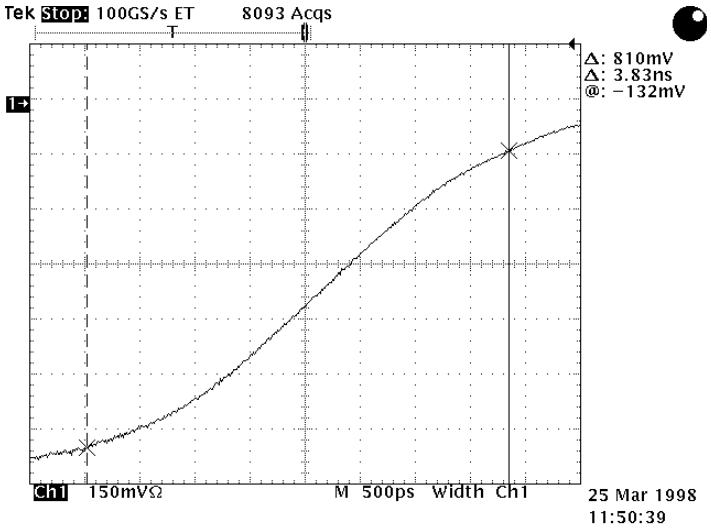
1 = The fall time (Δt) in Figure 12-4 is measured to be 3.63 ns.

Figure 12-4. Positive Fall Time Measurement



1 = The rise time (Δt) in Figure 12-5 is measured to be 3.68 ns.

Figure 12-5. Negative Rise Time Measurement



1 = The fall time (Δt) in Figure 12-6 is measured to be 3.83 ns.

Figure 12-6. Negative Fall Time Measurement

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13 100Base-TX Duty Cycle Distortion (DCD)

ANSI SECTION 9.1.8

13.1 Test Purpose

To measure the duty cycle at the four MLT-3 transitions using a pattern in non-scrambled mode.

13.2 Specification

Duty cycle distortion shall be measured at the 50% voltage points on rise and fall transitions of the differential output waveform. The 50% times at the four successive MLT-3 transitions generated by a 01010101 NRZ [non-return to zero] bit sequence shall be used. The deviations of the 50% crossing times from a best fit to a time grid of 16 ns spacing shall not exceed ±0.25 ns as shown in Figure 13-1.

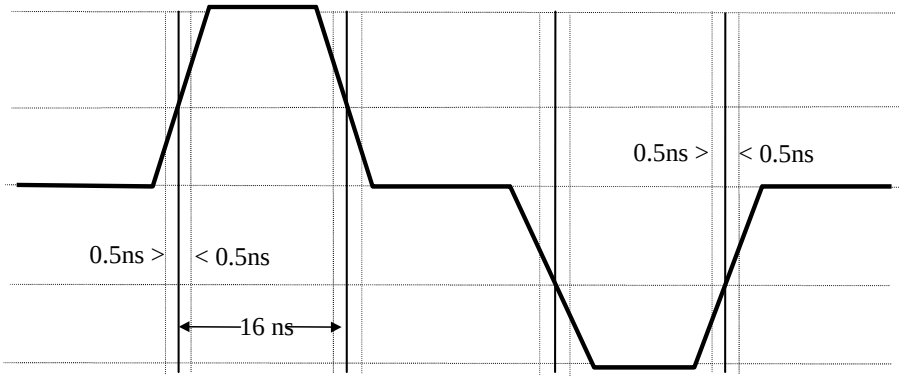

Figure 13-1. Active Output Interface Duty Cycle Distortion

13.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

13.4 Test Fixtures

100 Ω UTP test load (Appendix A.1)

1. ANSI X3 263-1995, p.28.
2. Based on ANSI X3 263-1995, p.30, Figure 9-3.

13.5 Test Procedure

1. Connect the test equipment and UUT as shown below.

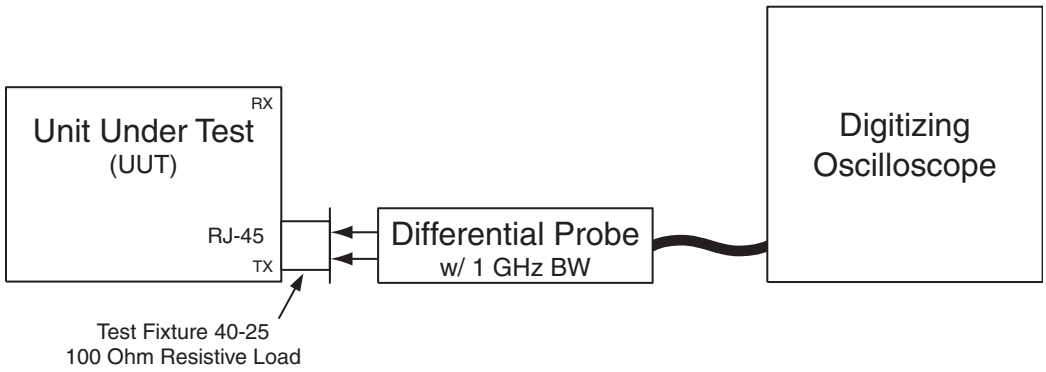

Figure 13-2. Test Setup 1

2. From the 100 BASE-TX PHY Configuration Tests menu, select the Duty Cycle Distortion: 9.1.8 test.
3. Configure the oscilloscope according to the following table.

Table 13-1. Setting for Duty Cycle Distortion (DCD)

Scope Parameter	Setting
Horizontal Scale	~5 ns/division
Vertical Range	-1200 mV to +1200 mV (2400 mV over the full vertical scale)
Trigger Type	Positive pulse width triggering: ~14 ns lower bound, ~18 ns upper bound
Trigger Level	400 mV
Display Type	Average

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level to approximately 400 mV.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 30 ns and the lower bound parameter to approximately 2 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 5 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 5 ns to 15 ns above the lower trigger bound parameter.

4. Measure the relative peak voltage of the waveform.
5. Calculate the 50% values. See Figure 13-3.

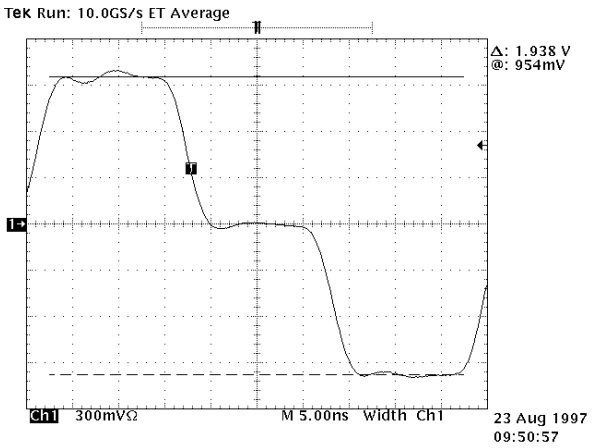

Figure 13-3. 16 ns Pulse Peaks Used to Calculate 50% Levels

6. Zoom in on the waveform to get the best resolution.
7. Select the split-dot (paired) cursors. Move on cursor to +Vout/2 on the rising edge of the waveform and move the other cursor to +Vout/2 on the falling edge of the waveform. See Figure 13-4.
8. Confirm that the deviations of the 50% crossing times do not exceed ±0.25 ns. In other words, the pulse should conform to the following: 15.50 ns ≤ Pulse Width ≤ 16.50 ns.
9. Record the results.
10. Repeat steps 4 through 9 for the mid-level negative waveform, as shown in Figure 13-5 and Figure 13-6.
11. Verify the measurements meet specifications.

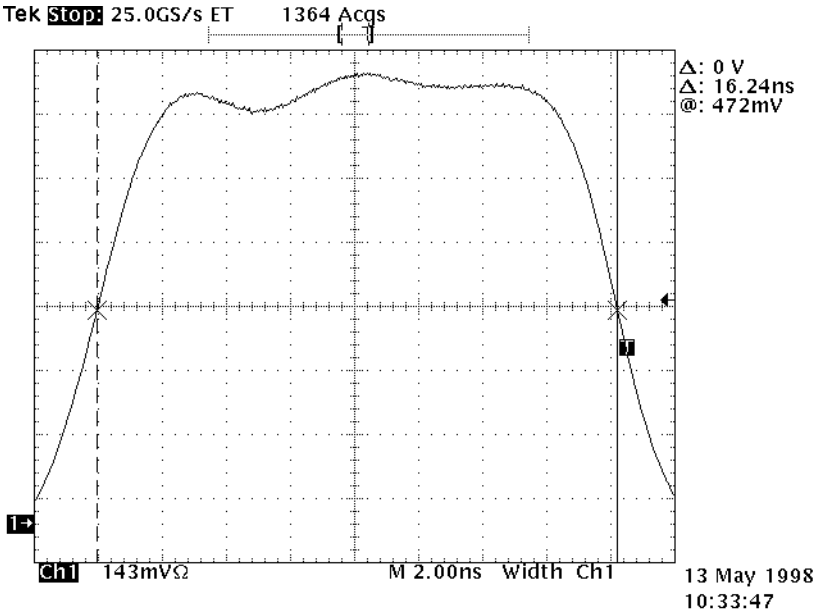

Figure 13-4. Positive Pulse Width at 50%

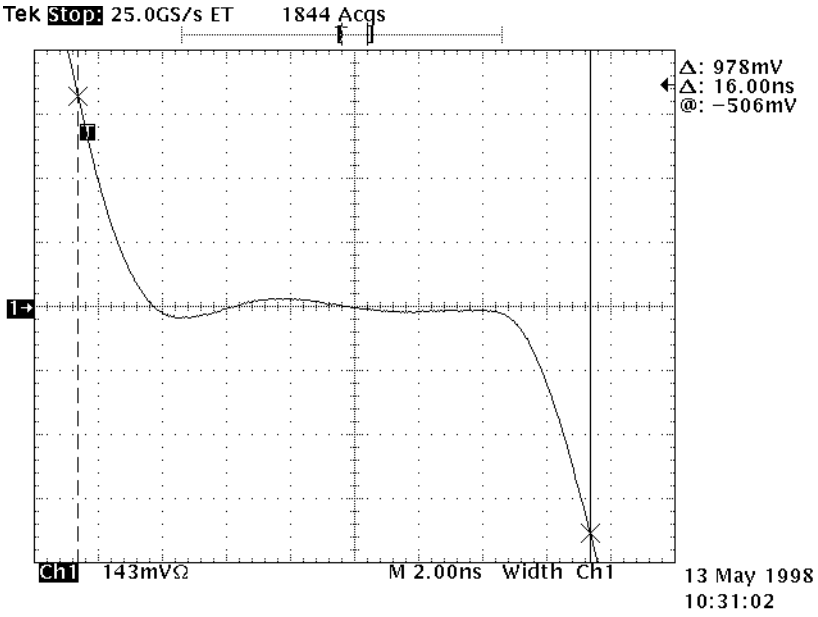

Figure 13-5. MLT-3 mid-level width at 50% levels

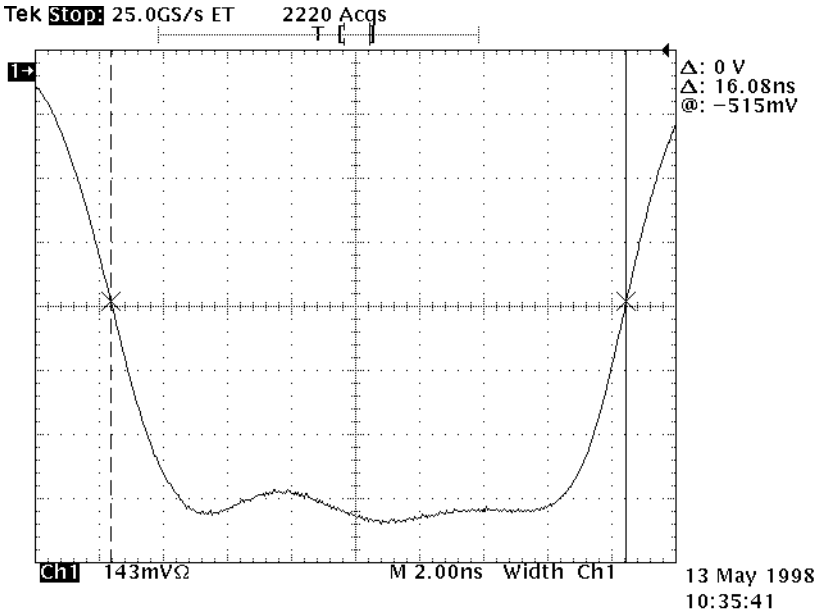

Figure 13-6. Negative pulse width at 50% amplitude level

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14 100Base-TX Transmit Jitter

ANSI SECTION 9.1.9

14.1 Test Purpose

To measure the jitter of a scrambled waveform output from the UUT.

14.2 Specification

"Peak to peak jitter shall be measured using the scrambled HALT line state. Total transmit jitter, including contributions from duty cycle distortion and Baseline Wander, shall not exceed 1.4 ns peak [to] peak."

14.3 Test Equipment

- Oscilloscope with at least 1 GHz bandwidth
- Differential probe with at least 1 GHz bandwidth and capacitance less than or equal to 1 pF
- Host computer running LANConf.exe

14.4 Test Fixtures

100 Ω UTP test load (Appendix A-1)

14.5 Test Procedure

1. Connect the test equipment and UUT as shown below.

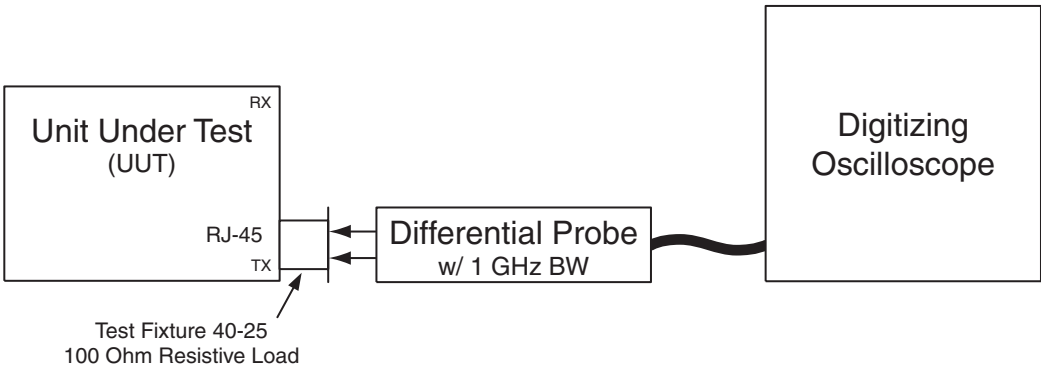


Figure 14-1. Test Setup 1

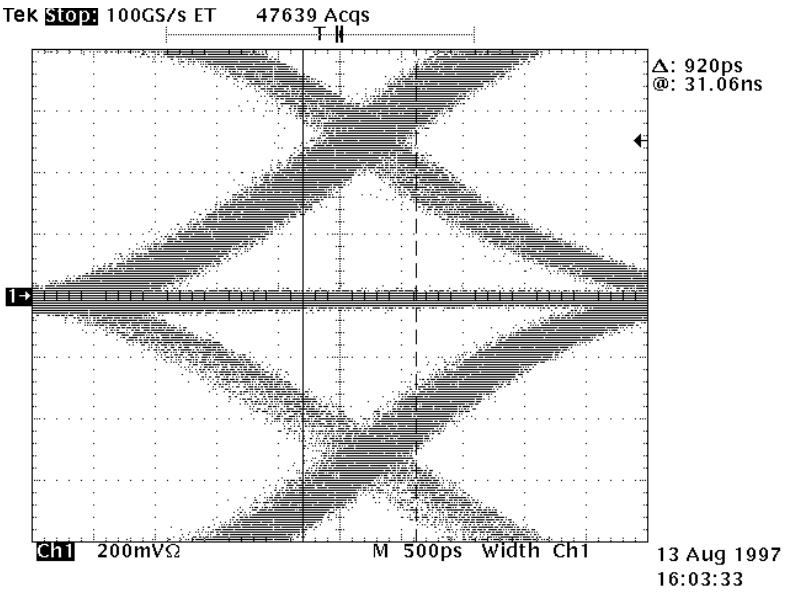
2. From the 100 BASE-TX PHY Configuration Tests menu, select the Jitter: 9.1.9 test
3. Configure the oscilloscope according to the Table 14-1.

ANSI X3.263-1995, p 31

Table 14-1. Setting for Transmit Jitter

Scope Parameter	Setting
Horizontal Scale	~500 ps/division
Vertical Range	-800 mV to +800 mV (1600 mV over the full vertical scale)
Trigger Type	Positive edge triggering
Trigger Level	500 mV
Display Type	Infinite persistence

4. Scroll horizontally until an eye pattern is found similar to that shown in Figure 14-2.



Note: The jitter of the waveform in Figure 14-2 is measured at 920ps.

Figure 14-2. Transmit Jitter Data

5. Allow data to accumulate for one to ten minutes.
6. Use the scope's vertical bar cursors to measure the widest "X" as shown in Figure 14-2.
7. Record the results.
8. Confirm that the resulting jitter is less than 1.4 ns.
9. Verify the measurements meet specifications.

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15 100Base-TX Differential Input Signals (BER)

ANSI SECTION 9.2.1

15.1 Test Purpose

To measure the Bit Error Rate (BER) of the UUT over CAT5 cable with specified insertion loss.

15.2 Specification

"The differential transmitted signals on TX+/- must meet the requirements of Section 9.1 of the ANSI X3.263 specification." See Sections 8 - 14 of this document. The receiver shall have a bit error rate of less than 10^{-8}.

This requirement can be accomplished by performing receive bit error rate tests with specification compliant Category 5 cables across a range of lengths from approximately 1 meter to greater than 100 meters (maximum specification). Insertion loss measurements and propagation delay measurements have shown high-quality Category 5 cable ranging from 115 m to 130 m may be equal to a maximum specification cable (depending on the vendor and the cable manufacturing lot). See Appendix E for details on constructing LAN cables.

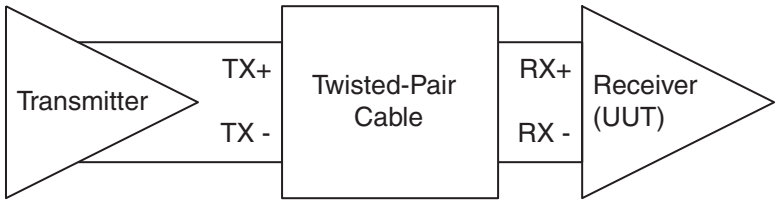

Figure 15-1. Differential Input Signals[2]

15.3 Test Equipment

- Transmit computer with a Network Interface Card (NIC) or LAN On Motherboard (LOM) running LANConf.exe
- Host computer running LANConf.exe

15.4 Test Fixtures

Various lengths of Category 5 cable between 1 and 100 meters.

15.5 Test Procedure

1. Connect the UUT and the link partner using the desired Category 5 cable length and verify that a gigabit link has been established.

1. ANSI X3 263-1995, p. 32
2. Based on ANSI X3 263, p32, Figure 15.

2. On the receiving system, go to the Transmit and Receive menu, and select the Receive option.
3. On the UUT, go to the Transmit and Receive menu, and select the Transmit option.
4. Allow the proper number of frames to be sent (see Section 15.6).
5. After transmissions is complete, press the <Esc> key on the receiver first and then the transmitter to stop the test and record the following results:
   a. Link partner: Transmit Good Packets and Transmit Total Packets
      Both of these statistics should equal each other.
   b. UUT: Receive Good Packets and Missed Packets.
6. Calculate the bit error rate (BER).
7. Repeat steps 1 through 7 for each cable length.
8. Verify the measurements meet specifications.

15.6 Calculating Bit Error Rate (BER)

The basic BER equation is as follows:

$$BER = \frac{TGP - MP - RGP}{TGP \times BF \times BB}$$

where:

- TGP = number of good frames transmitted (#_Transmit_Good_Packets)
- MP = number of missed packets (#_Missed_Packets)
- RGP = number of good frames received (#_Receive_Good_Packets)
- BF = number of bytes/frame
- BB = 8 (number of bits/byte)

Note: Conditions where the transmit link partner overwhelms the receive unit should be avoided. When this happens, the receive statistics counters may show “RX No Resources”, “RX No Buffers”, or a large number of missed packets. This complicates the BER calculation and the equations for the calculations will not yield accurate BER numbers. The TX transmit speed (frames per second) can be decreased to prevent this condition. Alternatively, the test operator can try to make sure the receive unit is always in a faster PC than the transmit unit.

If 1,199,995 good frames were received and 1,200,000 good frames were transmitted, then for 1,024 byte frames and zero missed packets the BER would be as follows:

$$BER = ((1{,}200{,}000 - 0) - 1{,}199{,}995)/(1{,}200{,}000*1{,}024*8) = 5.09 \times 10\text{^-}10$$

This example passes because the resulting BER is less than 1×10^{-8},, which is the maximum specification.

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16 100Base-TX Receiver Return Loss

ANSI SECTION 9.2.2

16.1 Test Purpose

To measure the receiver return loss.

16.2 Specification

"The differential input impedance shall be such that the return loss is as shown below. The requirement is specified for any reflection due to differential signals incident upon RX +/- from a twisted pair having any impedance within the range specified in [ANSI X3.263 Section] 11.1.1. The return loss shall be maintained when the receiver circuit is powered.

- Greater than 16 dB from 2 MHz to 30 mHz
- Greater than (16 - 20log(f/30 MHz)) dB from 30 MHz to 60 MHz [where f = frequency]
- Greater than 10 dB from 60 MHz to 80 MHz"[1]

The impedance environment for the measurement of the UTP AII (Active Input Interface) return loss shall be 100 Ω ± 15 Ω. The impedance environment shall be nominally resistive with a magnitude of phase angle less than 3° over the specified measurement frequency range.

16.3 Test Equipment

- Network analyzer (50 KHz to 500 MHz range)
- S-parameter test set (or transmission/reflection test set)
- Host computer running LANConf.exe

16.4 Test Fixtures

- 100Base-TX balun test fixture (Appendix D.2)
- BNC cable, with 50 Ω characteristic impedance (Appendix E)
- Network analyzer calibration fixture (Appendix A.5)
- CAT5 twisted pair cable (under 6 inches in length)

16.5 Test Procedure

1. Turn on the network analyzer and let it warm up for five to ten minutes.
2. Reset network analyzer to factory default settings.
3. Select the S11 measurement parameter if necessary.
4. Connect the test equipment and UUT as shown in Figure 16-1.

1. ANSI X3.263-1995, p 32

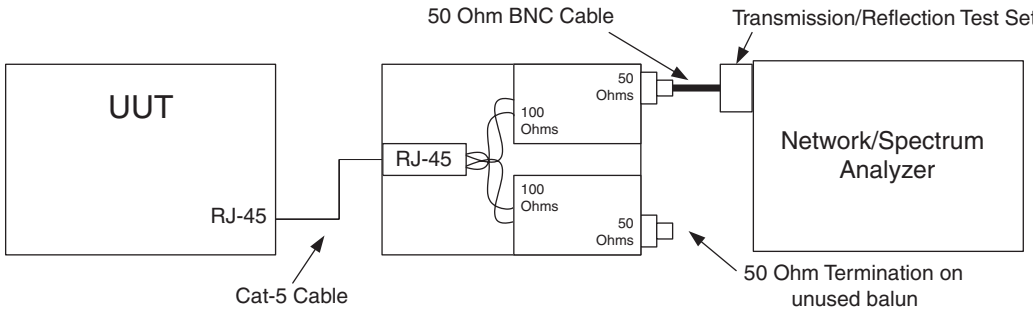


Figure 16-1. Test Setup for 100BASE-TX Receiver Return Loss

5. Disconnect the test fixture, but keep it close to the UUT.
6. Perform a 1-port, full calibration with an open, short, and 100 Ω load by connecting the calibration fixture to the RJ-45 connection in place of the UUT.

Note: It is important to try to keep the test setup as close as possible to its original position to achieve the best calibration.

7. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$
Balanced output impedance of the balun (for example, 100 Ω).

Z_{load}
The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{\left|Z_{transmitter} + Z_{load}\right|}{\left|Z_{transmitter} - Z_{load}\right|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{\left|100\Omega + Z_{load}\right|}{\left|100\Omega - Z_{load}\right|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

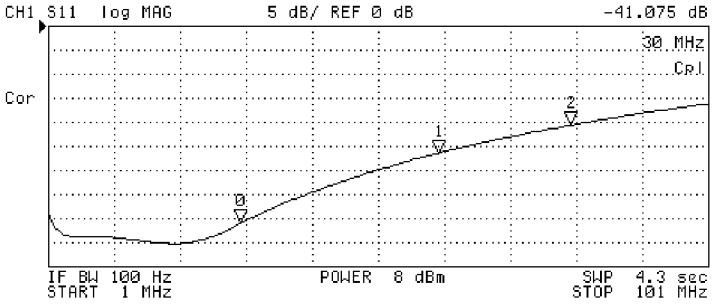
$$RL\_in\_dB = 20\log\frac{\left|100\Omega + 50\Omega\right|}{\left|100\Omega - 50\Omega\right|}$$

which simplifies to:

$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54$ dB

8. From the 100 BASE-TX PHY Configuration Tests menu in LANConf.exe, select the RX Return Loss: 9.2.2 test.
9. Reconnect the test fixture to the UUT.

The resulting network analyzer display should be similar to Figure 16-2.



N	SWP PARAM	VAL
0	30 MHz	-41.075 dB
1	60 MHz	-26.42 dB
2	80 MHz	-20.598 dB

Figure 16-2. Receiver Return Loss Data

10. Set the marker to the worst case return loss between 2 MHz and 30 MHz. Record the amplitude (dB of return loss).
11. Repeat step 11 from 30 MHz to 60 MHz and from 60 MHz to 80 MHz.
12. Verify the measurements meet specifications.

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17 10Base-T Peak Differential Output Voltage on TD Circuit

ANSI SECTION 1411.10.02

17.1 Test Purpose

To verify the TD circuit peak differential output voltage

17.2 Specification

The peak differential output voltage on the TD circuit when terminated with a 100-ohm resistive load shall be between 2.2 V-pk and 2.8 V-pk for all data sequences.

17.3 Test Equipment

- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater Bandwidth)
- Host computer running LANConf.exe

17.4 Test Fixtures

100 Ω resistive load (Appendix A)

17.5 Test Procedure

1. Connect the test equipment and UUT as shown in Figure 17-1.

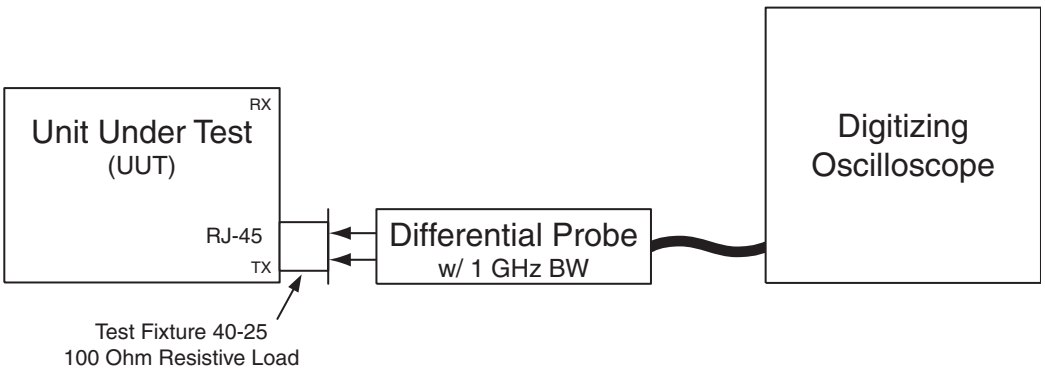

Figure 17-1. Setup for 10BASE-T Peak Differential Output Voltage on TD Circuit

2. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Amplitude 5MHz: 1411.10.02 test.
3. Configure the oscilloscope according to the table below.

Table 17-1. Scope Configuration for Peak Differential Output Voltage on TD Circuit

Scope Parameter	Setting
Horizontal Scale	10 to 50 ms/division
Vertical Scale	-3.1 V to +3.1 V (at 10 vertical divisions, use 620 mV/ division; at 8 divisions, use 775 mV/division)
Trigger Type	Pulse width: ~148 ns (lower bound); ~364 ns (upper bound)
Trigger Level	Typically 0.5 V to 1.7 V.

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specified in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

4. Locate the 5 MHz signal after a stable trigger is obtained and measure positive and negative peak voltages. See Figure 17-2. Locate regions of three periods for each signal to ensure the peak voltage is not affected by transitioning from a 5 MHz signal to a 10 MHz signal or from a 10 MHz signal to a 5 MHz signal.

'

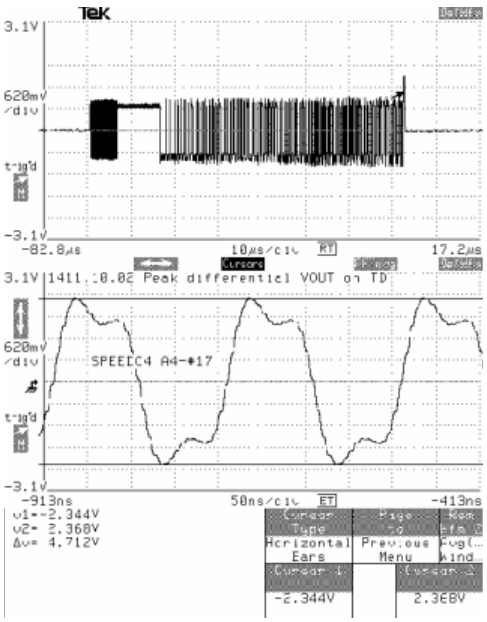

Figure 17-2. Example 5MHz Measurement

5. Record the values.
6. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Amplitude 10MHz: 1411.10.02 test.
7. Repeat step 3.
8. Locate the 10MHz signals after a stable trigger is obtained and measure positive and negative peak voltages. See Figure 17-3. Locate regions of three periods for each signal to ensure the peak voltage is not affected by transitioning from a 5 MHz signal to a 10 MHz signal or from a 10 MHz signal to a 5 MHz signal.
9. Record the values.
10. Verify the measurements meet specifications.

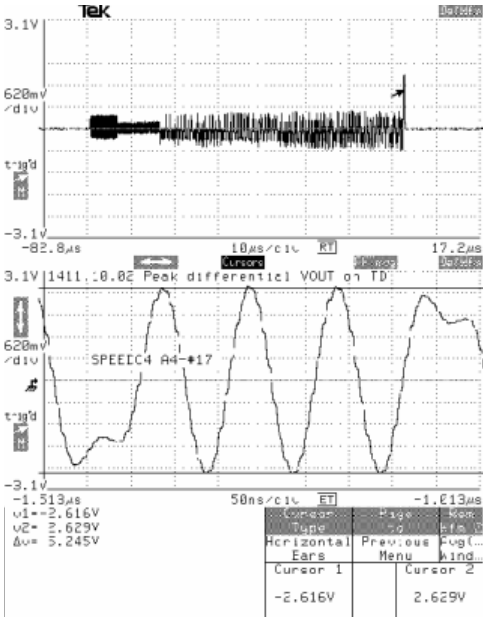

Figure 17-3. Example 10MHz Measurement

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18 10Base-T Harmonic Content

ANSI SECTION 1411.10.03

18.1 Test Purpose

To verify the harmonic content at the transmitter output.

18.2 Specification

When the UUT is driven by an all ones Manchester signal, each harmonic measured at the output of the transmitter shall be at least 27 dB below the fundamental frequency.

18.3 Test Equipment

- Spectrum Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance

18.4 Test Fixtures

Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D.5)

18.5 Test Procedure

1. Insert CAT 5 cable into transmitter side of Balun fixture and connect Balun to Spectrum Analyzer (or Network Analyzer) through a BNC cable as shown in Figure 18-1.

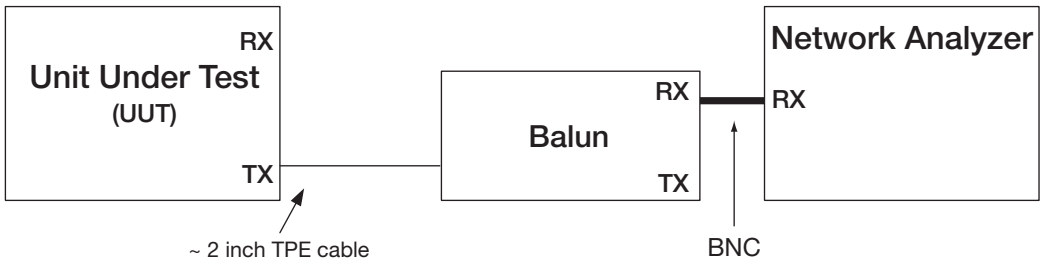


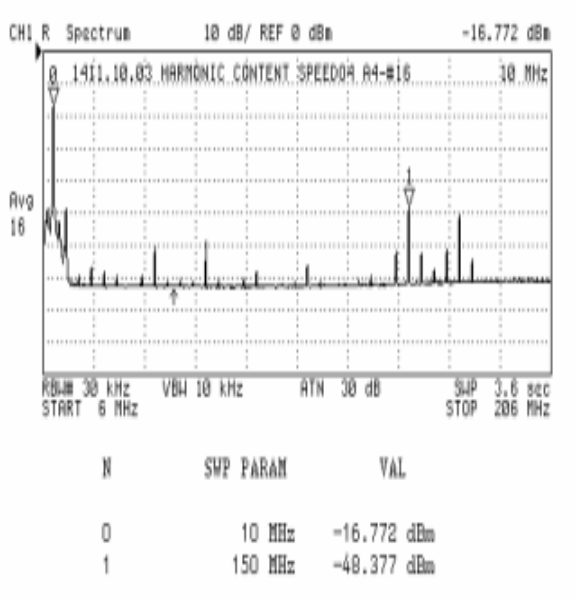
Figure 18-1. Test Setup for 10Base-T Harmonic Content

2. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Harmonic Content: 1411.10.03 test.
3. Adjust the spectrum analyzer as indicated below.

Table 18-1. Analyzer Configuration for Harmonic Content

Scope Parameter	Settings
Start Frequency	6 Mhz
Stop Frequency	206 MHz (a pre-scan to 500 MHz is okay)
Resolution BW or IF BW	Lowest practical BW supported by equipment in the range of 10 KHz and 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Spectrum Analyzer

4. Place a marker on 10 MHz (fundamental frequency) and the highest amplitude harmonic (must be a multiple of 10 MHz) between 6 MHz and 206 MHz. The figure below provides a reference.



Note: For a better display, The end frequency can be reduced to be closer to the frequency of the highest amplitude harmonic. The signal may need to be attenuated if it is out of range on the spectrum analyzer.

5. Record dBm at 10 MHz and dBm at highest amplitude harmonic. The difference between the two markers must be greater than 27 dBm to ensure compliance with IEEE standards and specifications.
6. Verify the measurements meet specifications.

§ §

19 10Base-T TD Circuit Impedance (Transmitter Return Loss)

ANSI SECTION 1411.10.07

19.1 Test Purpose

To measure the transmitter return loss.

19.2 Specification

The return loss shall be ≥ 15dB from 5 MHz to 10 MHz

19.3 Test Equipment

- Network Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance

19.4 Test Fixtures

- Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D.5)
- Load Fixture for Network Analyzer calibration (Appendix A.5)

19.5 Test Procedure

1. Insert CAT 5 cable from the UUT into transmitter side of Balun fixture and connect Balun to Network Analyzer with BNC cable as shown in Figure 19-1.

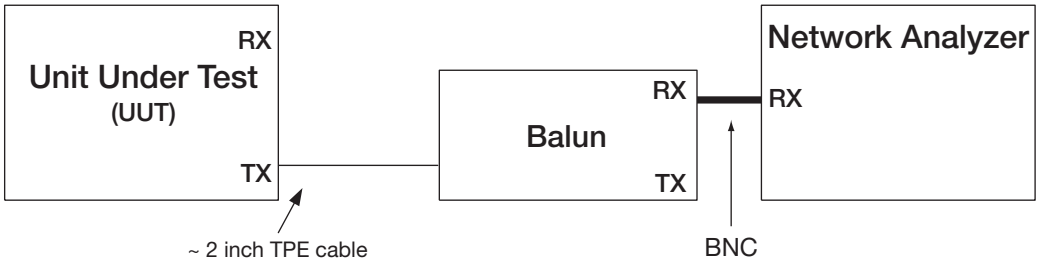


Figure 19-1 Test Setup for 10Base-T TD Circuit Impedance (Transmitter Return Loss)

2. Adjust the spectrum analyzer to the following settings.

Table 19-1 Analyzer Configuration for TD Circuit Impedance

Scope Parameters	Settings
Start Frequency	3 MHz
Stop Frequency	13 MHz
IF BW or Resolution BW	Lowest practical bandwidth supported by equipment in the range of 100 KHz and 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Network Analyzer

3. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Harmonic Content: 1411.10.07 test.
4. Connect the CAT 5 cable to the UUT as shown above.
5. Perform a calibration on the S11, S-parameter, port and turn correction on.
6. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$ Balanced output impedance of the balun (for example, 100 Ω).

Z_{load} The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{|Z_{transmitter} + Z_{load}|}{|Z_{transmitter} - Z_{load}|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{|100\Omega + Z_{load}|}{|100\Omega - Z_{load}|}$$

For a 50 Ω load with the 100 Ω output of the balun, this becomes:

$$RL\_in\_dB = 20\log\frac{|100\Omega + 50\Omega|}{|100\Omega - 50\Omega|}$$

which simplifies to:

$$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54\ dB$$

7. Set the marker to the worst-case return loss between 5 MHz and 10 MHz inclusive. (The figure below provides a reference.)
8. Record the amplitude (dB) of the return loss.
9. Verify the measurements meet specifications.

§ §

20 10Base-T TD Circuit Common-Mode Output Voltage

ANSI SECTION 1411.10.09

20.1 Test Purpose

To measure and record the common-mode output voltage of the transmitter.

20.2 Specification

Common-mode voltage shall be less than 50 mV peak.

20.3 Test Equipment

- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- Computer running LANConf.exe

20.4 Test Fixtures

Test Fixture 14-14 (Appendix D.6)

20.5 Test Procedure

1. Insert test fixture into the UUT and attach differential probe and BNC cable to common-mode terminals on the fixture as shown in Figure 20-1.

Note: It is important to pay close attention to the grounding of test fixture 14-14. Inadequate grounding may lead to erroneous results. All ground connections should be as short as possible and continuous. It is import to ensure that the ground on test fixture 14-14is connect to a stable (not floating) ground through the RJ-45 of the UUT.

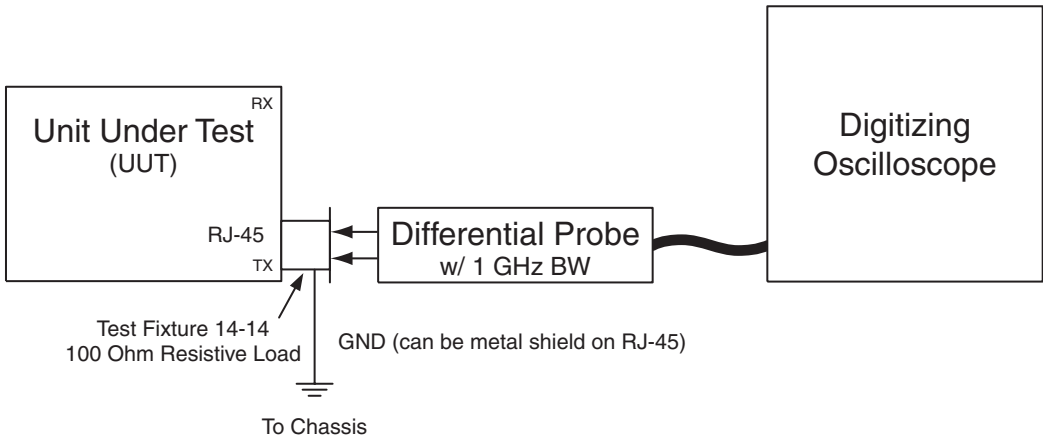


Figure 20-1 Test Setup for 10BASE-T TD Circuit Common-Mode Output Voltage

2. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Common Mode Output: 1411.10.09 test
3. Set scope settings for positive common-mode measurement as shown in the table below.

Table 20-1 Scope Configuration for TD Circuit Positive Common-Mode Output Voltage

Scope Parameter	Setting
Horizontal Scale	25 ns/division
Vertical Scale	-80 mV to +80 mV (at 8 divisions, this equals 20 mV/ division)
Trigger Type	Positive edge
Trigger Level	Typically 0 V to +50 mV
Display Persistence	Infinite persistence

4. Adjust trigger level until just triggering on signal. Place cursor on maximum or peak voltage. (The figure below provides a reference for the positive peak.)

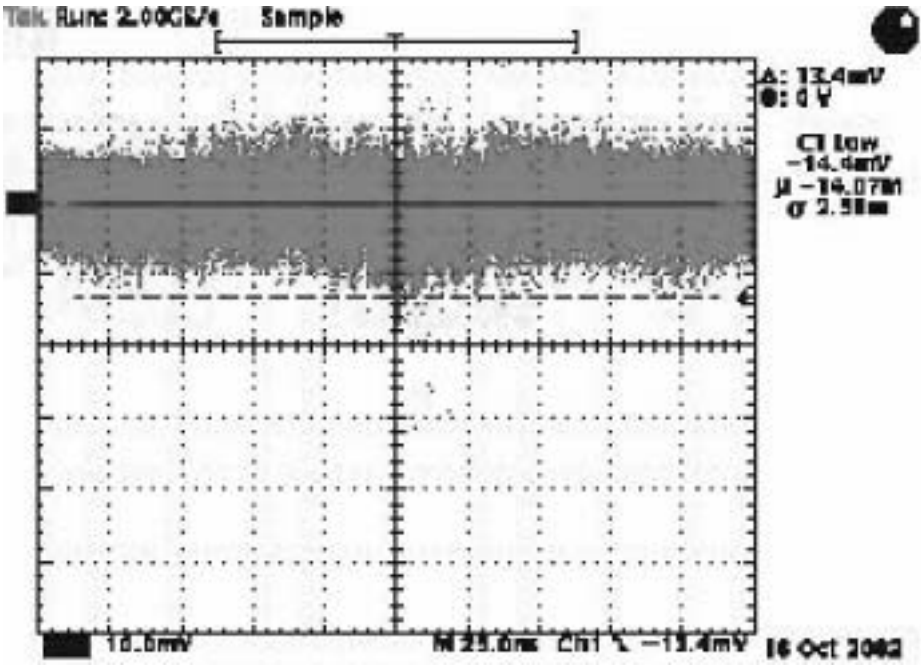


Figure 20-2 Positive Peak Voltage Scope Reference

5. Record max peak positive amplitude value.
6. Set scope settings for negative common-mode measurement as shown in the table below.

Table 20-2 Scope Configuration for TD Circuit Negative Common Mode Output Voltage

Scope Parameter	Setting
Horizontal Scale	10 ns/division
Vertical Scale	-80 mV to +80 mV (at 8 divisions, this equals 20 mV/ division)
Trigger Type	Negative edge
Trigger Level	Typically 0 V to -50 mV
Display Persistence	Infinite persistence

7. Adjust trigger level until just triggering on signal. Place cursor on maximum or peak voltage. (The figure below provides a negative peak reference.)

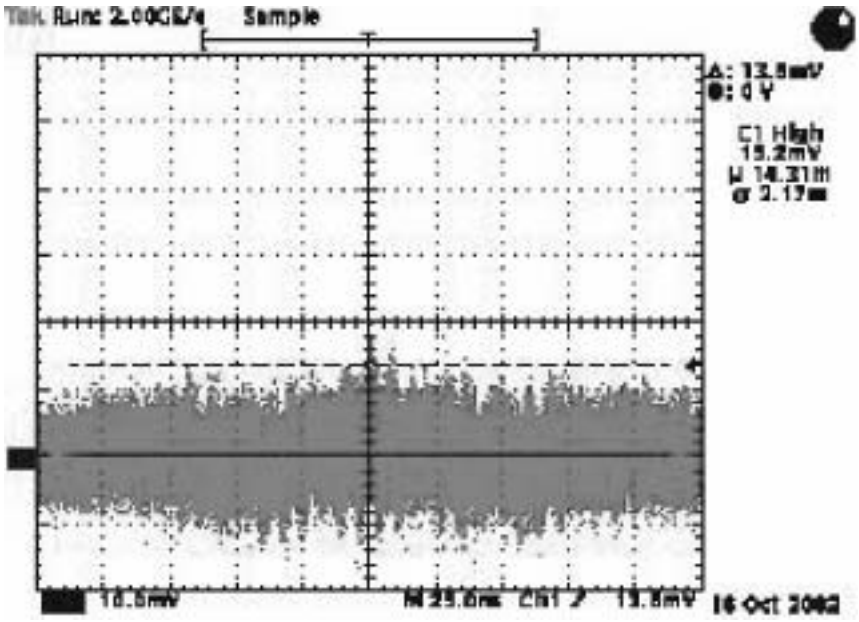


Figure 20-3 Negative Peak Voltage Scope Reference

8. 8.Record maximum or peak amplitude value(s).
9. 9.Verify the measurements meet specifications.

§ §

21 10Base-T Transmitter Output Timing Jitter with Cable Model

ANSI SECTION 1411.10.12

21.1 Test Purpose

To verify the jitter added by the UUT.

21.2 Specification

The jitter added to the signal on the DO circuit as it propagates through the UUT and twisted pair model shall be no more than 12.0 ns.

21.3 Test Equipment

- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- CAT 5 twisted pair cable (under 2 inches in length)

21.4 Test Fixtures

- 100 Ω UTP test load (Appendix A.1)
- Twisted pair model (Appendix C)

21.5 Test Procedure

1. Insert CAT 5 cable, connected to twisted pair model, into UUT and attach differential probe to the test load as shown in Figure 21-1.

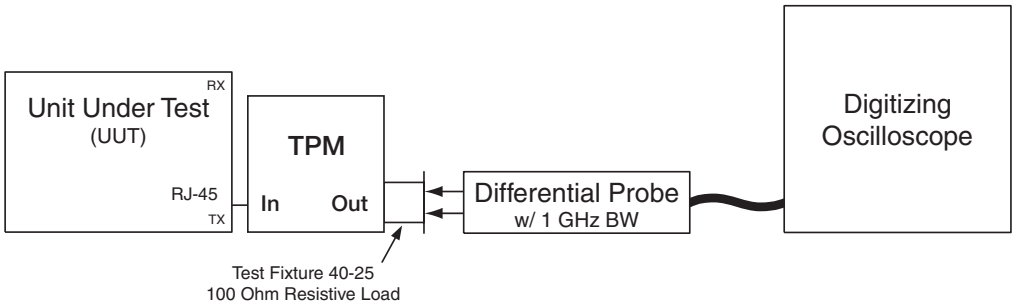


Figure 21-1 Test Setup for 10BASE-T Transmitter Output Timing Jitter with Cable Model

2. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Jitter With Cable Model: 1411.10.12 test
3. Configure the oscilloscope according to table below.

Table 21-1 Scope Configuration for Peak Differential Output on TD Circuit

Scope Parameter	Setting
Horizontal Scale	10 ns/division
Vertical Scale	-600 mV to +600 mV (at 10 vertical divisions, this equals 120 mV/division; at 8 divisions, 150 mV/division)
Trigger Type	Pulse width: ~220 ns (lower bound); ~320 ns (upper bound) Tight trigger (±10 ns of actual pulse width) is best.
Trigger Level	Typically 0.5 V to 1.7 V
Display Persistence	Infinite persistence

Pulse Width Triggering

1. Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.
2. Set the trigger level as specified in the above table.
3. Select pulse width triggering.
4. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
5. Set the trigger mode to normal.
6. Increase the lower bound parameter gradually until the triggering is lost.
7. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
8. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

4. Shift waveform to the right and find zero crossing at 8.0 BT ±7ns (approximately 800 ns). The graphic below provides a reference.

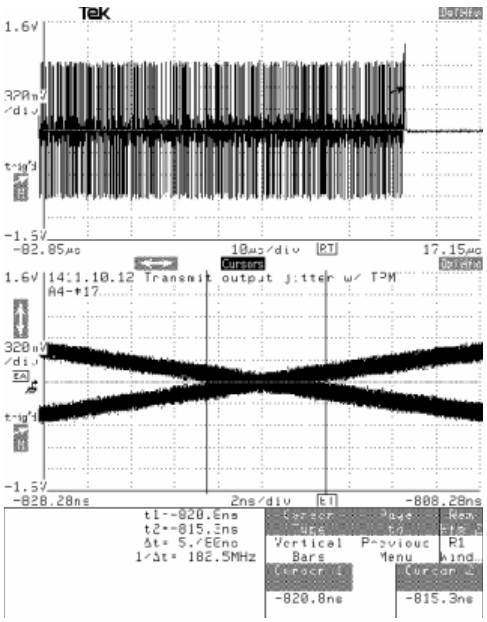


Figure 21-2 8.0 Bit Times (BT)

5. Set vertical cursors to record the maximum closing of the eye. The difference between the two cursors should be recorded as the jitter measurement.
6. Shift waveform to the right and find zero crossing at 8.5 BT ±7ns (approximately 850 ns). The graphic below provides a reference.

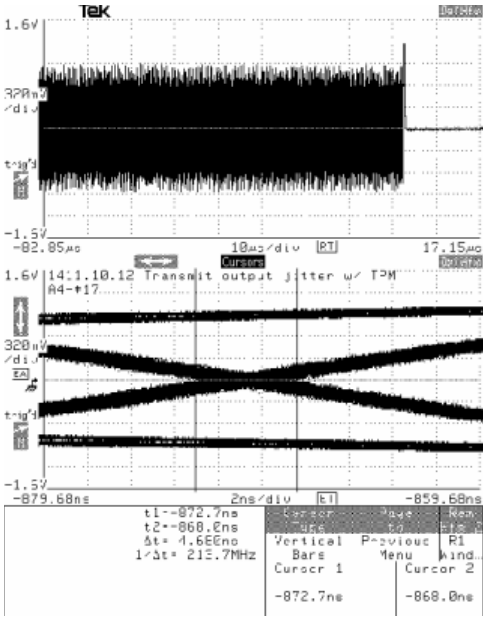


Figure 21-3 8.5 Bit Times (BT)

7. Set vertical cursors to record maximum closing of the eye. The difference between the two cursors should be recorded as the jitter measurement.
8. Verify the measurements meet specifications.

§ §

22 10Base-T Transmitter Output Timing Jitter without Cable Model

ANSI SECTION 1411.10.13

22.1 Test Purpose

To verify the jitter added by the UUT when directly driving a 100 W resistive load.

22.2 Specification

The jitter added to the signal on the DO circuit as it propagates through the UUT, driving a 100-ohm resistive load, shall be no more than 11.0 ns.

22.3 Test Equipment

- Digitizing Oscilloscope (100 MHz or greater bandwidth)
- Differential Probes (100 MHz or greater bandwidth)
- CAT 5 twisted pair cable (under 2 inches in length)

22.4 Test Fixtures

- 100 Ω UTP test load (Appendix A.1)

22.5 Test Procedure

1. Insert CAT 5 cable into UUT and attach differential probe to the test load as shown in Figure 22-1.

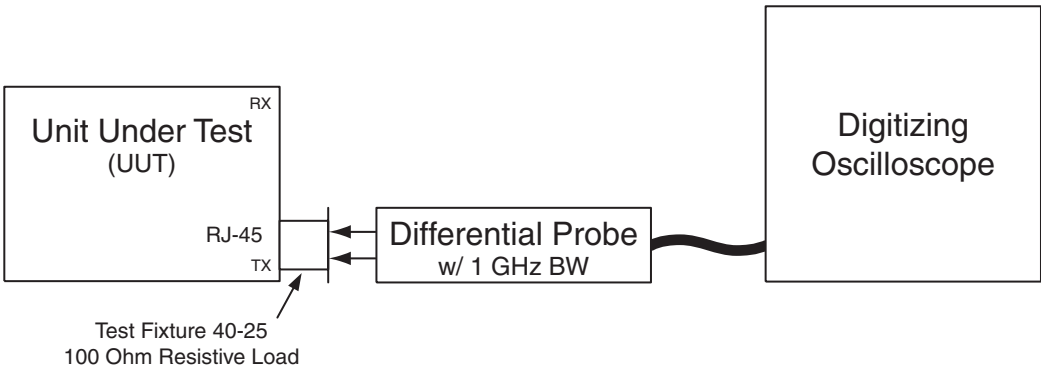


Figure 22-1. Test Setup for 10Base-T Transmitter Output Timing Jitter without Cable Model

2. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the Jitter Without Cable Model: 1411.10.13 test
3. Configure the oscilloscope according to the table below.

Table 22-1. Scope Configuration for Peak Differential Output Voltage on TD Circuit

Scope Parameter	Setting
Horizontal Scale	10 ns/division
Vertical Scale	-1.6 V to +1.6 V (at 10 vertical divisions, use 320 mV/division; at 8 divisions, 400 mV/division)
Trigger Type	Pulse width: ~220 ns (lower bound); ~320 ns (upper bound) Tight trigger (±10 ns of actual pulse width) is best.
Trigger Level	Typically 0.5 V to 1.7 V
Display Persistence	Infinite persistence

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specified in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

4. Shift waveform to the right and find zero crossing at 8.0 BT ±7 ns (approximately 800 ns). (The graphic below provides a reference.)

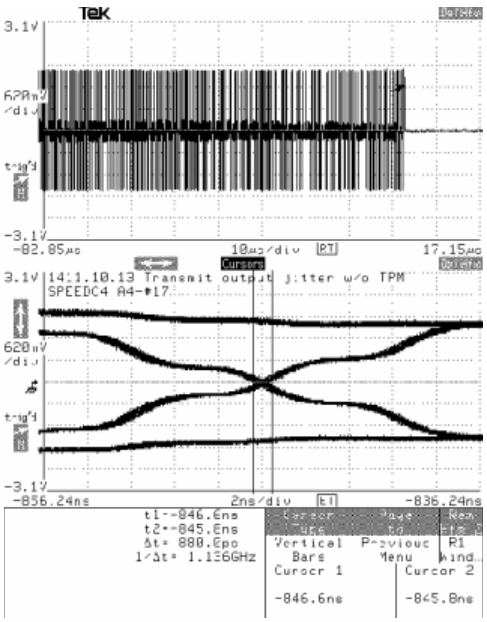


Figure 22-1. 8.0 Bit Times (BT)

5. Set vertical cursors to record the maximum closing of the eye. The difference between the two cursors should be recorded as the jitter measurement.
6. Shift the waveform to the right and find zero crossing at 8.5 BT ±7 ns (approximately 850 ns).

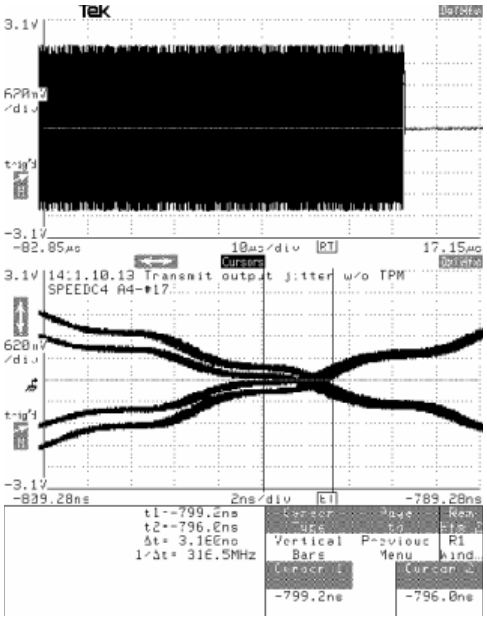


Figure 22-2. 8.5 Bit Times (BT)

7. Set vertical cursors to record the maximum closing of the eye. The difference between the two cursors should be recorded as the jitter measurement.
8. Verify the measurements meet specifications.

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23 10Base-T RD Receiver Circuit Signal Acceptance Test (BER)

23.1 Test Purpose

To measure the Bit Error Rate (BER) of the UUT.

23.2 Specification

"The differential transmitted signals on TX+/- must meet the requirements of Section 9.1 of the ANSI X3.263 specification."[1] See Sections 8 - 14 of this document. The receiver shall have a bit error rate of less than 10^{-8}.

This requirement can be accomplished by performing receive bit error rate tests with specification compliant Category 5 cables across a range of lengths from approximately 1 meter to greater than 100 meters (maximum specification). Insertion loss measurements and propagation delay measurements have shown high-quality Category 5 cable ranging from 115 m to 130 m may be equal to a maximum specification cable (depending on the vendor and the cable manufacturing lot). See Appendix E for details on constructing LAN cables.

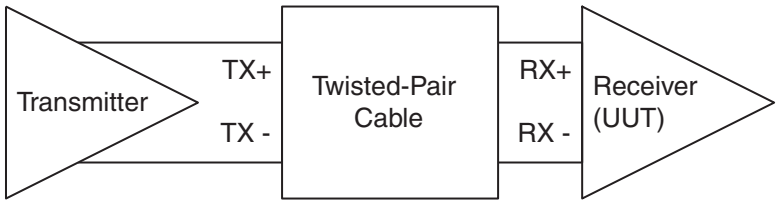


Figure 23-1 Differential Input Signals[2]

23.3 Test Equipment

- Transmit computer with a Network Interface Card (NIC) or LAN On Motherboard (LOM) running LANConf.exe
- Host computer running LANConf.exe

23.4 Test Fixtures

Various lengths of Category 5 and/or Category 3 cable between 1 and 100 spec. meters.

1. ANSI X3 263-1995, p. 32
2. Based on ANSI X3 263, p32, Figure 15.

23.5 Test Procedure

1. Connect the UUT and the link partner using the desired Category 5 cable length and verify that a gigabit link has been established.
2. On the receiving system, go to the Transmit and Receive menu, and select the Receive option.
3. On the UUT, go to the Transmit and Receive menu, and select the Transmit option.
4. Allow the proper number of frames to be sent (see Section 23.6).
5. After transmissions is complete, press the <Esc> key on the receiver first and then the transmitter to stop the test and record the following results:
   a. Link partner: Transmit Good Packets and Transmit Total Packets
      Both of these statistics should equal each other.
   b. UUT: Receive Good Packets and Missed Packets.
6. Calculate the bit error rate (BER).
7. Repeat steps 1 through 7 for each cable length.
8. Verify the measurements meet specifications.

23.6 Calculating Bit Error Rate (BER)

The basic BER equation is as follows:

$$BER = \frac{TGP - MP - RGP}{TGP \times BF \times BB}$$

where:

- TGP = number of good frames transmitted (#_Transmit_Good_Packets)
- MP = number of missed packets (#_Missed_Packets)
- RGP = number of good frames received (#_Receive_Good_Packets)
- BF = number of bytes/frame
- BB = 8 (number of bits/byte)

Note: Conditions where the transmit link partner overwhelms the receive unit should be avoided. When this happens, the receive statistics counters may show "RX No Resources", "RX No Buffers", or a large number of missed packets. This complicates the BER calculation and the equations for the calculations will not yield accurate BER numbers. The TX transmit speed (frames per second) can be decreased to prevent this condition. Alternatively, the test operator can try to make sure the receive unit is always in a faster PC than the transmit unit.

Example 23-1 BER Calculation Example

If 499,995 good frames were received and 500,000 good frames were transmitted, then for 1,024 byte frames and zero missed packets the BER would be as follows:

*BER = ((500,000 - 0) - 499,995)/(500,000 * 1,024 * 8) = 1.22 x 10^-9*

This example passes because the resulting BER is less than 1 x 10^{-8}, which is the maximum specification.

§ §

24 10Base-T RD Circuit Differential Input Impedance (Receiver Return Loss)

ANSI SECTION 1411.11.05

24.1 Test Purpose

To verify the differential input impedance.

24.2 Specification

The return loss shall be greater than or equal to 15 dB from 5 MHz to 10 MHz.

24.3 Test Equipment

- Network Analyzer
- CAT 5 twisted pair cable (under 2 inches in length)
- BNC cable, with 50-ohm characteristic impedance

24.4 Test Fixtures

- Balun Test Fixture with 200 MHz or greater bandwidth (Appendix D.2)
- Load Fixture for Network Analyzer calibration (Appendix A.5)

24.5 Test Procedure

1. Insert CAT 5 cable from UUT into transmitter side of Balun fixture and connect Balun to Network Analyzer with BNC cable as shown below. Do not connect the CAT 5 cable to the UUT at this time.
2. Adjust the spectrum analyzer to the following settings.

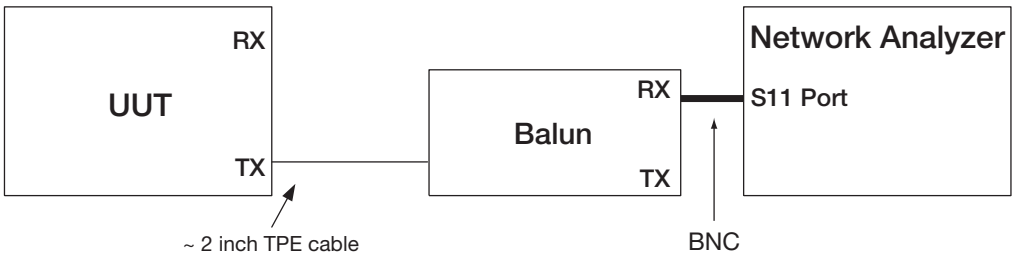


Table 24-1 Analyzer Configuration for RD Circuit Differential Input Impedance

Scope Parameter	Setting
Start Frequency	3 MHz
Stop Frequency	13 MHz
Resolution BW or IF BW	Lowest practical bandwidth supported by equipment in the range of 10 KHz to 200 KHz.
Number of Points (Resolution)	Maximum for instrument (≥ 401)
Acquire	Average (if necessary)
Vertical Division	10 dB/division
Mode	Network Analyzer

3. From the 10 BASE-T PHY Configuration Tests menu in LANConf.exe, select the RX Return Loss: 1411.10.05 test.
4. Perform a calibration on the S11, S-parameter, port and turn correction on.
5. Test the calibration by connecting the 50 Ω load and confirming the results are close to the theoretical value of 9.54 dB. Also verify that the open and short loads produce the expected results.

Calculating Theoretical Return Loss

To solve for theoretical return loss given known impedances:

$Z_{transmitter}$
Balanced output impedance of the balun (for example, 100 Ω).

Z_{load}
The impedance of any load connected to the output of the balun.

$$RL\_in\_dB = 20\log\frac{\left|Z_{transmitter} + Z_{load}\right|}{\left|Z_{transmitter} - Z_{load}\right|}$$

For any load on the 100 Ω output of the balun, this simplifies to:

$$RL\_in\_dB = 20\log\frac{\left|100\Omega + Z_{load}\right|}{\left|100\Omega - Z_{load}\right|}$$

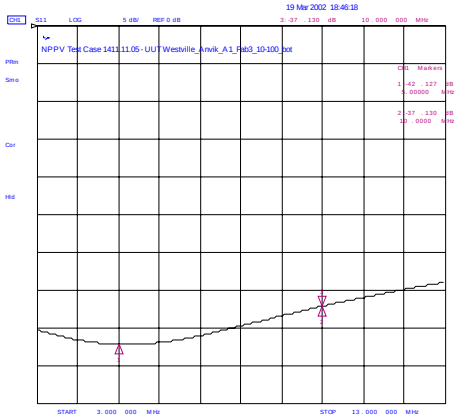
For a 50 Ω load with the 100 Ω output of the balun, this becomes:

$$RL\_in\_dB = 20\log\frac{\left|100\Omega + 50\Omega\right|}{\left|100\Omega - 50\Omega\right|}$$

which simplifies to:

$RL\_in\_dB = 20\log_{10}3 = 20 * 0.477 = 9.54$ dB

6. Connect the CAT5 cable to the UUT.
7. Set the marker to the worst-case return loss between 5 MHz and 10 MHz inclusive.



8. Record the amplitude (dB) of the return loss.
9. Verify the measurements meet specifications.

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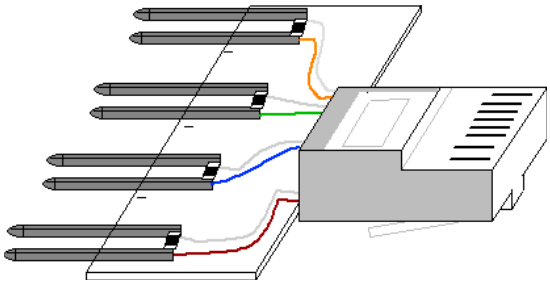
Appendix A 1000Base-T Test Fixtures and Calibration Load Fixtures

Note: When building test fixtures, it is important to remember that an improper or unstable design may cause measurement errors. Please refer to the IEEE specification for schematics for the needed test fixtures.

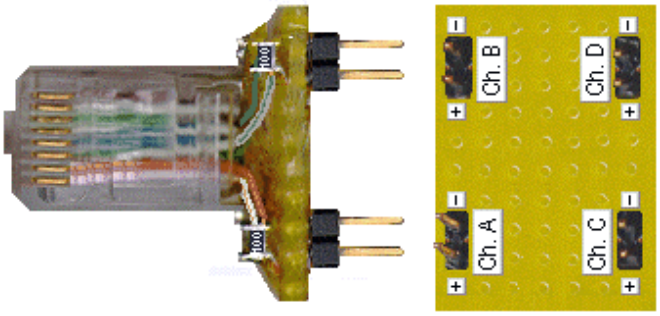
A.1 Fixture 40-25

Test fixture 40-25 terminates each channel with a 100-ohm load. Each Resistor is 100 Ω ±0.1 Ω. A 100 Ω resistor across all four MDI signals must be present at the same time.

Angled side view:



Side and end view:



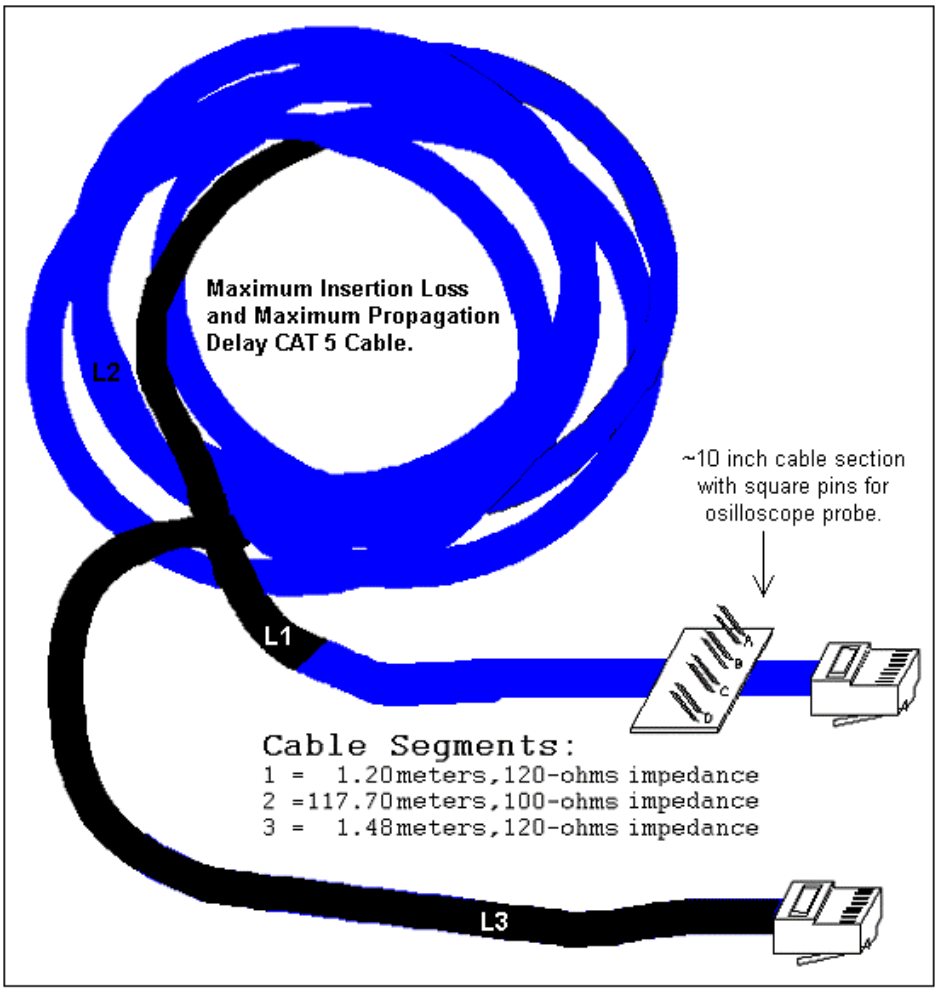
A.2 Fixture 40.6.1.1.1.A - Differential Breakout Cable

A short cable is required for the transmitter jitter test and for the alien crosstalk tests. It is connected to the end of long test cables by using a CAT 5 patch connector and is approximately 10 inches in length. It is a CAT 5 cable with four pairs of square test pins, with one pair on each differential pair within an inch of one of the male RJ-45 connectors.

A.3 Fixture 40.6.1.1.1 - Test Cable

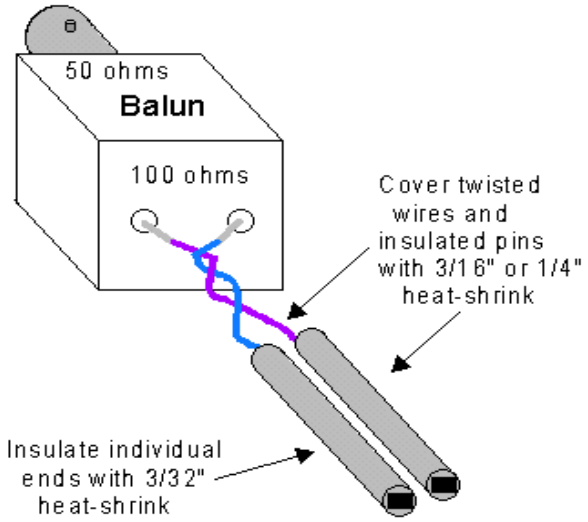
This cable is used for master and slave transmit jitter (IEEE 802.3, Section 40.6.1.2.5). It is made from three segments as defined in IEEE 802.3, Section 40.6.1.1.1.

There are two segments with 120-ohm characteristic impedance, and one long CAT 5 cable section with 100-ohm characteristic impedance. Near the UUT end of this cable, fixture 40.6.1.1.1.A (above) is attached. Appendix C provides detailed information for the construction of this cable.



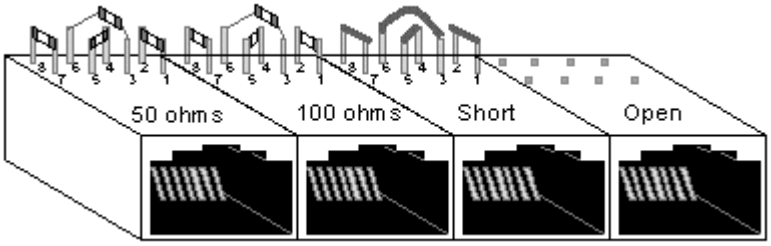
A.4 Fixture 40.8.3.1.A

Fixture 40.8.3.1.A is a Balun test fixture. A North Hills NH13732 or similar balun should be used.



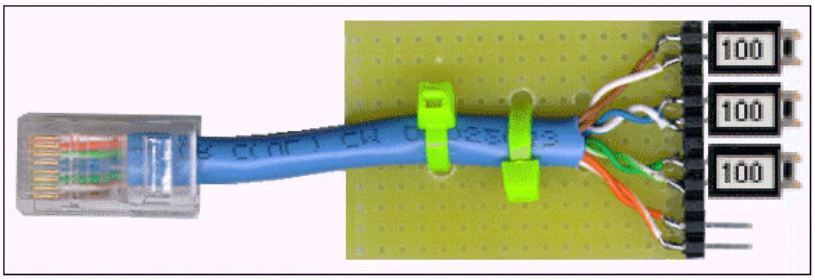
A.5 Fixture 40.8.3.1.B

Fixture 40.8.3.1.B is used to calibrate the network/spectrum analyzer. The illustration shows the network analyzer calibration loads.



A.6 Fixture 40.8.3.1.C

Fixture 40.8.3.1.C is a square pin fixture for MDI return loss. It allows a single Balun to test all 4 channels.



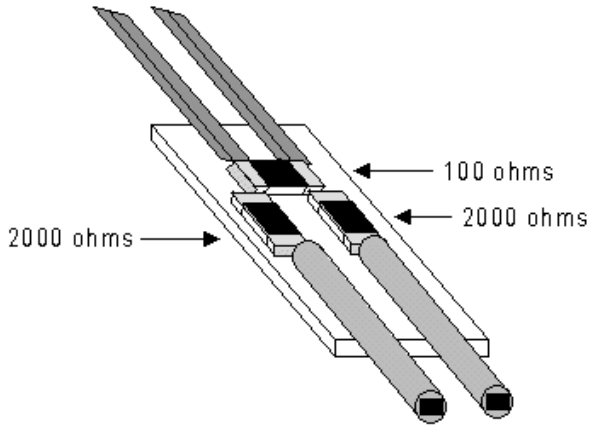
The short CAT 5 cable with four pairs of square pints mates to the Balun test fixture for return loss tests. 100-ohm resistor loads are installed on the channels that are not being tested.

A.7 Fixture 40-28A

Fixture 40-28A is used for the alien crosstalk noise rejection test. It requires one-half meter long CAT 5 cable with female test pins on the transmit differential (positive and negative) pins at one end. The transmit differential pins correspond to the orange and orange-white twisted cable pair in the CAT 5 cable.

A.8 Fixture 40-28B

Fixture 40-28B is also used for the alien crosstalk noise rejection test.



A.9 Fixture 40-32

Fixture 40-32 is used to test common-mode output voltage and is required for IEEE 802.3, Section 40.8.3.3. A schematic for fixture 40-32 can be obtained in the IEEE 802.3 specifications.

A 47.5-ohm resistor is soldered to the end of each wire on each differential pair. At the opposite ends, each pair of 47.5-ohm resistors is soldered together. Where the 47.5-ohm resistors are soldered together, they are also both soldered to one of the square pins in the top row. All of the 47.5-ohm resistors, and all of the top-row square pins are insulated from the copper ground plane by a layer of kapton tape. The bottom row of right-angle square pins are soldered to the copper ground plane (diagram below shows the four solder joints in the bottom view just below “Output V” on the label). The shield on the RJ-45 connector is soldered to the fixture’s copper ground plane.

Note: On the top-side, each top row square pin has a 49.9 ohm resistor soldered to it, which is not visible. The other end of each 49.9-ohm resistor is soldered to the corresponding ground pin in the bottom row of square pins.

Another way to visualize how the resistors are arranged:

> On each test channel, two 47.5-ohm resistors and one 49.9-ohm resistor form a “Y.” A top-row square pin is soldered to the center of the “Y.” The top-row square pin is soldered to all three resistors, at this single point on the “Y.” The opposite end of the 49.9-ohm resistor is soldered to a ground pin. Kapton tape insulates the top-row square pins and the 47.5-ohm resistors from ground.

Note: Fixture 40-32’s copper tape ground plane is soldered directly to the metal shield on the RJ-45. The fixture’s RJ-45 shield connects to the UUT shielded connector. The lower row of test pins are all connected to the UUT chassis ground (indirectly) through the fixture’s copper ground plane.

Fixture 40-32: Top View

Fixture 40-32: Side View

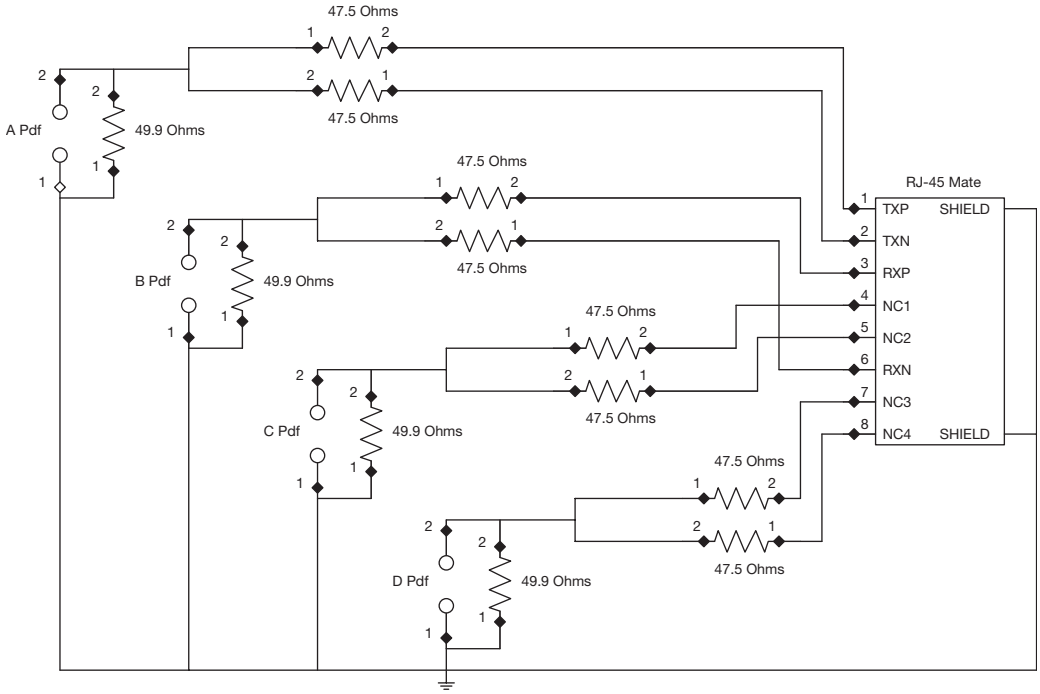


Figure A-1 40-32 Schematic

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Appendix B Test Fixture Construction Tips and Information

B.1 General Test Fixture Construction Guidelines

1. Unless otherwise specified, always use solid 22 AWG wire or solid 24 AWG wire. Ideally, the wires for differential test fixtures can be taken from a scrap piece of high-quality, solid-conductor, Category 5 cable.
   - — Keep both sides of each differential pair balanced.
   - — Keep lead lengths the same on each side of each differential pair.
   - — Route both leads, within a differential pair, next to each other.
   - — Center resistors and other components that are soldered between differential pairs between the pair of wires or traces.
   - — Match values and lengths as closely as possible when two of same value components are shown in an illustration.
2. Always keep lead lengths as short as possible, without violating the rules listed under the second bullet in guideline 1 (above).
3. If the differential leads on a test fixture need to be more than one or two inches long and if possible, twist the two leads (of the differential pair) around each other.
4. Tightly toleranced components should be used wherever possible.
   - — When using an ohm meter to “cherry-pick” best resistor values, subtract the meter’s lead resistance from the measured resistance values.
   - — As a starting point, resistors should be 1% or better tolerance. Use an ohm meter, and select resistors that are within 0.1 Ω of the required value. When a pair of the same value is used, they should be matched within 0.1 Ω before soldering, and within 0.2 Ω after soldering. If an illustration shows a tighter tolerance, follow the illustration.
   - — Capacitors should be 5% or better tolerance. When a pair of the same value is used, they should be matched as close as possible. If an illustration shows a tighter tolerance, follow the illustration.
   - — Inductors should be 10% or better tolerance. When a pair of the same value is used, they should be matched as close as possible. If an illustration shows a tighter tolerance, follow the illustration.
5. Each test fixture and cable should be labeled with its function and identity.
6. When using twisted pair Ethernet cable to build test fixtures (or very short test cables), use solid conductor Category 5 cable. The impedance is better controlled than Category 5 patch cable and Category 3 cable. Also, solid conductor Category 5 cable has lower insertion loss.

B.2 RJ-45 Connector Pin-Out, and Ethernet Cable Wire Assignment

The following Ethernet cable wire assignments apply to all network speeds.

RJ-45 Connector Pinout:

- Pin 1 is channel A+, white/orange wire

- Pin 2 is channel A-, orange wire
- Pin 3 is channel B+, white/green wire
- Pin 6 is channel B-, green wire
- Pin 4 is channel C+, white/blue wire
- Pin 5 is channel C-, blue wire
- Pin 7 is channel D+, white/brown wire
- Pin 8 is channel D-, brown wire

Table B-1 Contact (pin)Straight Through Cable Crossover Cable

Contact (pin)	Straight Through Cable	Crossover Cable
1	A+ to A+	A+ to B+
2	A- to A-	A- to B-
3	B+ to B+	B+ to A+
4	C+ to C-	C+ to D+
5	C- to C+	C- to D-
6	B- to B-	B- to A-
7	D+ to D+	D+ to C+
8	D- to D-	D- to C-

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Appendix C Worst-Case Cable for Jitter

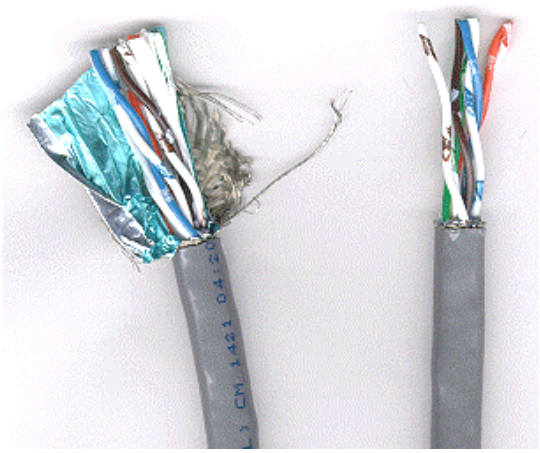
The cable used for the transmit jitter test is comprised of three sections: 2 120-ohm characteristic impedance sections and 1 long CAT 5 100-ohm characteristic impedance section.

Note: This cable is under development.

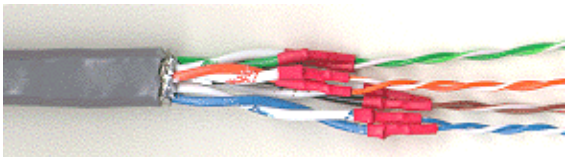
C.1 Constructing the 120-ohm Impedance Segments (L1 and L3)

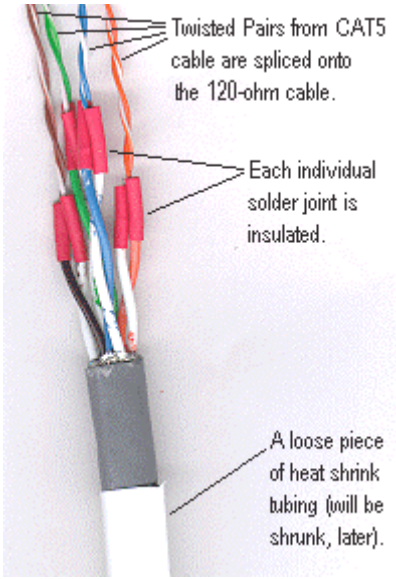
It is recommended that a shielded 120-ohm impedance twisted-pair cable is used for construction. (Shielded four-pair twisted pair 120-ohm cable is available from Alcatel [Alcatel 6806 GigaMatch FTP 4P] and Belden [Belden YR44160 CM 4PR24 Shielded.)

1. Cut the cable (preferably, one of the cables mentioned above) to the lengths specified in the IEEE 802.3ab specifications or this document.
2. Trim the outer insulating jacket and shield back about 1.5 inches.



3. Slide two four inch pieces of 3/8-inch or 1/2-inch diameter heat shrink tubing to the middle of the cable. (Do not heat or shrink the tubing.)
4. Splice individual, insulated 1.5 inch pieces of 24 AWG CAT 5 wires at each end of each cable on each of the eight conductors. (The wires in the shielded cables are too think to fit inside the RJ-45 crimp-on connectors.)
5. Verify that the splices will not create a short on any of the twisted pair wires with each other. Heat shrink or kapton tape can be should be used to insulate the splices.





6. Place the wires at each end of each cable in the correct order for the crimp-on connectors.
7. Trim the wire ends to equals lengths.
8. Slide the 3/8-inch or 1/2-inch heat shrink tubing down to the connectors and shrink them by applying heat.

9. Crimp the male RJ-45 connectors onto the cable.

Note: This procedure has been used to construct unshielded 120-ohm impedance twisted pair cable. However, it is not recommended for the following reasons:

1. The required calculations only approximate the desired target impedance. They do not take into account the loading effects of the adjacent twisted pairs.
2. It is labor intensive. The individual pairs need to be twisted to a consistent number of twists per foot and wrapped with an insulator.
3. Post construction testing is rigorous. Measurements are required for all four channels.

The following tables provide additional information regarding Jitter test cable.

Table C-1 Constructed Jitter Test Cable Segments Lengths

Cable Segment / Type	Meters	Feet	Inches	Notes
L1 (constructed cable)	1.20	3.94	47.24	3 feet, 11.24 inches
L2 (quality CAT5 cable)	117.7	386.15	4633.85	386 feet, 1.85 inches
L3 (constructed cable)	1.48	4.86	58.27	4 feet, 10.27 inches
TOTAL CABLE	120.38			

Table C-2 Constructed Jitter Test Cable Delay Specifications

Delay	Cable Type
4.75 nsec/meter	Quality CAT5 cable
4.673935 nsec/meter	Constructed cable
10.8 nsec	Constructed cable segments L1 and L3 (L1 + L3 = 1.20 + 1.48 = 2.68 meters)
559.2 nsec	Quality CAT5 cable of segment L2. (117.72632 meters of standard CAT5 cable is required for a 559.2 nsec delay.)

Table C-3 Average Insertion Loss Comparison

	16 MHz	31.25 MHz	50 MHz	80 MHz	100 MHz
Quality CAT5 cable of 120 meters	8.61	12.22	15.62	20.08	22.73
Quality CAT5 cable of 117.7 meters	8.44	11.99	15.32	19.7	22.29
Constructed cable of 2.68 meters	0.18	0.24	0.33	0.48	0.46
Total Insertion Loss of 117.7 m quality CAT5 cable + 2.68 m constructed cable	8.62	12.23	15.65	20.18	22.76
IEEE specification maximum Insertion Loss	9.13	12.98	16.64	21.33	24

Table C-4 Constructed Jitter Test Cable Average Insertion Loss per 9.9062 Meters

	16 MHz	31.25 MHz	50 MHz	80 MHz	100 MHz
rb	0.6333	0.8905	1.1827	1.632	1.6982
vg	0.6695	0.9165	1.262	1.9602	1.7455
blbr	0.6674	0.8969	1.1465	1.8189	1.6671
gw	0.6896	0.8907	1.219	1.7077	1.7382
Average	0.66	0.90	1.20	1.78	1.71

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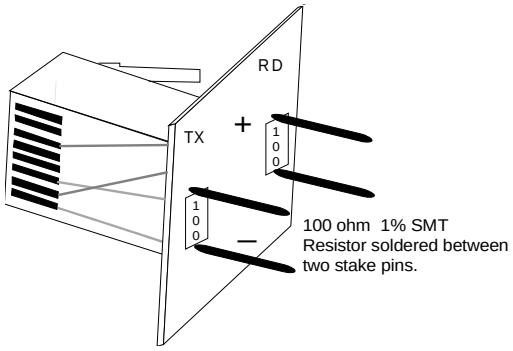
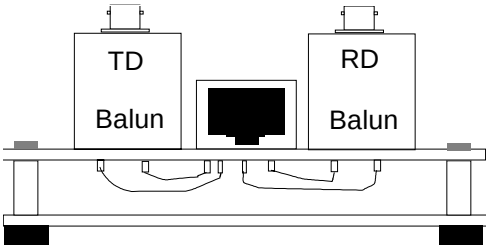
Appendix D Other Test Fixtures

D.1 100 Ohm UTP Test Load

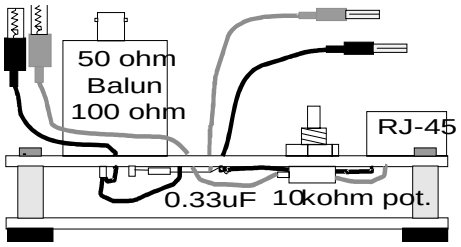


D.2 100Base-TX Balun Test Fixture



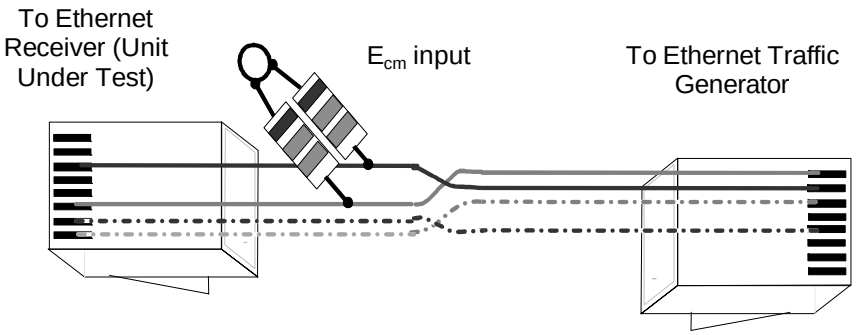
D.3 Open Circuit Inductance Test Fixture

Note: This is an optional test, not currently documented.



D.4 Receiver Common-Mode Rejection Test Fixture

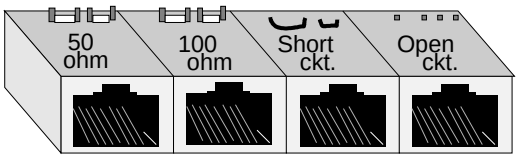
Note: This is an optional test, not currently documented.



Receiver Common-Mode Rejection Test cable with two identical value resistors
$R_1 = R_2$, and $449\Omega \leq R \leq 560\Omega$

Note: Each Resistor must be soldered an equal distance from the end of the RJ-45 connector (i.e. both sides of the receive signal path must be symmetric). Also, the wires in each pair must be ***twisted*** CAT5 wire (to make the signal path clear, the illustration does not show twists, but the real fixture must have twisted wires in each differential pair).

D.5 10Base-T Balun Test Fixture



Four, female RJ-45 connectors, glued to each other.

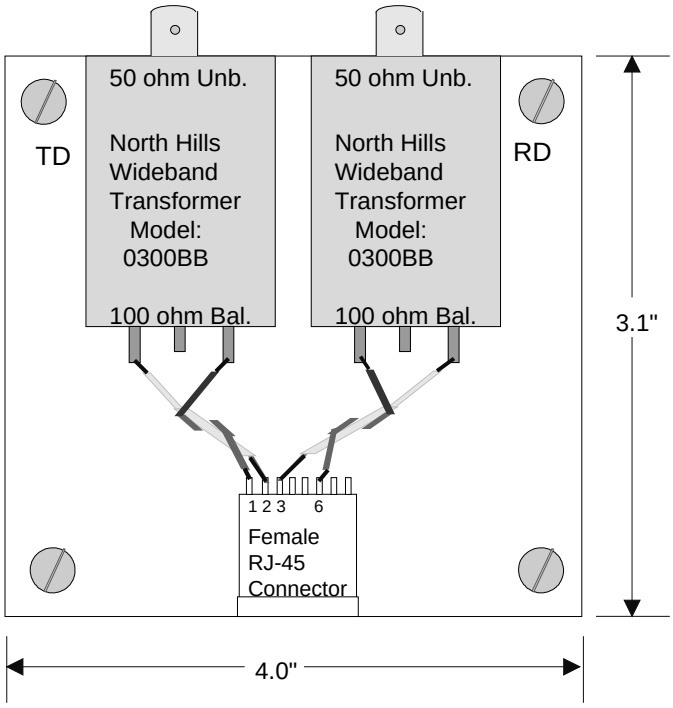
Open ckt. - Cut pins flush to the connector.

Short ckt. - Tie pin 1 to pin 2. Tie pin 3 to pin 6. Cut off the excess.

100 ohm - Solder 100 ohm SMT resistors between: pin 1 and pin 2, and between pin 3 and pin 6.

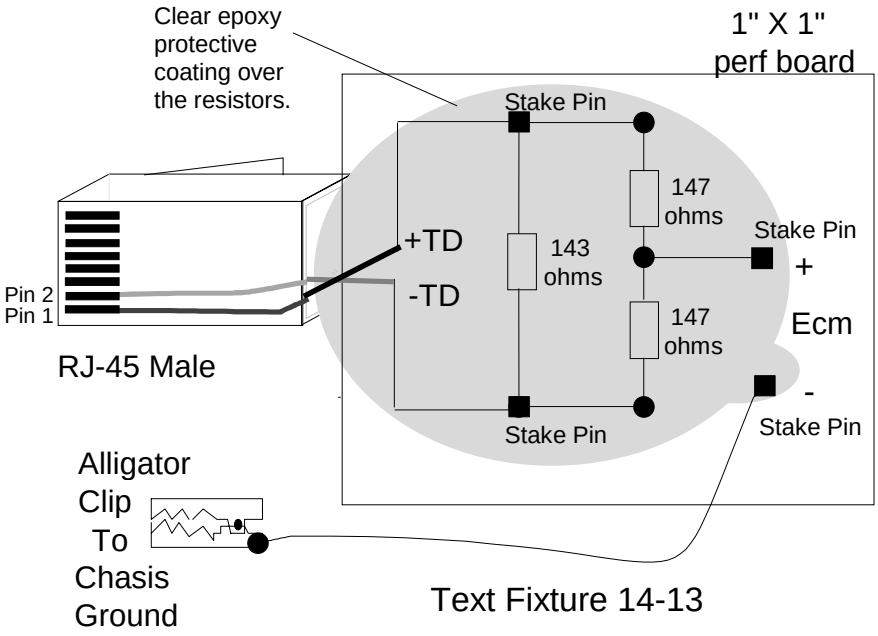
50 ohm - Solder 50 ohm SMT resistors between: pin 1 and pin 2, and between pin 3 and pin 6.

Load Fixture for Network Analyzer Calibration



10Base-T Balun Test Fixture, Top View

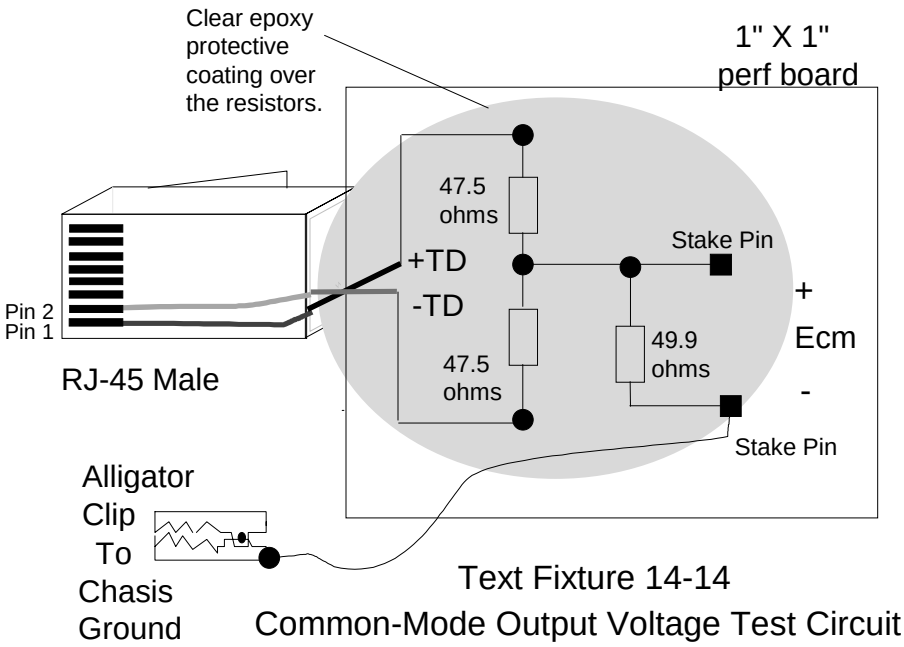
D.6 Common-Mode Output Voltage Test Circuit (Fixture 14-14)



Text Fixture 14-13

Transmitter Impedance Balance and Common-Mode Rejection Test Circuit

(Used for Test Cases 1411.10.08 and 1411.10.10)



Text Fixture 14-14

Common-Mode Output Voltage Test Circuit

(Used for Test Case 1411.10.09)

D.7 10BASE-TX 14_7 Twisted-Pair Model

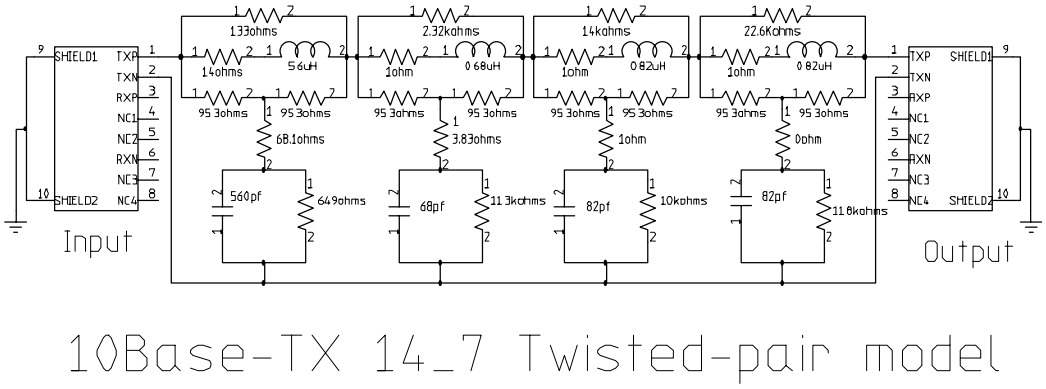


Figure D-1 10BASE-TX 14_7 Twisted-Pair Model

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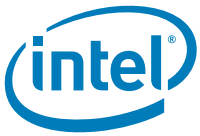

Appendix E Building and Testing UTP LAN Cables to Insertion Loss Specifications

The ANSI TP-PMD specification requires the use of “standard” test cables to perform common-mode rejection and standard bit error rate tests. In Annex A.1.1 of the ANSI standard, the TP-PMD partially defines these cables by their intended insertion loss, rather than their physical length. (For a list of required cables, see Table E-1. For more detail, read the TP-PMD.)

The insertion loss of the test cables must be characterized by measurement. Do not assume 1.0 dB of loss per 10 meters of CAT 5 cable. Almost all CAT 5 cable is either much lower in loss, or significantly higher. Because the cables are not consistent, measure the characteristic insertion loss of the appropriate type of cable, cut it to length (the length that provides the desired loss), and add connectors.

E.1 Purpose

This section explains a general method of measuring the insertion loss of twisted pair Ethernet cable, and how to calculate the desired cable length based on a target insertion loss. This section is not an exhaustive treatment of this topic, nor is it a replacement for a network analyzer’s instruction manual.

E.2 Network Analyzer Setup and Calibration

Measuring a cable with a network analyzer is relatively straightforward. A vector network analyzer is more accurate than a scalar network analyzer. Use two 50 ohm unbalanced to 100 ohm balanced transformers to match the cable impedance with that of the network analyzer. (North Hills Balun model NH13734 is okay, and so is model 0300BB).

1. Connect the 50Ω side of one balun to port one on the network analyzer via a BNC cable.
2. Connect the 50Ω side of the other balun to port two of the network analyzer through a second BNC cable. See Figure E-1.
3. In two-port or S21 (insertion loss) mode, set the network analyzer's start frequency to 1 MHz, and the stop frequency to 101 MHz (If your analyzer or baluns are BW limited, calibrate to a little over 16 MHz instead of to 101 MHz).
4. Set the analyzer's display format to insertion loss in dB.
5. Perform a two-port calibration (Through connect & Isolation):

Note: Two port calibration methods may vary for different network analyzers. Refer to the equipment’s users manual for more details.

- For the through connect, connect the 100Ω side of one balun to the 100Ω side of the other balun via a very short CAT5 twisted pair cable.
- For the isolation measurement, terminate each balun’s 100Ω side with a 100Ω resistor.

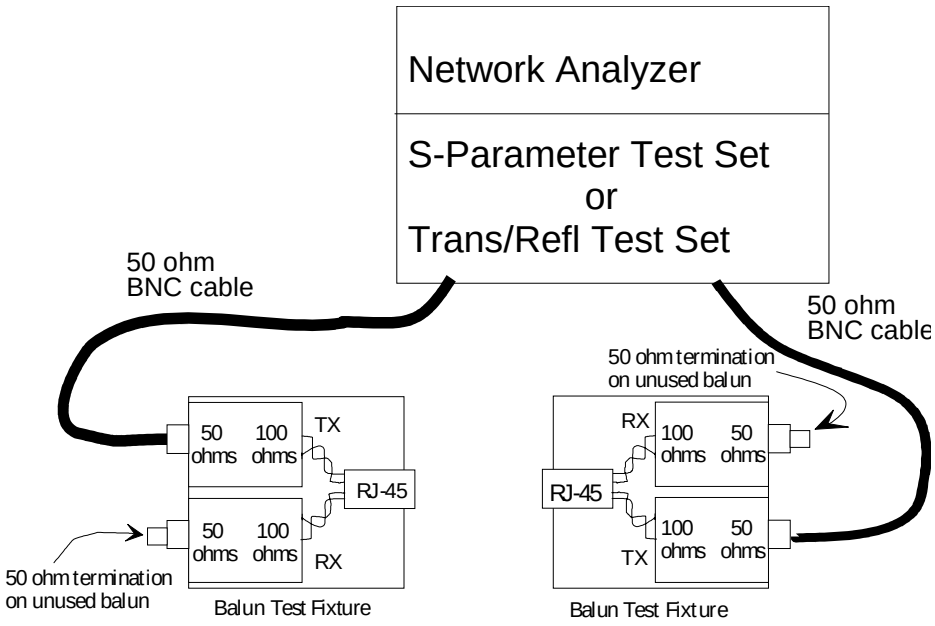

Figure E-1 Network Analyzer Setups for Calibration and Measurement of Insertion Loss

6. Turn correction on.
7. Set triggering to continuous sweep.
8. Put a marker on 16 MHz.
9. After calibration, check the calibration quality by measuring the two calibration standards.
   a. Reconnect the short CAT5 through cable between the two baluns. Insertion loss should be zero dB. Most network analyzers should be capable of zero dB within +/- 0.05 dB or less.
   b. Put the 100 ohm resistor loads back on each balun. The insertion loss (isolation) should be greater than 40 dB (On many network analyzers, isolation will be > 60 dB).

Note: Treat all loss and isolation levels as absolute values. If your analyzer displays an isolation/insertion loss of -65 dB, it is actually 65 dB, unless you are measuring an amplifier or a device with greater than unity gain (i.e. negative loss = gain).

E.3 Measuring the Insertion Loss of the Twisted Pair Cable

1. Connect a known length (preferably 50 meters or more) of the twisted pair cable between the two baluns' 100 ohm sides (Connect the network analyzer to the cable's TX pair: orange & orange/white at both ends).
2. Record the insertion loss value for the marker at 16 MHz. The analyzer in should be in continuous sweep mode.
3. Recalibrate if required, and measure the cable's RX insertion loss (green & green/white).
4. Divide the insertion loss at 16 MHz by the length in meters. The result of this calculation is the characteristic dB/meter. It is not uncommon for TX cable loss and

RX cable loss to be slightly different. Average the numbers to calculate a single insertion loss/meter for the cable.

5. To calculate the length of cable for a required insertion loss, divide the required insertion loss by the loss/meter.
6. Build cables to the length(s) that you calculated.
7. Repeat steps 10 through 14 to measure the TX and RX insertion loss of the cables that were built in step 15.

E.4 Alternate Insertion Loss Measurement Techniques

Cable insertion loss can also be measured/calculated by more difficult and/or less accurate methods:

- Signal generator, two baluns, and a couple of power meters.
- Signal generator, two baluns, and an oscilloscope with one or two differential probes (in lieu of one or both power meters).

Note: A variation on the last method dispenses with the baluns and the differential probes, but requires the use of two (matched) channels on the oscilloscope, two phase-matched coaxial cables, and a signal generator.

All of the alternative measurements require the user to manually add or subtract some correction factors, and/or convert from voltage to decibels in order to obtain the cable's insertion loss.

Note: A network analyzer is more accurate than the alternate measurement methods.

Table E-1 Test Cables 1-5

Test Cable	Type	Insertion Loss	Frequency	Error
1	CAT5	0.5 dB	16 MHz	± 0.20 dB
2	CAT5	2.5 dB	16 MHz	± 0.20 dB
3	CAT5	5.0 dB	16 MHz	± 0.20 dB
4	CAT5	7.5 dB	16 MHz	± 0.20 dB
5	CAT5	10.0 dB	16 MHz	± 0.20 dB

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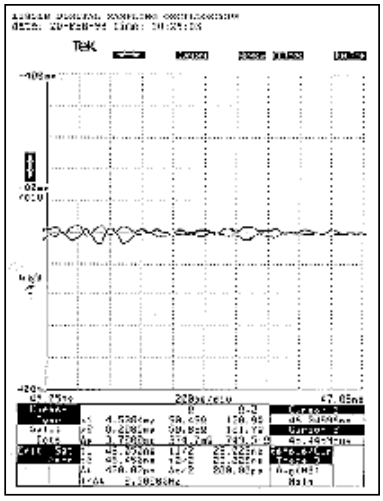
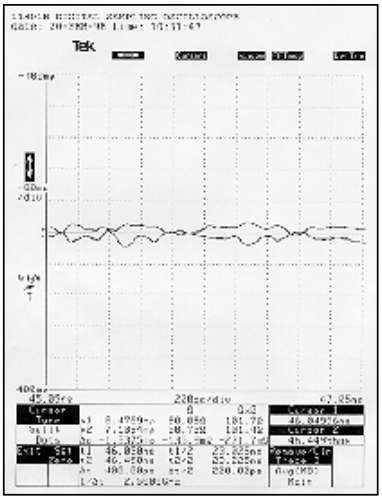
Appendix F Reducing Measurement Error by Avoiding Cable Bending

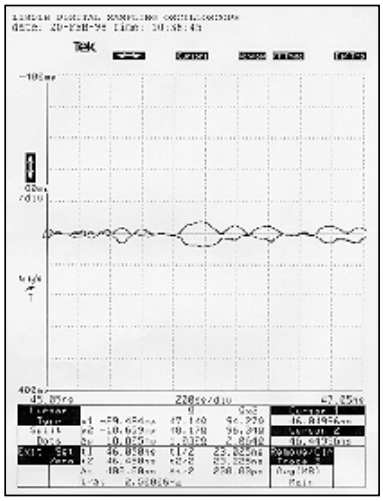
It is important to avoid bends or other cable irregularities when performing tests since they can affect the impedance of twisted-pair cables. The following scope displays show the results of bending approximately 1 meter of CAT5 Twisted-Pair Cable connected to a differential TDR plug-in on a Tektronix 11801 oscilloscope. Split Dot Cursor positions are fixed at the fifth and seventh graticles (cursors at 23.025ns and 23.225ns).



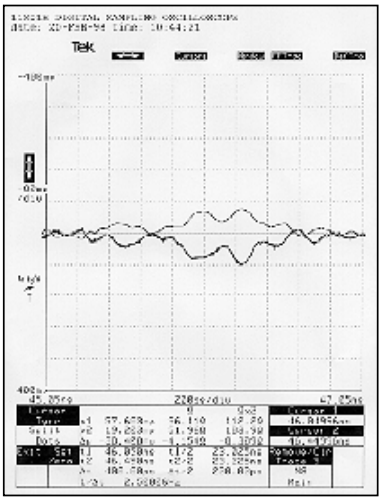
Cable Straight
Cursor 1 = 100.9 Ω
Cursor 2 = 101.7 Ω



Cable with 2" diameter loop in cursor area.
Cursor 1 = 101.7 Ω
Cursor 2 = 101.4 Ω
Note: A gentle bend has little affect.



Cable with half-knot in cursor area.
Cursor 1 = 94.3 Ω ; Cursor 2 = 96.3 Ω
Lower Z is caused by dielectric compression (Conductors are closer together).



Half-knot is untied & straightened.
Cursor 1 = 112.2 Ω ; Cursor 2 = 103.9 Ω
Higher Z is caused by "bird cage" effect (Conductors are farther apart).

$$Z_0 = \frac{276}{\sqrt{Er}} LOG \frac{2D}{d}$$

Figure F-1 Equation for Twin-Lead (Twisted-Pair) Cable

$$Z_0 = \frac{138}{\sqrt{Er}} LOG \frac{D}{d}$$

Figure F-2 Equation for Co-axial Cable

Using the Twin-Lead equation for the CAT 5 cable shown in Figure F-1, we can calculate the effect of compressing the cable (during sharp bends) or separating the wires (straightening after a sharp bend).

By compressing the dielectric between the two wires by 0.002 inches, the cable impedance was decreased to 95.3 ohms at the point of compression. This is similar to the impedance produced by the knot.

By separating the wires in the pair by 0.003 inches, the cable impedance increased to 111.9 ohms at the point of separation. This is similar to the impedance produced when a kinked cable is straightened— the wires can “birdcage” or separate.

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Appendix G Troubleshooting Guide

Many problems can occur during PHY conformance testing relating to problems with the equipment and software as well as with the Unit Under Test. This section provides troubleshooting tips to help debug these problems.

G.1 Test Problems

The most common problems which occur during testing involve displaying waveforms. Familiarity with the scope being used will greatly reduce the problems in this area. Refer to the scope's user's manual for more information. Most other problems are caused by the test setup and software configuration.

Some of the steps below may not be applicable to all of the procedures. Use only the ones that make sense for the test being performed.

G.1.1 Oscilloscope Setups

- Make sure all test equipment meets or exceeds the specifications listed in the introduction to this manual.
- Confirm that the expected voltage range of the signal does not exceed the capabilities of the differential probe being used. The probe listed in Appendix B requires the attenuation to be turned on in order to perform the measurements correctly.
- Confirm that the correct channel has been selected on the scope. Also confirm that the correct channel has been selected to be triggered on.
- Verify that the test fixture(s) and scope are connected as shown in. Make sure the scope probe is connected to the test fixture with the correct polarity.
- Check that the host computer for the UUT has been booted under DOS, and that LANConf.exe is running.
- Confirm that the UUT has been forced into 100Mbps mode. Once this has occurred (and before any other settings have been changed) scrambled MLT-3 waveforms should appear on the scope display. If the scope has a feature to automatically adjust scope settings, use it to make sure a signal is present. If no signal appears, power down the computer, unplug it, plug it back in, and restart it. Start LANConf.exe and force the UUT into 100Mbps mode.
- Check all LANConf.exe settings listed in the test procedure. Many problems are caused by simply forgetting to "Write" a change to memory. In order to make a change to a register value in LANConf.exe, it is necessary to first "Read" the relevant register values, "Write" the changes, and finally "Read" to confirm that the changes have been made. Make sure that the correct "Write" is used, as there may be more than one per screen.
- Do not use the automatic measurement features on the scope (if available). These features often do not correctly measure the desired waveform characteristics and as such are unreliable.

G.1.2 Network Analyzer Setups

- Make sure all test equipment meets or exceeds the specifications listed in the introduction to this manual.

- Verify that the analyzer is in “Network Analyzer” mode if it is a Spectrum/Network Analyzer.
- Make sure that the test equipment has been configured as shown in the test procedure.
- Check that the test fixtures have been connected as shown in Appendix B.
- Make sure the host computer is on and LANConf.exe is running. Although it may appear that the test can be done with the unit off, it does not always provide the same results. The only valid results are those that are taken when the UUT is powered up and LANConf.exe has been configured.
- Recalibrate the network analyzer as described in the test procedure. After calibration, confirm that the 50 ohm load shows a return loss of 9.54 dB. Also verify that the open and short loads produce the expected results.
- Check the cables connecting the network analyzer to the test fixture, and the test fixture to the UUT. If the analyzer reading changes noticeably when any of the equipment is moved (especially the coaxial cable) the cabling or fixture may need to be replaced.

G.2 Conformance Problems

Several factors can cause boards to fail PHY conformance testing. The best way to prevent failure is to follow Intel’s reference schematic and board layout guidelines which can be found in the product design kit.

Many of the tests described in this document deal with the transmitter characteristics. If the transmitter fails to meet specification, the link partner’s receiver may fail to correctly receive the signals, resulting in high Bit Error Rates on the receiving unit.

G.3 Differential Output Voltage (UTP) (ANSI specification 9.1.2.2)

This is one of the more important tests conducted during PHY conformance testing. If the design exhibits output voltage that is too high, the networking subsystem will, most likely, not pass FCC and EN55022 emissions testing.

In a networking environment, a system with this condition would not be able to communicate with other TP-PMD compliant systems. Receiving units would ignore any signal with an amplitude greater than the TP-PMD specified maximum.

A different set of problems characterize a design which fails to meet the minimum differential output voltage specification. A particularly significant symptom of this condition is the inability to establish communication with receive partners at the end of long cables (for example, 100 meters).

Verify that the appropriate component values have been used to implement the voltage reference component. This involves revisiting resistor and diode values for an external voltage reference or a resistor value for an internal voltage reference. The 10 and 100 Mbit biasing resistors should be verified against the values provided on reference designs. These biasing resistors should be tuned.

G.4 Overshoot (ANSI specification 9.1.3)

Excessive overshoot can cause problems because other receivers may not be designed to compensate for large amounts of overshoot.

It is absolutely imperative that low capacitance/high bandwidth probes be used for these measurements. Probes with greater than 1 pf capacitance and/or less than 1 GHz bandwidth may show false failures.

The value of the coupling capacitor between TDP and TDN should be increased in order to decrease transmit overshoot. However, increasing the value of this capacitor will reduce the transmit return loss. Additionally, it will increase the rise and fall times. Thus, an optimal value should be found through experimentation. A valid range for this capacitor on the 82558 is from 0 pF to 20 pF, with an average value of between 7 pF and 15 pF depending on the design. The required value of this capacitor is affected by both trace and magnetics capacitance.

G.5 Amplitude Symmetry (ANSI specification 9.1.4)

Incorrect amplitude symmetry can have a couple of undesired effects. First, it can decrease the distance apart two network stations can be before performance starts to seriously degrade. Assume that the receiver can pick up a 1 V peak signal over 100 meters of spec length cable. If the signal is asymmetric as shown in the figure below, the signal will only be able to be received to 95 meters of spec length cable. Even though the negative peak is 1050 mV, the limiting factor is the positive peak which is 950 mV.

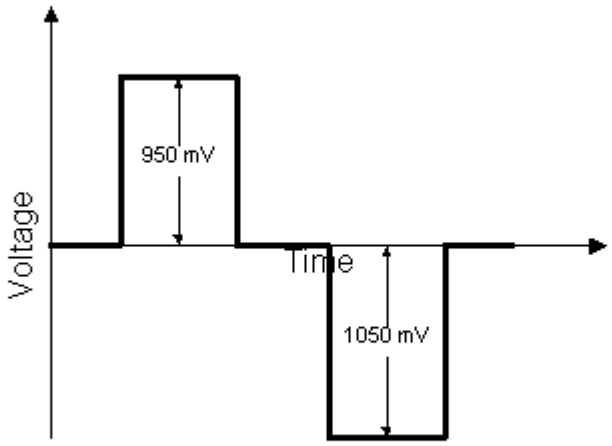

Figure G-1 Asymmetric Amplitudes

Additionally, asymmetric amplitudes could cause problems with the receiver's peak detectors, because they may be expecting both the positive and negative peaks to be at the same level. They could try to adjust the signal to make the peaks equal by adding in a DC offset, and in doing so would distort the waveform even more (because the zero point would become ambiguous).

Confirm that the resistors on TDN and TDP are identical (within 1%) and that they add up to 100 ohms. Also verify that the proper reference resistor values have been used.

G.6 Return Loss (ANSI specifications 9.1.5 and 9.2.2)

A system failing to meet return loss specifications indicates that substantial power is being reflected. Reflections are typically related to an impedance mismatch between the PHY and the transmit and receive signal traces. A system failing return loss would have a high BER on long cables, short cables, or both.

Trace geometry is a key factor in determining the impedance of traces on a board, which directly affect the design requirements. The proper impedance for both the transmit and the receive traces should be verified. Many design tools will miscalculate board parameters which affect the trace impedance. If the actual trace impedance is too low, the value can be improved by asking the board manufacturer for trace impedances higher than 100 ohms. This should provide higher impedances which are closer to 100 ohms.

If a capacitor is used between TDP and TDN to control rise time and overshoot, its value should not be too large. If the capacitance is too large, it can result in low return loss.

Trace length is also very important. Transmit and receive differential pairs should be routed at equal lengths from the PHY. The sum of all segments in one trace should be equal to the sum of all segments of its corresponding differential pair (in other words, the sum of all TDP segments equals the sum of all TDN segments). Also note that each trace in the differential pair should be run in parallel and on the same layer. Splitting the traces onto two different layers will cause poor common mode rejection.

G.7 Rise and Fall Times (ANSI specification 9.1.6)

Rise and fall times measure the time it takes for a pulse to rise to (and fall from) its peak amplitude. Slow rise and/or fall times may cause narrow pulses not to reach their maximum amplitude. Additionally, fast rise and/or fall times may increase the apparent width of the pulse and increase overshoot.

Rise and fall times are most directly affected by the capacitance between TDN and TDP, which includes both the capacitor and the trace capacitance. Increasing the capacitance increases the rise and fall times. Decreasing the capacitance will decrease the rise and fall times. This capacitance also has an impact on the transmitter return loss and overshoot. Increasing the capacitance decreases the return loss, and vice versa. Increasing the capacitance also reduces overshoot, while decreasing the capacitance increases overshoot. Experiment until a capacitance value is found that produces the best results.

G.8 Open Circuit Inductance (ANSI specification 9.1.7)

Transformers only pass AC current. If the signal being transmitted stays at ‘1’ or ‘0’ for any great length of time, it will begin to look like a DC signal to the transformer.

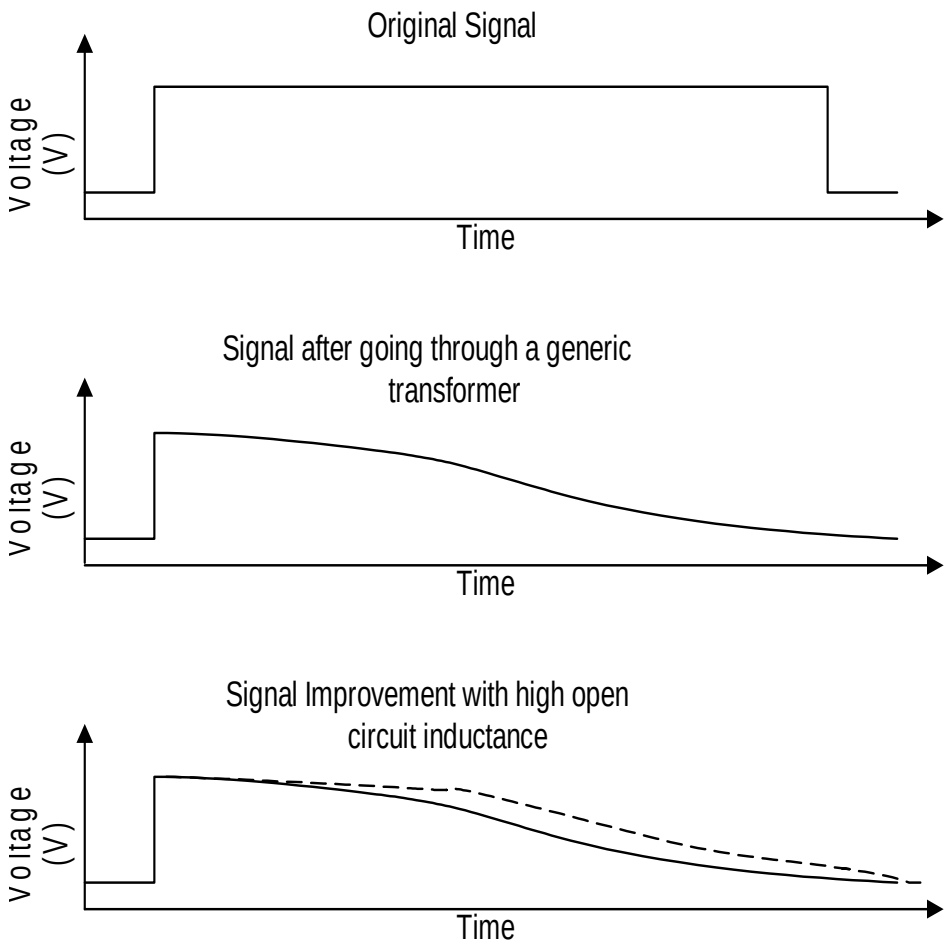

Figure G-2 Effects of low open circuit inductance for $0 \leq t \leq \infty$.

Note: The long pulse in the graphic above is meant to represent the effect of tens to hundreds of wide positive pulses in a row.

Magnetics that meet the open circuit inductance specification keep the signal quality from degrading as quickly. Systems that fail this specification may have poor BER results over long cables depending on the ability of the receiver to handle these degrading signals. Fortunately, these types of signals are never as long as shown above, so the problem will not usually be so dramatic that all of the packets will disappear. Normally, the extra inductance in the magnetics will improve the signals enough to prevent the majority of the errors.

G.9 Duty Cycle Distortion (ANSI specification 9.1.8)

Different receivers handle signals with duty cycle distortion differently. The general symptom of this problem will be that the receiver may drop some bits or it may think some bits are present when they really are not. This problem can be aggravated on a longer cable.

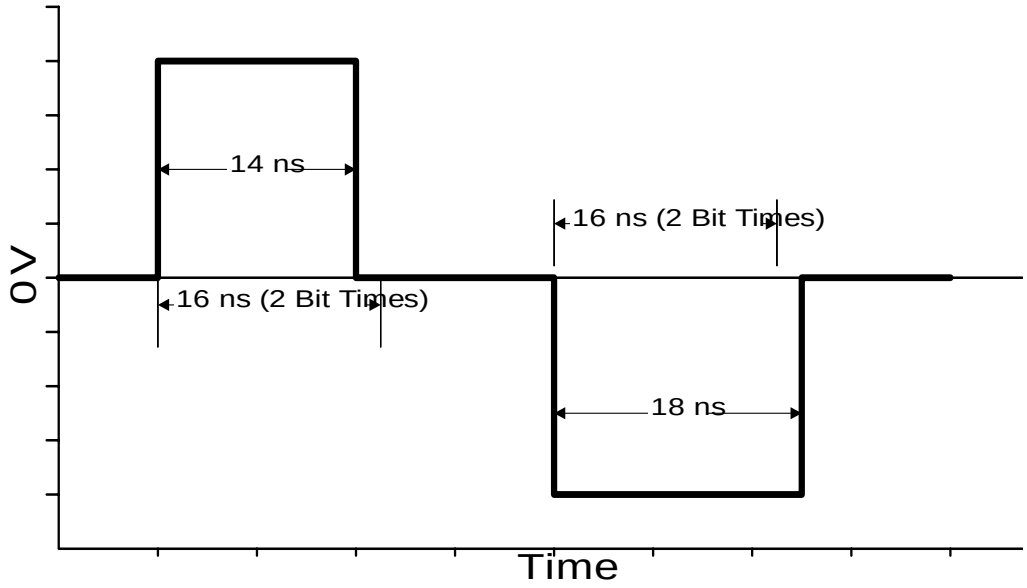

Figure G-3 Possible problems arising from duty cycle distortion. Each pulse above is meant to be two bit times.

Figure G-3 gives an idea of what could happen. Depending on the algorithm the receiver uses to detect the signal levels each bit time, it may decide that the first pulse above is only 1 bit instead of 2, and/or it may decide that the negative pulse is 3 bits instead of two. Thus, problems may only appear when transmitting to certain receive partners (with different Phy's).

If a crystal is being used, check that the loading capacitors are correct and are of equal values.

G.10 Transmit Jitter (ANSI specification 9.1.9)

Transmit jitter causes problems for the receiving unit because it becomes more difficult to distinguish the value of bits as jitter increases. Systems with excessive jitter will therefore cause the receiving unit to have high Bit Error Rates.

There are several causes of jitter that can be addressed in board design and layout. Noisy boards and poor common mode rejection will increase jitter. The noise can be made even worse by running high speed traces near the network controller or in parallel with the differential traces. To reduce noise, try as much as possible to maximize ground fill under the chip. Also make sure there is adequate decoupling between VCC and Ground around the networking chip and around other chips that may add noise to VCC. A metal top layer with several large via's down to the ground plane can reduce the problem.

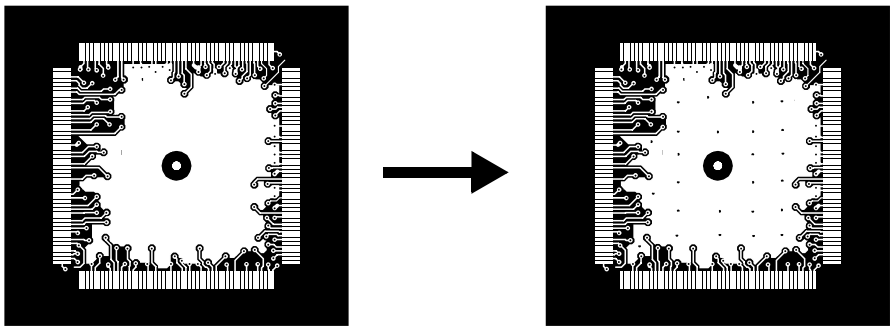

Figure G-4 Reducing jitter by reducing noise under the network controller.

Poor common mode rejection can be caused by asymmetric traces. They should be the same length, and should run parallel to each other from end to end.

Jitter can also be caused by a crystal or oscillator that is not producing the required output frequency.

G.11 Differential Input Signals (ANSI specification 9.2.1)

Bit error rate testing provides some of the most important test data. It is the data that can be most readily seen by customers. If the board is incapable of receiving without large numbers of errors, it will result in poor network performance.

Poor performance on this test can be caused by receiver circuit asymmetry or poor impedance matching as well as failure on any of the other tests in this document. Make sure that the transmitting unit is a known good unit. For example, don't use two systems with new designs to perform Bit Error tests, since any problems with the transmitter on one unit will cause the receiver to have high BER.

G.12 Receiver Common Mode Rejection (ANSI specification 9.2.3)

Common mode noise is noise which affects both wires in the differential pair simultaneously and in phase. Because it is the same across the pair, it can be rejected by the receive unit. The TP-PMD spec defines that the receiver should be able to withstand a 1 V peak-to-peak sine wave with frequencies between 0 – 125 MHz. This simulates common mode noise that could be picked up from running cables near power or telephony wiring.

For systems failing to meet common mode rejection specifications, verify that the common mode choke functionality of the magnetics module has been properly implemented. Make sure the ground planes and power planes under the magnetics module are separated by at least one-tenth of an inch between the PHY side of the magnetics module and the chassis side. Usually, this prevents common mode noise from bypassing the common mode chokes that are internal to the magnetics module.

Verify the following for both of the differential pairs (TDP and TDN, RDP and RDN) from the PHY to the magnetics module:

- Each trace is the same length.
- Each trace is the same impedance.

- One trace should mirror the other within the maximum suggested separation of one-tenth of an inch.
- Each trace needs to encounter common (or shared) components at the same distance from the PHY as the other trace in the same differential pair.

Good power to ground decoupling is important around the PHY and out to the RJ-45 connector. There are two types of decoupling capacitors, high frequency and bulk. The high frequency decoupling capacitors usually have a value of 0.1 µF and are placed throughout the board, especially close to power, ground, and fast switching signals. The bulk capacitors are used to keep the VCC and ground from bouncing. These are typically 22 µF tantalum capacitors on motherboards. However, for the family of Intel® EtherExpress™ PRO/100 adapters 4.7 µF ceramic capacitors are used.

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Appendix H Manual Register Settings

In some cases, the user may chose to perform the recommended tests manually. This appendix contains information on the manual register settings that must be completed to perform various tests in various 1000BASE-T silicon. For information on how to perform the manual test procedure, please refer to the appropriate IEEE specification document.

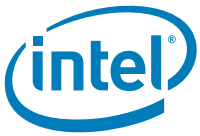
Note: Some tests require the same register to be adjusted more than once or in a specific sequence. Adjust the registers in the order listed from left to right.

H.1 82540 and 82546 Families

Test	Registers			
10Base-T Register Settings				
1411.10.02	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.03	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.07	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.09	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.12	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.13	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.11.05	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
100Base-Tx Register Settings				
9.1.2.2	Reg 0 = 2100	Reg 16 = 0F68	Reg 29 = 0002	Reg 30 = 0008
9.1.5	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	Reg 16 = 0F68
9.1.6	Reg 0 = 2100	Reg 16 = 0F68	Reg 29 = 0002	Reg 30 = 0008
9.1.8	Reg 0 = 2100	Reg 16 = 0F68	Reg 29 = 0002	Reg 30 = 000C
9.1.9	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	None
9.2.2	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	Reg 16 = 3B08
1000Base-T Register Settings				
40.6.1.2.1	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 2200
40.6.1.2.2	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 2200
40.8.3.1	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 8200
40.8.3.3	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 8200

H.2 82541 and 82547 Families

Test	Registers				
10Base-T Register Settings					
1411.10.02	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.10.03	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.10.07	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.10.09	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.10.12[1]	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.10.13[1]	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
1411.11.05[1]	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 0000	Reg 4 = 0021	Reg 9 = 1000
100Base-Tx Register Settings					
9.1.2.2	Reg 0 = 2100	Reg 12 = 0809	Reg 0 = 1800	None	None
9.1.5	Reg 0 = 2100	Reg 12 = 0809	Reg 0 = 1800	None	None
9.1.6	Reg 0 = 2100	Reg 12 = 0809	Reg 0 = 1800	None	None
9.1.8	Reg 0 = 2100	Reg 12 = 0808	Reg 0 = 1800	None	None
9.1.9[1]	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 1000
9.2.2[1]	Reg 16 = 41A0	Reg 18 = 0E00	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 1000
1000Base-T Register Settings					
40.6.1.2.1	Reg 0 = 0140	Reg 9 = 3B00	None	None	None



40.6.1.2.2	Reg 0 = 0140	Reg 9 = 3B00	None	None	None
40.6.1.2.5	Reg 0 = 0140	Reg 9 = 7B00	None	None	None
40.8.3.1	Reg 0 = 0140	Reg 9 = 9B00	None	None	None
40.8.3.3	Reg 0 = 0140	Reg 9 = 9B00	None	None	None

1. Set last four digits to 1840 before adjusting other registers.

H.3 82544 Family

Test	Registers			
10Base-T Register Settings				
1411.10.02	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.03	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.07	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.09	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.12	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.10.13	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
1411.11.05	Reg 0 = 8000	Reg 4 = 0021	Reg 9 = 0000	Reg 16 = 3C08
100Base-Tx Register Settings				
9.1.2.2	Please see the 82544 appendix			
9.1.5	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	Reg 16 = 0F68
9.1.6	Please see the 82544 appendix			
9.1.8	Please see the 82544 appendix			
9.1.9	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	None
9.2.2	Reg 0 = 2100	Reg 4 = 0101	Reg 9 = 0000	Reg 16 = 3B08
1000Base-T Register Settings				
40.6.1.2.1	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 2200
40.6.1.2.2	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 2200
40.8.3.1	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 8200
40.8.3.3	Reg 16 = 0B08	Reg 0 = 8140	Reg 16 = 0F08	Reg 9 = 8200

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Appendix I 100Base-TX Test Procedure for the 82544 Chip

I.1 Introduction

A few of our prior test procedures will not work well with the 82544 chip. This document has been written to enable 100Base-TX physical layer testing with the 82544.

To make 100Base-TX testing easier, most Intel 825xx physical layer chips allow the test operator to disable scrambling and 4B/5B encoding, by setting the appropriate bits in the phy registers. By disabling both scrambling and 4B/5B, and by transmitting certain fixed data patterns, it was easier to repetitively generate the required waveforms for performing some of the 100Base-TX physical layer tests. Continuous, repetitive waveforms are easier to trigger on, and they allow the operator to use an oscilloscope's averaging function while viewing the repetitively captured waveforms.

Note: 82544 does not have a test feature, to disable 4B/5B encoding. Consequently, continuously transmitting the same pulse widths with the same width mid-level shoulders is virtually impossible. This means that each captured pulse is more likely to have different amounts of "DC offset" (due to baseline wander, which is related to the pulse-width and polarity of the preceding pulses, which can not always be controlled with 82544.)

Although it is still possible to pulse-width trigger on 100Base-TX waveforms, which are transmitted by the 82544, the constantly changing DC offsets cause a large amount of amplitude jitter in the acquired waveform. Normally, averaging reduces the level of jitter that is visible to the operator, and averaging makes it easier to accurately place an oscilloscope's horizontal cursor on key parts of the 100Base-TX pulse. Unfortunately, because the widths of the mid-level, MLT-3 "shoulders" cannot be controlled and are not continuously repetitive. Selecting the appropriate location for the oscilloscope's horizontal cursors, on the mid-level shoulder of an averaged 100Base-TX waveform is virtually impossible. Immediately to the left and right of the trigger pulse, the waveform is continuously changing shape and level. On an averaged 82544 waveform, there is no obvious place to place the cursor, when the operator is trying to locate the base of an averaged 100Base-TX pulse.

Note: It is still possible to perform 100Base-TX phy conformance tests, as long as oscilloscope averaging is disabled. This document provides modified versions of some 100Base-TX phy conformance test procedures, to make it easier for test operators to perform these tests, and to get consistent and accurate test results.

This document provides alternate test procedures for 100Base-TX:

- Differential Output Amplitude
  (ANSI TP-PMD specification 9.1.2.2) - Section I.3.
- Rise and Fall Time (ANSI TP-PMD specification 9.1.6) - Section I.4.
- Transmitter Duty Cycle Distortion
  (ANSI TP-PMD specification 9.1.8) - Section I.5.

I.2 Equipment Used for This Procedure

- Test Equipment

  - — Tektronix® TDS784C oscilloscope (1 GHz BW) in single-shot, hi-resolution mode.
  - — P6248 Differential Probe (1.5 GHz BW) Mode = /10, or P6247 Differential Probe (1 GHz BW) Mode = /10.
- PCs, Adapter Cards, and Test Software
  - — 82554 based LAN adapter or LOM design as Unit Under Test LANConf.exe test software can be used to force A0 82554 to transmit random data.
  - — A 82559 LAN adapter (Albany) installed in a PII desktop PC requires LANConf to force the 82544 UUT to transmit 100Base-TX scrambles idles.
- LANConf.exe Software
  - — Register settings are provided in Appendix H.
  - — This software can be used if an Intel 10/100 LAN partner is used to transmit 100Base-TX scrambled idles. Register settings are provided in a separate document.
- Test Fixtures
  - — See Appendix A.2.
  - — See Appendix A.7.

I.3 Specification 9.1.2.2 - Differential Output Voltage (UTP)

I.3.1 Test Case

Differential Output Voltage (specification 9.1.2.2)

I.3.2 Test Purpose

To measure the peak differential output voltage at the transmit pins of the RJ-45 connector (also called the Active Output Interface or AOI).

I.3.3 Specification

At the RJ-45 connector, the differential output voltage, +Vout, shall be within the range between +950 mV and +1050 mV, and Vout, shall be within the range between -950 mV and -1050 mV.

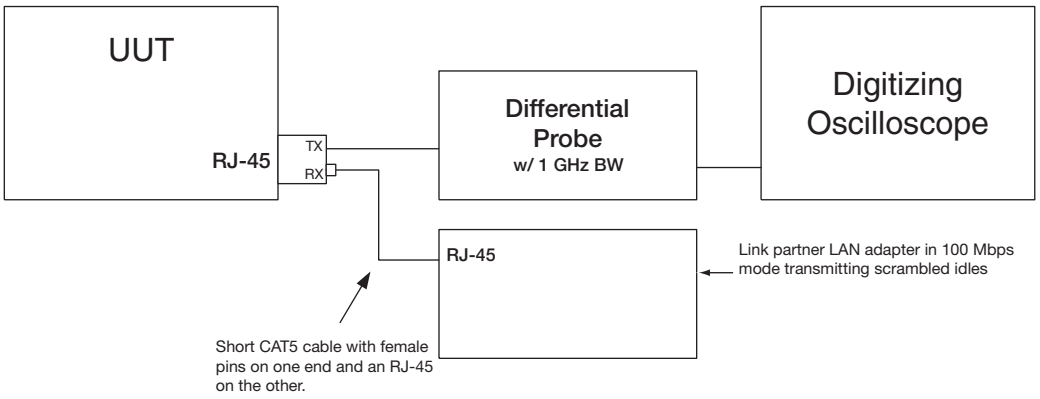


Figure I-1 Waveform at Active Output Interface

I.3.4 Test Equipment

- Digitizing Oscilloscope with at least 1 GHz bandwidth
- Differential Probe with 1 GHz or greater bandwidth (like P6247)
- Host computer with LANConf.exe software (for 82554 silicon).

I.3.5 Test Fixtures

100 Ohm UTP Test Load. Fixture: F9.1.2.A.

The test load shall consist of a single 100 ohm + 0.1% resistor connected across the transmit pins of a mating RJ-45 connector. The series inductance of the load shall not be greater than 20 nH, and the parallel capacitance shall not be greater than 2 pF.

I.3.6 Test Procedure

1. Connect the Test equipment and Unit Under Test (UUT) as shown in Figure I-2 on page I-138 (which shows the setup for test specifications 9.1.2.2, 9.16, and 9.1.8).
2. Use software or firmware control to force the unit under test to transmit frames in 100BASE-TX mode. The data pattern is NOT important. Leave Scrambling ENABLED (the phy's default or normal mode of operation).
3. Configure the oscilloscope according to Table I-1 and Table I-2.

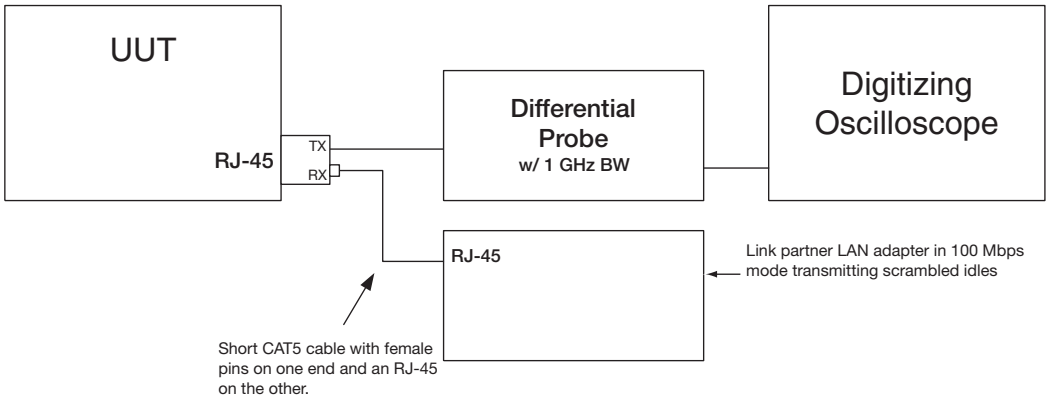


Figure I-2 Test Setup Number

Table I-1 For Positive Peak Differential Output Amplitude (see Figure I-3)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-100 mV to +1100 mV (1200 mV over the full vertical scale)
Vertical Position	-3.5 divisions to -4.0 divisions
Trigger Type	Positive, Pulse Width Triggering: ~108 ns lower bound, ~116 ns upper bound
Trigger Level	+500 mV
Trigger Signal	Differential signal at the pins of the test load.

Table I-2 For Negative Peak Differential Output Amplitude (see Figure I-4)

Scope Parameter	Setting
Horizontal Scale	~25 ns/division
Vertical Range	-1100 mV to +100 mV (1200 mV over the full vertical scale)
Vertical Position	+3.5 divisions to +4.0 divisions
Trigger Type	Negative, Pulse Width Triggering: ~108 ns lower bound, ~116 ns upper bound
Trigger Level	-500 mV
Trigger Signal	Differential signal at the pins of the test load.

Pulse Width Triggering

Triggering information is provided to give a good starting point for measurement. The following guidelines will help the tester achieve the most stable display.

1. Set the trigger level as specified in the above table.
2. Select pulse width triggering.
3. Set the upper bound parameter to approximately 400 ns and the lower bound parameter to approximately 125 ns.
4. Set the trigger mode to normal.
5. Increase the lower bound parameter gradually until the triggering is lost.
6. Decrease the lower bound parameter slowly in 6 ns increments until triggering resumes.
7. Decrease the upper bound parameter until it is 6 ns to 15 ns above the lower trigger bound parameter.

Following the above method should ensure a good trigger with minimal added jitter.

4. Use the horizontal offset to position the waveform, as shown in Figure I-1.
5. Change the Oscilloscope's signal acquisition mode to "Single Sequence" and/or "One-Shot" acquisition mode. [Do NOT use averaging. Do NOT use sampling mode.]
6. Push the trigger button; then observe the captured waveform. Keep doing manual triggers, until a pulse is acquired that has mid-level "shoulders" on both sides; with each shoulder being at least 20 nseconds wide (see Figure I-1, Figure I-3, and Figure I-4).
7. Select the horizontal cursors. Move one cursor to +Vout, and move the other cursor to -Vout. The differential output voltage is the difference between the two cursors.

See Figure I-1 for measurement points. +Vout is the difference (delta) between the average MLT-3 mid-level (~0 volts), and the average peak positive output voltage. This does not include overshoot. If there is ripple or overshoot at either level, the amplitude cursor may slice through it.

Although it is not specifically mentioned in specification 9.1.2.2, -Vout should be between –950 mV and –1050 mV. Figure I-3 and Figure I-3 provide examples of data for differential output voltage.

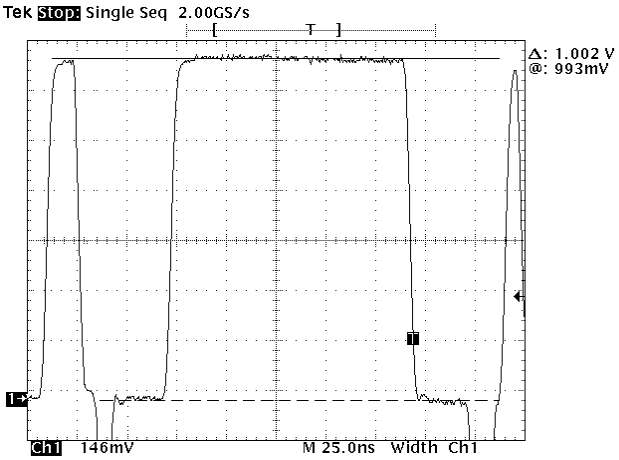


Figure I-3 Positive Peak Differential Output Voltage

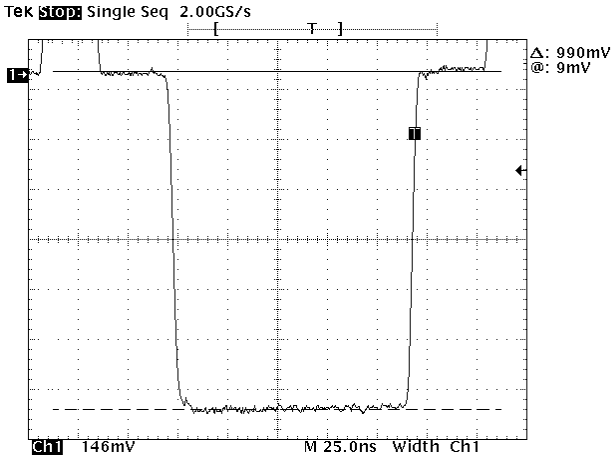


Figure I-4 Negative Peak Differential Output Voltage

I.4 Specification 9.1.6 - Rise/Fall Times

I.4.1 Test Purpose

To measure the rise and fall times of a 100Base-TX transmit waveform. Both positive and negative waveforms need to be measured.

I.4.2 Specification

Rise time is the time it takes for the differential output signal to rise from the MLT-3 mid-level (~0 volts) to either +Vout or to –Vout. Fall time is the time it takes for a signal to fall from either +Vout or –Vout back to the MLT-3 mid-level (~0 volts).

Rise and fall times for the positive differential output will be the time difference (delta nsec.) between 10% of +Vout and 90% of +Vout.

Rise and fall times for the negative differential output will be the time difference (delta nsec.) between 10% of -Vout and 90% of -Vout.

Note: Note that measured rise and fall times must be within the range between 3.0 nsec. and 5.0 nsec. The maximum variation in any rise time with respect to any fall time shall be 0.5 nsec or less.

I.4.3 Test Equipment

- Digitizing Oscilloscope with at least 1 GHz bandwidth
- Differential Probe with 1 GHz or greater bandwidth (like P6247)
- Host computer with LANConf.exe software (for 82554 silicon).

I.4.4 Test Fixtures

100 Ohm UTP Test Load. Fixture: F9.1.2.A.

I.4.5 Test Procedure

1. Connect the test equipment and Unit Under Test (UUT), as shown in Figure I-2.
2. Use software or firmware control to force the unit under test to transmit frames in 100BASE-TX mode.
3. Configure the oscilloscope according to Table I-3 and Table I-4.

Table I-1 For Positive Peak Differential Output Amplitude

Scope Parameter	Setting
Horizontal Scale	1 ns/division
Vertical Range	-100 mV to +1100 mV (1200 mV over the full vertical scale)
Vertical Position	-3.5 divisions to -4.0 divisions
Trigger Type	Positive, Pulse Width Triggering: ~116 ns lower bound, ~124 ns upper bound (If shorter pulses are used, the lower bound may be lowered.)
Trigger Level	+500 mV
Trigger Signal	Differential signal at the pins of the test load.

Table I-2 For Negative Peak Differential Output Amplitude

Scope Parameter	Setting
Horizontal Scale	1 ns/division
Vertical Range	-1100 mV to +100 mV (1200 mV over the full vertical scale)
Vertical Position	+3.5 divisions to +4.0 divisions
Trigger Type	Negative, Pulse Width Triggering: ~116 ns lower bound, ~124 ns upper bound (If shorter pulses are used, the lower bound may be lowered.)
Trigger Level	-500 mV
Trigger Signal	Differential signal at the pins of the test load.

I.4.6 Notes for Using Pulse-Width Triggering

Note: Most of the following procedure is very similar to the procedure for 9.1.2.1 Differential Output Voltage (Appendix I.3) except: (1) the horizontal scale is only 1 nsec per division, and (2) the operator is required to scroll left and right through the pulse -- to see if the MLT mid-level shoulders are at least 20 nsec wide on both sides of the pulse; AND for rise and fall times, the operator must make several different plots with both horizontal cursors and “cross-hair” cursors.

1. Set the trigger level to ~500 mV.
2. Select Pulse-Width triggering.
3. Start with the upper bound at ~118 nsec, and the lower bound at ~106 nsec.

4. Set the Trigger Mode to NORMAL.
5. Set both the Trigger Position and the Horizontal Position to appear on the display.
6. Gradually increase the lower trigger limit, until all triggering is lost,
7. Then slowly decrease the lower trigger limit by (about 5 nsec), until triggering resumes.
8. Decrease the upper trigger limit until it is ~5 nsec to 12 nsec above lower trigger limit.
9. Following the above method should ensure a good trigger with minimal added jitter.
10. Use the horizontal offset to position the waveform, as shown in Figure I-1 on page I-137.
11. Change the Oscilloscope's signal acquisition mode to "Single Sequence" and/or "One-Shot" acquisition mode. (Do NOT use averaging. Do NOT use sampling mode.)
12. Push the trigger button; then scroll all the way to the left edge and all the way to the right edge of the captured pulse. Note the MLT-3 mid-level shoulders (are they at least 20 nseconds wide?). Keep doing manual triggers, until a pulse is acquired that has mid-level "shoulders" on both sides; with each shoulder being at least 20 nseconds wide (see Figure I-1, Figure I-3, and Figure I-4).
13. Scroll horizontally through the waveform, until the left shoulder is occupying the width of the oscilloscope display. Select the horizontal cursors. Move one cursor to the top side of the mid-level shoulder. Move the other cursor to the bottom side of the mid-level shoulder. Record the values of both cursors. [See Figure I-5 and Figure I-6.]

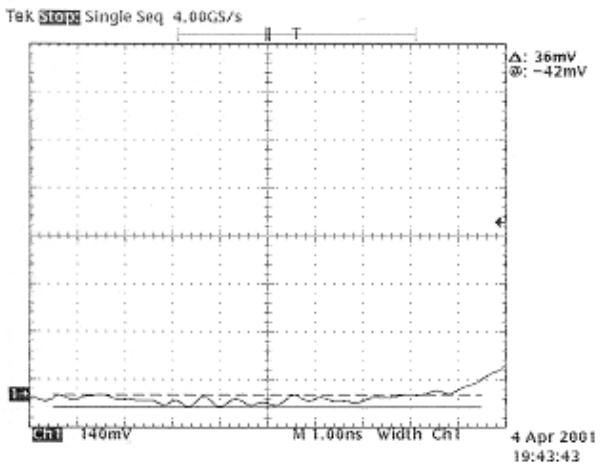


Figure I-5 Lower-left MLT-3 mid-level, lower cursor

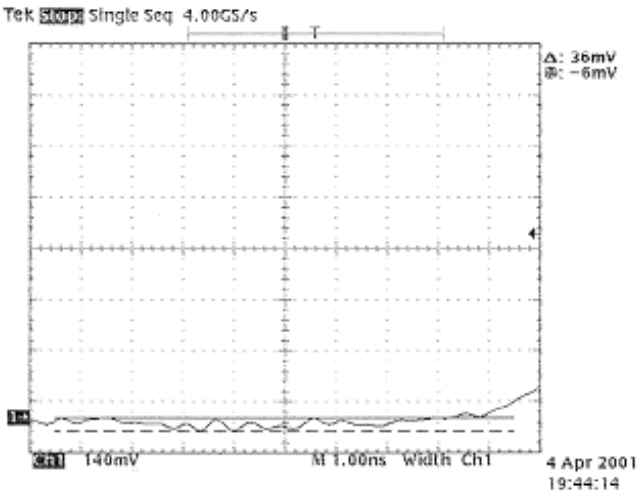


Figure I-6 Upper-left MLT-3 mid-level, upper cursor

14. Scroll horizontally through the waveform, until the right shoulder is occupying the width of the oscilloscope display. Select the horizontal cursors. Move one cursor to the top side of the mid-level shoulder. Move the other cursor to the bottom side of the mid-level shoulder. Record the values of both cursors. [See Figure I-7 and Figure I-8.]

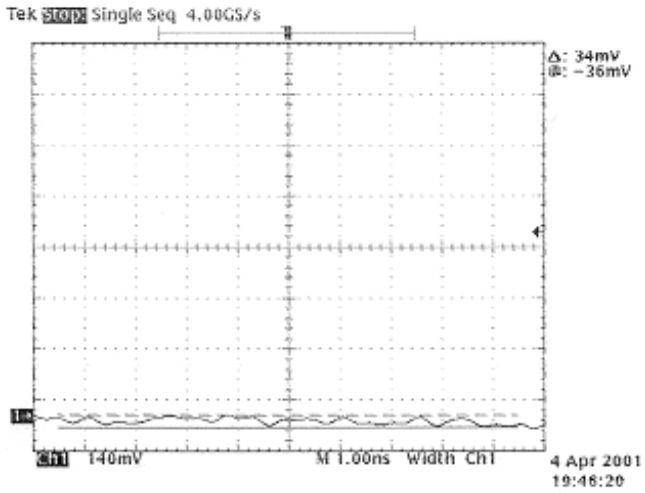


Figure I-7 Lower-right MLT-3 mid-level, lower cursor

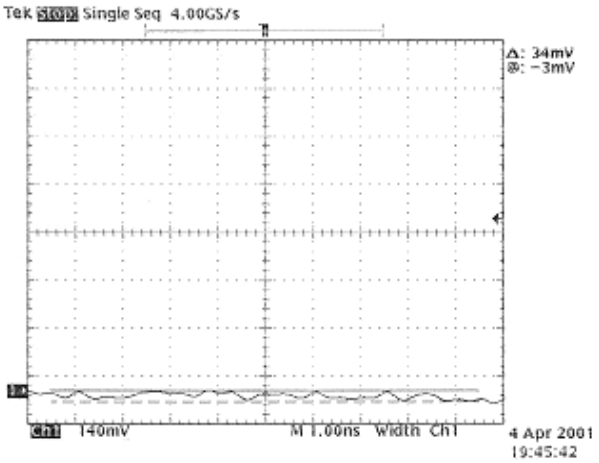


Figure I-8 Upper-right MLT-3 mid-level, upper cursor

15. AVERAGE the values of the cursors from the last two steps (average four cursor values). The result is the mid-level value that will be considered the base of the pulse. [-21.75 mV is the average mid-level, from example Figure I-5 through Figure I-8]
16. Scroll horizontally through the waveform, until the approximate center of the pulse peak is visible on the oscilloscope display. Select the horizontal cursors. Move one cursor to the top of the ripple on the peak voltage. Move the second cursor to the bottom of the ripple on the peak voltage. The average of these two cursor levels is the pulse top voltage that is used to calculate the 10% and 90% points on the rising and falling edges. [See Figure I-9 and Figure I-10.]

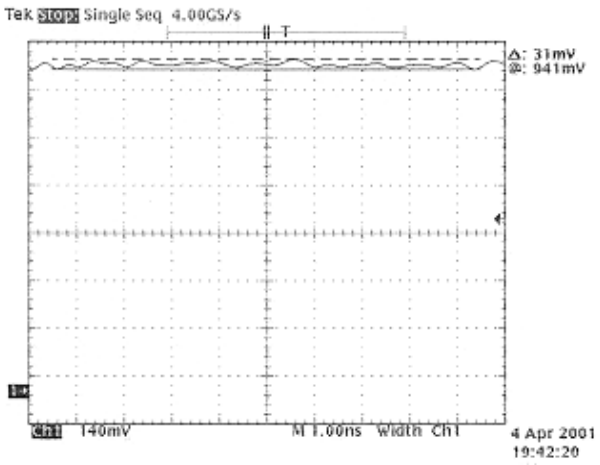


Figure I-9 Positive Pulse Peak, lower cursor

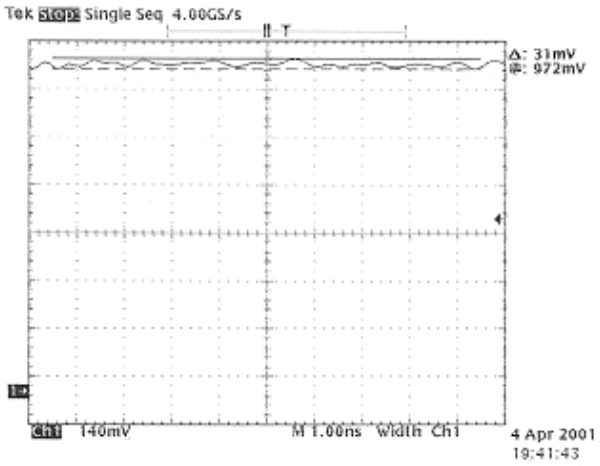


Figure I-10 Positive Pulse Peak, upper cursor

17. Use the data from the last two steps, two calculate the 10% and 90% points for the pulse rise time and fall time. [See Table I-2 in Section I.4.7.]
18. Select the cross-hair cursors. Move one cursor to 10% of +Vout on the rising edge of the waveform, and move the other cursor to 90% of +Vout on the rising edge. Rise time is the difference in time (Dt) between the two markers. To measure the fall time, position the cursors at 10% and 90% of +Vout on the falling edge of the waveform. Fall time is the difference in time (Dt) between the two markers. Repeat these measurements on the negative-going waveform.

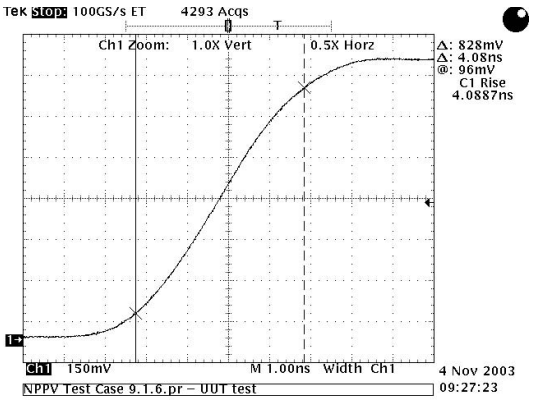
Note: Repeat all of these steps for both a positive pulse and for a negative pulse.

For the sake of brevity (and to avoid repetition) example plots are not provided for a negative pulse.

Figure I-11 and Figure I-12 in Section I.4.7 are examples of what the data may look like for a positive pulse.

I.4.7 10% and 90% of Positive Peak Voltage Calculations

Four mid-level cursor positions (two for each mid-level shoulder)	MLT-3 mid-level (mV)	Two cursors, which "sandwich" the pulse top.	Peak Level (mV)
Left shoulder, top cursor	-6	Positive Pulse, top: upper cursor	972
Left shoulder, bottom cursor	-42	Positive Pulse top, lower cursor	941
Right shoulder, top cursor	-3	Averaged Pulse Peak Level (mV)	956.5
Right shoulder, bottom cursor	-36		
Average MLT-3 mid-level (mV)	-21.75		
10% voltage point on slope = (0.1 x (Averaged Peak - Averaged mid-level)) + Averaged MLT-3 mid-level			
90% voltage point on slope = (0.9 x (Averaged Peak - Averaged mid-level)) + Averaged MLT-3 mid-level			
10% pt = -21.75 mV + 97.825 mV = 76.075mV; 90% pt = 956.5 – 97.825 mV = 858.675mV			
Target 10% point = 76.075mV			
Target 90% point = 858.675mV			



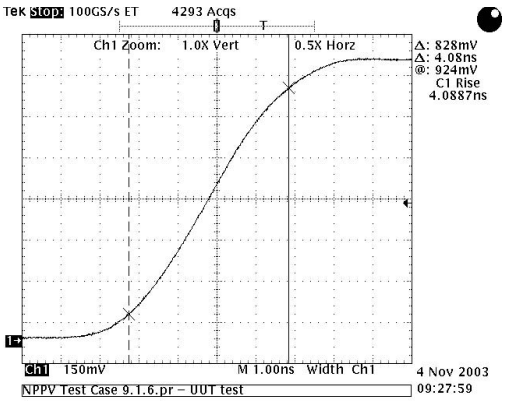


Figure I-11 Rise-Time, 10% Cursor (left) and 90% Cursor (right)

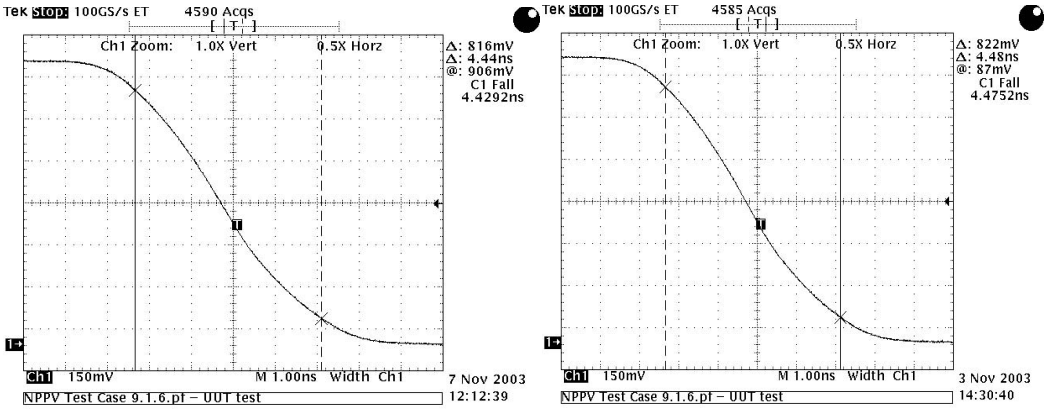


Figure I-12 Fall-Time, 90% Cursor (left) and 10% Cursor (right)

Note: In many plots, the cursors almost never end up exactly on the 10% and 90% voltage levels. This is because even with the vertical scale set to provide best-case vertical resolution, the smallest discrete vertical increment is 3 mV. Consequently, one should try to position both cursors to the closest adjacent points on the slope nearest to the 10% and 90% voltage points.

For the sake of brevity (and to avoid repetition) example plots are NOT provided for a negative pulse.

Repeat all of these steps for both a positive pulse and for a negative pulse.

I.4.8 9.1.6 Rise and Fall Times

Measured Rise and Fall times shall be between 3.0 and 5.0 nsec.

Rise to Fall delta shall be < 0.5 nsec.

Table I-3 9.1.6 Rise and Fall Times

UUT	Time (nsec.)
Positive Rise Time ns.	4.88
Positive Fall Time ns.	4.84
delta Pos. rise/fall time	0.04 nsec.
Negative Rise Time ns.	4.72
Negative Fall Time ns.	4.88
delta Neg. rise/fall time	0.16 nsec
Pass/Fail	PASS

Measured rise and fall times must be within the range between 3.0 nsec. and 5.0 nsec.

The maximum variation in any rise time with respect to any fall time shall be 0.5 nsec or less.

I.5 Specification 9.1.8 - Duty Cycle Distortion (DCD)

I.5.1 Test Case

Duty Cycle Distortion (specification 9.1.8)

I.5.2 Test Purpose

To measure the Duty Cycle at the four MLT-3 transitions, using a pattern in non-scrambled mode.

I.5.3 Specification

When measured between 50% voltage points on +Vout and –Vout, all positive pulse widths, negative pulse widths, and mid-level time periods must be between 15.50 nsec and 16.50 nsec.

Note: The specification wording within the ANSI TP-PMD can be confusing, but the illustration in the TP-PMD clearly shows that +/- 0.5 nsec variation is allowed.

I.5.4 Test Equipment

- Digitizing oscilloscope with at least 1 GHz bandwidth
- P6247 Differential Probe (or equivalent differential probe)
- Host computer with LANConf.exe software

I.5.5 Test Fixtures

100 ohm termination fixture 9.1.2.A.

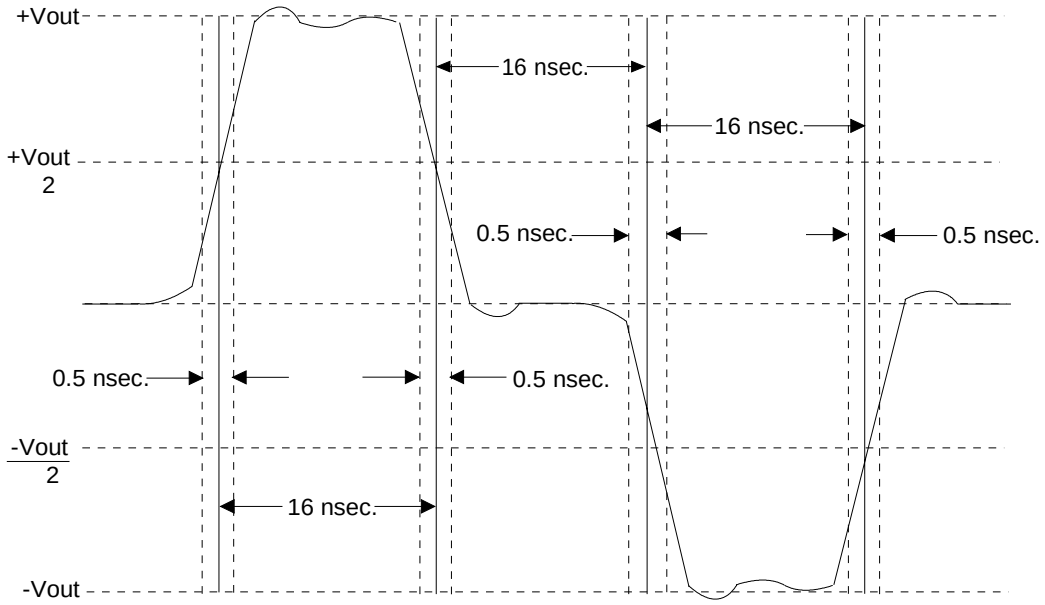


Figure I-13 Active Output Interface Duty Cycle Distortion (Figure 9-3)

I.5.6 Test Procedure

Connect the test equipment and Unit Under Test (UUT), as shown in Figure I-2. If available, use register settings or test pins to:

- Disable Scrambling.
- Force 100 Mbps Good Link.
- Transmit a hexadecimal 3,4,3,4,3,4... data pattern (creates16 nsec wide pulses).

If the above settings are implemented, the Phy will automatically transmit 16ns wide pulses.

I.5.7 Generic Oscilloscope Settings

Table I-4 For Duty Cycle Distortion Measurements

Scope Parameter	Setting
Horizontal Scale	~5 ns/division, and 2 ns/division
Vertical Range	-1200 mV to +1200 mV (2400 mV over the full vertical scale)
Trigger Type	Positive, Pulse Width Triggering: ~14 ns lower bound, ~18 ns upper bound (If shorter pulses are used, the lower bound may be lowered.)
Trigger Level	+400 mV
Trigger Signal	16 ns positive pulse.

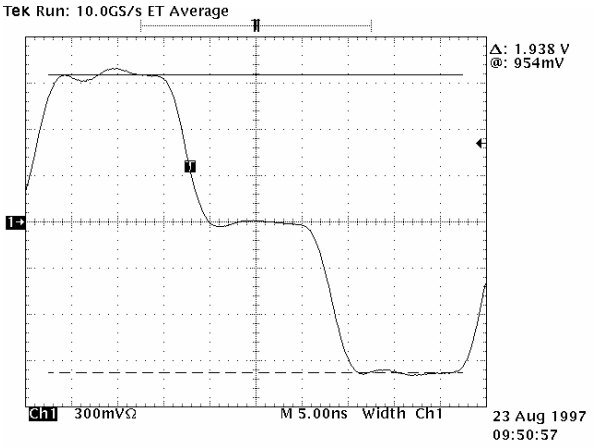


Figure I-14 16 ns pulse peaks used to calculate 50% levels

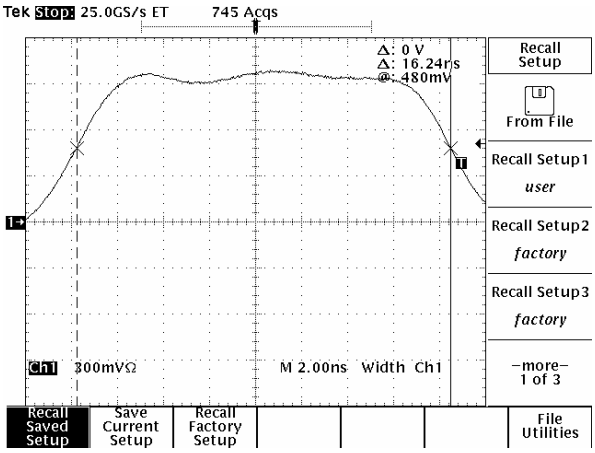


Figure I-15 Positive pulse width at 50% amplitude level

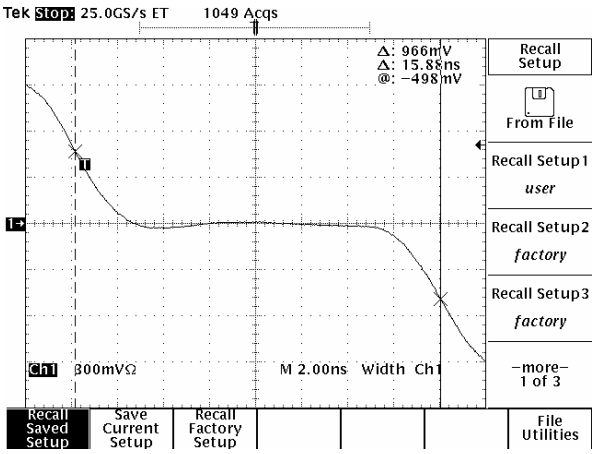


Figure I-16 MLT-3 mid-level width at 50% levels.

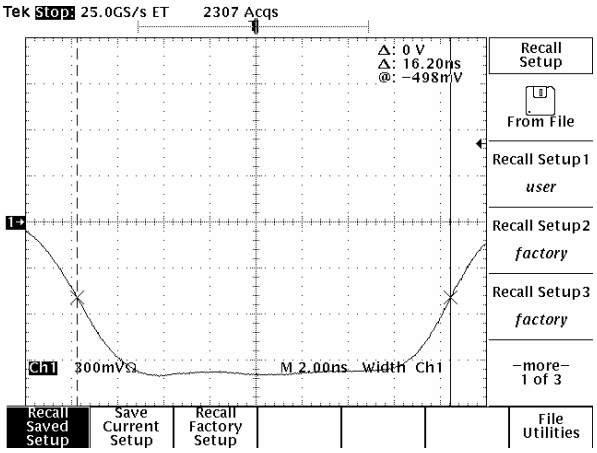


Figure I-17 Negative pulse width at 50% amplitude level

I.5.8 Duty Cycle Distortion Data

For Figure I-14 through Figure I-17.

When measured between 50% voltage points on +Vout and –Vout, positive pulse widths, negative pulse widths, and mid-level time periods must be between 15.50 nsec and 16.50 nsec.

Interpretation the ANSI TP-PMD version of this spec is somewhat confusing. The text suggests the acceptable range for each pulse is 15.75 nsec to 16.25 nseconds, but the 9.3 illustration in the specification clearly shows a range from 15.50 to 16.50 nsec. We believe the illustration is correct, and it helps to explain the text within the spec, regarding a fit to a time grid with 16 nsec spacing – That is, *each edge of each pulse is allowed +/- 25 nsec deviation, so the net result is a range from 15.50 nsec to 16.50 nsec.*

§ §