

8

7

6

5

4

3

2

1

REFERENCE DESIGN

PCIE SINGLE LANE 1000/100/10 BASE-T

INTEL 82574 ETHERNET CONTROLER

F

F

E

E

D

D

C

C

B

B

A

A

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TITLE 82574 REFERENCE DESIGN

SIZE CODE DOCUMENT NUMBER

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SHEET 1

8

7

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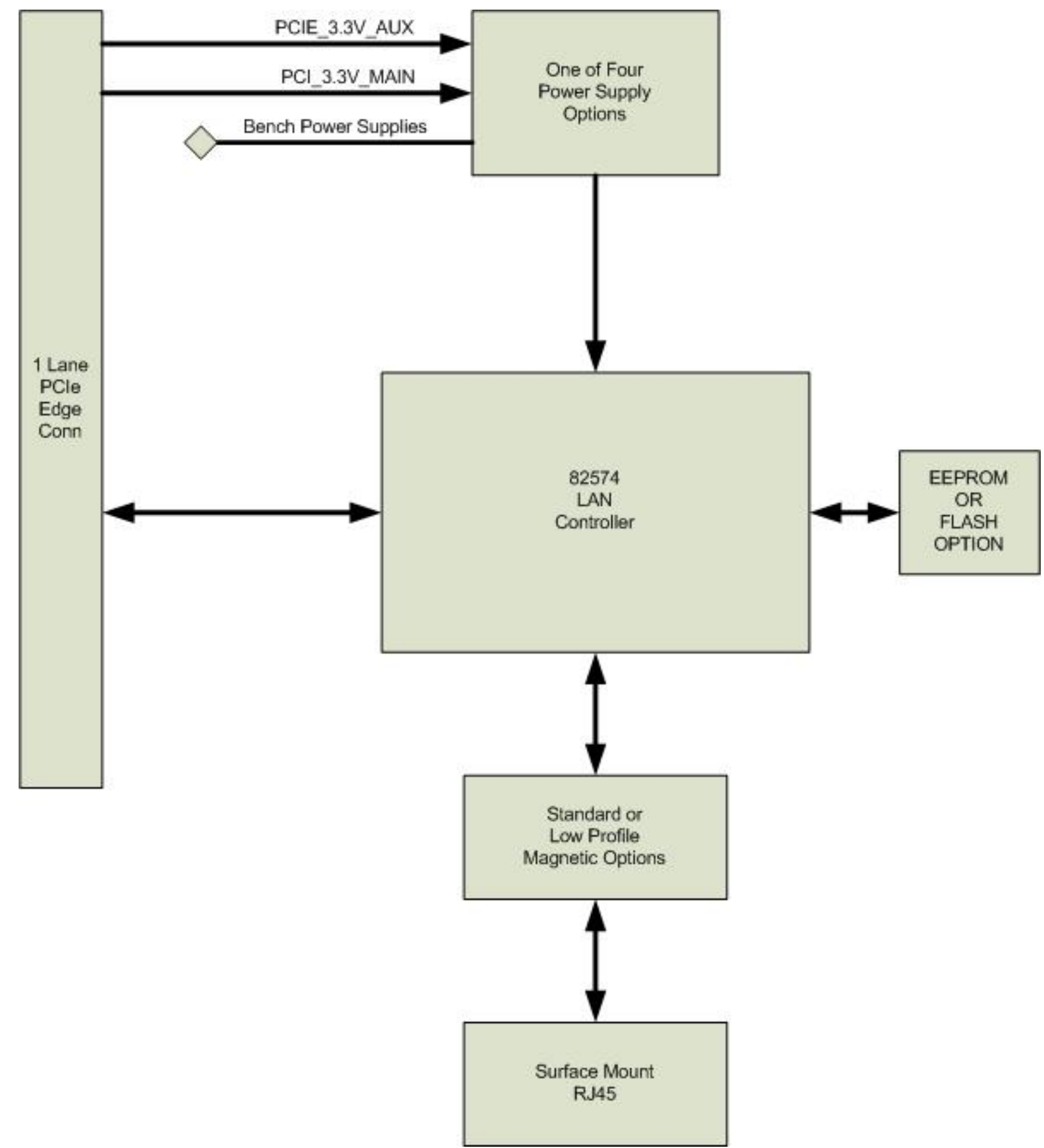
4

3

2

1

FUNCTIONAL BLOCK DIAGRAM



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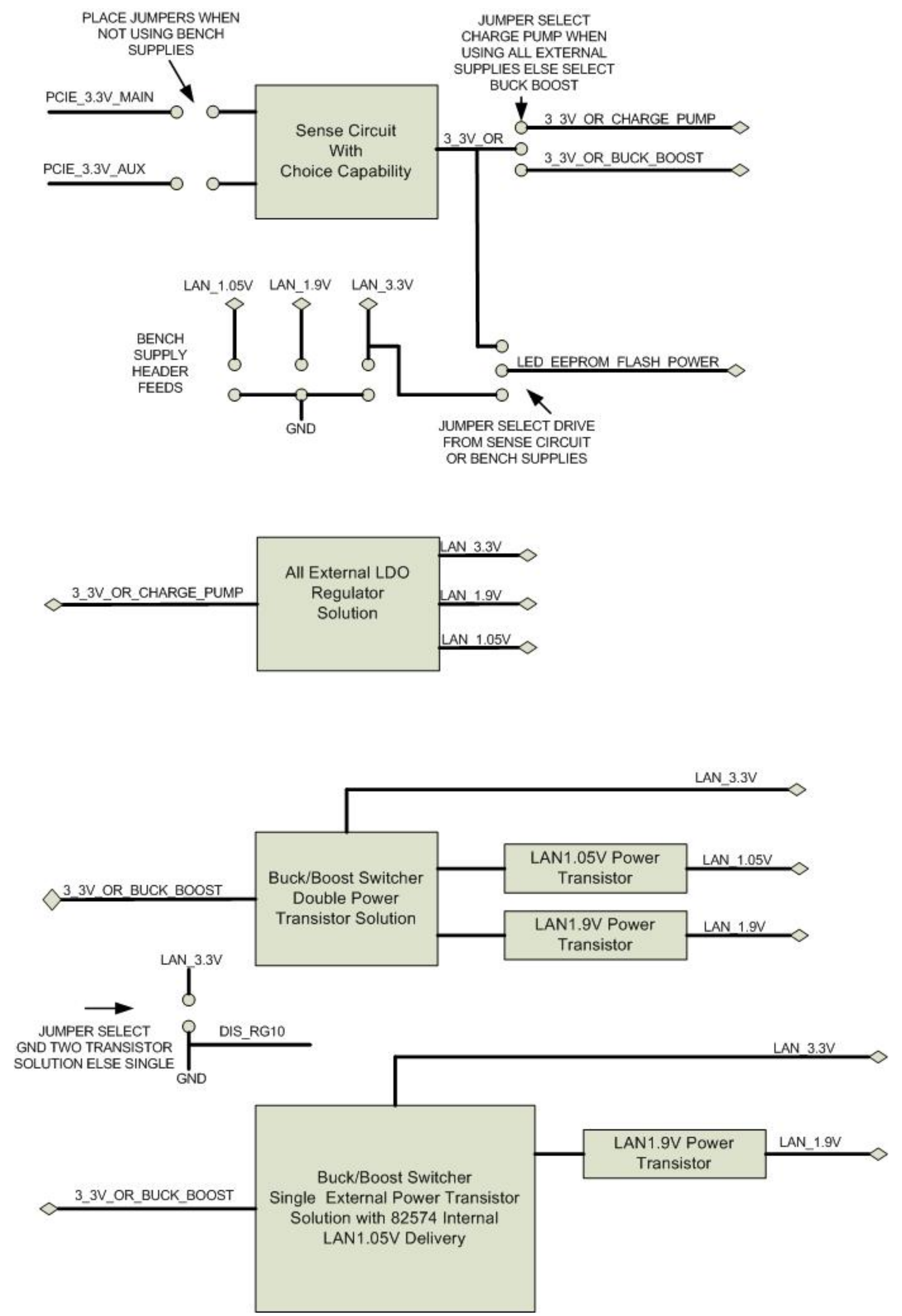
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SHEET 2

POWER BLOCK DIAGRAM

JUMPER_TABLE ON_SHEET_08



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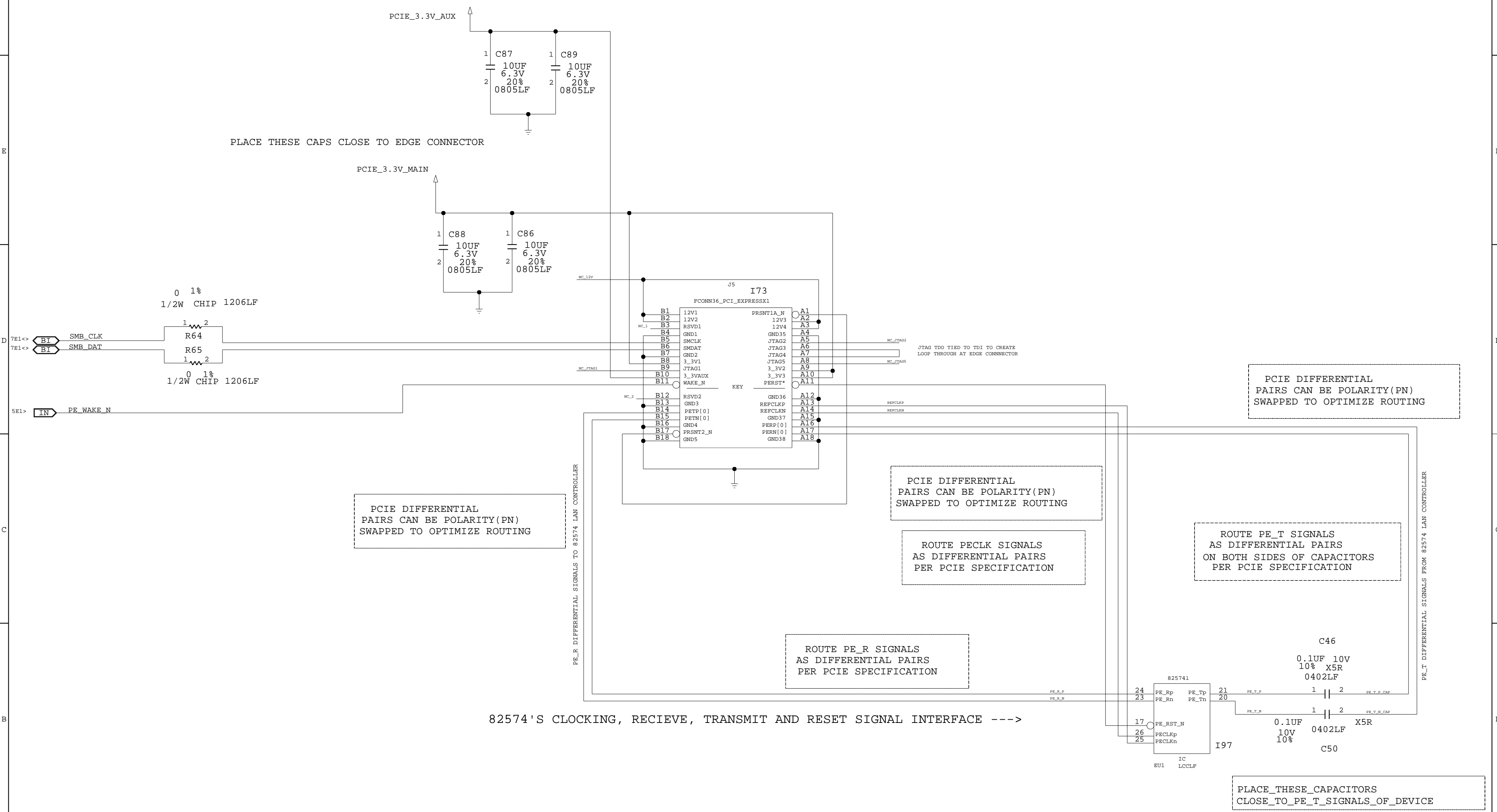
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SHEET 3

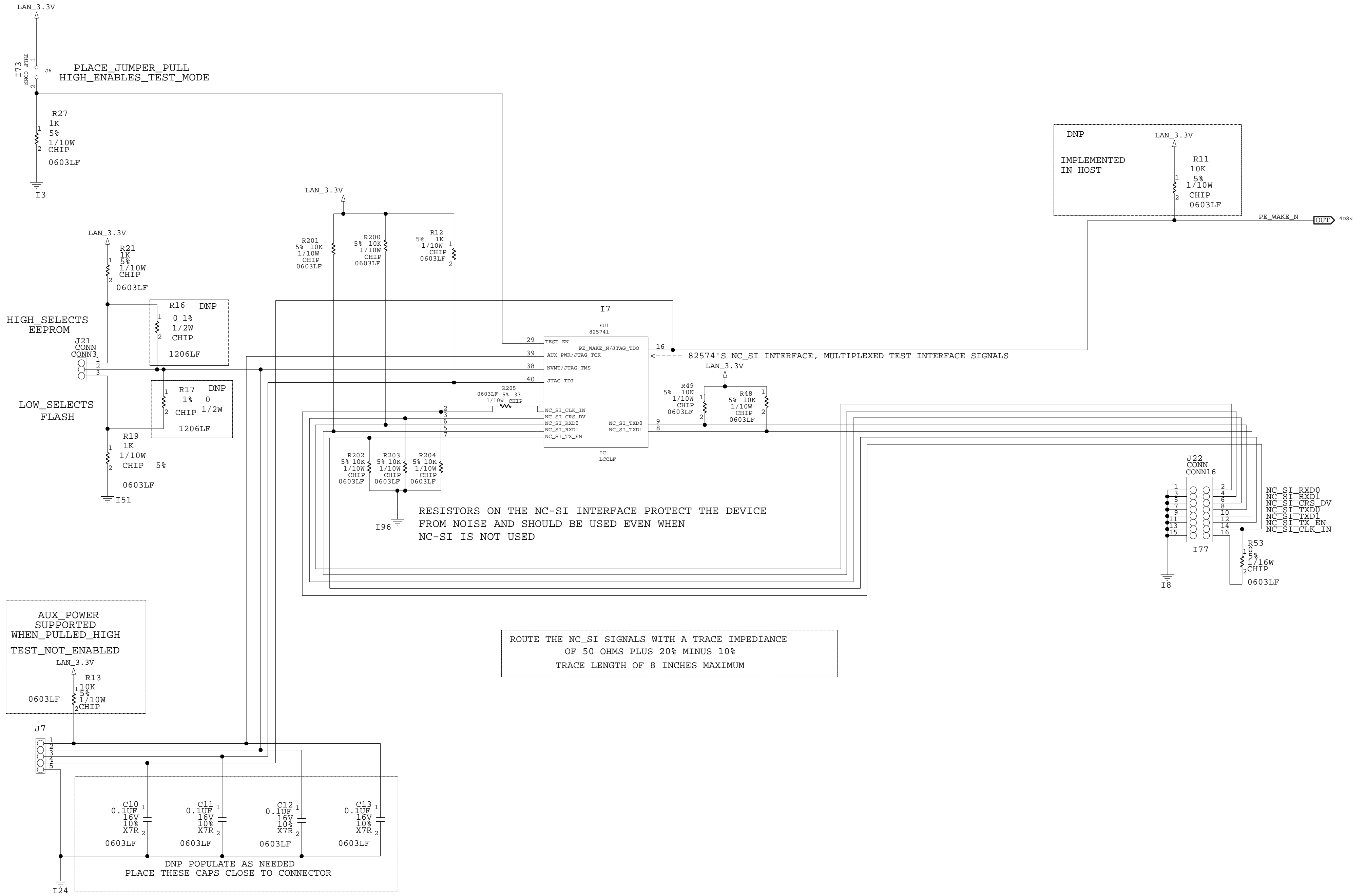
PCIE X1 LANE EDGE CONNECTOR WITH 82574'S CLOCKING, RECV, XMIT AND RESET SIGNAL INTERFACE



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82574'S NC_SI AND MULIPEXED TEST SIGNAL INTERFACE



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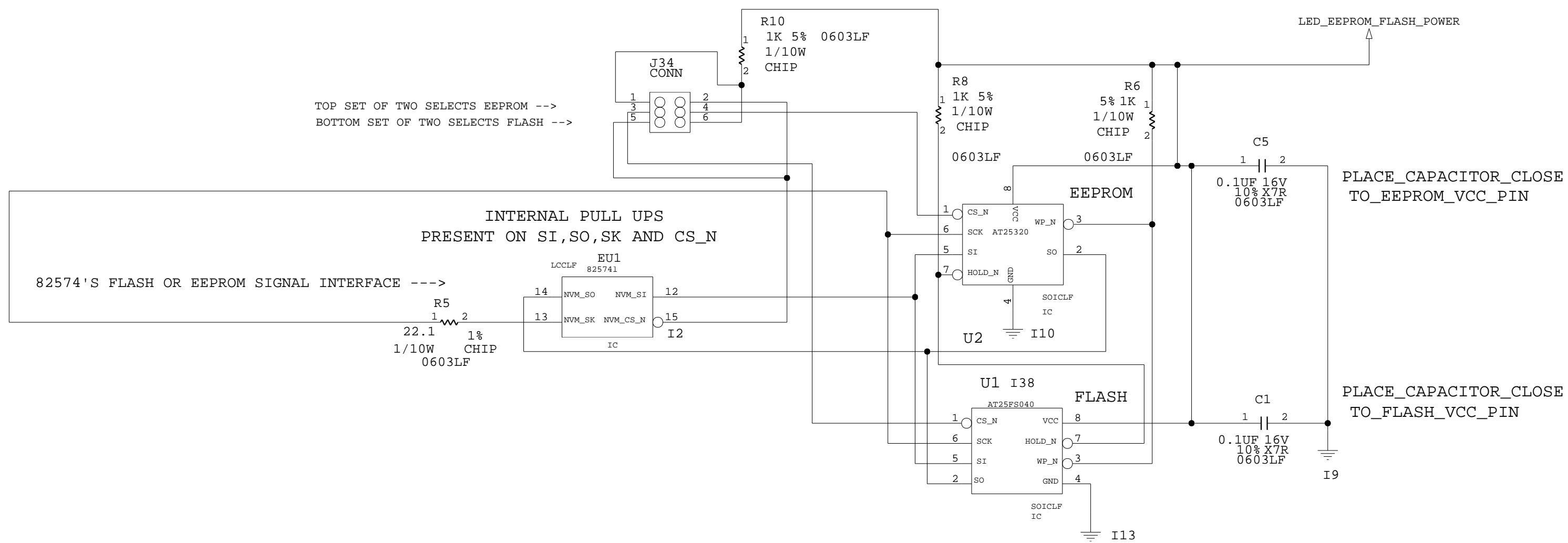
SIZE CODE DOCUMENT NUMBER

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SHEET 5

82574'S FLASH, EEPROM, XTAL AND LED SIGNAL INTERFACE



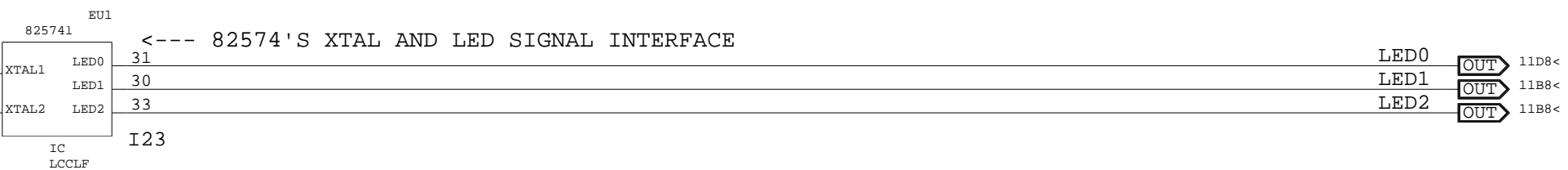
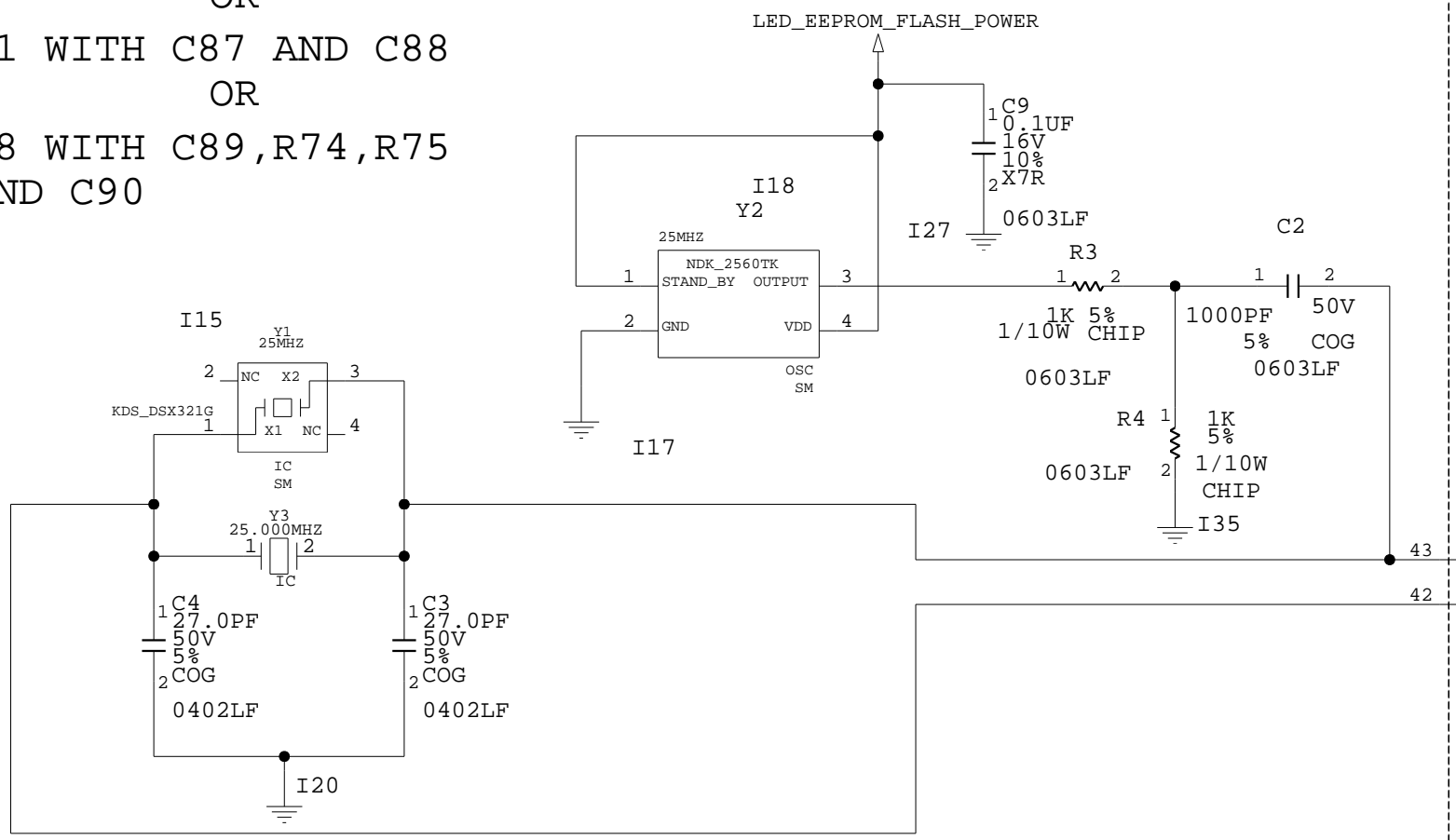
IMPORTANT!!

POPULATE ONLY ONE OF THESE COMPONENT BLOCKS

- Y2 WITH C87 AND C88
- OR
- Y1 WITH C87 AND C88
- OR
- U8 WITH C89, R74, R75 AND C90

PLACE R74, R75 AND C90 CLOSE U8 MINIMIZING STUB LENGTHS WHEN UNPOPULATED

PLACE C89 CLOSE TO U8'S VDD



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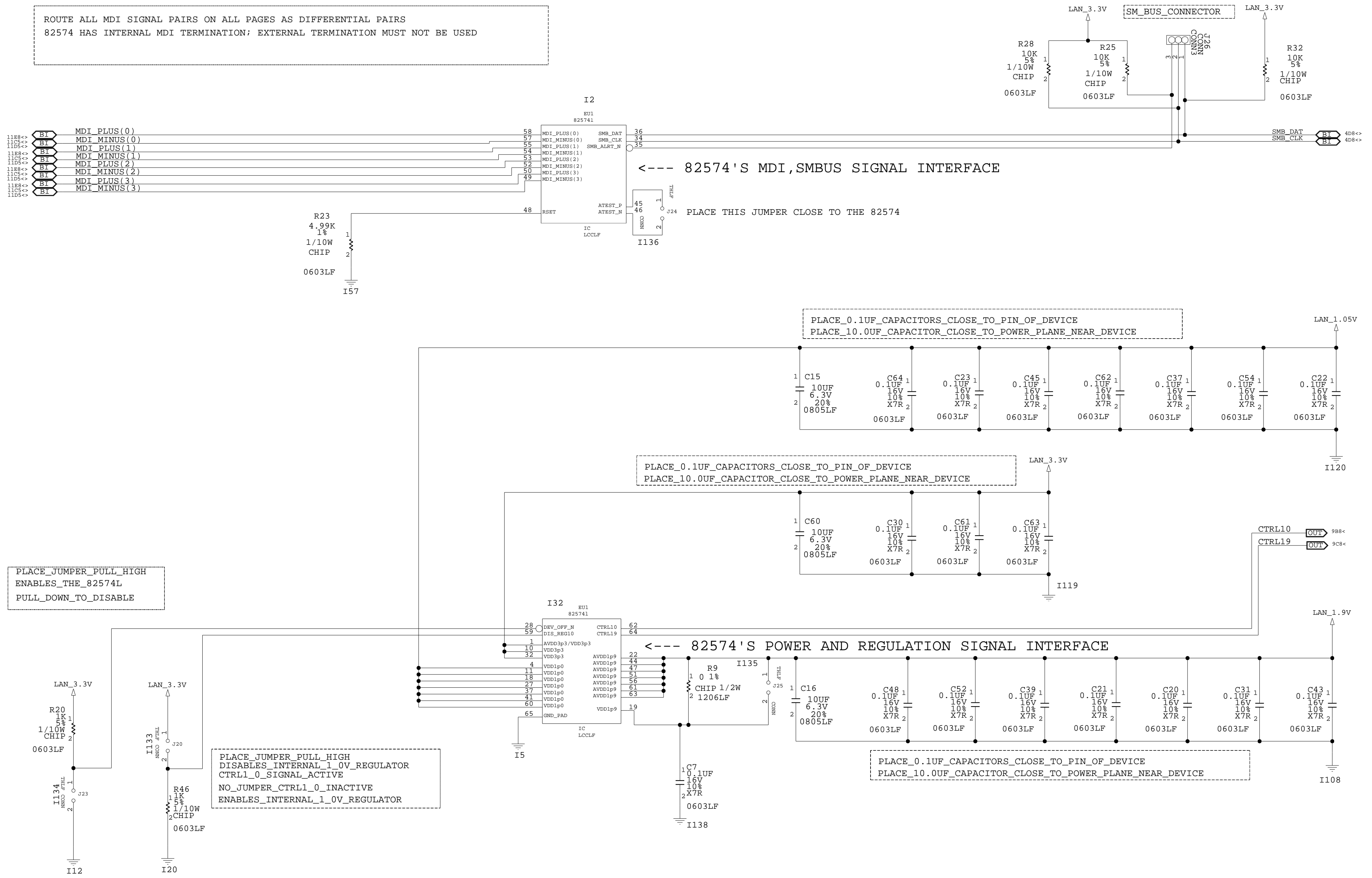
REV 2.1

DATE 08-04-2008

SHEET 6

82574'S MDI, SMBUS, POWER AND REGULATION SIGNAL INTERFACE

ROUTE ALL MDI SIGNAL PAIRS ON ALL PAGES AS DIFFERENTIAL PAIRS
 82574 HAS INTERNAL MDI TERMINATION; EXTERNAL TERMINATION MUST NOT BE USED



JUMPER TABLE

SET_JUMPERS_AS_LISTED_BELOW_TO_GENERATE DESIRED_CONFIGURATION

Jumper Number	Function	To Use Bench supplies	To Use Fully External LDO Supplies	To Use 2 External Power Transistors	To Use 1 External and 1 Internal Power Transistor
J1, 2 pin	PCIE 3.3V MAIN	-	1-2	1-2	1-2
J2, 2 pin	PCIE 3.3V AUX	-	1-2	1-2	1-2
J3, 3 pin	3.3V Charge Pump OR 3.3V Buck/Boost	-	1-2 (Select Charge Pump)	2-3 (Select Buck/Boost)	2-3 (Select Buck/Boost)
J4, 3 pin	LED EEPROM FLASH POWER	1-2 (Select LAN 3.3V)	2-3 (Select 3 3V OR)	2-3 (Select 3 3V OR)	2-3 (Select 3 3V OR)
J5	PCIe Connector	-	-	-	-
J6, 2 pin	TEST EN	-	-	-	-
J7, 5 pin	JTAG	-	-	-	-
J8, 3 pin	CHARGE PUMP ENABLE	2-3 (Select GND)	1-2 (Select HIGH)	2-3 (Select GND)	2-3 (Select GND)
J9, 2 pin	3.3V CHARGE PUMP OUT	-	1-2	-	-
J10, 2 pin	1.9V LDO OUT	-	1-2	-	-
J11, 2 pin	1.05V LDO OUT	-	1-2	-	-
J12, 3 pin	BUCK/BOOST ENABLE	2-3 (Select GND)	2-3 (Select GND)	1-2 (Select HIGH)	1-2 (Select HIGH)
J13, 2 pin	BUCK/BOOST OUT	-	-	1-2	1-2
J14, 2 pin	1.05V PNP OUT	-	-	1-2	-
J15, 2 pin	1.05V PNP IN	-	-	1-2	-
J16, 2 pin	1.9V PNP OUT	-	-	1-2	1-2
J17, 2 pin	1.9V PNP IN	-	-	1-2	1-2
J18, 2 pin	CTRL10	-	-	1-2	-
J19, 2 pin	CTRL19	-	-	1-2	1-2
J20, 2 pin	DIS_REG10	1-2	1-2	1-2	-
J21, 3 pin	NVMT	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH
J22, 16 pin	NC_SI	-	-	-	-
J23, 2 pin	DEV_OFF_N	-	-	-	-
J24, 2 pin	ATEST	-	-	-	-
J25, 2 pin	VDD1p9	-	-	-	-
J26, 3 pin	SMBUS	-	-	-	-
J27, 4 pin	3.3V Bench Feed	3.3V Bench Feed	-	-	-
J28, 4 pin	1.9V Bench Feed	1.9V Bench Feed	-	-	-
J29, 4 pin	1.05V Bench Feed	1.05V Bench Feed	-	-	-
J30, 3 pin	Center Tap Feed	-	-	-	-
J34, 6 pin	NVM Chip Select	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH

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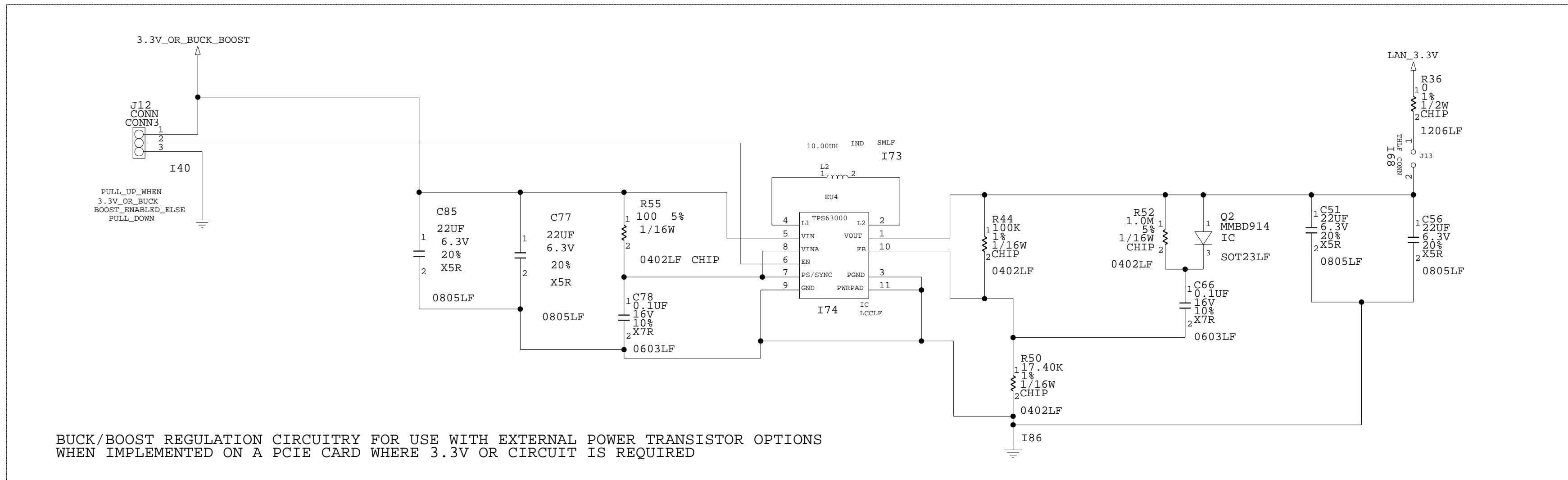
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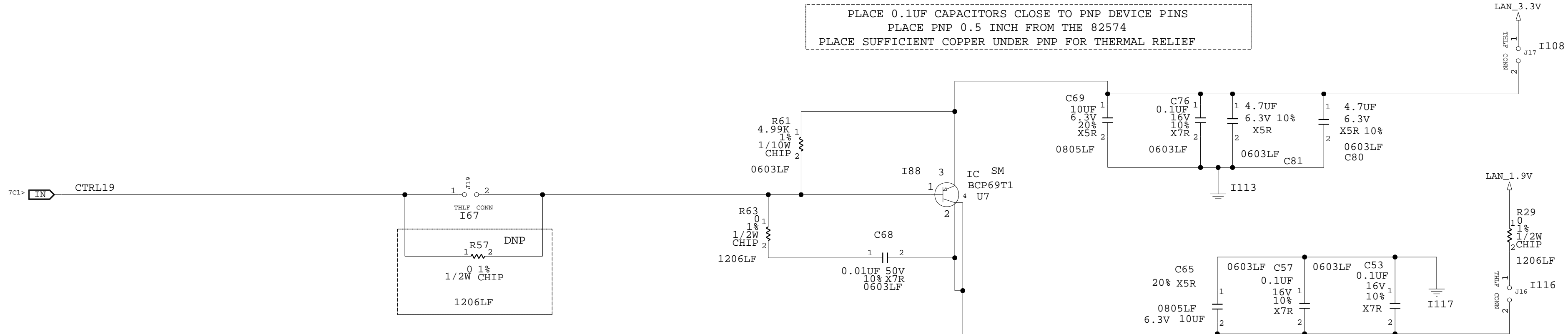
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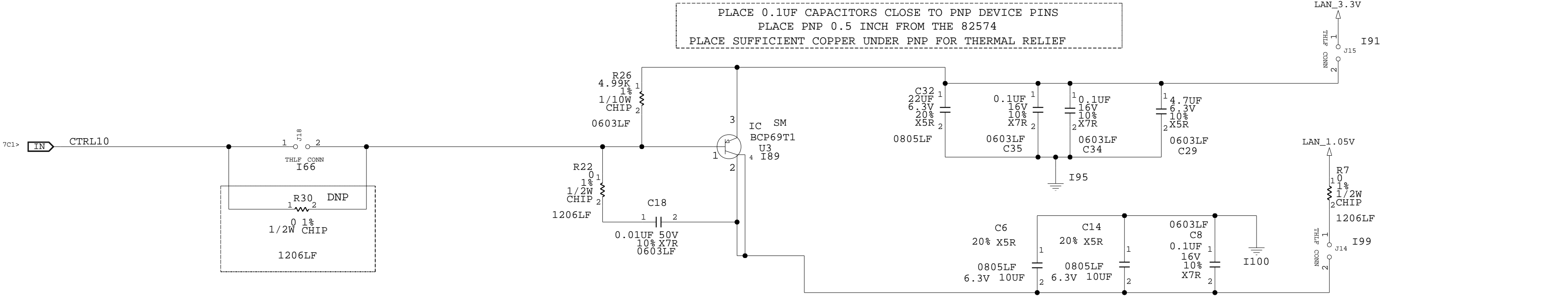
82574'S 2 EXTERNAL OR 1 EXTERNAL POWER TRANSISTOR OPTIONS



PLACE 0.1UF CAPACITORS CLOSE TO PNP DEVICE PINS
 PLACE PNP 0.5 INCH FROM THE 82574
 PLACE SUFFICIENT COPPER UNDER PNP FOR THERMAL RELIEF



PLACE 0.1UF CAPACITORS CLOSE TO PNP DEVICE PINS
 PLACE PNP 0.5 INCH FROM THE 82574
 PLACE SUFFICIENT COPPER UNDER PNP FOR THERMAL RELIEF



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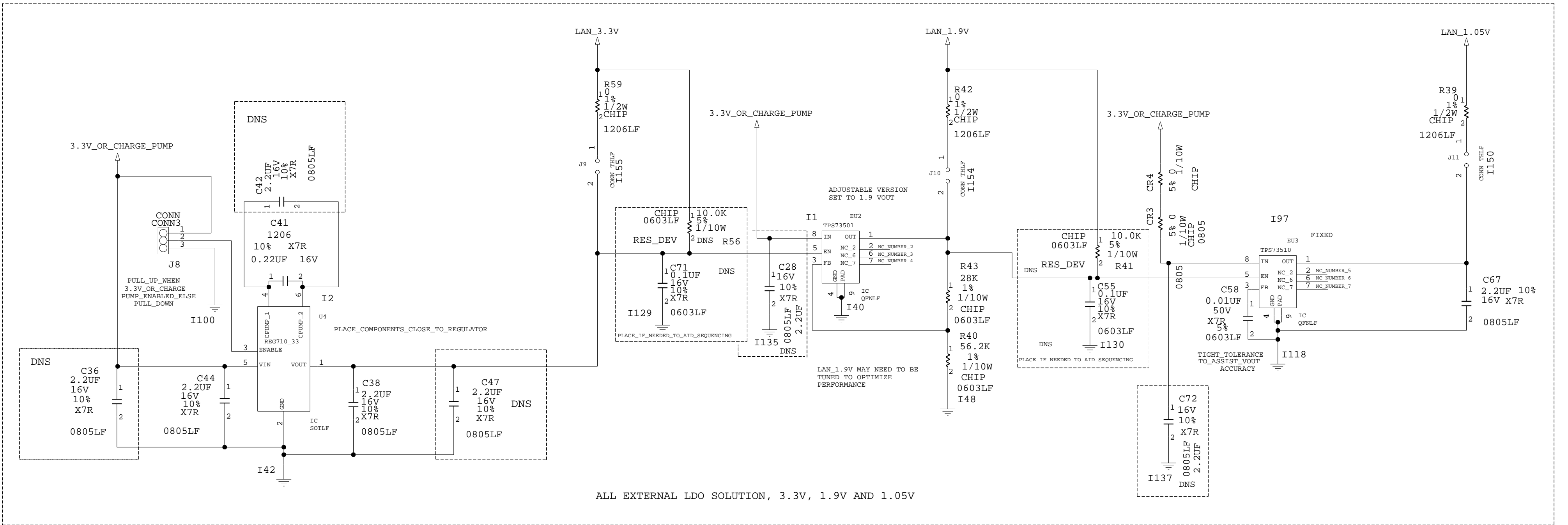
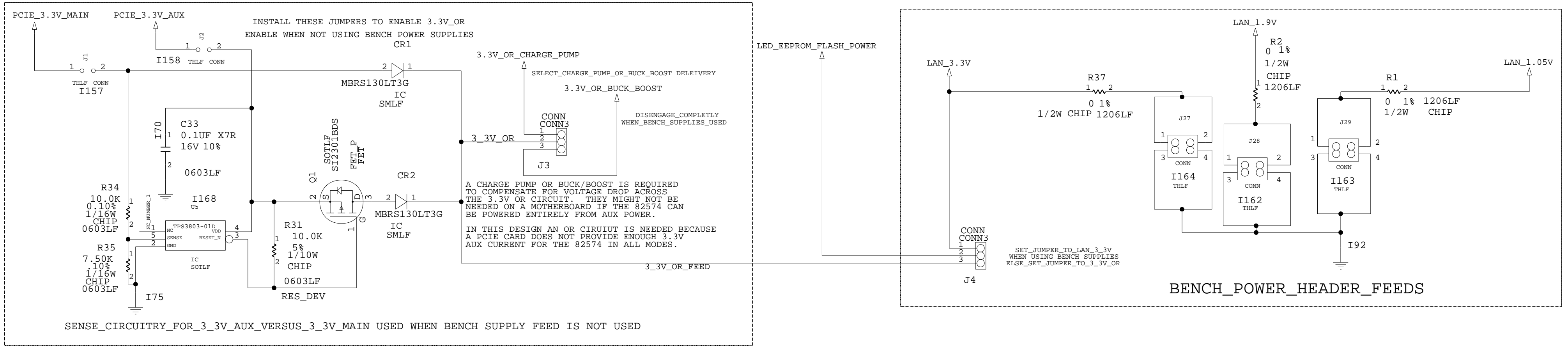
SIZE CODE DOCUMENT NUMBER

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SHEET 9

82574'S BENCH OR ALL EXTERNAL LDO POWER SUPPLY OPTIONS



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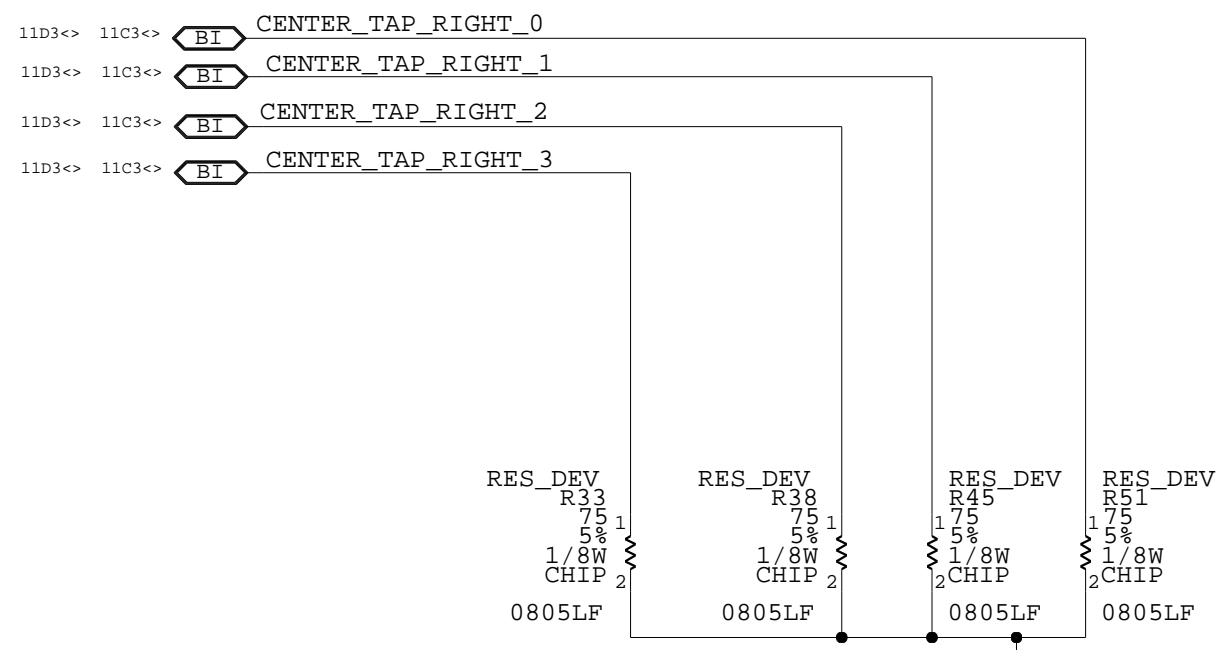
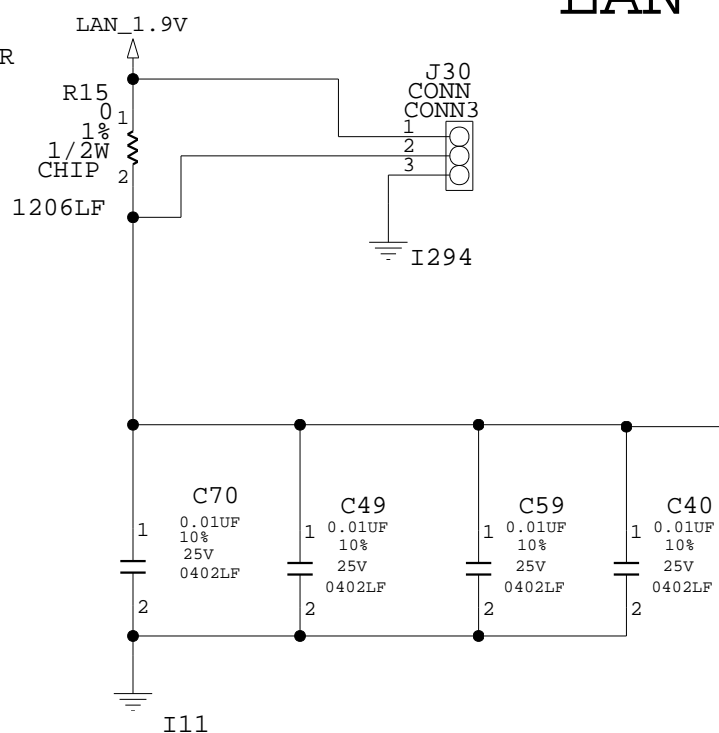
DATE 08-04-2008

SHEET 10

LAN PORT W/MAGNETIC OPTION

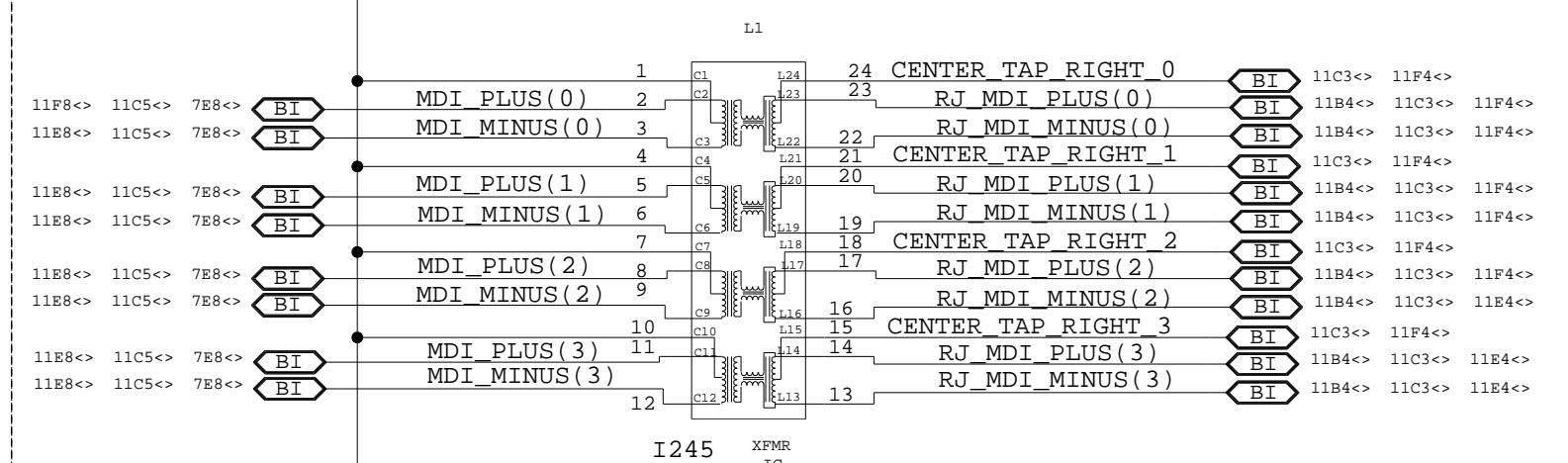
IF MDI TRACES ARE LONGER THAN 4" OR A LAN SWITCH IS USED, AN ADDITIONAL POWER SUPPLY TO BOOST THE CENTER TAP VOLTAGE MAY BE REQUIRED

CENTER TAP POWER

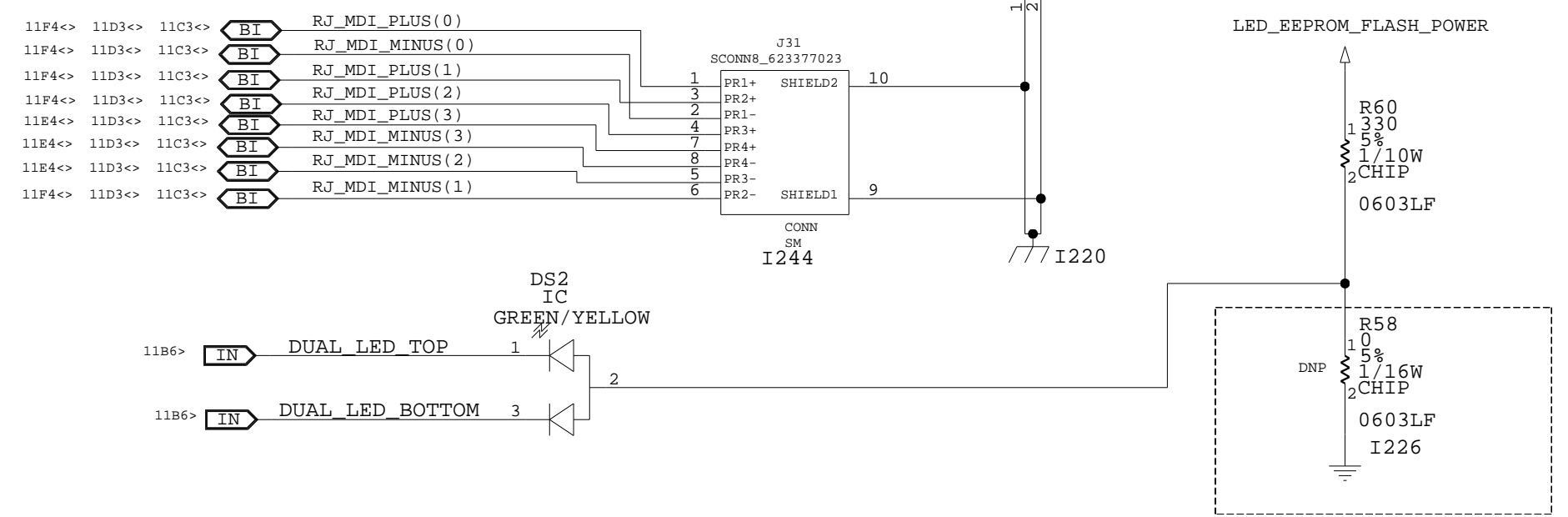
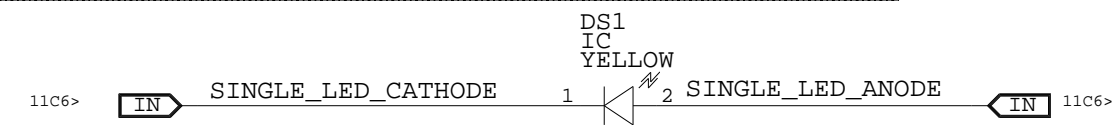
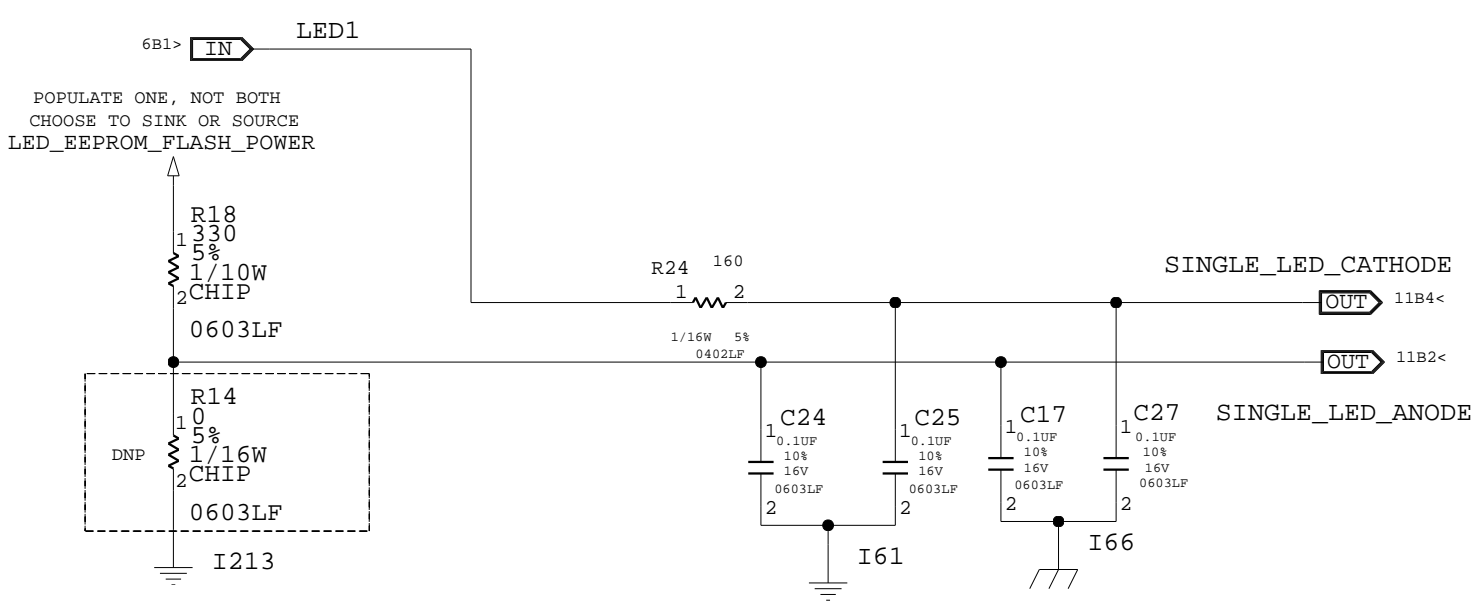
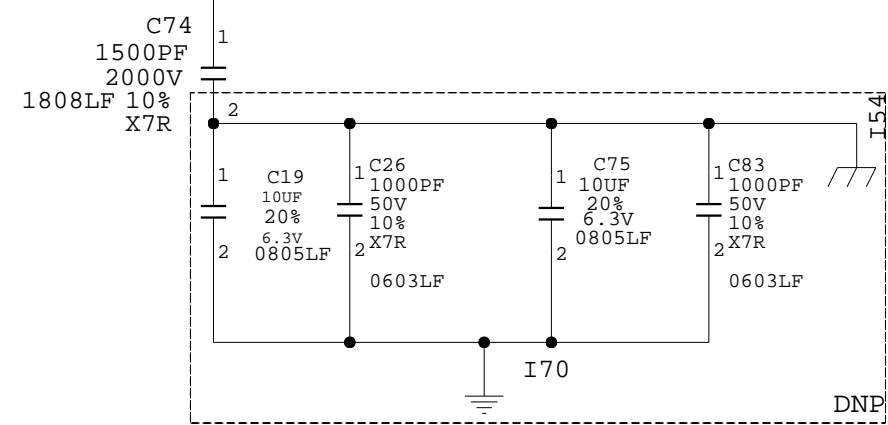
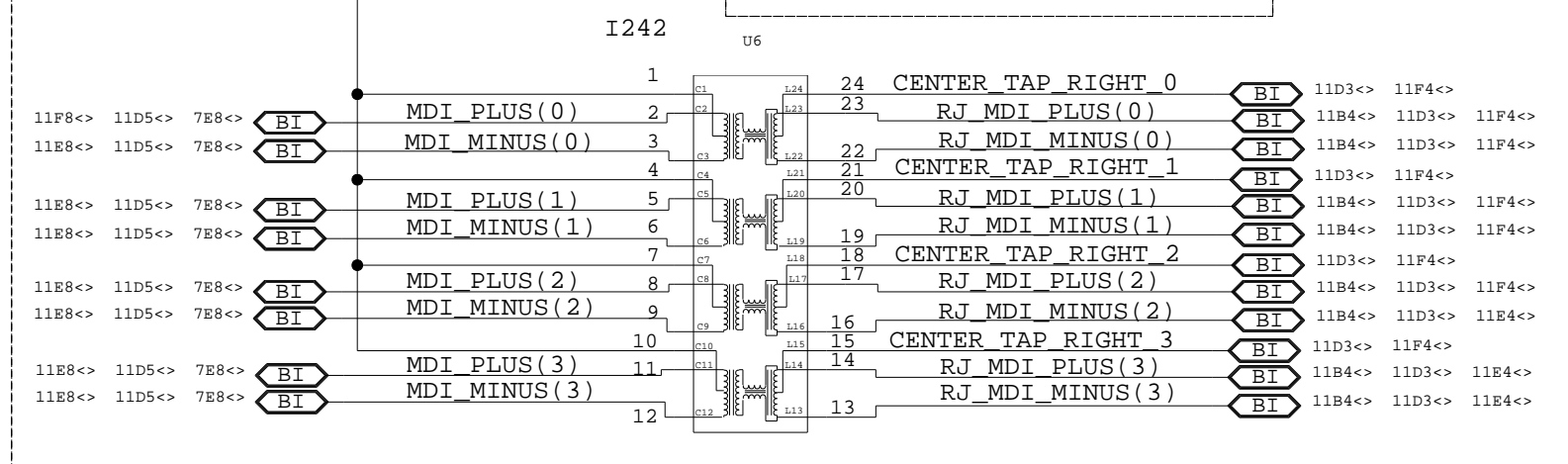


TWO OPTIONS FOR MAGNETIC MODULES ON TOP OF EACH OTHER

STANDARD PROFILE MAGNETIC OPTION



LOW PROFILE MAGNETIC OPTION



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