Interlaken IP datasheet

Key words：Interlaken, MAC, PCS, SERDES

Abstract：Interlaken MAC/PCS implementation per Interlaken protocol v1.2

Table of Contents

List of Tables

List of Figures

List of abbreviations

Abbreviations	Full spelling	Explanation

List of reference

1. Interlaken_Protocol_Definition_v1.2.pdf

1. Introduction

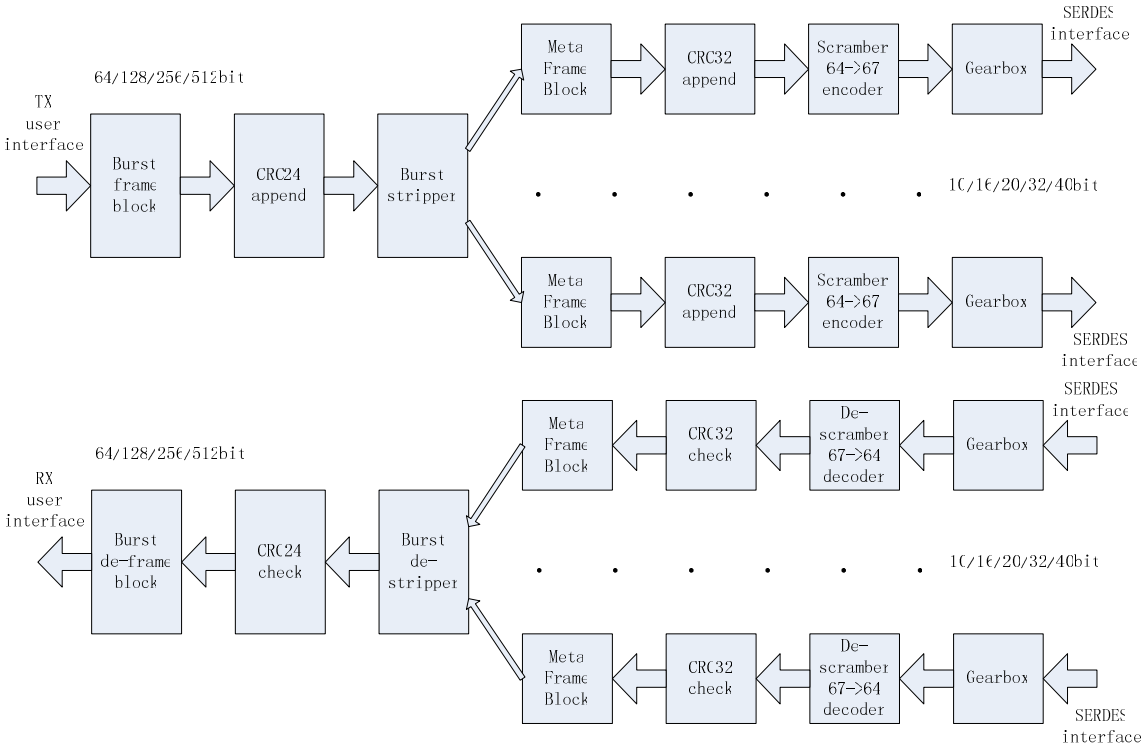
This datasheet describes Interlaken MAC/PCS implementation per Interlaken protocol v1.2.

2. Specification

1. Compliant with the Interlaken Protocol Definition, Rev 1.2.
2. Support for up to 10 Gbps serial data rate. SERDES interface width 10/16/20/32/40 option.
3. Configurable internal data bus width of 64, 128, 256 or 512 bits.
4. In-Band flow control and out of band flow control option, up to 256 channels.
5. Data striping and de-striping across 1 to 24 lanes.
6. Programmable BurstMax, BurstMin, BurstShort and MetaFrameSize parameters.
7. 64/67 encoding and decoding.
8. Automatic word and lane alignment.
9. Self-synchronizing data scrambler.
10. CRC24 generation and checking for burst data integrity.
11. CRC32 generation and checking for lane data integrity.
12. Error checking and recovery.
13. Technology independent. Can be targeted to different FPGAs and ASICs.

3. Architecture

Figure 1 Interlaken IP Architecture



4. Port List

Table 1 Parameters

Name	Destription
WORD_NUMBER	Data bus width multiplies 64. 1 is 64bits, 2 is 128bits, 4 is 256bits, 8 is 512bits.
LANE_NUMBER	SERDES lane number.
SERDES_WIDTH	SERDES interface width; options are 10/16/20/32/40.

Table 2 Post list

Name	Destription
input rst_mac_tx_n	Transmit MAC asynchronous reset, active low.
input rst_mac_rx_n	Receiver MAC asynchronous reset, active low.
input [LANE_NUMBER-1:0] rst_pcs_tx_n	Transmit PCS asynchronous reset per lane, active low.
input [LANE_NUMBER-1:0]	Receiver PCS asynchronous reset per lane, active low.

rst_pcs_rx_n	
input clk_mac_tx	Transmit MAC clock. If the data bytes of each cycle is valid, then clk_mac = (LANE_NUMBER * LANE_RATE) / (WORD_NUMBER * 64).
input clk_mac_rx	Receiver MAC clock. If the data bytes of each cycle is valid, then clk_mac = (LANE_NUMBER * LANE_RATE) / (WORD_NUMBER * 64).
input [LANE_NUMBER-1:0] clk_pcs_tx	Transmit PCS clock. clk_pcs = LANE_RATE / SERDES_WIDTH.
input [LANE_NUMBER-1:0] clk_pcs_rx	Receiver PCS clock. clk_pcs = LANE_RATE / SERDES_WIDTH.
input tx_disable_burstmin	Transmit BurstMin selection. 1 diable, 0 enable. Enable this feature can minimize extra IDLE control words and improve bandwidth utilization.
input tx_disable_pad	Transmit EOP IDLE control word pad selection. 1 disable, 0 enable. When enabled and at EOP cycle not all words are valid, then automatically pad IDLE control word. Enable this feature can lower the MAC clock frequency and bandwidth utilization.
input [1:0] tx_burstmax	Transmit BurstMax. Value is (tx_burstmax + 1)*64bytes. The value should be configured as a multiple of WORD_NUMBER*8bytes.
input [1:0] tx_burstmin	Transmit BurstMin. Value is (tx_burstmin + 1)*32bytes. The value should be configured as a multiple of WORD_NUMBER*8bytes.
input [2:0] tx_burstshort	Transmit BurstShort. Value is (tx_burstshort + 1)*32bytes. The value should be configured as a multiple of WORD_NUMBER*8bytes.
input [7:0] tx_mbits	Transmit multi-use control bits. Only transmits the configured value.
input tx_disable_crc24	Transmit CRC24 selection. 1 disable CRC24 calculation, 0 enable CRC24 calculation. Disable this feature can save resources and easy timing closure.
input tx_fc_ib_en	Transmit in band flow control enable. 1 enable in band flow control insertion. 0 disable, all in band flow

	control bits are zero.
input [3:0] tx_fc_pages	Transmit in band flow control pages, each page contains 16 calendar bits. 0 is 1 pages containing 0 – 15 channel calendar bits. 1 is 2 pages containing 0 – 31 channel calendar bits. 2 is 3 pages containing 0 – 47 channel calendar bits. …
input [255:0] tx_fc	Transmit flow control status. Bit 0 is for channel 0, bit 1 for is channel 1, …bit 255 is for channel 255.
input tx_vld_in	Transmit data valid, active high.
input tx_sop_in	Transmit start of packet, active high.
input tx_eop_in	Transmit end of packet, active high.
input [MOD_WITDH-1:0] tx_mod_in	Transmit mod, indicate how many bytes are valid at EOP cycle. Other valid cycles should be 0. 0: WORD_NUMBER * 8 bytes valid. 1: 1 bytes valid. 2: 2 bytes valid. …
input [7:0] tx_chan_in	Transmit channel number.
input [WORD_NUMBER*64-1:0] tx_din	Transmit data.
output tx_prog_full_bf	Buffer programmable full, active high. When high, user should stop sending data.
output tx_full_bf	Buffer full, active high. When high, indicates user sends data too fast.
output [LANE_NUMBER-1:0] tx_full_lf	Buffer full, active high. Should never happen when normal operation. When high, user should assert tx_reset_lf to reset the buffer.
output [LANE_NUMBER-1:0] tx_empty_lf	Buffer empty, active high. Should never happen when normal operation. When high, user should assert tx_reset_lf to reset the buffer.

input tx_reset_lf	Buffer reset, active high. When transmit un-normal behavior happens, reset buffer.
input [15:0] tx_metaframelength	Transmit Metaframe length. Should be 2^n, minimum is 32.
input [LANE_NUMBER-1:0] tx_status_lane	Transmit lane status per lane.
input [LANE_NUMBER-1:0] tx_status_intf	Transmit interface status per lane.
input [LANE_NUMBER-1:0] tx_disable_crc32	Transmit CRC32 selection per lane. 1 disable CRC32 calculation, 0 enable CRC32 calculation. Disable CRC32 can save resource and easy timing closure.
input [LANE_NUMBER-1:0] tx_disable_scrambler	Transmit scrambler selection per lane. 1 disable scrambler, 0 enable scrambler.
input [LANE_NUMBER-1:0] tx_disable_disparity	Transmit disparity selection per lane. 1 disable disparity, 0 enable disparity.
output [LANE_NUMBER*SERDES_WIDTH-1:0] tx_dout	Transmit data to SERDES per lane.
input [LANE_NUMBER-1:0] rx_disable_disparity	Receiver disparity selection per lane. 1 disable disparity, 0 enable disparity.
input [15:0] rx_metaframelength	Receiver Metaframe length. Should be 2^n, minimum is 32.
input [LANE_NUMBER-1:0] rx_disable_scrambler	Receiver scrambler selection per lane. 1 disable scrambler, 0 enable scrambler.
input [LANE_NUMBER-1:0] rx_disable_crc32	Receiver CRC32 selection per lane. 1 disable CRC32 calculation, 0 enable CRC32 calculation. Disable CRC32 can save resource and easy timing closure.
input	Receiver data input from SERDES.

[LANE_NUMBER*SERDES_WIDTH-1:0] rx_din	
output [LANE_NUMBER-1:0] rx_word_locked	Receiver word locked per lane, active high, indicates word boundary is found correctly.
output [LANE_NUMBER-1:0] rx_framing_error	Receiver framing bits error per lane, active high, indicates [66:65] is not valid.
output [LANE_NUMBER-1:0] rx_sync_locked	Receiver Metaframe synchronous locked per lane, active high.
output [LANE_NUMBER-1:0] rx_scra_mismatch	Receiver scrambler word mismatch per lane, active high.
output [LANE_NUMBER-1:0] rx_crc32_error	Receiver CRC32 checksum error per lane, active high.
output [LANE_NUMBER-1:0] rx_status_lane	Receiver lane status per lane.
output [LANE_NUMBER-1:0] rx_status_intf	Receiver interface status per lane.
input [1:0] rx_burstmax	Receiver BurstMax. Value is (rx_burstmax + 1)*64bytes. The value should be configured as a multiple of WORD_NUMBER*8bytes.
input [2:0] rx_burstshort	Receiver BurstShort. Value is (rx_burstshort + 1)*32bytes. The value should be configured as a multiple of WORD_NUMBER*8bytes.
input rx_disable_crc24	Receiver CRC24 selection. 1 is disable CRC24 calculation, 0 is enable CRC24 calculation. Disable this feature can save some resources and easy timing closure.
output [LANE_NUMBER-1:0] rx_full_lf	Receiver buffer full, active high. Should never happen when normal operation. When high, user should assert rx_reset_lf to reset the buffer.
output [LANE_NUMBER-1:0]	Receiver buffer empty, active high. Should never happen when normal operation. When high, user

rx_empty_lf	should assert rx_reset_lf to reset the buffer.
input rx_reset_lf	Buffer reset, active high. When receiver un-normal behavior happens, reset buffer.
output rx_lane_aligned	Receiver lane aligned, active high.
output rx_fully_locked	Receiver all lanes sync locked and lane aligned, active high.
output [WORD_NUMBER-1:0] rx_crc24_error	Receiver CRC24 checksum error, active high. Each bit indicates one error.
output [7:0] rx_mbits	Receiver multi-use control bits extracted.
output rx_full_bs	Receiver buffer full, active high. Should never happen when normal operation. When high, indicates receiver MAC clock is too slow to process the data, user should increase the rx MAC clock to avoid this situation.
output rx_burst_error	Receiver burst error, active high. When high, indicates burst sequence is un-normal.
output rx_burstmax_error	Receiver data burst length larger than rx_burstmax, active high.
output rx_burstshort_error	Receiver burst length less than rx_burstshort, active high.
output rx_vld_out	Receiver data valid, active high.
output rx_sop_out	Receiver start of packet, active high.
output rx_eop_out	Receiver end of packet, active high.
output rx_err_out	Receiver error, active high.
output [MOD_WITDH-1:0] rx_mod_out	Receiver mod, indicate how many bytes are valid at EOP cycle. Other valid cycles should be 0. 0: WORD_NUMBER * 8 bytes valid. 1: 1 bytes valid. 2: 2 bytes valid. …

output [7:0] rx_chan_out	Receiver channel number.
output [WORD_NUMBER*64-1:0] rx_dout	Receiver data.
output [255:0] rx_fc_ib	Receiver in band flow control status. Bit 0 is for channel 0, bit 1 for is channel 1, …bit 255 is for channel 255.
output [255:0] rx_fc_ob	Receiver out of band flow control status. Bit 0 is for channel 0, bit 1 for is channel 1, …bit 255 is for channel 255.
input rst_tx_fc_n	Transmit out of band asynchronous reset, active low.
input clk2x_tx_fc	Transmit out of band clock, the frequency is twice of the output FC clock.
input [7:0] tx_fc_cal_bits	Transmit out of band flow control calendar bits. 0 is 1 channel calendar bit 1 is 2 channel calendar bits 2 is 3 channel calendar bits … 255 is 256 channel calendar bits
output tx_fc_data	Transmit out of band data.
output fc_tx_sync	Transmit out of band sync.
input rst_rx_fc_n	Receiver out of band asynchronous reset, active low.
input clk2x_rx_fc	Receiver out of band clock, the frequency is twice of the input FC clock.
input rx_fc_data	Receiver out of band data.
input rx_fc_sync	Receiver out of band sync.
output rx_crc4_error	Receiver out of band CRC4 checksum error, active high.

Note:

1. Burst parameters should follow the rule: Burstmax > Burstmin >= burstshort
2. Out of Band required clock should be generated using PLL or other methods not mentioned in this document.
3. Out of band status messaging is not supported.

5. Performance and Resource Utilization

The Interlaken IP is technology independent and can be targeted to different FPGAs and ASICs.

An example is shown as the below.

Table 3 Performance and Resource Example

Altera Stratix IV	Combinational ALUTs	Logic Registers	Memory (bits)	SERDES width(bits)	MAC f_{MAX} (MHz)
64bits 4lane@3.125Gbps	9K	8K	25K	16	200
128bits 8lane@3.125Gbps	17K	16K	80K	20	200
256bits 8lane@6.25Gbps	21K	20K	200K	32	280
512bits 24lane@6.25Gbps	65K	55K	300K	40	312.5
Xilinx Virtex 5	LUTs	FFs	Block RAMs	SERDES width(bits)	MAC f_{MAX} (MHz)

6. Contact information

Please contact hpiclab@sina.com

Revision record

Date	Revision version	Description	Author
2011/8/5	1.00	Initial	