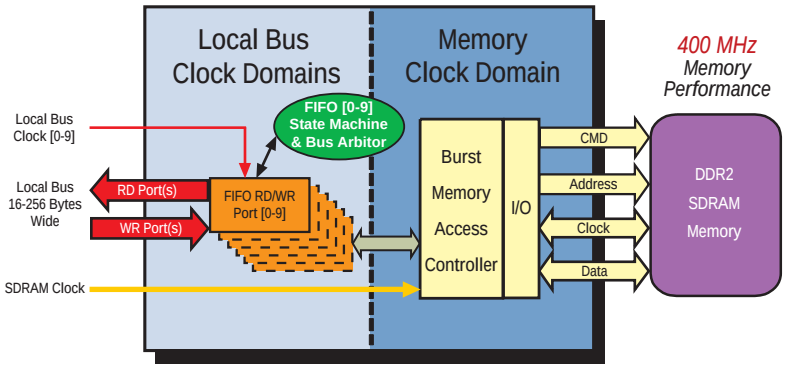
microtronix

Ultra Performance

HyperDrive Multi-port DDR2 Memory Controller IP Core

Product DATA SHEET



Features

- 400 MHz DDR2 Memory Performance
- Up to 10 local bus RD or WR ports
- Full or half-rate local bus
- Configurable FIFO depth: 16 to 2048 bytes
- Memory data width: up to 128 bits
- Local bus width from 16 to 256-bits
- Intelligent SDRAM burst caching minimizes wait-states
- Layout independent DDR Round-Trip capture scheme
- Multiple time domain clocking
- Configuration GUI streamlines design process
- Supports Cyclone I, II, III*, Stratix I, II, III* and GX

* Pending Hardware Verification

DESCRIPTION

The Microtronix *HyperDrive* Multi-port DDR2 Memory Controller IP Core levitates FPGA based hardware designs to a whole new level of performance. Built around a new DDR2 state machine controller, and an interleaved FIFO architecture which allows the local bus data path operates either at full-rate, (twice the DDR2 data bus width) or at half-rate with a bus width of four times the DDR2 data bus interface. In a Cyclone device, the local bus operates at half-rate only. A proprietary Microtronix data capture technique enables 400 MHz DDR2 performance in a Stratix II device.

The memory controller supports burst memory RD/WR access cycles and handles all memory tasks, including initialization and refresh cycles. The core integrates: a burst DDR2 memory controller core, a port arbitrator and an intelligent look-ahead FIFO controller into one easy-to-use core.

The core supports up to ten independently clocked streaming-data sources operating from one shared high bandwidth memory system. With a few clicks of a mouse and within minutes, using the intuitive Microtronix GUI interface, designers can create a multi-port system, a design task which would normally take several man-months of effort!

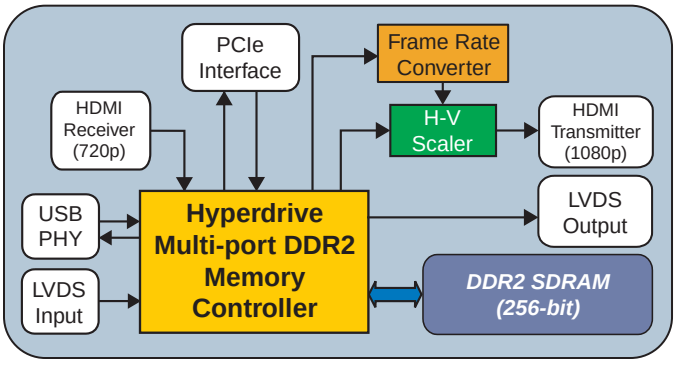
Target Applications

The HyperDrive DDR2 core is targeted at applications requiring ultra high-performance memory subsystems including; HDTV consumer electronics, video conversion / enhancement equipment, military vision systems, medical imaging, data networking, Ethernet, PCIe, data recorders.

Advanced Performance Architecture

- 267 / 400 MHz Cyclone II / Stratix II memory performance
- Source synchronous clocking simplifies timing closure
- Configurable FIFO optimizes streaming video applications
- Configurable memory and local bus data width
- SDRAM DQ/DQS groups not restricted to dedicated DQ pins
- Local bus operates at full / Half-rate of DDR2 bus
- Round-robin bus arbitration

9-Port Example: Medical Equipment HDTV Display



Technical Description

The Microtronix **HyperDrive DDR2 Memory Controller IP Core** builds upon the proprietary source-synchronous data capture technology developed in our first generation SDRAM controllers. The core decouples the DDR2 state machine controller from the high-speed data path, decreasing timing constraints and improves timing closure boosting performance by over 30%. The fmax performance constraint of the internal memory blocks is resolved by interleaving the local bus FIFOs enabling them to operate at half data rate of the memory interface. The Cyclone II core implementation operates in this half-rate mode only.

A proprietary source-synchronous design technique is used for capturing the high-speed DDR2 data from the memory devices independent of the round-trip delay. The scheme makes IP core timings independent of the PCB layout trace length signal delay and any associated impedance variance of the board fabrication process. The use of source-synchronous data capture clocking also frees the IP core design task from the PCB design step and reduces the FPGA design compilation to a simple two-step process!

Source-synchronous data capture also boosts memory performance by removing the extra resynchronization clocks required by PLL based designs. This expands the data capture timing margins extending temperature performance and enabling faster timing closure in the design fitting process. An additional side benefit is that the SDRAM data pins are no longer restricted to the use of dedicated DQ pins, increasing design flexibility and available IO pins thus reducing package constraints.

The ports can be configured for either RD or WR access. By using FIFO's to bridge the time domain of the local bus ports to the SDRAM memory clock domain, each port can be independently clocked at their optimal design frequency. Port FIFO buffer depth can also be configured (from 16 to 2048 bytes) to the match characteristics of the streaming data device and provided for extended burst pipelined memory cycles eliminating CAS latency overhead encountered using a short burst access controller. Internally the FIFOs are partitioned into two banks allowing the input and output of each to be filled or emptied simultaneously.

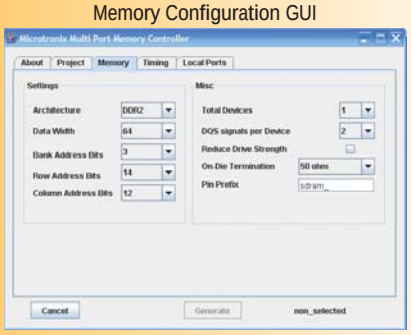
Other Features

- ModelSim / VHDL precompiled simulations library
- On Die Termination (ODT) improves signal integrity
- Includes license and 1 year of updates
- Altera OpenCore Plus evaluation

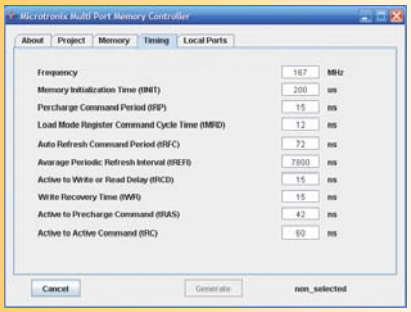
ALTERA®
AMPP℠ Approved
*Pending Approval

Custom IP Cores are available. Contact sales with your requirements.

Memory Configuration GUI



Memory Timing GUI



Port Configuration GUI

ORDERING INFORMATION

PART NUMBER	DESCRIPTION	US UNIT PRICE
6243-01-01	Hyperdrive Multi-port SDRAM Memory Controller IP Core License	Contact Sales

MEMORY PERFORMANCE (MHz)

DEVICE	SPEED GRADE (Commercial)	DDR2
Stratix II / GX	-5, -4, -3	300, 333, 400
Cyclone II / III**	-8, -7, -6	233, 267, 267

**Note: Pending Hardware Verification.

The IP Core license pricing is:

1. Based on a 1-1-1 License model, 1-User, 1-Company, and 1-Year maintenance.
2. Includes 1 hour of Installation Support.

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Microtronix reserves the right to change the IP Core specification without notice.