Title: Color Bars using Altera Video and Image Processing Suite (VIP)
Date: January 2013

FPGA Tools: Quartus II 12.0 Web Edition

Software Tools:
Eclipse IDE for C/C++ Developers
Version: Helios Service Release 1
Build id: 20100917-0705

IP used: Altera VIP Suite (Test Pattern Generator & Clocked Video Output) as stand-alone Blocks (Not inside SOPC or Qsys)

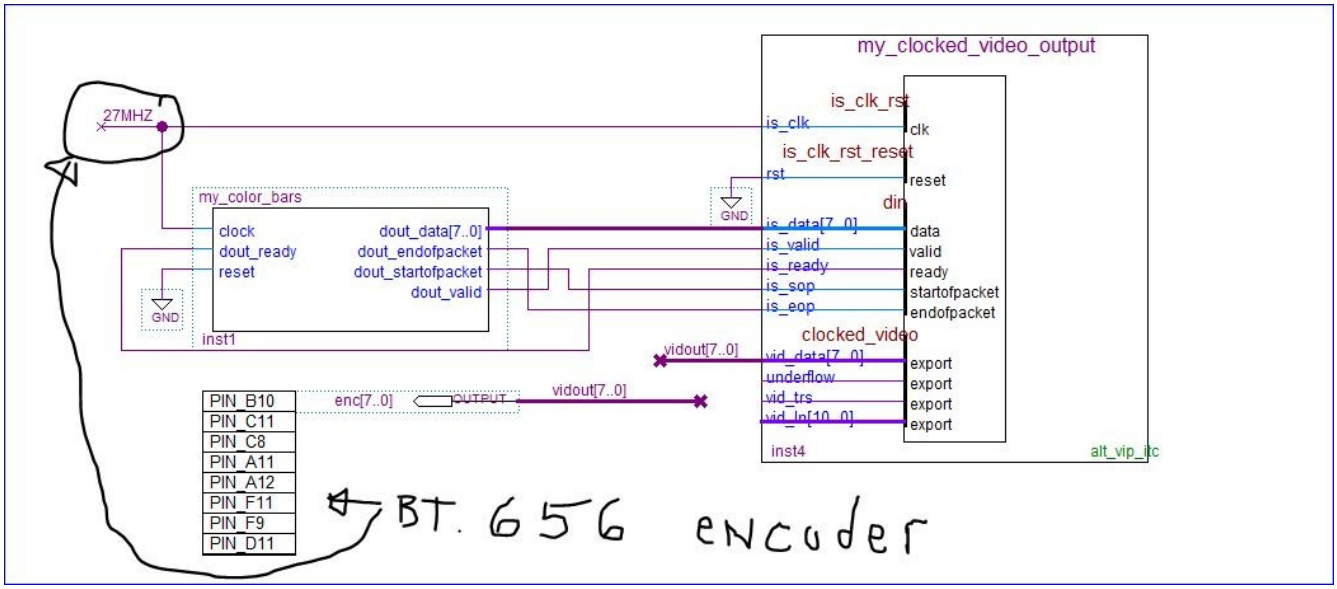
Board: C4 Custom Board with

- Cyclone IV/EP4GX15BF14C8
- Video Encoder: ADV7393BCPZ-ND at I2C address $54
- Nios II processor (for initializing the I2C bus using OpenCores I2C IP)

Step 1: Reset the video encoder with negative reset for 100ms then high 100mS (wait)
Step 2. Initialize video encoder via I2C bus and dump values to verify I2C is working
Step 3: Test output video path with internally generated Color Bars and/or Gray Bars
Step 4: Set video-encoder to process BT656 8 bit data with embedded syncs via I2C

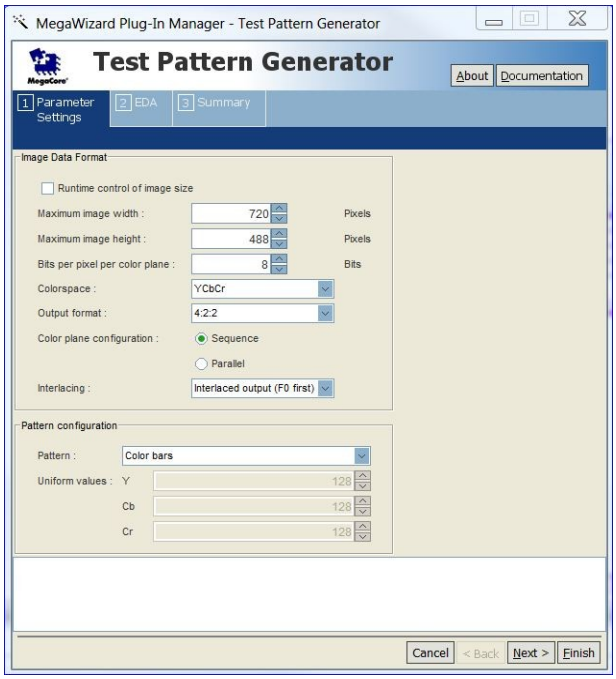
```
Calling: init_video_encoder
  Write $54: $01: 0x0
  Write $54: $07: 0x24
  Write $54: $09: 0x7c
  Dump Video Encoder Registers

  $54 Sub-0= 12
  $54 Sub-1= 0
  $54 Sub-2= 20
  $54 Sub-3= 3
  $54 Sub-4= f0
  $54 Sub-5= 4e
  $54 Sub-6= e
  $54 Sub-7= 24
  $54 Sub-8= 92
  $54 Sub-9= 7c
  $54 Sub-a= 0
  $54 Sub-b= 0
  $54 Sub-c= 0
  $54 Sub-d= 0
  $54 Sub-e= 0
  $54 Sub-f= 0
  $54 Sub-10= 0
  $54 Sub-11= 1b
  $54 Sub-12= ff
  $54 Sub-13= 23
  $54 Sub-14= ff
  $54 Sub-15= 3c
  $54 Sub-16= 5f
  $54 Sub-17= 0
  $54 Sub-18= 0
  $54 Sub-19= 0
```

Step 5: Instantiate two blocks in Quartus II and connect them per image below.
Note: These blocks need a stable 27MHZ clock. The BT656 (8 bit) output must route to OUPUT pins on the FPGA and the 27 MHZ clock must also go to the video-encoder clock input.



Step 6: Set up the Test Pattern Generator

1. Set to 720 pixels wide.
2. Set to 488 Lines. (vertical blanking is trashed if you use a different value here)
3. Set to 8 Bits (if you use 10 bits you must use it everywhere in the design)
4. Set to YcbCr/4:2:2/Interlaced (F0 First)
5. Set to Color Bars

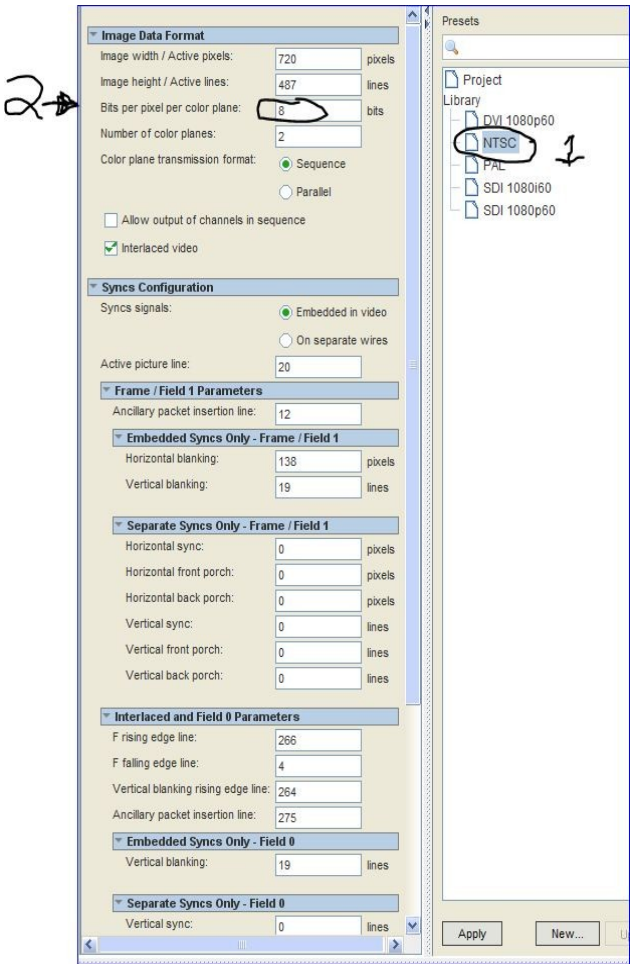


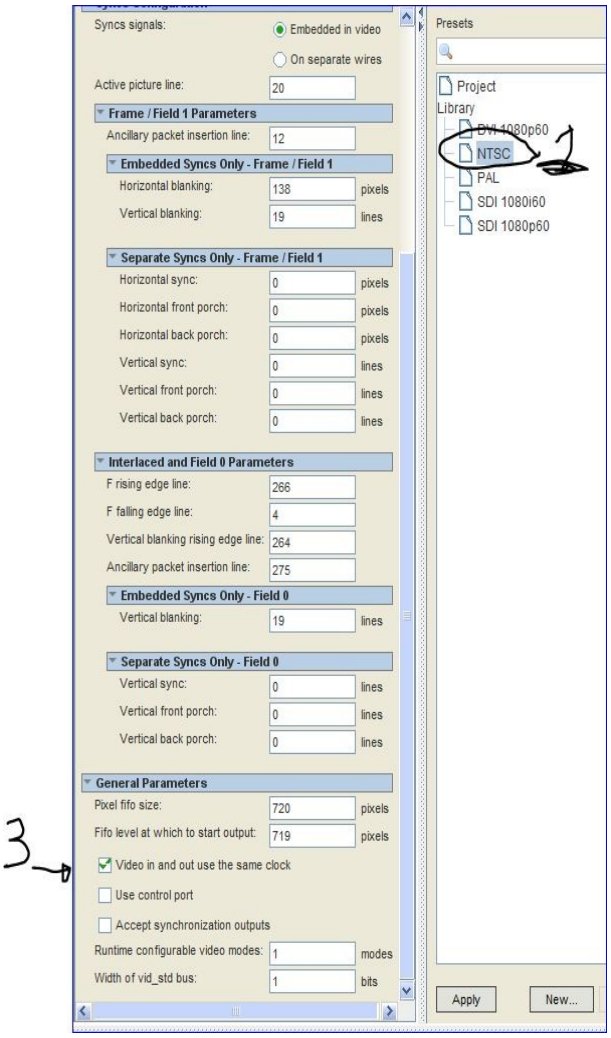
Step 7: Set up the Clocked Video Output

1: Press NTSC on right panel.

2. Edit to use 8 bit bus. (if you use 10 bits you must use it everywhere)

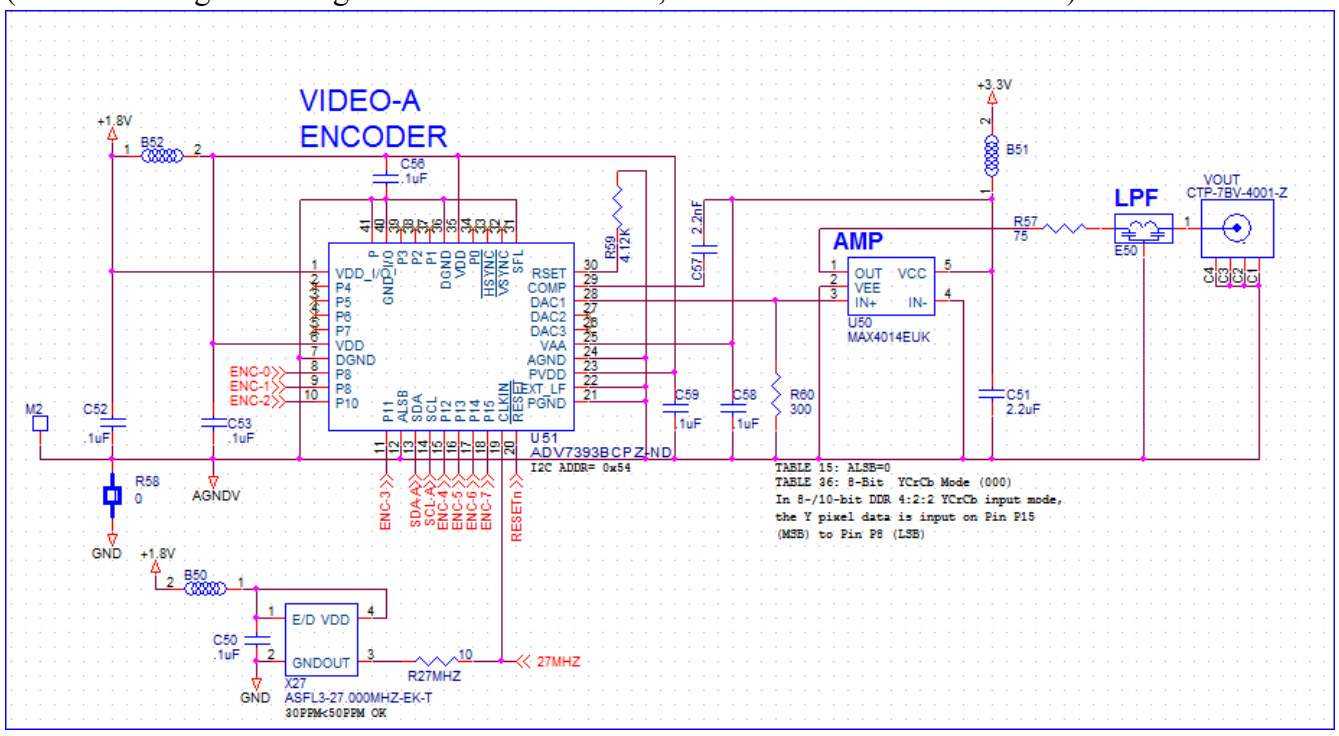
3. Set to use same clock.





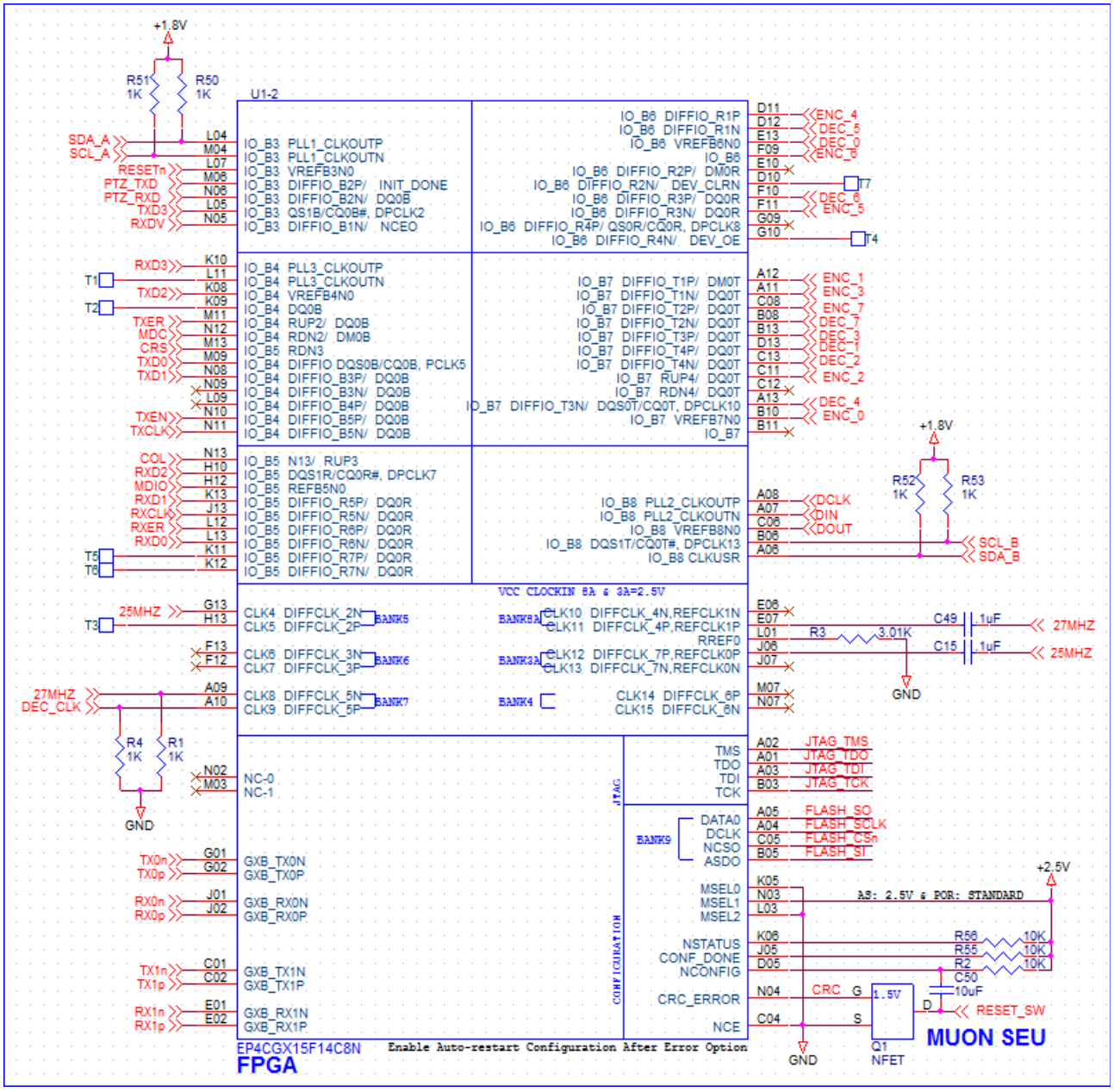
Appendix A: Video Encoder Schematic

(Need matching I/O voltage for Video Encoder I/O, 27MHZ oscillator and I2C bus)



Appendix B: FPGA Schematic

(Need SDA_A, SCL_A &ENC(7..0) and 27MHZ clock portion only)



Appendix C: Signal Tap

(Set up Signal Tap to monitor output. Look at output with BT656 receiver or monitor output sting for ff 00 00 XY pattern that indicate F/V/H fields in Bits 6/5/4 respectively) Note the CrYCbY data.