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ALTGX

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General | PLL/Ports | Ports/Calibration | Rx Analog | Tx Analog

sata_transceiver

rx_datain[0]
tx_datain[15..0]
pll_inclk
tx_ctrlenable[1..0]
rx_digitalreset[0]
rx_analogreset[0]
tx_digitalreset[0]
rx_locktorefclk[0]
rx_locktodata[0]
cal_blk_clk
rx_enapatternalign[0]
tx_invpolarity[0]

rx_dataout[15..0]
tx_dataout[0]
pll_locked[0]
rx_pll_locked[0]
rx_freqlocked[0]
rx_clkout[0]
tx_clkout[0]
rx_patterndetect[1..0]
rx_ctrldetect[1..0]
rx_errdetect[1..0]
rx_disperr[1..0]

Protocol: Basic None
Operation mode: Receiver and Transmitter
Effective data rate: 3000 Mbps
inclk frequency: 150.00 MHz
GXB Transmitter PLL bandwidth mode: Auto
RX PLL bandwidth mode: High
RX Vcm: 0.82
Force RX signal detection
VCCHTX: 1.5
TX Vcm: 0.65
Preemphasis Pre-tap Setting: 0
Preemphasis First Post-tap Setting: 0
Preemphasis Second Post-tap Setting: 0
Self Test mode: none
Word alignment: manual word alignment
Word alignment width: 20
Word alignment pattern: AA07C
8b10b mode: cascaded

Currently selected device family: Arria II GX

Match project/default

Able to implement the requested GXB

General

Which protocol will you be using? Basic

Which subprotocol will you be using? No Loopback

Enforce default settings for this protocol

What is the operation mode? Receiver and Transmitter

What is the number of channels? 1

What is the deserializer block width?

Single (valid data rates: 600 Mbps - 3.200 Gbps)

Double (valid data rates: > 1.000 Gbps)

What is the channel width? 16 bits

Input Data

What would you like to base the setting on? Data Rate

What is the data rate? 3000 Mbps

What is the input clock frequency? 150.0 MHz

What is the data rate division factor? 1

The effective data rate is 3000 Mbps

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Able to implement the requested GXB

PLL Settings

- [x] Train receiver PLL from pll_inclk
- [ ] Use Auxiliary Transmitter(ATX) PLL
- [ ] Enable PLL phase frequency detector(PFD) feedback to compensate latency uncertainty in Tx dataout and Tx clkout paths relative to the reference clock

What is the GXB transmitter PLL bandwidth mode? High

What is the receiver PLL bandwidth mode? High

What is the acceptable PPM threshold between the receiver PLL voltage-controlled-oscillator(VCO) and the CRU clock? +/- 1000

Optional Ports

- [ ] Create 'gxb_powerdown' port to powerdown the Quad
- [ ] Create 'gxb_enable' port to enable the Quad
- [x] Create 'rx_analogreset' port for the analog portion of the receiver
- [x] Create 'rx_digitalreset' port for the digital portion of the receiver
- [x] Create 'tx_digitalreset' port for the digital portion of the transmitter
- [x] Create 'pll_locked' port to indicate PLLs in lock with the reference input clock
- [x] Create 'rx_locktorefclk' port to lock the Rx PLL to the reference clock
- [x] Create 'rx_locktodata' port to lock the Rx PLL to the received data
- [x] Create 'rx_pll_locked' port to indicate Rx PLL is locked to the input reference clock
- [x] Create 'rx_freqlocked' port to indicate Rx PLL is locked to the received data
- [ ] Create 'rx_recovclkout' port from RX PLL

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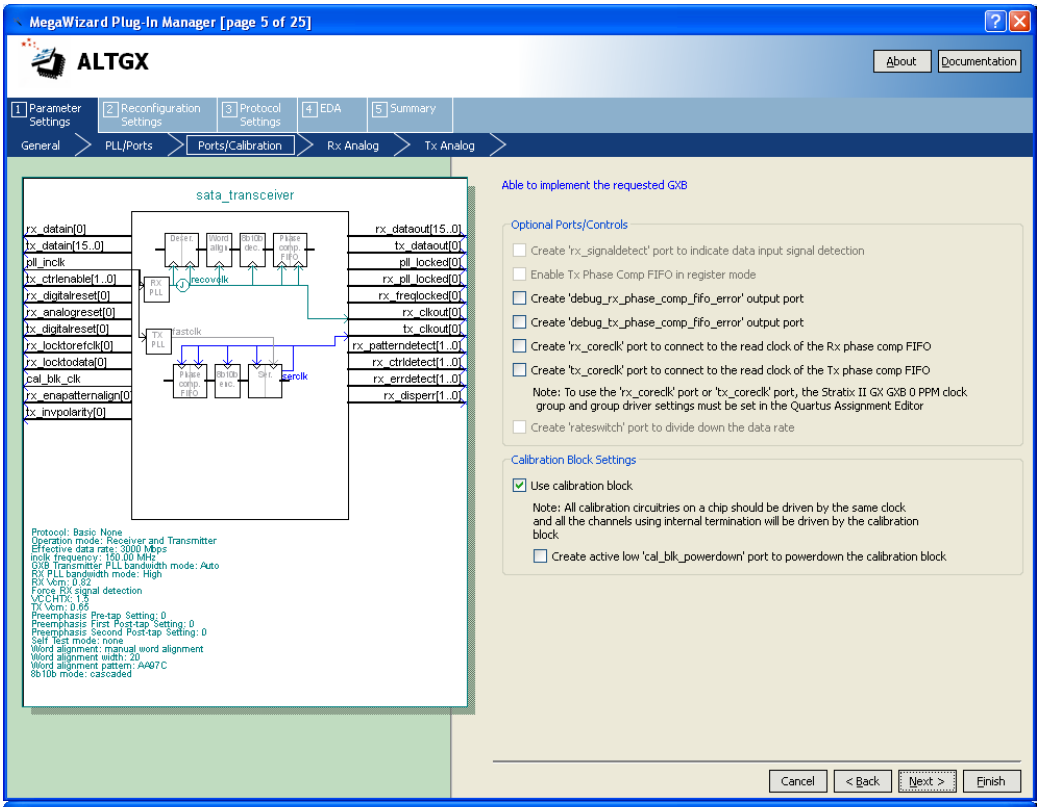
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recovclk
fastclk
coreclk
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Word alignment: manual word alignment
Word alignment width: 20
Word alignment pattern: AA07C
8b10b mode: cascaded
Able to implement the requested GXB
Optional Ports/Controls
Create 'rx_signaldetect' port to indicate data input signal detection
Enable Tx Phase Comp FIFO in register mode
Create 'debug_rx_phase_comp_fifo_error' output port
Create 'debug_tx_phase_comp_fifo_error' output port
Create 'rx_coreclk' port to connect to the read clock of the Rx phase comp FIFO
Create 'tx_coreclk' port to connect to the read clock of the Tx phase comp FIFO
Note: To use the 'rx_coreclk' port or 'tx_coreclk' port, the Stratix II GX GXB 0 PPM clock group and group driver settings must be set in the Quartus Assignment Editor
Create 'rateswitch' port to divide down the data rate
Calibration Block Settings
Use calibration block
Note: All calibration circuitries on a chip should be driven by the same clock and all the channels using internal termination will be driven by the calibration block
Create active low 'cal_blk_powerdown' port to powerdown the calibration block
Cancel
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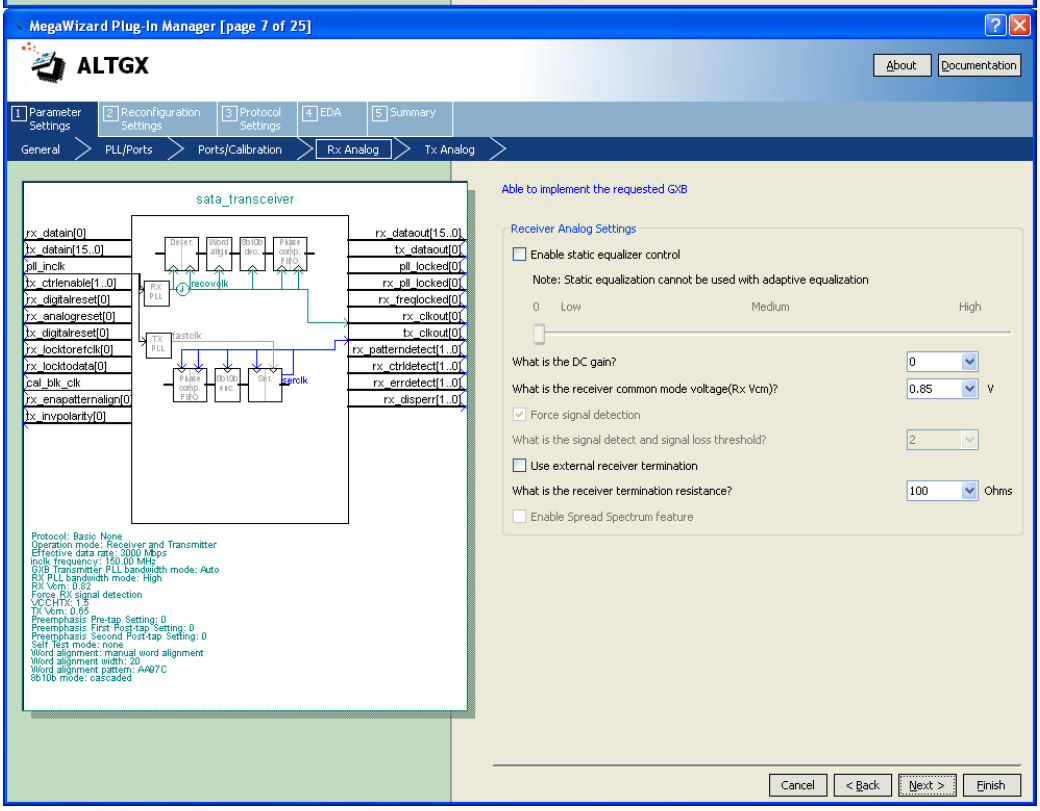
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Word alignment: manual word alignment
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Word alignment pattern: AA07C
8b10b mode: cascaded
Able to implement the requested GXB
Receiver Analog Settings
Enable static equalizer control
Note: Static equalization cannot be used with adaptive equalization
0
Low
Medium
High
What is the DC gain?
0
What is the receiver common mode voltage(Rx Vcm)?
0.85
V
Force signal detection
What is the signal detect and signal loss threshold?
2
Use external receiver termination
What is the receiver termination resistance?
100
Ohms
Enable Spread Spectrum feature
Cancel
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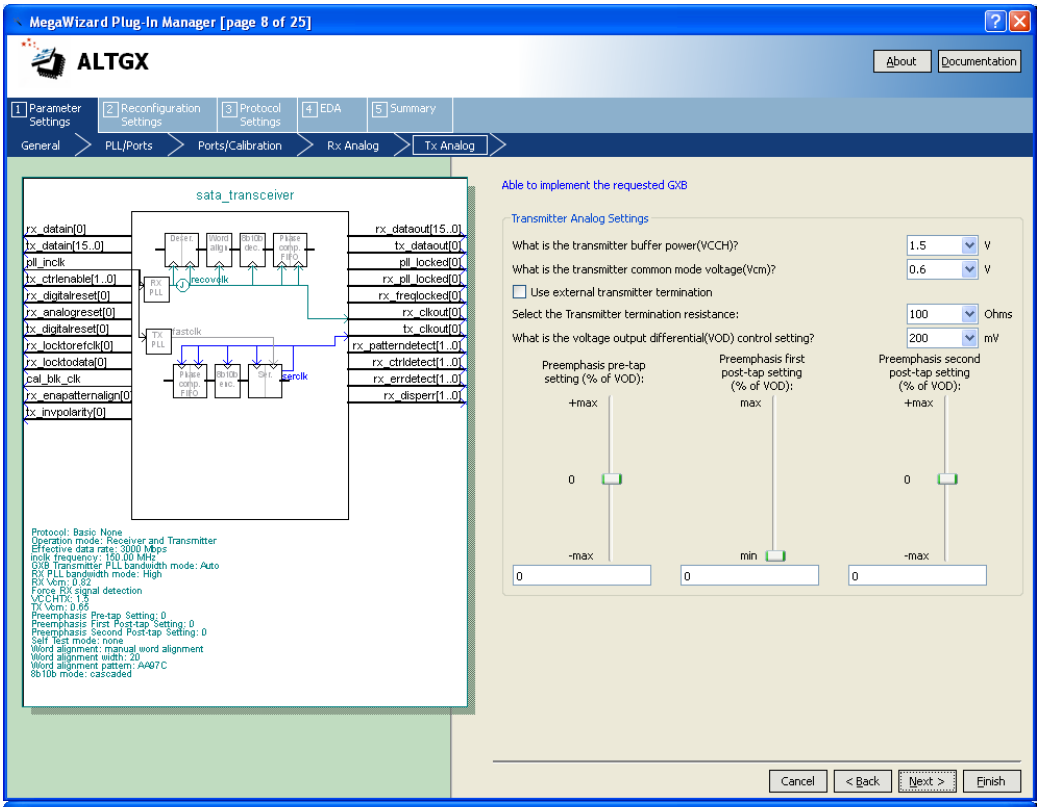
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rx_ctrldetect[1..0]
rx_errdetect[1..0]
rx_disperr[1..0]
recovclk
fastclk
Protocol: Basic None
Able to implement the requested GXB
Transmitter Analog Settings
What is the transmitter buffer power(VCCH)?
What is the transmitter common mode voltage(Vcm)?
Use external transmitter termination
Select the Transmitter termination resistance:
What is the voltage output differential(VOD) control setting?
Preemphasis pre-tap setting (% of VOD):
Preemphasis first post-tap setting (% of VOD):
Preemphasis second post-tap setting (% of VOD):
Cancel
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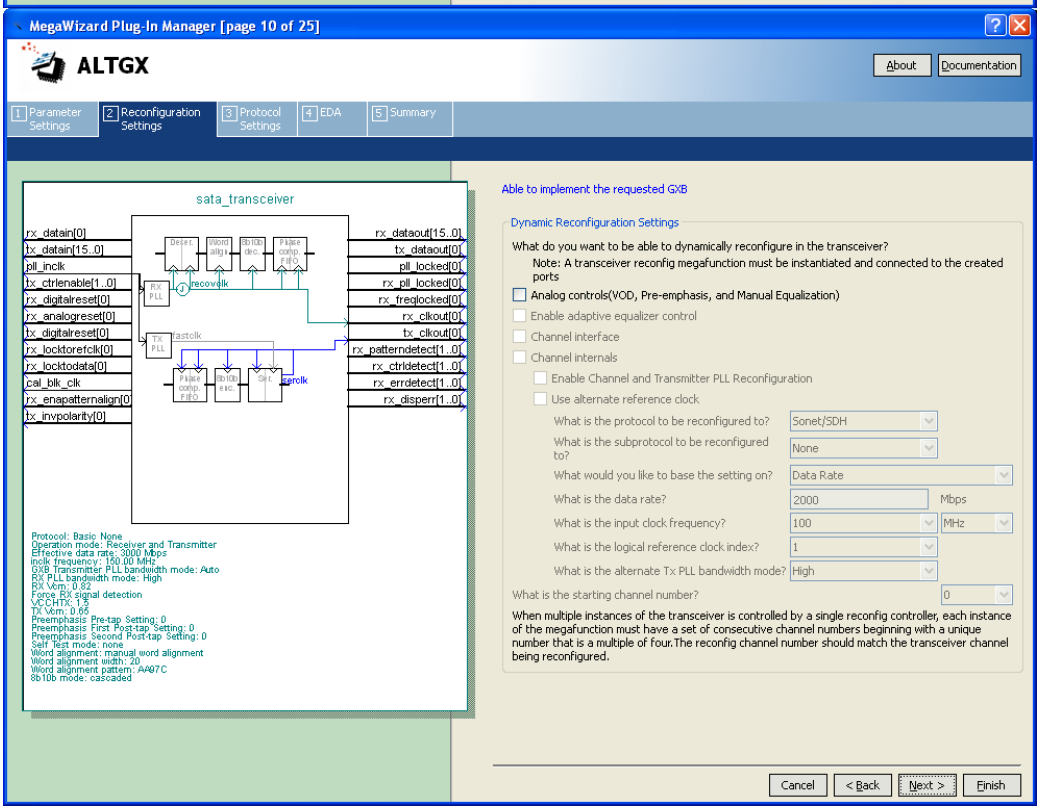
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Able to implement the requested GXB
Dynamic Reconfiguration Settings
What do you want to be able to dynamically reconfigure in the transceiver?
Note: A transceiver reconfig megafunction must be instantiated and connected to the created ports
Analog controls(VOD, Pre-emphasis, and Manual Equalization)
Enable adaptive equalizer control
Channel interface
Channel internals
Enable Channel and Transmitter PLL Reconfiguration
Use alternate reference clock
What is the protocol to be reconfigured to?
What is the subprotocol to be reconfigured to?
What would you like to base the setting on?
What is the data rate?
What is the input clock frequency?
What is the logical reference clock index?
What is the alternate Tx PLL bandwidth mode?
What is the starting channel number?
When multiple instances of the transceiver is controlled by a single reconfig controller, each instance of the megafunction must have a set of consecutive channel numbers beginning with a unique number that is a multiple of four.The reconfig channel number should match the transceiver channel being reconfigured.
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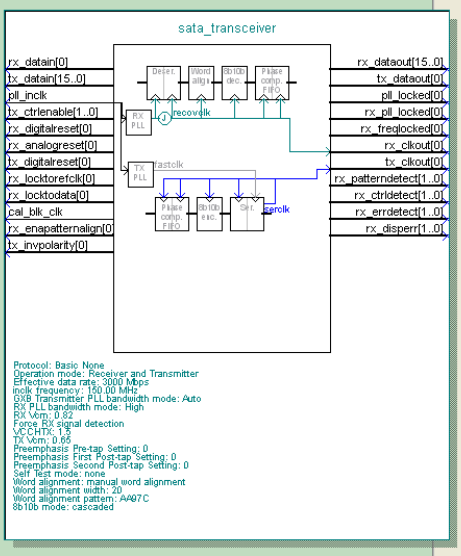
Basic/8B10B | Word Aligner | Rate match/Byte order



Able to implement the requested GXB

- [ ] Enable low latency PCS mode

Note: This option disables all PCS blocks except the Phase Comp FIFO and the optional byte serializer

8b10b Decoder/Encoder

- [x] Enable 8b10b decoder/encoder
  - [ ] Create 'tx_forcedisp' to enable force disparity and use 'tx_dispval' to code up the incoming word using positive or negative disparity
  - [x] Create 'rx_ctrldetect' to indicate 8b10b decoder has detected a control code
  - [x] Create 'rx_errdetect' to indicate 8b10b decoder has detected an error code
  - [x] Create 'rx_disperr' to indicate 8b10b decoder has detected a disparity error
  - [ ] Create 'rx_runningdisp' to indicate the current running disparity of the 8b10b decoded byte
- [ ] Flip receiver output data bits
- [ ] Flip transmitter input data bits
- [ ] Enable transmitter bit reversal
- [x] Create 'tx_invpolarity' to enable transmitter polarity inversion
- [ ] Create 'tx_bitslipboundaryselect' port to control the number of words slipped in the Tx bitslipper

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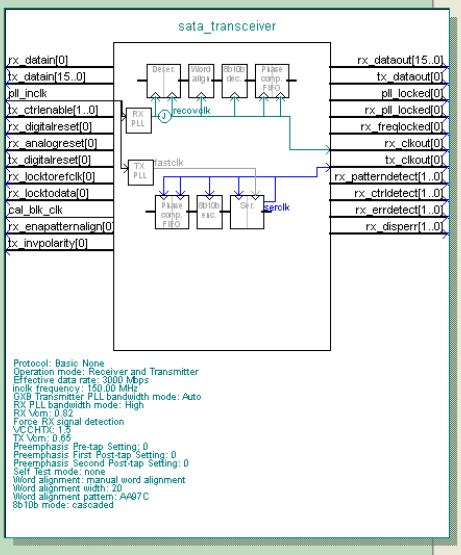
Basic/8B10B | Word Aligner | Rate match/Byte order



Able to implement the requested GXB

Word Aligner

- (•) Use manual word alignment mode
  - When should the word aligner realign?
    - ( ) Realign continuously when 'rx_enapatternalign' is high
    - (•) Realign at the rising edge of 'rx_enapatternalign'
- ( ) Use manual bitslipping mode
- ( ) Use the built-in 'synchronization state machine'
  - Number of valid patterns before synch state is reached: 1
  - Number of consecutive valid words before synch state is reached: 1
  - Number of bad data words before loss of synch state: 1

What is the word alignment pattern length? 10

What is the word alignment pattern? 0101111100 K28.5-

- [ ] Flip word alignment pattern bits
- [ ] Enable run length violation checking with a run length of 40
- [ ] Enable word aligner output reverse bit ordering
- [ ] Create 'rx_syncstatus' output port for pattern detector and word aligner
- [x] Create 'rx_patterndetect' port to indicate pattern detected
- [ ] Create 'rx_invpolarity' to enable word aligner polarity inversion
- [ ] Create 'rx_revbyteorderwa' to enable receiver symbol swap
- [ ] Create 'rx_bitslipboundaryselectout' to indicate the number of bits slipped in the word aligner

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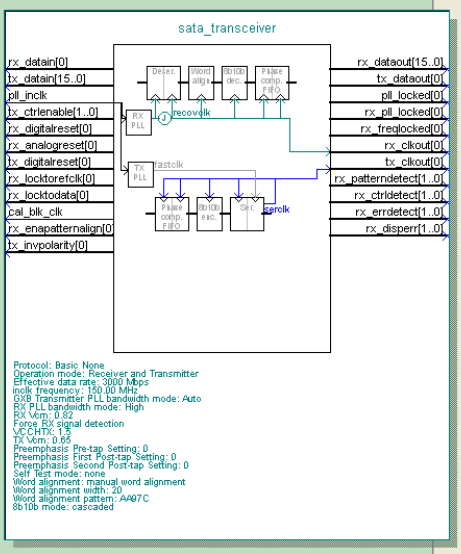

Able to implement the requested GXB

Rate Match FIFO

- [x] Enable rate match FIFO

	(Skip pattern)	(Control pattern)
What is the 20-bit rate match pattern1? (usually used for +ve disparity pattern)	1101000011	1010000011
What is the 20-bit rate match pattern2? (usually used for -ve disparity pattern)	0010111100	0101111100

- [ ] Create 'rx_rmfifofull' to indicate when the rate match FIFO is full
- [ ] Create 'rx_rmfifoempty' to indicate when the rate match FIFO is empty
- [ ] Create 'rx_rmfifodatainserted' to indicate when data is inserted into the rate match FIFO
- [ ] Create 'rx_rmfifodatadeleted' to indicate when data is deleted from the rate match FIFO
- [x] Enable insertion or deletion of consecutive characters or ordered sets

Byte Ordering Block

- [ ] Enable byte ordering block

What do you want the byte ordering block to be based on?

- (•) The syncstatus signal from the word aligner
- ( ) The enabyteord signal from the PLD
- [ ] Use a two word byte ordering pattern

What is the byte ordering pattern?	0000000000	111111011
What is the byte ordering pad pattern?	000000000	

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