Arria-V FPGA interface to DAC/ADC Demo

1. Scope

- Demonstrate Arria-V FPGA on dev.kit communicates to TI High-Speed DAC and ADC
- Demonstrate signal path from DAC to ADC is operating as part of the signal chain
- Present the data in graphical way to visualize the overall functionality in Matlab
- Describe Altera tools and way forward for DPD development.
- Operational Sampling Rates:

    i. DAC 307.2Msps

    ii. ADC 614.4Msps

2. Requirements

Hardware:

- Altera AV dev kit (rev B – tested FMC) (USB cable+ power adaptor)
- TI adaptor rev C
- TSW 30H84   (USB cable+ power adaptor)
- TSW 1266   (USB cable+ power adaptor)
- TSW 1265   (USB cable+ power adaptor) (optional)
- LO Generator   (USB cable or power adaptor)
- Coupler (optional)
- Spectrum analyzer (optional)
- SMA cables:

    1x clock sync from 30H84

    2x LO generator to 30H84 and 1266

    1x loop back from DAC to coupler

    1x loop back from coupler to ADC

    1x from coupler to spectrum analyzer   (optional)

- PC with 4 available USB sockets

Software:

- TI DAC – GUI ver 2.1
- TI ADC – GUI ver 1.0
- Quartus 12.0 SP1
- Matlab ver R2010+
- Windows 7

3. Technical Background

The following block diagram present the overall HW and signal flow:
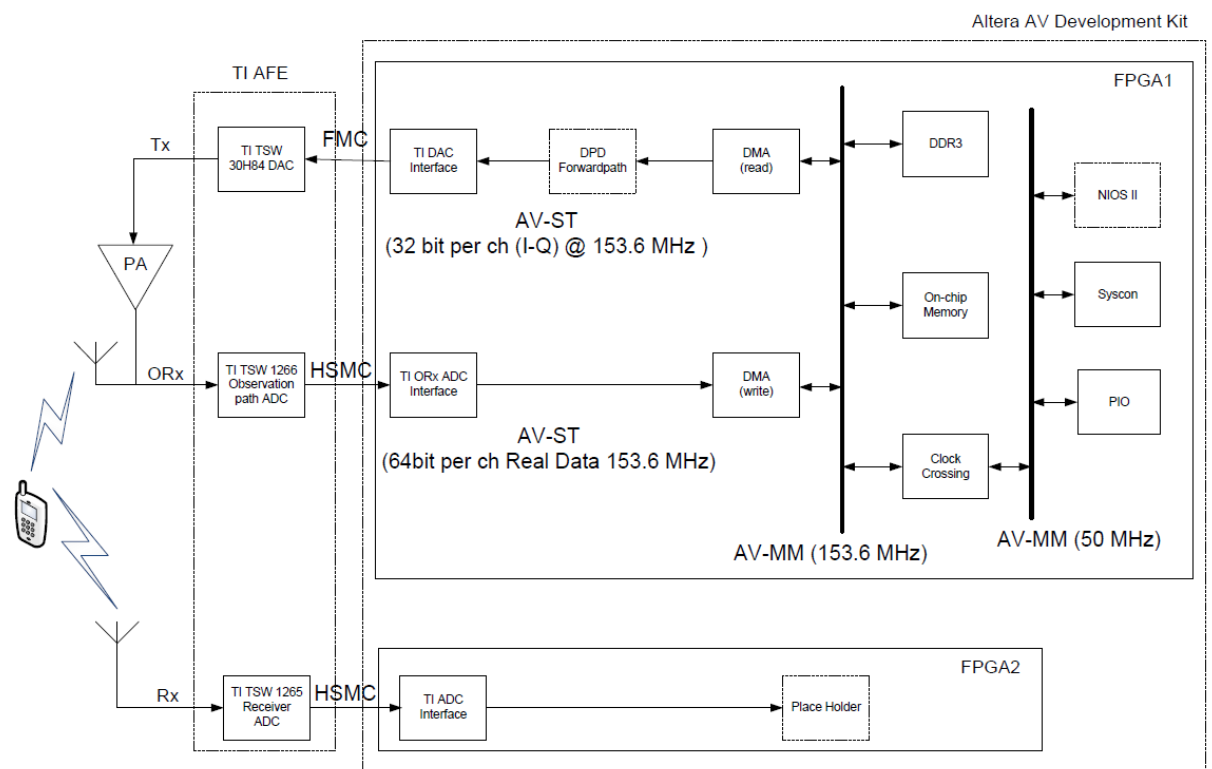
Current demo focuses on TSW30H84 DAC and TSW1266 ADC.

TX:

- On-chip memory (DAC Memory) will be pre-loaded with complex (LTE) signal

- The data from DAC Memory will be streamed out in circular way towards DAC in I/Q format

- DAC will generate analog signal at defined IF frequency

- The signal will be up-converted by complex mixer and LO @ 2.14GHz

- ■ The signal will be routed towards receiver HW through coaxial cable

Observation path RX:

- ■ The input signal will be down-converted by mixer and LO @ 2.14GHz

- ■ The signal will be samples by ADC in I/Q format and the samples will be sent to FPGA

- ■ FPGA will store the samples in on-chip memory (ADC Memory) with defined capture length

- ■ The data from ADC memory will be retrieved from PC and presented in visual way

4. HW Setup

4.1 PC Cards Connection

- Connect the card as showed on the following picture:

  Please note that FPGA NHJ.

4.2 LO Oscillator TSW3065EVM

- Connect USB cable
- Set switch "Supply Select" to "USB"
- Set switch "Ref. Select" to "internal"
- Set DIP switch to following: 1-OFF, 2-OFF, 3-ON, 4-OFF
- Connect sma coax cable from "LO Diff M Out" to TSW30H84 J19 "LO in1"
- Connect sma coax cable from "LO Diff P Out" to TSW1266 "LO IN"

4.3 TSW30H84 DAC setup

- Connect USB cable
- Connect power to J18 "6V in"
- Connect sma coax cable from J5 "clkout6p" to TSW1266 J8 "CLKIN"

- Connect sma coax cable from J7 "RFout1" to TSW1266 "RFIN"

4.4 TSW1266 ADC setup

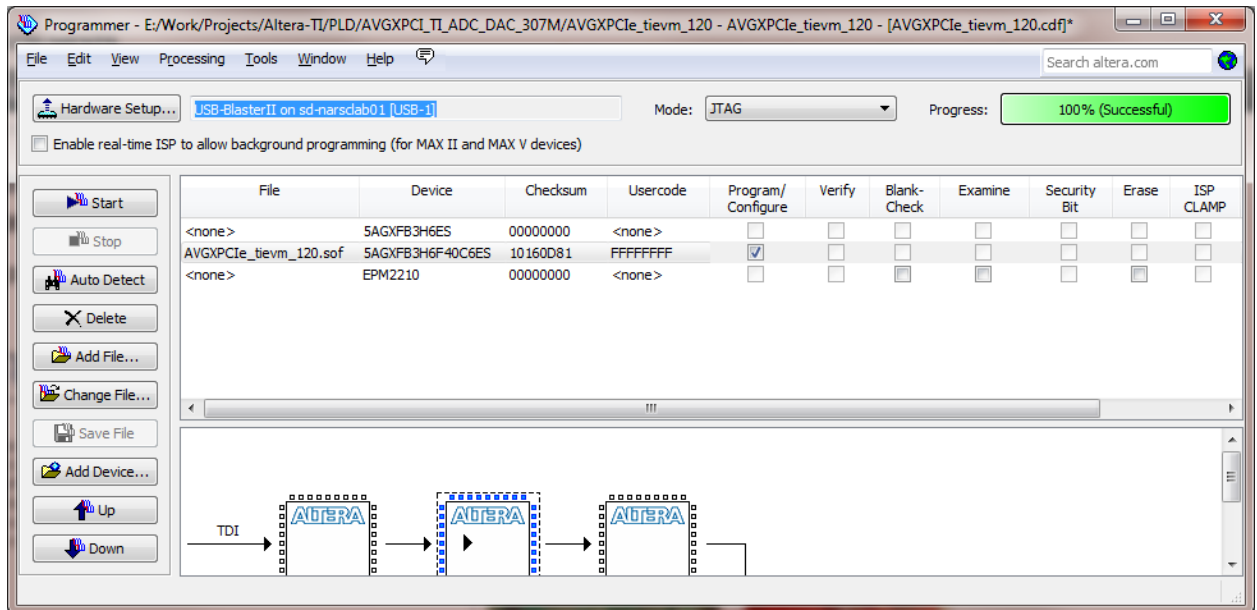- Connect USB cable
- Connect power to J15 "6V in"

4.5 Arria-V dev.kit setup

- Connect USB cable to J7 "USB"
- Connect power to J6 "Power"
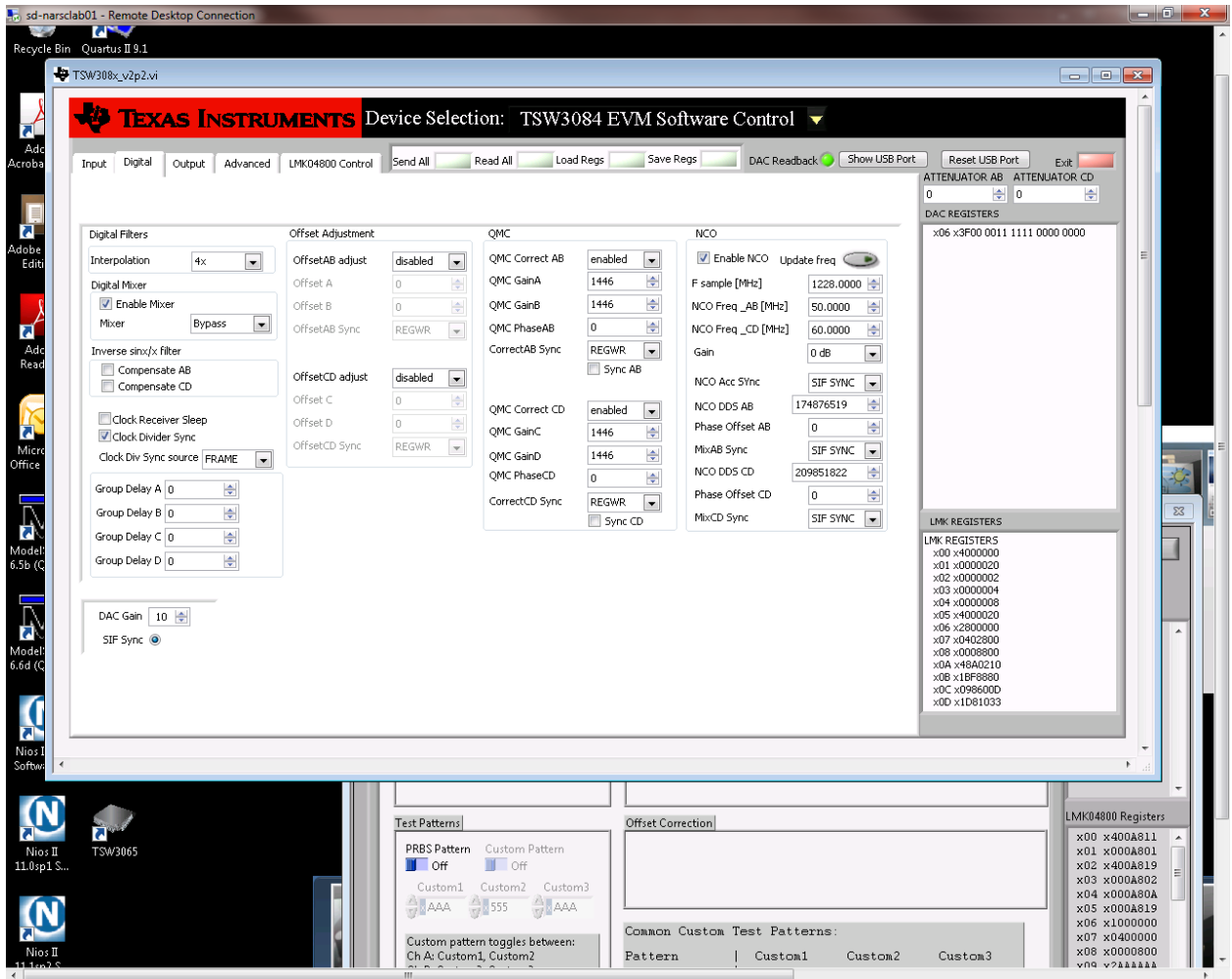
5. Configure Setup

5.1 Arria-V FPGA

- Configure FPGA **2** using AVGXPCIe_tievm_120.sof
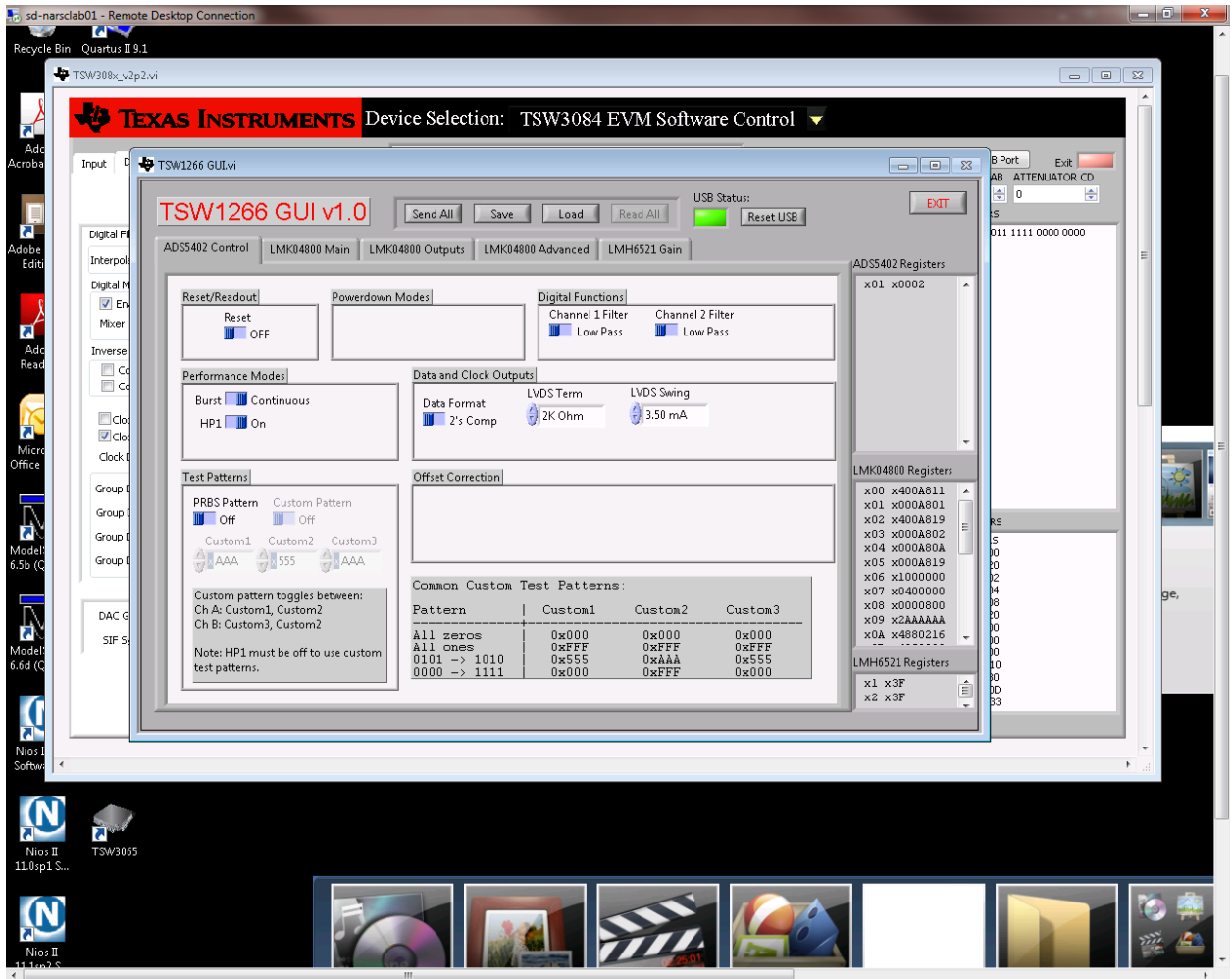

5.2 TSW30H84 DAC

- Run TSW30H84 GUI
- Load registers set from file TSW30H84_307M_demo.
- Hit "Send all" button
- Digital Tab: Update NCO "F sample [Mhz]" to 1228 , "NCO Freq_AB" to 50 and hit "Update freq" button.

- Hit twice SIF Sync radio button to resync the DAC to new settings

5.3 TSW1266 ADC

- Run TSW1266 GUI
- Load registers set from file tsw1266_conf_307M_demo.
- Hit "Send all" button

Now the HW is ready to run the Demo

6. Running Demo

- Run Matlab software and change the "Current Directory" to the path that contains demo files
- Before running the demo you need to make sure if USB Blaster address is correct. This is needed to make sure the demo would be able to communicate with Arria-V HW.
  If just one USB-Blaster (Local or other) defined in system the jtag chain will have index 0. You should modify all (3) .tcl files to point to right jtag chain

    set hardware [lindex [get_hardware_names] 0]

- In "AlteraTI_HW_Demo2.m" script, ensure that Quarus path is point to your local installed version of Quartus 12.0sp1.
- Run "AlteraTI_HW_Demo2.m" script
- Script will continue to run in indefinite loop and present the following figure:
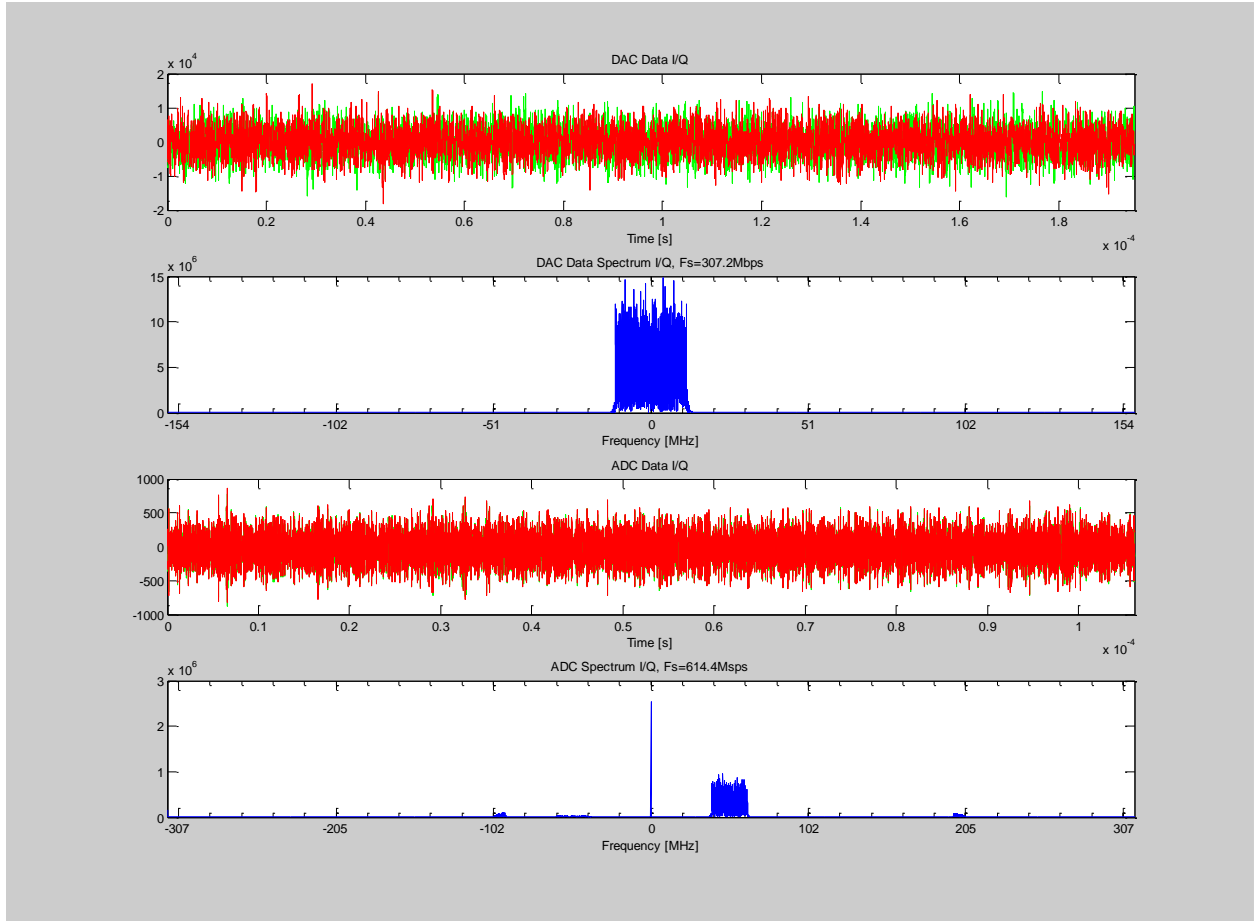
- Two upper charts represent the data that is streamed out towards the DAC. Two bottom represent the data that is read back by ADC
- In order to stop "in clean way" the Demo, you should click the X button to close the chart. This operation will close the chart and stop in controlled way the demo

7. References

http://www.altera.com/corporate/news_room/releases/2012/products/nr-ti-rf-devkit.html

http://www.ti.com/ww/en/analog/dataconverters/wideband_feedback_rf_solution.html?DCMP=analog_signalchain_mr&HQS=arria-v-devkit-pr

Revisions:

Revision	Reviewer	Comments
0	Dan Pritsker	
1	Shahin Gheitanchi	

Link for auto-updating .mif files:

http://www.alteraforum.com/forum/archive/index.php/t-1925.html