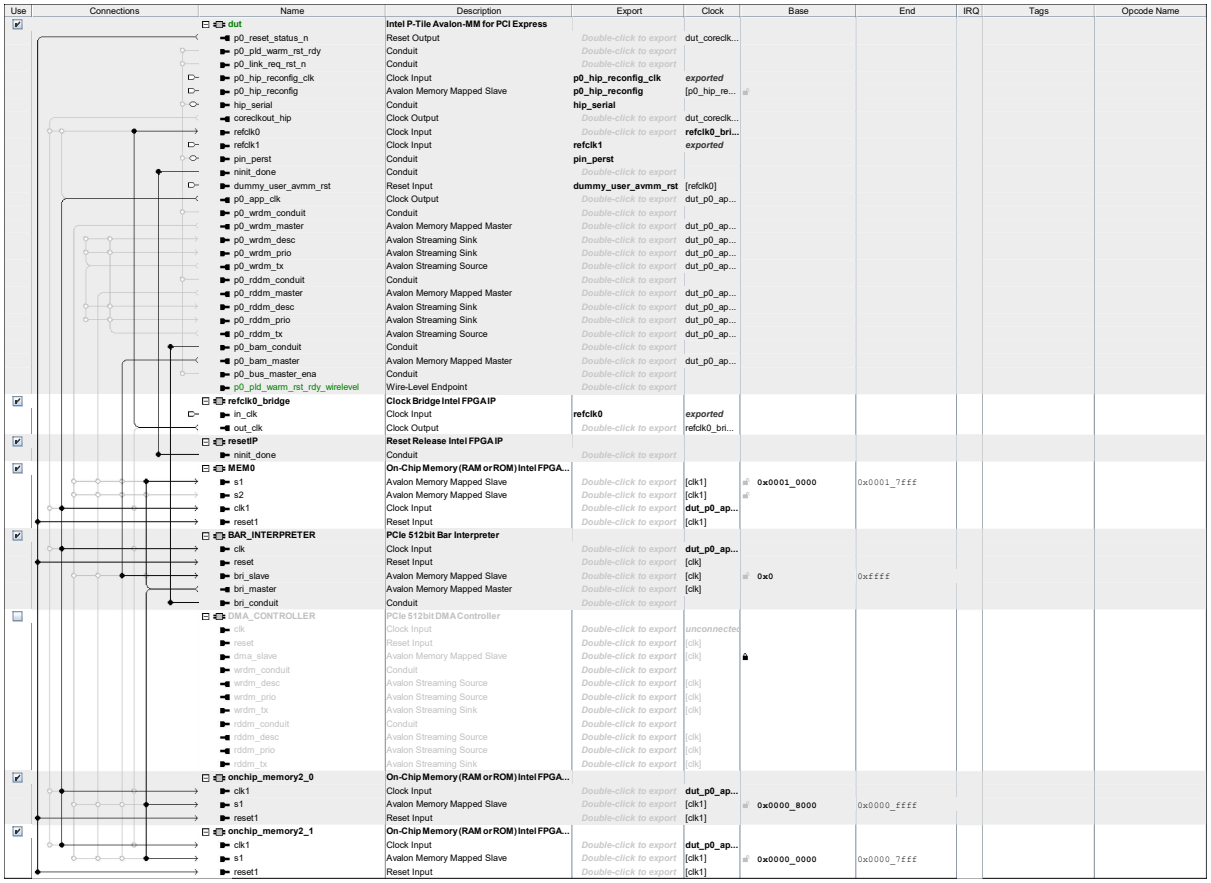

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opcode Name
☑		**dut**	**Intel P-Tile Avalon-MM for PCI Express**							
		p0_reset_status_n	Reset Output	*Double-click to export*	dut_coreclk...					
		p0_pld_warm_rst_rdy	Conduit	*Double-click to export*						
		p0_link_req_rst_n	Conduit	*Double-click to export*						
		p0_hip_reconfig_clk	Clock Input	**p0_hip_reconfig_clk**	*exported*					
		p0_hip_reconfig	Avalon Memory Mapped Slave	**p0_hip_reconfig**	[p0_hip_re...					
		hip_serial	Conduit	**hip_serial**						
		coreclkout_hip	Clock Output	*Double-click to export*	dut_coreclk...					
		refclk0	Clock Input	*Double-click to export*	**refclk0_bri...**					
		refclk1	Clock Input	**refclk1**	*exported*					
		pin_perst	Conduit	**pin_perst**						
		ninit_done	Conduit	*Double-click to export*						
		dummy_user_avmm_rst	Reset Input	**dummy_user_avmm_rst**	[refclk0]					
		p0_app_clk	Clock Output	*Double-click to export*	dut_p0_ap...					
		p0_wrdm_conduit	Conduit	*Double-click to export*						
		p0_wrdm_master	Avalon Memory Mapped Master	*Double-click to export*	dut_p0_ap...					
		p0_wrdm_desc	Avalon Streaming Sink	*Double-click to export*	dut_p0_ap...					
		p0_wrdm_prio	Avalon Streaming Sink	*Double-click to export*	dut_p0_ap...					
		p0_wrdm_tx	Avalon Streaming Source	*Double-click to export*	dut_p0_ap...					
		p0_rddm_conduit	Conduit	*Double-click to export*						
		p0_rddm_master	Avalon Memory Mapped Master	*Double-click to export*	dut_p0_ap...					
		p0_rddm_desc	Avalon Streaming Sink	*Double-click to export*	dut_p0_ap...					
		p0_rddm_prio	Avalon Streaming Sink	*Double-click to export*	dut_p0_ap...					
		p0_rddm_tx	Avalon Streaming Source	*Double-click to export*	dut_p0_ap...					
		p0_bam_conduit	Conduit	*Double-click to export*						
		p0_bam_master	Avalon Memory Mapped Master	*Double-click to export*	dut_p0_ap...					
		p0_bus_master_ena	Conduit	*Double-click to export*						
		p0_pld_warm_rst_rdy_wirelevel	Wire-Level Endpoint	*Double-click to export*						
☑		**refclk0_bridge**	**Clock Bridge Intel FPGA IP**							
		in_clk	Clock Input	**refclk0**	*exported*					
		out_clk	Clock Output	*Double-click to export*	refclk0_bri...					
☑		**resetIP**	**Reset Release Intel FPGA IP**							
		ninit_done	Conduit	*Double-click to export*						
☑		**MEM0**	**On-Chip Memory (RAM or ROM) Intel FPGA...**							
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk1]	**0x0001_0000**	0x0001_7fff			
		s2	Avalon Memory Mapped Slave	*Double-click to export*	[clk1]					
		clk1	Clock Input	*Double-click to export*	**dut_p0_ap...**					
		reset1	Reset Input	*Double-click to export*	[clk1]					
☑		**BAR_INTERPRETER**	**PCIe 512bit Bar Interpreter**							
		clk	Clock Input	*Double-click to export*	**dut_p0_ap...**					
		reset	Reset Input	*Double-click to export*	[clk]					
		bri_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	**0x0**	0xffff			
		bri_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]					
		bri_conduit	Conduit	*Double-click to export*						
☐		**DMA_CONTROLLER**	**PCIe 512bit DMA Controller**							
		clk	Clock Input	*Double-click to export*	*unconnected*					
		reset	Reset Input	*Double-click to export*	[clk]					
		dma_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]					
		wrdm_conduit	Conduit	*Double-click to export*						
		wrdm_desc	Avalon Streaming Source	*Double-click to export*	[clk]					
		wrdm_prio	Avalon Streaming Source	*Double-click to export*	[clk]					
		wrdm_tx	Avalon Streaming Sink	*Double-click to export*	[clk]					
		rddm_conduit	Conduit	*Double-click to export*						
		rddm_desc	Avalon Streaming Source	*Double-click to export*	[clk]					
		rddm_prio	Avalon Streaming Source	*Double-click to export*	[clk]					
		rddm_tx	Avalon Streaming Sink	*Double-click to export*	[clk]					
☑		**onchip_memory2_0**	**On-Chip Memory (RAM or ROM) Intel FPGA...**							
		clk1	Clock Input	*Double-click to export*	**dut_p0_ap...**					
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk1]	**0x0000_8000**	0x0000_ffff			
		reset1	Reset Input	*Double-click to export*	[clk1]					
☑		**onchip_memory2_1**	**On-Chip Memory (RAM or ROM) Intel FPGA...**							
		clk1	Clock Input	*Double-click to export*	**dut_p0_ap...**					
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk1]	**0x0000_0000**	0x0000_7fff			
		reset1	Reset Input	*Double-click to export*	[clk1]					