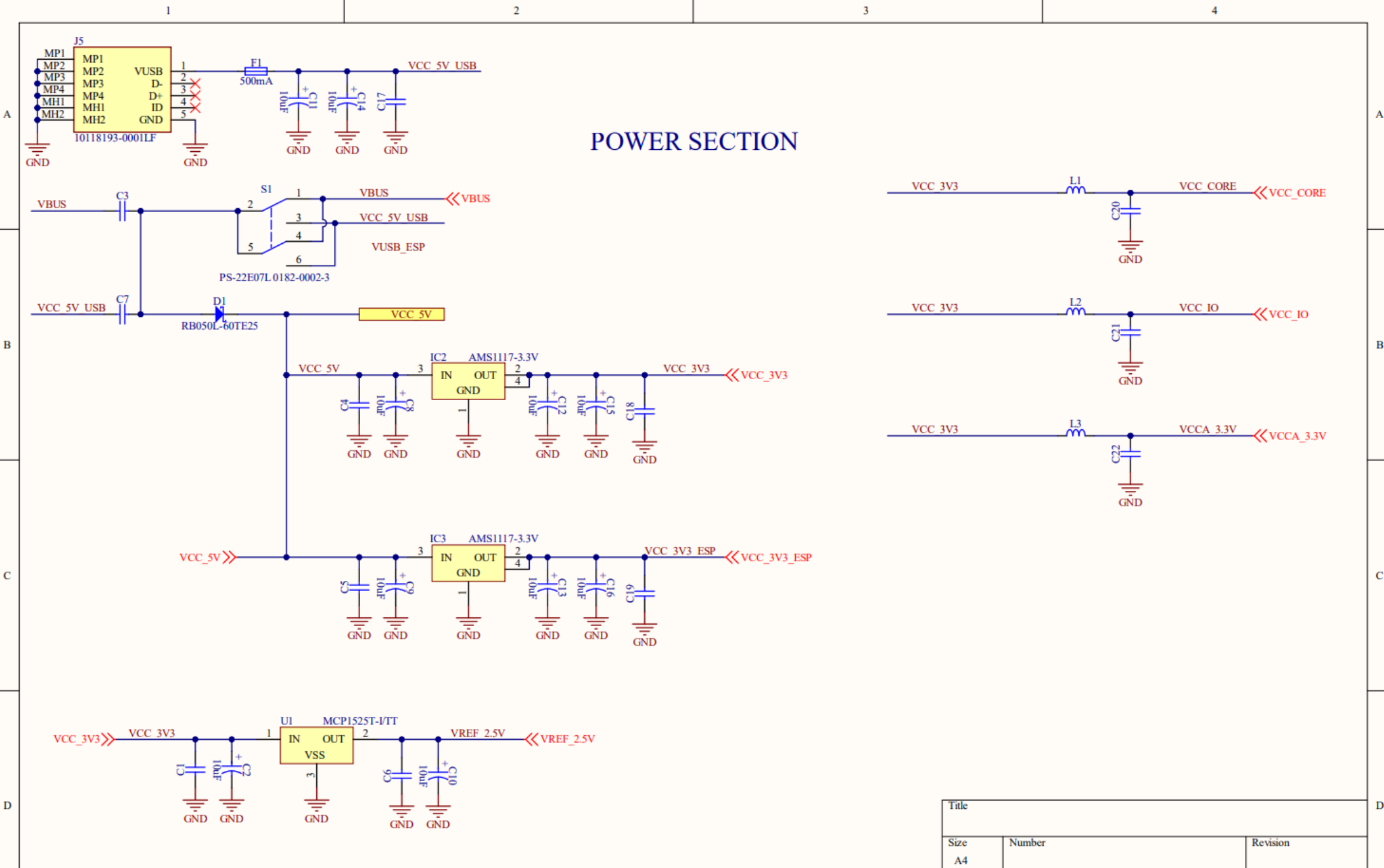
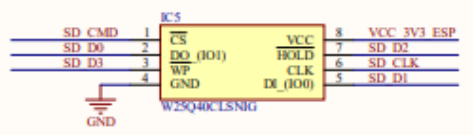
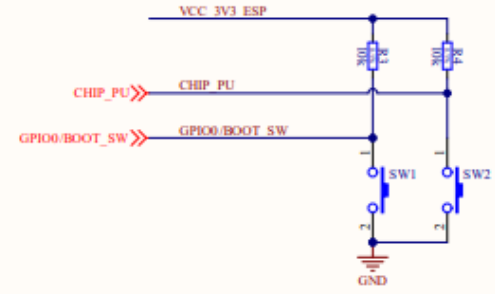
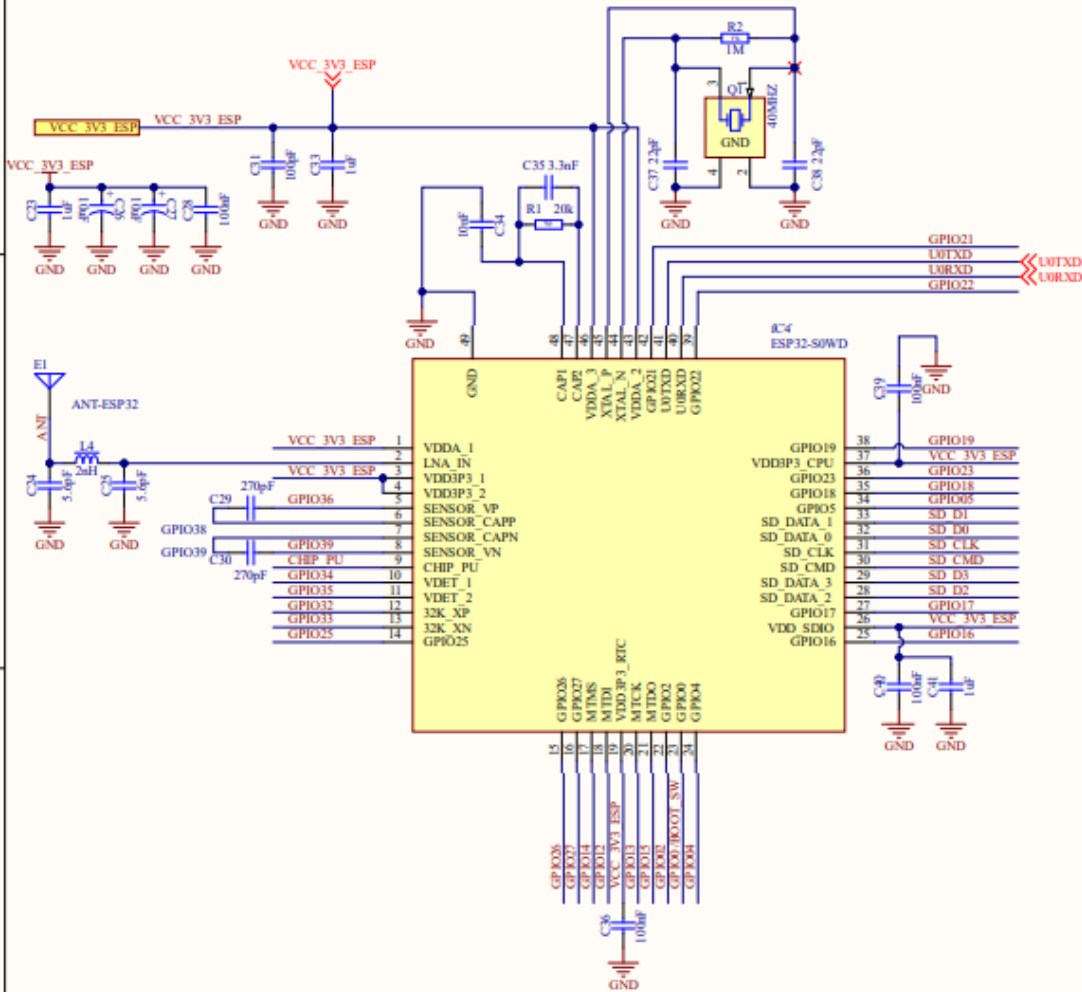
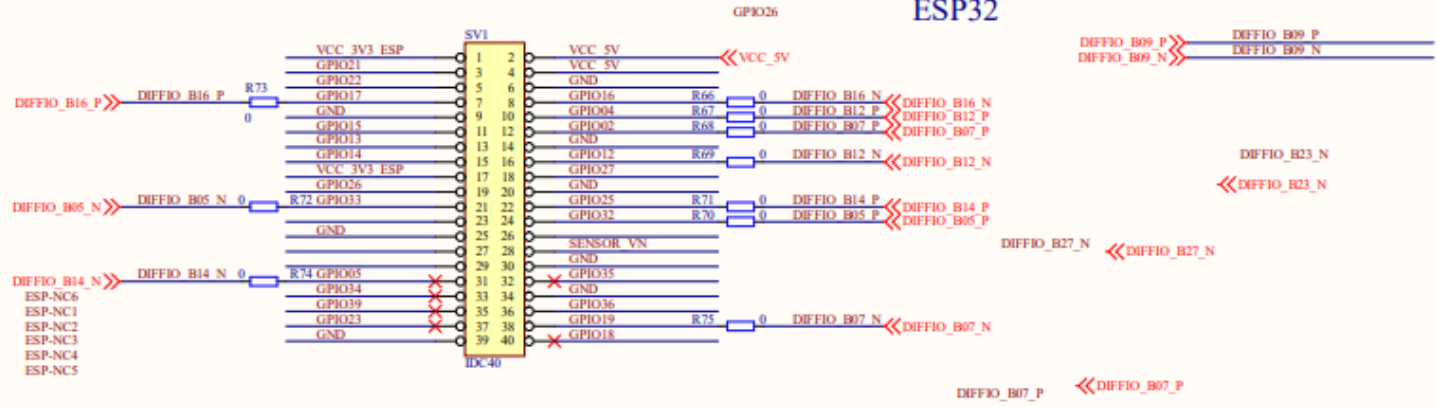


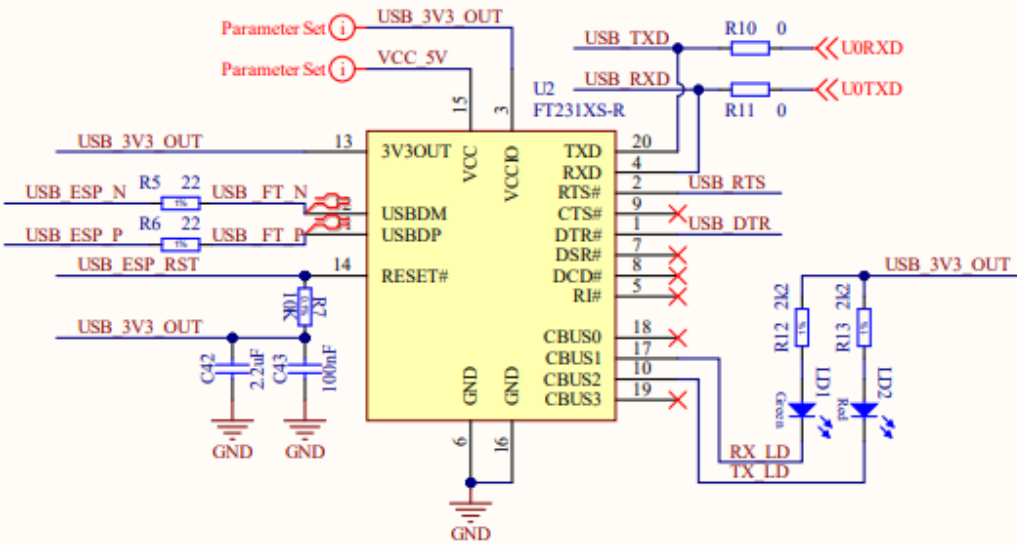
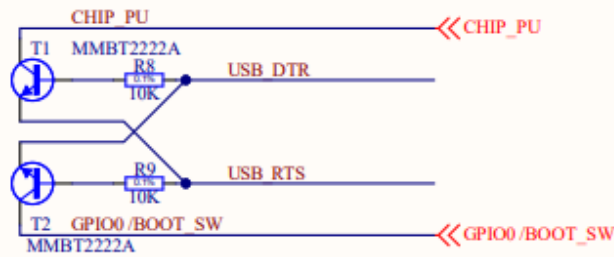
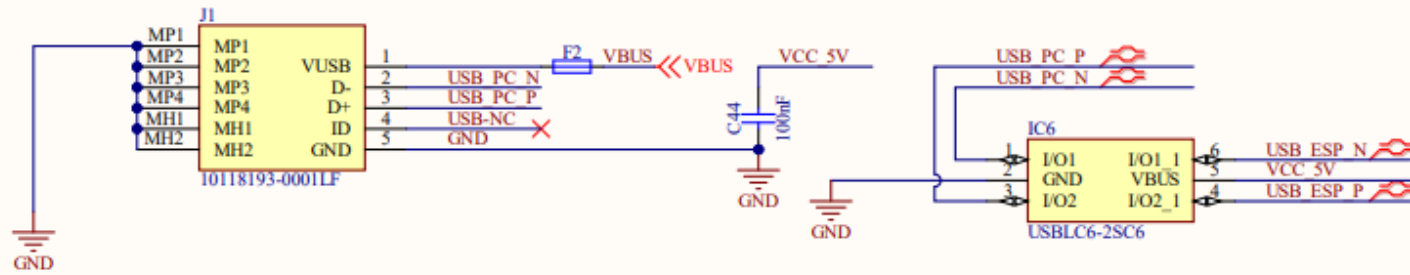
POWER SECTION



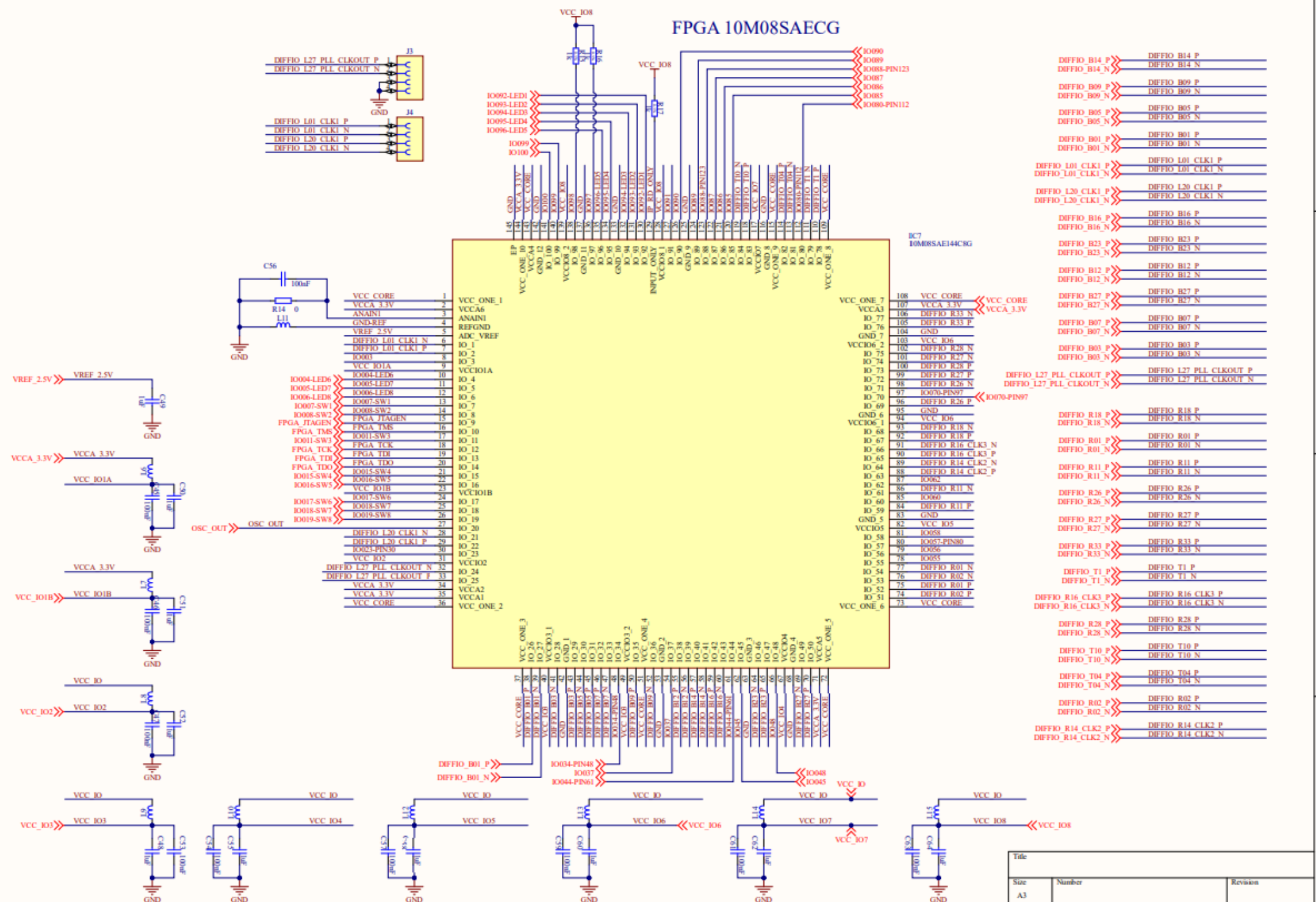
Title		
Size	Number	Revision
A4		

ESP32





FPGA 10M08SAECG



Title		Revision	
Site	Number		
A3			
Date:	11/04/2020	Sheet of	
File:	C:\Users\... Sheet04 FPGA Sheet SchDoc	Drawn By:	

CONFIGURATION & BANK2,BANK3 BREAKOUT BANK6,BANK7 BREAKOUT

