Pin Information for the Intel® Cyclone®10 10CL040 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B1	VREFB1N0	IO			DIFFIO_L1p	G4
B1	VREFB1N0	IO			DIFFIO_L1n	G3
B1	VREFB1N0	IO			DIFFIO_L2p	B2
B1	VREFB1N0	IO			DIFFIO_L2n	B1
B1	VREFB1N0	IO	VREFB1N0			G5
B1	VREFB1N0	IO			DIFFIO_L4p	E4
B1	VREFB1N0	IO			DIFFIO_L4n	E3
B1	VREFB1N1	IO			DIFFIO_L8p	D2
B1	VREFB1N1	IO		DATA1,ASDO	DIFFIO_L8n	D1
B1	VREFB1N1	IO	VREFB1N1			H7
B1	VREFB1N1	IO			DIFFIO_L9p	H6
B1	VREFB1N1	IO			DIFFIO_L9n	J6
B1	VREFB1N1	IO		FLASH_nCE,nCSO	DIFFIO_L10p	E2
B1	VREFB1N1	IO			DIFFIO_L10n	E1
B1	VREFB1N1	IO			DIFFIO_L12p	F2
B1	VREFB1N1	IO			DIFFIO_L12n	F1
B1	VREFB1N1	IO			DIFFIO_L14p	H8
B1	VREFB1N1	IO			DIFFIO_L14n	J8
B1	VREFB1N2	IO			DIFFIO_L18n	J5
B1	VREFB1N2	nSTATUS		nSTATUS		K6
B1	VREFB1N2	IO	VREFB1N2			H5
B1	VREFB1N2	IO			DIFFIO_L20p	L8
B1	VREFB1N2	IO			DIFFIO_L20n	K8
B1	VREFB1N2	IO			DIFFIO_L21p	J7
B1	VREFB1N2	IO			DIFFIO_L21n	K7
B1	VREFB1N3	IO	DPCLK0			J4
B1	VREFB1N3	IO			DIFFIO_L23p	H2
B1	VREFB1N3	IO			DIFFIO_L23n	H1
B1	VREFB1N3	IO	VREFB1N3			J3
B1	VREFB1N3	IO			DIFFIO_L24p	J2
B1	VREFB1N3	IO			DIFFIO_L24n	J1
B1	VREFB1N3	IO		DCLK		K2
B1	VREFB1N3	IO		DATA0		K1
B1	VREFB1N3	nCONFIG		nCONFIG		K5
B1	VREFB1N3	TDI		TDI		L5
B1	VREFB1N3	TCK		TCK		L2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B1	VREFB1N3	TMS		TMS		L1
B1	VREFB1N3	TDO		TDO		L4
B1	VREFB1N3	nCE		nCE		L3
B1	VREFB1N3	CLK0	DIFFCLK_0p			G2
B1	VREFB1N3	CLK1	DIFFCLK_0n			G1
B2	VREFB2N0	CLK2	DIFFCLK_1p			T2
B2	VREFB2N0	CLK3	DIFFCLK_1n			T1
B2	VREFB2N0	IO			DIFFIO_L26p	L6
B2	VREFB2N0	IO			DIFFIO_L26n	M6
B2	VREFB2N0	IO			DIFFIO_L27p	M2
B2	VREFB2N0	IO			DIFFIO_L27n	M1
B2	VREFB2N0	IO			DIFFIO_L28p	M4
B2	VREFB2N0	IO			DIFFIO_L28n	M3
B2	VREFB2N0	IO			DIFFIO_L29p	N2
B2	VREFB2N0	IO			DIFFIO_L29n	N1
B2	VREFB2N0	IO			DIFFIO_L30n	L7
B2	VREFB2N0	IO	VREFB2N0			M5
B2	VREFB2N0	IO			DIFFIO_L32p	P2
B2	VREFB2N0	IO			DIFFIO_L32n	P1
B2	VREFB2N0	IO			DIFFIO_L33p	R2
B2	VREFB2N0	IO			DIFFIO_L33n	R1
B2	VREFB2N1	IO				N5
B2	VREFB2N1	IO	DPCLK1		DIFFIO_L34p	P4
B2	VREFB2N1	IO			DIFFIO_L34n	P3
B2	VREFB2N1	IO			DIFFIO_L35p	U2
B2	VREFB2N1	IO			DIFFIO_L35n	U1
B2	VREFB2N1	IO			DIFFIO_L38p	V2
B2	VREFB2N1	IO			DIFFIO_L38n	V1
B2	VREFB2N1	IO	VREFB2N1			P5
B2	VREFB2N1	IO			DIFFIO_L41p	N6
B2	VREFB2N1	IO			DIFFIO_L41n	M7
B2	VREFB2N1	IO			DIFFIO_L42p	M8
B2	VREFB2N2	IO			DIFFIO_L42n	N8
B2	VREFB2N2	IO			DIFFIO_L44p	W2
B2	VREFB2N2	IO			DIFFIO_L44n	W1
B2	VREFB2N2	IO			DIFFIO_L45p	Y2

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Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B2	VREFB2N2	IO			DIFFIO_L45n	Y1
B2	VREFB2N2	IO	VREFB2N2			T3
B2	VREFB2N2	IO			DIFFIO_L49p	N7
B2	VREFB2N2	IO			DIFFIO_L49n	P7
B2	VREFB2N3	IO	RUP1			V4
B2	VREFB2N3	IO	RDN1			V3
B2	VREFB2N3	IO			DIFFIO_L52p	P6
B2	VREFB2N3	IO				T5
B2	VREFB2N3	IO	CDPCLK1			T4
B2	VREFB2N3	IO	VREFB2N3			R5
B2	VREFB2N3	IO				R6
B2	VREFB2N3	IO			DIFFIO_L53p	R7
B2	VREFB2N3	IO			DIFFIO_L53n	T7
B3	VREFB3N3	IO			DIFFIO_B1p	V6
B3	VREFB3N3	IO			DIFFIO_B1n	V5
B3	VREFB3N3	IO			DIFFIO_B3p	U7
B3	VREFB3N3	IO			DIFFIO_B3n	U8
B3	VREFB3N3	IO	VREFB3N3			Y4
B3	VREFB3N3	IO			DIFFIO_B4p	Y3
B3	VREFB3N3	IO	CDPCLK2		DIFFIO_B6p	Y6
B3	VREFB3N2	IO	PLL1_CLKOUTp			AA3
B3	VREFB3N2	IO	PLL1_CLKOUTn			AB3
B3	VREFB3N2	IO			DIFFIO_B7p	W6
B3	VREFB3N2	IO			DIFFIO_B7n	V7
B3	VREFB3N2	IO				AA4
B3	VREFB3N2	IO	VREFB3N2			AB4
B3	VREFB3N2	IO			DIFFIO_B8p	AA5
B3	VREFB3N2	IO			DIFFIO_B8n	AB5
B3	VREFB3N2	IO			DIFFIO_B11p	T8
B3	VREFB3N2	IO			DIFFIO_B11n	T9
B3	VREFB3N2	IO			DIFFIO_B12p	W7
B3	VREFB3N2	IO			DIFFIO_B12n	Y7
B3	VREFB3N2	IO			DIFFIO_B13p	U9
B3	VREFB3N2	IO			DIFFIO_B13n	V8
B3	VREFB3N2	IO				W8
B3	VREFB3N1	IO			DIFFIO_B14p	AA7

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B3	VREFB3N1	IO			DIFFIO_B14n	AB7
B3	VREFB3N1	IO				Y8
B3	VREFB3N1	IO			DIFFIO_B15p	T10
B3	VREFB3N1	IO			DIFFIO_B15n	T11
B3	VREFB3N1	IO	VREFB3N1			V9
B3	VREFB3N1	IO	DPCLK2		DIFFIO_B16p	V10
B3	VREFB3N1	IO			DIFFIO_B17n	U10
B3	VREFB3N1	IO			DIFFIO_B18p	AA8
B3	VREFB3N1	IO			DIFFIO_B18n	AB8
B3	VREFB3N1	IO			DIFFIO_B21p	AA9
B3	VREFB3N1	IO	DPCLK3		DIFFIO_B21n	AB9
B3	VREFB3N0	IO	VREFB3N0			U11
B3	VREFB3N0	IO			DIFFIO_B25n	V11
B3	VREFB3N0	IO			DIFFIO_B26p	W10
B3	VREFB3N0	IO			DIFFIO_B26n	Y10
B3	VREFB3N0	IO			DIFFIO_B27p	AA10
B3	VREFB3N0	IO			DIFFIO_B27n	AB10
B3	VREFB3N0	CLK15	DIFFCLK_6p			AA11
B3	VREFB3N0	CLK14	DIFFCLK_6n			AB11
B4	VREFB4N3	CLK13	DIFFCLK_7p			AA12
B4	VREFB4N3	CLK12	DIFFCLK_7n			AB12
B4	VREFB4N3	IO			DIFFIO_B28p	AA13
B4	VREFB4N3	IO			DIFFIO_B28n	AB13
B4	VREFB4N3	IO			DIFFIO_B29p	AA14
B4	VREFB4N3	IO			DIFFIO_B29n	AB14
B4	VREFB4N3	IO	VREFB4N3			V12
B4	VREFB4N3	IO			DIFFIO_B32p	W13
B4	VREFB4N3	IO	DPCLK4		DIFFIO_B32n	Y13
B4	VREFB4N3	IO			DIFFIO_B33p	AA15
B4	VREFB4N3	IO			DIFFIO_B33n	AB15
B4	VREFB4N3	IO			DIFFIO_B34p	U12
B4	VREFB4N2	IO			DIFFIO_B35p	AA16
B4	VREFB4N2	IO			DIFFIO_B35n	AB16
B4	VREFB4N2	IO			DIFFIO_B36p	T12
B4	VREFB4N2	IO			DIFFIO_B36n	T13
B4	VREFB4N2	IO	DPCLK5			V13

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B4	VREFB4N2	IO	VREFB4N2			W14
B4	VREFB4N2	IO			DIFFIO_B38n	U13
B4	VREFB4N2	IO			DIFFIO_B39p	V14
B4	VREFB4N2	IO			DIFFIO_B39n	U14
B4	VREFB4N2	IO			DIFFIO_B40p	U15
B4	VREFB4N2	IO			DIFFIO_B40n	V15
B4	VREFB4N1	IO			DIFFIO_B41n	W15
B4	VREFB4N1	IO			DIFFIO_B42p	T14
B4	VREFB4N1	IO			DIFFIO_B42n	T15
B4	VREFB4N1	IO				AB18
B4	VREFB4N1	IO	VREFB4N1			AA18
B4	VREFB4N1	IO	RUP2			AA19
B4	VREFB4N1	IO	RDN2			AB19
B4	VREFB4N0	IO			DIFFIO_B48p	W17
B4	VREFB4N0	IO	CDPCLK3		DIFFIO_B48n	Y17
B4	VREFB4N0	IO			DIFFIO_B49p	AA20
B4	VREFB4N0	IO			DIFFIO_B49n	AB20
B4	VREFB4N0	IO	VREFB4N0			V16
B4	VREFB4N0	IO			DIFFIO_B50p	U16
B4	VREFB4N0	IO			DIFFIO_B50n	U17
B4	VREFB4N0	IO	PLL4_CLKOUTp			T16
B4	VREFB4N0	IO	PLL4_CLKOUTn			R16
B4	VREFB4N0	IO			DIFFIO_B52p	R14
B4	VREFB4N0	IO			DIFFIO_B52n	R15
B5	VREFB5N3	IO			DIFFIO_R56n	AA22
B5	VREFB5N3	IO			DIFFIO_R56p	AA21
B5	VREFB5N3	IO	RUP3			T17
B5	VREFB5N3	IO	RDN3			T18
B5	VREFB5N3	IO	CDPCLK4			W20
B5	VREFB5N3	IO	VREFB5N3			W19
B5	VREFB5N3	IO			DIFFIO_R51n	Y22
B5	VREFB5N2	IO			DIFFIO_R51p	Y21
B5	VREFB5N2	IO			DIFFIO_R50n	U20
B5	VREFB5N2	IO			DIFFIO_R50p	U19
B5	VREFB5N2	IO			DIFFIO_R49n	W22
B5	VREFB5N2	IO			DIFFIO_R49p	W21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B5	VREFB5N2	IO			DIFFIO_R46n	P15
B5	VREFB5N2	IO			DIFFIO_R46p	P16
B5	VREFB5N2	IO	VREFB5N2			R17
B5	VREFB5N2	IO				P17
B5	VREFB5N2	IO			DIFFIO_R45n	V22
B5	VREFB5N2	IO			DIFFIO_R45p	V21
B5	VREFB5N2	IO			DIFFIO_R44n	R20
B5	VREFB5N2	IO			DIFFIO_R43n	U22
B5	VREFB5N1	IO			DIFFIO_R43p	U21
B5	VREFB5N1	IO			DIFFIO_R42n	R18
B5	VREFB5N1	IO			DIFFIO_R42p	R19
B5	VREFB5N1	IO			DIFFIO_R40p	N16
B5	VREFB5N1	IO			DIFFIO_R39n	R22
B5	VREFB5N1	IO			DIFFIO_R39p	R21
B5	VREFB5N1	IO	VREFB5N1			P20
B5	VREFB5N1	IO			DIFFIO_R38n	P22
B5	VREFB5N1	IO			DIFFIO_R38p	P21
B5	VREFB5N1	IO			DIFFIO_R36n	N20
B5	VREFB5N1	IO			DIFFIO_R36p	N19
B5	VREFB5N0	IO			DIFFIO_R33n	N17
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R33p	N18
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R32n	N22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R32p	N21
B5	VREFB5N0	IO			DIFFIO_R31n	M22
B5	VREFB5N0	IO			DIFFIO_R31p	M21
B5	VREFB5N0	IO			DIFFIO_R30n	M20
B5	VREFB5N0	IO			DIFFIO_R30p	M19
B5	VREFB5N0	IO	VREFB5N0			M16
B5	VREFB5N0	CLK7	DIFFCLK_3n			T22
B5	VREFB5N0	CLK6	DIFFCLK_3p			T21
B6	VREFB6N3	CLK5	DIFFCLK_2n			G22
B6	VREFB6N3	CLK4	DIFFCLK_2p			G21
B6	VREFB6N3	CONF_DONE		CONF_DONE		M18
B6	VREFB6N3	MSEL0		MSEL0		M17
B6	VREFB6N3	MSEL1		MSEL1		L18
B6	VREFB6N3	MSEL2		MSEL2		L17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B6	VREFB6N3	MSEL3		MSEL3		K20
B6	VREFB6N3	IO		INIT_DONE	DIFFIO_R27n	L22
B6	VREFB6N3	IO		CRC_ERROR	DIFFIO_R27p	L21
B6	VREFB6N3	IO	VREFB6N3			K19
B6	VREFB6N3	IO		nCEO	DIFFIO_R24n	K22
B6	VREFB6N3	IO		CLKUSR	DIFFIO_R24p	K21
B6	VREFB6N3	IO	DPCLK7		DIFFIO_R23n	J22
B6	VREFB6N3	IO			DIFFIO_R23p	J21
B6	VREFB6N3	IO			DIFFIO_R22n	H22
B6	VREFB6N2	IO			DIFFIO_R22p	H21
B6	VREFB6N2	IO			DIFFIO_R20n	K17
B6	VREFB6N2	IO			DIFFIO_R20p	K18
B6	VREFB6N2	IO	VREFB6N2			J18
B6	VREFB6N2	IO			DIFFIO_R18n	F22
B6	VREFB6N2	IO			DIFFIO_R18p	F21
B6	VREFB6N1	IO			DIFFIO_R13n	H20
B6	VREFB6N1	IO			DIFFIO_R13p	H19
B6	VREFB6N1	IO			DIFFIO_R12n	E22
B6	VREFB6N1	IO			DIFFIO_R12p	E21
B6	VREFB6N1	IO	VREFB6N1			H18
B6	VREFB6N1	IO			DIFFIO_R10n	J17
B6	VREFB6N1	IO			DIFFIO_R10p	H16
B6	VREFB6N1	IO			DIFFIO_R9n	D22
B6	VREFB6N1	IO			DIFFIO_R9p	D21
B6	VREFB6N1	IO			DIFFIO_R8n	F20
B6	VREFB6N1	IO			DIFFIO_R8p	F19
B6	VREFB6N1	IO			DIFFIO_R7n	G18
B6	VREFB6N1	IO			DIFFIO_R7p	H17
B6	VREFB6N1	IO			DIFFIO_R6n	C22
B6	VREFB6N0	IO			DIFFIO_R6p	C21
B6	VREFB6N0	IO			DIFFIO_R5n	B22
B6	VREFB6N0	IO			DIFFIO_R5p	B21
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R4n	C20
B6	VREFB6N0	IO	VREFB6N0			D20
B6	VREFB6N0	IO			DIFFIO_R2n	F17
B6	VREFB6N0	IO			DIFFIO_R2p	G17

Pin Information for the Intel® Cyclone®10 10CL040 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B7	VREFB7N0	IO			DIFFIO_T51n	F16
B7	VREFB7N0	IO			DIFFIO_T51p	E16
B7	VREFB7N0	IO			DIFFIO_T50n	F15
B7	VREFB7N0	IO			DIFFIO_T50p	G16
B7	VREFB7N0	IO			DIFFIO_T49n	G15
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T49p	F14
B7	VREFB7N0	IO			DIFFIO_T48n	H15
B7	VREFB7N0	IO			DIFFIO_T48p	H14
B7	VREFB7N0	IO	VREFB7N0			D17
B7	VREFB7N0	IO			DIFFIO_T47n	C19
B7	VREFB7N0	IO			DIFFIO_T47p	D19
B7	VREFB7N0	IO	PLL2_CLKOUTn			A20
B7	VREFB7N1	IO	PLL2_CLKOUTp			B20
B7	VREFB7N1	IO			DIFFIO_T46p	C17
B7	VREFB7N1	IO	RUP4			B19
B7	VREFB7N1	IO	RDN4			A19
B7	VREFB7N1	IO			DIFFIO_T45n	A18
B7	VREFB7N1	IO			DIFFIO_T45p	B18
B7	VREFB7N1	IO	VREFB7N1			D15
B7	VREFB7N1	IO			DIFFIO_T44n	E15
B7	VREFB7N1	IO			DIFFIO_T44p	G14
B7	VREFB7N1	IO			DIFFIO_T42n	G13
B7	VREFB7N1	IO			DIFFIO_T41n	A17
B7	VREFB7N2	IO			DIFFIO_T41p	B17
B7	VREFB7N2	IO			DIFFIO_T40n	A16
B7	VREFB7N2	IO			DIFFIO_T40p	B16
B7	VREFB7N2	IO	VREFB7N2			C15
B7	VREFB7N2	IO			DIFFIO_T38n	E14
B7	VREFB7N2	IO	DPCLK8		DIFFIO_T37p	F13
B7	VREFB7N2	IO			DIFFIO_T36n	A15
B7	VREFB7N3	IO			DIFFIO_T36p	B15
B7	VREFB7N3	IO			DIFFIO_T35n	C13
B7	VREFB7N3	IO			DIFFIO_T35p	D13
B7	VREFB7N3	IO	VREFB7N3			E13
B7	VREFB7N3	IO			DIFFIO_T31n	A14
B7	VREFB7N3	IO			DIFFIO_T31p	B14

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B7	VREFB7N3	IO			DIFFIO_T29n	A13
B7	VREFB7N3	IO	DPCLK9		DIFFIO_T29p	B13
B7	VREFB7N3	IO			DIFFIO_T28p	E12
B7	VREFB7N3	IO			DIFFIO_T27n	E11
B7	VREFB7N3	IO			DIFFIO_T27p	F11
B7	VREFB7N3	CLK8	DIFFCLK_5n			A12
B7	VREFB7N3	CLK9	DIFFCLK_5p			B12
B8	VREFB8N0	CLK10	DIFFCLK_4n			A11
B8	VREFB8N0	CLK11	DIFFCLK_4p			B11
B8	VREFB8N0	IO			DIFFIO_T26n	D10
B8	VREFB8N0	IO			DIFFIO_T26p	E10
B8	VREFB8N0	IO			DIFFIO_T25n	A10
B8	VREFB8N0	IO			DIFFIO_T25p	B10
B8	VREFB8N0	IO			DIFFIO_T24n	A9
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T24p	B9
B8	VREFB8N0	IO	VREFB8N0			C10
B8	VREFB8N0	IO			DIFFIO_T22n	G11
B8	VREFB8N0	IO		DATA2	DIFFIO_T20n	A8
B8	VREFB8N1	IO		DATA3	DIFFIO_T20p	B8
B8	VREFB8N1	IO			DIFFIO_T19n	A7
B8	VREFB8N1	IO		DATA4	DIFFIO_T19p	B7
B8	VREFB8N1	IO			DIFFIO_T18n	A6
B8	VREFB8N1	IO			DIFFIO_T18p	B6
B8	VREFB8N1	IO	VREFB8N1			E9
B8	VREFB8N1	IO	DPCLK11		DIFFIO_T16n	C8
B8	VREFB8N1	IO			DIFFIO_T16p	C7
B8	VREFB8N1	IO			DIFFIO_T14n	H11
B8	VREFB8N1	IO			DIFFIO_T14p	H10
B8	VREFB8N2	IO		DATA5	DIFFIO_T11p	A5
B8	VREFB8N2	IO	VREFB8N2			B5
B8	VREFB8N2	IO			DIFFIO_T8n	G10
B8	VREFB8N2	IO		DATA6	DIFFIO_T8p	F10
B8	VREFB8N2	IO		DATA7	DIFFIO_T7n	C6
B8	VREFB8N2	IO			DIFFIO_T7p	D7
B8	VREFB8N2	IO			DIFFIO_T6n	A4
B8	VREFB8N3	IO			DIFFIO_T6p	B4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
B8	VREFB8N3	IO			DIFFIO_T5n	F8
B8	VREFB8N3	IO			DIFFIO_T5p	G8
B8	VREFB8N3	IO			DIFFIO_T4n	A3
B8	VREFB8N3	IO			DIFFIO_T4p	B3
B8	VREFB8N3	IO	VREFB8N3			D6
B8	VREFB8N3	IO				E7
B8	VREFB8N3	IO			DIFFIO_T3n	C3
B8	VREFB8N3	IO	CDPCLK7		DIFFIO_T3p	C4
B8	VREFB8N3	IO			DIFFIO_T1n	F7
B8	VREFB8N3	IO			DIFFIO_T1p	G7
B8	VREFB8N3	IO				F9
B8	VREFB8N3	IO	PLL3_CLKOUTn			E6
B8	VREFB8N3	IO	PLL3_CLKOUTp			E5
B8	VREFB8N3	IO				G9
		GND				L10
		GND				L11
		GND				M10
		GND				M11
		GND				L12
		GND				L13
		GND				M12
		GND				M13
		GND				N11
		GND				K11
		GND				N12
		GND				K12
		GND				K13
		GND				N13
		GND				N10
		GND				K10
		GND				J9
		GND				F12
		GND				H12
		GND				H13
		GND				J15
		GND				K16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				L15
		GND				N15
		GND				R13
		GND				R11
		GND				R9
		GND				P8
		GND				A1
		GND				C5
		GND				C9
		GND				C11
		GND				C12
		GND				C14
		GND				C16
		GND				A22
		GND				E20
		GND				G20
		GND				L20
		GND				P19
		GND				V20
		GND				Y20
		GND				AB22
		GND				Y18
		GND				Y16
		GND				Y12
		GND				Y11
		GND				Y9
		GND				Y5
		GND				AB1
		GND				N3
		GND				U3
		GND				W3
		GND				D3
		GND				F3
		GND				K3
		GND				AA2
		GND				H3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		GND				R3
		GND				AB6
		GND				Y15
		GND				T20
		GND				J19
		GND				C18
		GND				D8
		GND				AA1
		GND				AA17
		GND				AB17
		GND				C1
		GND				C2
		GNDA1				U5
		GNDA2				E18
		GNDA3				F5
		GNDA4				V18
		VCCD_PLL1				U6
		VCCD_PLL2				E17
		VCCD_PLL3				F6
		VCCD_PLL4				V17
		VCCIO1				D4
		VCCIO1				F4
		VCCIO1				K4
		VCCIO1				H4
		VCCIO2				N4
		VCCIO2				U4
		VCCIO2				W4
		VCCIO2				R4
		VCCIO3				AB2
		VCCIO3				W5
		VCCIO3				W9
		VCCIO3				W11
		VCCIO3				AA6
		VCCIO4				AB21
		VCCIO4				W12
		VCCIO4				W16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCIO4				W18
		VCCIO4				Y14
		VCCIO5				P18
		VCCIO5				V19
		VCCIO5				Y19
		VCCIO5				T19
		VCCIO6				E19
		VCCIO6				G19
		VCCIO6				L19
		VCCIO6				J20
		VCCIO7				A21
		VCCIO7				D12
		VCCIO7				D14
		VCCIO7				D16
		VCCIO7				D18
		VCCIO8				A2
		VCCIO8				D5
		VCCIO8				D9
		VCCIO8				D11
		VCCIO8				E8
		VCCA1				T6
		VCCA2				F18
		VCCA3				G6
		VCCA4				U18
		VCCINT				J11
		VCCINT				J12
		VCCINT				L14
		VCCINT				M14
		VCCINT				P11
		VCCINT				P12
		VCCINT				L9
		VCCINT				M9
		VCCINT				J13
		VCCINT				J14
		VCCINT				K14
		VCCINT				J10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	F484
		VCCINT				K9
		VCCINT				N9
		VCCINT				P9
		VCCINT				P10
		VCCINT				P13
		VCCINT				P14
		VCCINT				N14
		VCCINT				J16
		VCCINT				K15
		VCCINT				L16
		VCCINT				M15
		VCCINT				R12
		VCCINT				R10
		VCCINT				R8
		VCCINT				H9
		VCCINT				G12

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B1	VREFB1N0	IO			DIFFIO_L1p	G4
B1	VREFB1N0	IO			DIFFIO_L1n	G3
B1	VREFB1N0	IO			DIFFIO_L2p	B2
B1	VREFB1N0	IO			DIFFIO_L2n	B1
B1	VREFB1N0	IO	VREFB1N0			G5
B1	VREFB1N0	IO			DIFFIO_L4p	E4
B1	VREFB1N0	IO			DIFFIO_L4n	E3
B1	VREFB1N1	IO			DIFFIO_L8p	D2
B1	VREFB1N1	IO		DATA1,ASDO	DIFFIO_L8n	D1
B1	VREFB1N1	IO	VREFB1N1			H7
B1	VREFB1N1	IO			DIFFIO_L9p	H6
B1	VREFB1N1	IO			DIFFIO_L9n	J6
B1	VREFB1N1	IO		FLASH_nCE,nCSO	DIFFIO_L10p	E2
B1	VREFB1N1	IO			DIFFIO_L10n	E1
B1	VREFB1N1	IO			DIFFIO_L12p	F2
B1	VREFB1N1	IO			DIFFIO_L12n	F1
B1	VREFB1N1	IO			DIFFIO_L14p	H8
B1	VREFB1N1	IO			DIFFIO_L14n	J8
B1	VREFB1N2	IO			DIFFIO_L18n	J5
B1	VREFB1N2	nSTATUS		nSTATUS		K6
B1	VREFB1N2	IO	VREFB1N2			H5
B1	VREFB1N2	IO			DIFFIO_L20p	L8
B1	VREFB1N2	IO			DIFFIO_L20n	K8
B1	VREFB1N2	IO			DIFFIO_L21p	J7
B1	VREFB1N2	IO			DIFFIO_L21n	K7
B1	VREFB1N3	IO	DPCLK0			J4
B1	VREFB1N3	IO			DIFFIO_L23p	H2
B1	VREFB1N3	IO			DIFFIO_L23n	H1
B1	VREFB1N3	IO	VREFB1N3			J3
B1	VREFB1N3	IO			DIFFIO_L24p	J2
B1	VREFB1N3	IO			DIFFIO_L24n	J1
B1	VREFB1N3	IO		DCLK		K2
B1	VREFB1N3	IO		DATA0		K1
B1	VREFB1N3	nCONFIG		nCONFIG		K5
B1	VREFB1N3	TDI		TDI		L5
B1	VREFB1N3	TCK		TCK		L2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B1	VREFB1N3	TMS		TMS		L1
B1	VREFB1N3	TDO		TDO		L4
B1	VREFB1N3	nCE		nCE		L3
B1	VREFB1N3	CLK0	DIFFCLK_0p			G2
B1	VREFB1N3	CLK1	DIFFCLK_0n			G1
B2	VREFB2N0	CLK2	DIFFCLK_1p			T2
B2	VREFB2N0	CLK3	DIFFCLK_1n			T1
B2	VREFB2N0	IO			DIFFIO_L26p	L6
B2	VREFB2N0	IO			DIFFIO_L26n	M6
B2	VREFB2N0	IO			DIFFIO_L27p	M2
B2	VREFB2N0	IO			DIFFIO_L27n	M1
B2	VREFB2N0	IO			DIFFIO_L28p	M4
B2	VREFB2N0	IO			DIFFIO_L28n	M3
B2	VREFB2N0	IO			DIFFIO_L29p	N2
B2	VREFB2N0	IO			DIFFIO_L29n	N1
B2	VREFB2N0	IO			DIFFIO_L30n	L7
B2	VREFB2N0	IO	VREFB2N0			M5
B2	VREFB2N0	IO			DIFFIO_L32p	P2
B2	VREFB2N0	IO			DIFFIO_L32n	P1
B2	VREFB2N0	IO			DIFFIO_L33p	R2
B2	VREFB2N0	IO			DIFFIO_L33n	R1
B2	VREFB2N1	IO				N5
B2	VREFB2N1	IO	DPCLK1		DIFFIO_L34p	P4
B2	VREFB2N1	IO			DIFFIO_L34n	P3
B2	VREFB2N1	IO			DIFFIO_L35p	U2
B2	VREFB2N1	IO			DIFFIO_L35n	U1
B2	VREFB2N1	IO			DIFFIO_L38p	V2
B2	VREFB2N1	IO			DIFFIO_L38n	V1
B2	VREFB2N1	IO	VREFB2N1			P5
B2	VREFB2N1	IO			DIFFIO_L41p	N6
B2	VREFB2N1	IO			DIFFIO_L41n	M7
B2	VREFB2N1	IO			DIFFIO_L42p	M8
B2	VREFB2N2	IO			DIFFIO_L42n	N8
B2	VREFB2N2	IO			DIFFIO_L44p	W2
B2	VREFB2N2	IO			DIFFIO_L44n	W1
B2	VREFB2N2	IO			DIFFIO_L45p	Y2

Pin Information for the Intel® Cyclone®10 10CL040 Device
Version 2019.03.29
Notes (1), (2)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B2	VREFB2N2	IO			DIFFIO_L45n	Y1
B2	VREFB2N2	IO	VREFB2N2			T3
B2	VREFB2N2	IO			DIFFIO_L49p	N7
B2	VREFB2N2	IO			DIFFIO_L49n	P7
B2	VREFB2N3	IO	RUP1			V4
B2	VREFB2N3	IO	RDN1			V3
B2	VREFB2N3	IO			DIFFIO_L52p	P6
B2	VREFB2N3	IO				T5
B2	VREFB2N3	IO	CDPCLK1			T4
B2	VREFB2N3	IO	VREFB2N3			R5
B2	VREFB2N3	IO				R6
B2	VREFB2N3	IO			DIFFIO_L53p	R7
B2	VREFB2N3	IO			DIFFIO_L53n	T7
B3	VREFB3N3	IO			DIFFIO_B1p	V6
B3	VREFB3N3	IO			DIFFIO_B1n	V5
B3	VREFB3N3	IO			DIFFIO_B3p	U7
B3	VREFB3N3	IO			DIFFIO_B3n	U8
B3	VREFB3N3	IO	VREFB3N3			Y4
B3	VREFB3N3	IO			DIFFIO_B4p	Y3
B3	VREFB3N3	IO	CDPCLK2		DIFFIO_B6p	Y6
B3	VREFB3N2	IO	PLL1_CLKOUTp			AA3
B3	VREFB3N2	IO	PLL1_CLKOUTn			AB3
B3	VREFB3N2	IO			DIFFIO_B7p	W6
B3	VREFB3N2	IO			DIFFIO_B7n	V7
B3	VREFB3N2	IO				AA4
B3	VREFB3N2	IO	VREFB3N2			AB4
B3	VREFB3N2	IO			DIFFIO_B8p	AA5
B3	VREFB3N2	IO			DIFFIO_B8n	AB5
B3	VREFB3N2	IO			DIFFIO_B11p	T8
B3	VREFB3N2	IO			DIFFIO_B11n	T9
B3	VREFB3N2	IO			DIFFIO_B12p	W7
B3	VREFB3N2	IO			DIFFIO_B12n	Y7
B3	VREFB3N2	IO			DIFFIO_B13p	U9
B3	VREFB3N2	IO			DIFFIO_B13n	V8
B3	VREFB3N2	IO				W8
B3	VREFB3N1	IO			DIFFIO_B14p	AA7

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B3	VREFB3N1	IO			DIFFIO_B14n	AB7
B3	VREFB3N1	IO				Y8
B3	VREFB3N1	IO			DIFFIO_B15p	T10
B3	VREFB3N1	IO			DIFFIO_B15n	T11
B3	VREFB3N1	IO	VREFB3N1			V9
B3	VREFB3N1	IO	DPCLK2		DIFFIO_B16p	V10
B3	VREFB3N1	IO			DIFFIO_B17n	U10
B3	VREFB3N1	IO			DIFFIO_B18p	AA8
B3	VREFB3N1	IO			DIFFIO_B18n	AB8
B3	VREFB3N1	IO			DIFFIO_B21p	AA9
B3	VREFB3N1	IO	DPCLK3		DIFFIO_B21n	AB9
B3	VREFB3N0	IO	VREFB3N0			U11
B3	VREFB3N0	IO			DIFFIO_B25n	V11
B3	VREFB3N0	IO			DIFFIO_B26p	W10
B3	VREFB3N0	IO			DIFFIO_B26n	Y10
B3	VREFB3N0	IO			DIFFIO_B27p	AA10
B3	VREFB3N0	IO			DIFFIO_B27n	AB10
B3	VREFB3N0	CLK15	DIFFCLK_6p			AA11
B3	VREFB3N0	CLK14	DIFFCLK_6n			AB11
B4	VREFB4N3	CLK13	DIFFCLK_7p			AA12
B4	VREFB4N3	CLK12	DIFFCLK_7n			AB12
B4	VREFB4N3	IO			DIFFIO_B28p	AA13
B4	VREFB4N3	IO			DIFFIO_B28n	AB13
B4	VREFB4N3	IO			DIFFIO_B29p	AA14
B4	VREFB4N3	IO			DIFFIO_B29n	AB14
B4	VREFB4N3	IO	VREFB4N3			V12
B4	VREFB4N3	IO			DIFFIO_B32p	W13
B4	VREFB4N3	IO	DPCLK4		DIFFIO_B32n	Y13
B4	VREFB4N3	IO			DIFFIO_B33p	AA15
B4	VREFB4N3	IO			DIFFIO_B33n	AB15
B4	VREFB4N3	IO			DIFFIO_B34p	U12
B4	VREFB4N2	IO			DIFFIO_B35p	AA16
B4	VREFB4N2	IO			DIFFIO_B35n	AB16
B4	VREFB4N2	IO			DIFFIO_B36p	T12
B4	VREFB4N2	IO			DIFFIO_B36n	T13
B4	VREFB4N2	IO	DPCLK5			V13

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B4	VREFB4N2	IO	VREFB4N2			W14
B4	VREFB4N2	IO			DIFFIO_B38n	U13
B4	VREFB4N2	IO			DIFFIO_B39p	V14
B4	VREFB4N2	IO			DIFFIO_B39n	U14
B4	VREFB4N2	IO			DIFFIO_B40p	U15
B4	VREFB4N2	IO			DIFFIO_B40n	V15
B4	VREFB4N1	IO			DIFFIO_B41n	W15
B4	VREFB4N1	IO			DIFFIO_B42p	T14
B4	VREFB4N1	IO			DIFFIO_B42n	T15
B4	VREFB4N1	IO				AB18
B4	VREFB4N1	IO	VREFB4N1			AA18
B4	VREFB4N1	IO	RUP2			AA19
B4	VREFB4N1	IO	RDN2			AB19
B4	VREFB4N0	IO			DIFFIO_B48p	W17
B4	VREFB4N0	IO	CDPCLK3		DIFFIO_B48n	Y17
B4	VREFB4N0	IO			DIFFIO_B49p	AA20
B4	VREFB4N0	IO			DIFFIO_B49n	AB20
B4	VREFB4N0	IO	VREFB4N0			V16
B4	VREFB4N0	IO			DIFFIO_B50p	U16
B4	VREFB4N0	IO			DIFFIO_B50n	U17
B4	VREFB4N0	IO	PLL4_CLKOUTp			T16
B4	VREFB4N0	IO	PLL4_CLKOUTn			R16
B4	VREFB4N0	IO			DIFFIO_B52p	R14
B4	VREFB4N0	IO			DIFFIO_B52n	R15
B5	VREFB5N3	IO			DIFFIO_R56n	AA22
B5	VREFB5N3	IO			DIFFIO_R56p	AA21
B5	VREFB5N3	IO	RUP3			T17
B5	VREFB5N3	IO	RDN3			T18
B5	VREFB5N3	IO	CDPCLK4			W20
B5	VREFB5N3	IO	VREFB5N3			W19
B5	VREFB5N3	IO			DIFFIO_R51n	Y22
B5	VREFB5N2	IO			DIFFIO_R51p	Y21
B5	VREFB5N2	IO			DIFFIO_R50n	U20
B5	VREFB5N2	IO			DIFFIO_R50p	U19
B5	VREFB5N2	IO			DIFFIO_R49n	W22
B5	VREFB5N2	IO			DIFFIO_R49p	W21

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B5	VREFB5N2	IO			DIFFIO_R46n	P15
B5	VREFB5N2	IO			DIFFIO_R46p	P16
B5	VREFB5N2	IO	VREFB5N2			R17
B5	VREFB5N2	IO				P17
B5	VREFB5N2	IO			DIFFIO_R45n	V22
B5	VREFB5N2	IO			DIFFIO_R45p	V21
B5	VREFB5N2	IO			DIFFIO_R44n	R20
B5	VREFB5N2	IO			DIFFIO_R43n	U22
B5	VREFB5N1	IO			DIFFIO_R43p	U21
B5	VREFB5N1	IO			DIFFIO_R42n	R18
B5	VREFB5N1	IO			DIFFIO_R42p	R19
B5	VREFB5N1	IO			DIFFIO_R40p	N16
B5	VREFB5N1	IO			DIFFIO_R39n	R22
B5	VREFB5N1	IO			DIFFIO_R39p	R21
B5	VREFB5N1	IO	VREFB5N1			P20
B5	VREFB5N1	IO			DIFFIO_R38n	P22
B5	VREFB5N1	IO			DIFFIO_R38p	P21
B5	VREFB5N1	IO			DIFFIO_R36n	N20
B5	VREFB5N1	IO			DIFFIO_R36p	N19
B5	VREFB5N0	IO			DIFFIO_R33n	N17
B5	VREFB5N0	IO	DPCLK6		DIFFIO_R33p	N18
B5	VREFB5N0	IO		DEV_OE	DIFFIO_R32n	N22
B5	VREFB5N0	IO		DEV_CLRn	DIFFIO_R32p	N21
B5	VREFB5N0	IO			DIFFIO_R31n	M22
B5	VREFB5N0	IO			DIFFIO_R31p	M21
B5	VREFB5N0	IO			DIFFIO_R30n	M20
B5	VREFB5N0	IO			DIFFIO_R30p	M19
B5	VREFB5N0	IO	VREFB5N0			M16
B5	VREFB5N0	CLK7	DIFFCLK_3n			T22
B5	VREFB5N0	CLK6	DIFFCLK_3p			T21
B6	VREFB6N3	CLK5	DIFFCLK_2n			G22
B6	VREFB6N3	CLK4	DIFFCLK_2p			G21
B6	VREFB6N3	CONF_DONE		CONF_DONE		M18
B6	VREFB6N3	MSEL0		MSEL0		M17
B6	VREFB6N3	MSEL1		MSEL1		L18
B6	VREFB6N3	MSEL2		MSEL2		L17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B6	VREFB6N3	MSEL3		MSEL3		K20
B6	VREFB6N3	IO		INIT_DONE	DIFFIO_R27n	L22
B6	VREFB6N3	IO		CRC_ERROR	DIFFIO_R27p	L21
B6	VREFB6N3	IO	VREFB6N3			K19
B6	VREFB6N3	IO		nCEO	DIFFIO_R24n	K22
B6	VREFB6N3	IO		CLKUSR	DIFFIO_R24p	K21
B6	VREFB6N3	IO	DPCLK7		DIFFIO_R23n	J22
B6	VREFB6N3	IO			DIFFIO_R23p	J21
B6	VREFB6N3	IO			DIFFIO_R22n	H22
B6	VREFB6N2	IO			DIFFIO_R22p	H21
B6	VREFB6N2	IO			DIFFIO_R20n	K17
B6	VREFB6N2	IO			DIFFIO_R20p	K18
B6	VREFB6N2	IO	VREFB6N2			J18
B6	VREFB6N2	IO			DIFFIO_R18n	F22
B6	VREFB6N2	IO			DIFFIO_R18p	F21
B6	VREFB6N1	IO			DIFFIO_R13n	H20
B6	VREFB6N1	IO			DIFFIO_R13p	H19
B6	VREFB6N1	IO			DIFFIO_R12n	E22
B6	VREFB6N1	IO			DIFFIO_R12p	E21
B6	VREFB6N1	IO	VREFB6N1			H18
B6	VREFB6N1	IO			DIFFIO_R10n	J17
B6	VREFB6N1	IO			DIFFIO_R10p	H16
B6	VREFB6N1	IO			DIFFIO_R9n	D22
B6	VREFB6N1	IO			DIFFIO_R9p	D21
B6	VREFB6N1	IO			DIFFIO_R8n	F20
B6	VREFB6N1	IO			DIFFIO_R8p	F19
B6	VREFB6N1	IO			DIFFIO_R7n	G18
B6	VREFB6N1	IO			DIFFIO_R7p	H17
B6	VREFB6N1	IO			DIFFIO_R6n	C22
B6	VREFB6N0	IO			DIFFIO_R6p	C21
B6	VREFB6N0	IO			DIFFIO_R5n	B22
B6	VREFB6N0	IO			DIFFIO_R5p	B21
B6	VREFB6N0	IO	CDPCLK5		DIFFIO_R4n	C20
B6	VREFB6N0	IO	VREFB6N0			D20
B6	VREFB6N0	IO			DIFFIO_R2n	F17
B6	VREFB6N0	IO			DIFFIO_R2p	G17

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B7	VREFB7N0	IO			DIFFIO_T51n	F16
B7	VREFB7N0	IO			DIFFIO_T51p	E16
B7	VREFB7N0	IO			DIFFIO_T50n	F15
B7	VREFB7N0	IO			DIFFIO_T50p	G16
B7	VREFB7N0	IO			DIFFIO_T49n	G15
B7	VREFB7N0	IO	CDPCLK6		DIFFIO_T49p	F14
B7	VREFB7N0	IO			DIFFIO_T48n	H15
B7	VREFB7N0	IO			DIFFIO_T48p	H14
B7	VREFB7N0	IO	VREFB7N0			D17
B7	VREFB7N0	IO			DIFFIO_T47n	C19
B7	VREFB7N0	IO			DIFFIO_T47p	D19
B7	VREFB7N0	IO	PLL2_CLKOUTn			A20
B7	VREFB7N1	IO	PLL2_CLKOUTp			B20
B7	VREFB7N1	IO			DIFFIO_T46p	C17
B7	VREFB7N1	IO	RUP4			B19
B7	VREFB7N1	IO	RDN4			A19
B7	VREFB7N1	IO			DIFFIO_T45n	A18
B7	VREFB7N1	IO			DIFFIO_T45p	B18
B7	VREFB7N1	IO	VREFB7N1			D15
B7	VREFB7N1	IO			DIFFIO_T44n	E15
B7	VREFB7N1	IO			DIFFIO_T44p	G14
B7	VREFB7N1	IO			DIFFIO_T42n	G13
B7	VREFB7N1	IO			DIFFIO_T41n	A17
B7	VREFB7N2	IO			DIFFIO_T41p	B17
B7	VREFB7N2	IO			DIFFIO_T40n	A16
B7	VREFB7N2	IO			DIFFIO_T40p	B16
B7	VREFB7N2	IO	VREFB7N2			C15
B7	VREFB7N2	IO			DIFFIO_T38n	E14
B7	VREFB7N2	IO	DPCLK8		DIFFIO_T37p	F13
B7	VREFB7N2	IO			DIFFIO_T36n	A15
B7	VREFB7N3	IO			DIFFIO_T36p	B15
B7	VREFB7N3	IO			DIFFIO_T35n	C13
B7	VREFB7N3	IO			DIFFIO_T35p	D13
B7	VREFB7N3	IO	VREFB7N3			E13
B7	VREFB7N3	IO			DIFFIO_T31n	A14
B7	VREFB7N3	IO			DIFFIO_T31p	B14

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B7	VREFB7N3	IO			DIFFIO_T29n	A13
B7	VREFB7N3	IO	DPCLK9		DIFFIO_T29p	B13
B7	VREFB7N3	IO			DIFFIO_T28p	E12
B7	VREFB7N3	IO			DIFFIO_T27n	E11
B7	VREFB7N3	IO			DIFFIO_T27p	F11
B7	VREFB7N3	CLK8	DIFFCLK_5n			A12
B7	VREFB7N3	CLK9	DIFFCLK_5p			B12
B8	VREFB8N0	CLK10	DIFFCLK_4n			A11
B8	VREFB8N0	CLK11	DIFFCLK_4p			B11
B8	VREFB8N0	IO			DIFFIO_T26n	D10
B8	VREFB8N0	IO			DIFFIO_T26p	E10
B8	VREFB8N0	IO			DIFFIO_T25n	A10
B8	VREFB8N0	IO			DIFFIO_T25p	B10
B8	VREFB8N0	IO			DIFFIO_T24n	A9
B8	VREFB8N0	IO	DPCLK10		DIFFIO_T24p	B9
B8	VREFB8N0	IO	VREFB8N0			C10
B8	VREFB8N0	IO			DIFFIO_T22n	G11
B8	VREFB8N0	IO		DATA2	DIFFIO_T20n	A8
B8	VREFB8N1	IO		DATA3	DIFFIO_T20p	B8
B8	VREFB8N1	IO			DIFFIO_T19n	A7
B8	VREFB8N1	IO		DATA4	DIFFIO_T19p	B7
B8	VREFB8N1	IO			DIFFIO_T18n	A6
B8	VREFB8N1	IO			DIFFIO_T18p	B6
B8	VREFB8N1	IO	VREFB8N1			E9
B8	VREFB8N1	IO	DPCLK11		DIFFIO_T16n	C8
B8	VREFB8N1	IO			DIFFIO_T16p	C7
B8	VREFB8N1	IO			DIFFIO_T14n	H11
B8	VREFB8N1	IO			DIFFIO_T14p	H10
B8	VREFB8N2	IO		DATA5	DIFFIO_T11p	A5
B8	VREFB8N2	IO	VREFB8N2			B5
B8	VREFB8N2	IO			DIFFIO_T8n	G10
B8	VREFB8N2	IO		DATA6	DIFFIO_T8p	F10
B8	VREFB8N2	IO		DATA7	DIFFIO_T7n	C6
B8	VREFB8N2	IO			DIFFIO_T7p	D7
B8	VREFB8N2	IO			DIFFIO_T6n	A4
B8	VREFB8N3	IO			DIFFIO_T6p	B4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
B8	VREFB8N3	IO			DIFFIO_T5n	F8
B8	VREFB8N3	IO			DIFFIO_T5p	G8
B8	VREFB8N3	IO			DIFFIO_T4n	A3
B8	VREFB8N3	IO			DIFFIO_T4p	B3
B8	VREFB8N3	IO	VREFB8N3			D6
B8	VREFB8N3	IO				E7
B8	VREFB8N3	IO			DIFFIO_T3n	C3
B8	VREFB8N3	IO	CDPCLK7		DIFFIO_T3p	C4
B8	VREFB8N3	IO			DIFFIO_T1n	F7
B8	VREFB8N3	IO			DIFFIO_T1p	G7
B8	VREFB8N3	IO				F9
B8	VREFB8N3	IO	PLL3_CLKOUTn			E6
B8	VREFB8N3	IO	PLL3_CLKOUTp			E5
B8	VREFB8N3	IO				G9
		GND				L10
		GND				L11
		GND				M10
		GND				M11
		GND				L12
		GND				L13
		GND				M12
		GND				M13
		GND				N11
		GND				K11
		GND				N12
		GND				K12
		GND				K13
		GND				N13
		GND				N10
		GND				K10
		GND				J9
		GND				F12
		GND				H12
		GND				H13
		GND				J15
		GND				K16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		GND				L15
		GND				N15
		GND				R13
		GND				R11
		GND				R9
		GND				P8
		GND				A1
		GND				C5
		GND				C9
		GND				C11
		GND				C12
		GND				C14
		GND				C16
		GND				A22
		GND				E20
		GND				G20
		GND				L20
		GND				P19
		GND				V20
		GND				Y20
		GND				AB22
		GND				Y18
		GND				Y16
		GND				Y12
		GND				Y11
		GND				Y9
		GND				Y5
		GND				AB1
		GND				N3
		GND				U3
		GND				W3
		GND				D3
		GND				F3
		GND				K3
		GND				AA2
		GND				H3

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		GND				R3
		GND				AB6
		GND				Y15
		GND				T20
		GND				J19
		GND				C18
		GND				D8
		GND				AA1
		GND				AA17
		GND				AB17
		GND				C1
		GND				C2
		GNDA1				U5
		GNDA2				E18
		GNDA3				F5
		GNDA4				V18
		VCCD_PLL1				U6
		VCCD_PLL2				E17
		VCCD_PLL3				F6
		VCCD_PLL4				V17
		VCCIO1				D4
		VCCIO1				F4
		VCCIO1				K4
		VCCIO1				H4
		VCCIO2				N4
		VCCIO2				U4
		VCCIO2				W4
		VCCIO2				R4
		VCCIO3				AB2
		VCCIO3				W5
		VCCIO3				W9
		VCCIO3				W11
		VCCIO3				AA6
		VCCIO4				AB21
		VCCIO4				W12
		VCCIO4				W16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		VCCIO4				W18
		VCCIO4				Y14
		VCCIO5				P18
		VCCIO5				V19
		VCCIO5				Y19
		VCCIO5				T19
		VCCIO6				E19
		VCCIO6				G19
		VCCIO6				L19
		VCCIO6				J20
		VCCIO7				A21
		VCCIO7				D12
		VCCIO7				D14
		VCCIO7				D16
		VCCIO7				D18
		VCCIO8				A2
		VCCIO8				D5
		VCCIO8				D9
		VCCIO8				D11
		VCCIO8				E8
		VCCA1				T6
		VCCA2				F18
		VCCA3				G6
		VCCA4				U18
		VCCINT				J11
		VCCINT				J12
		VCCINT				L14
		VCCINT				M14
		VCCINT				P11
		VCCINT				P12
		VCCINT				L9
		VCCINT				M9
		VCCINT				J13
		VCCINT				J14
		VCCINT				K14
		VCCINT				J10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Emulated LVDS Output Channel	U484
		VCCINT				K9
		VCCINT				N9
		VCCINT				P9
		VCCINT				P10
		VCCINT				P13
		VCCINT				P14
		VCCINT				N14
		VCCINT				J16
		VCCINT				K15
		VCCINT				L16
		VCCINT				M15
		VCCINT				R12
		VCCINT				R10
		VCCINT				R8
		VCCINT				H9
		VCCINT				G12

Notes:

(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.

(2) For more information about pin definition and pin connection guidelines, refer to the Cyclone 10 LP Device Family Pin Connection Guidelines.

Date	Version	Changes
February 2017	2017.02.13	Initial release.
May 2017	2017.05.19	Updated description for the Configuration pins.
March 2019	2019.03.29	Added DPCLK and CDPCLK support in optional pin function column.