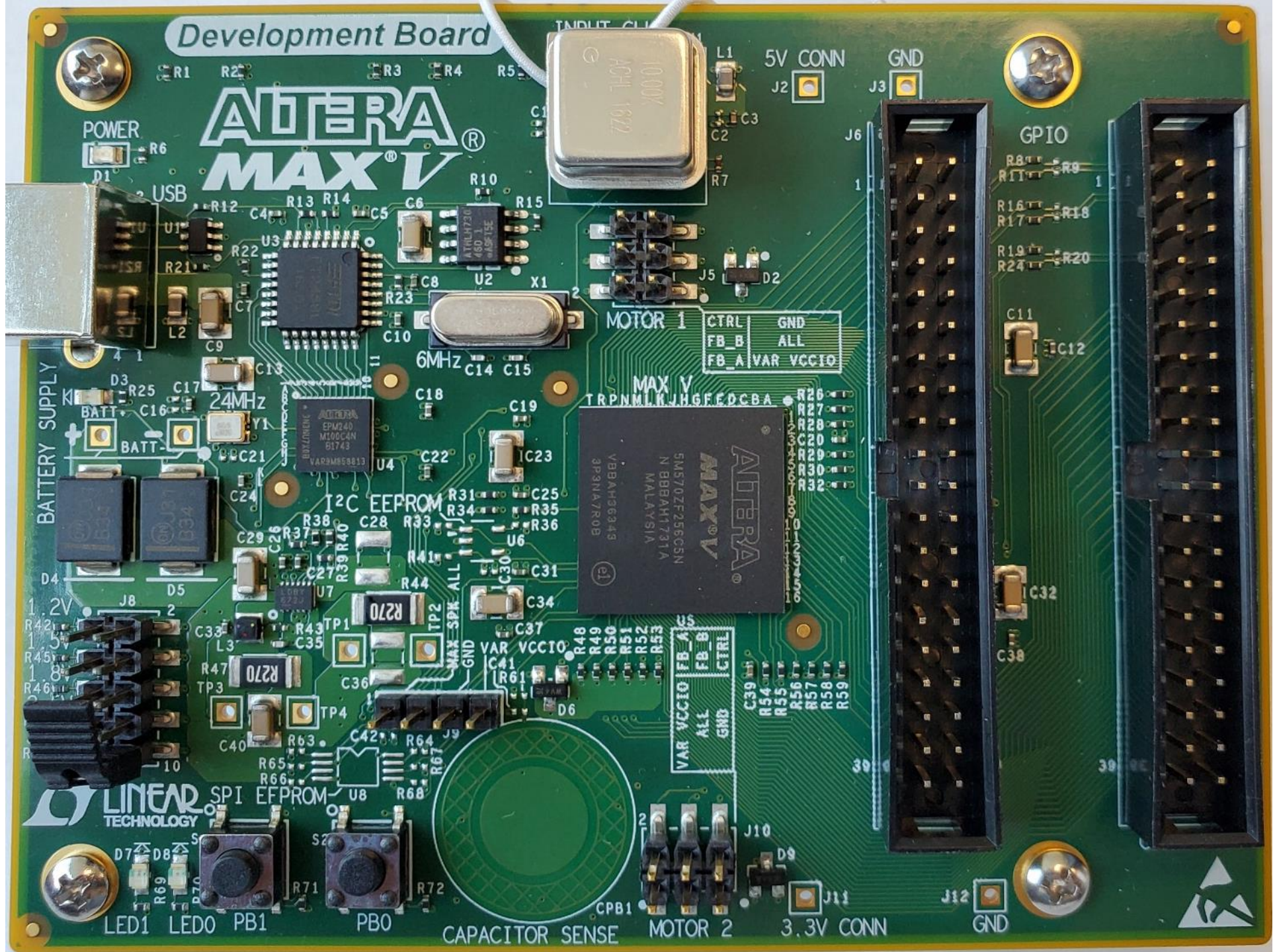
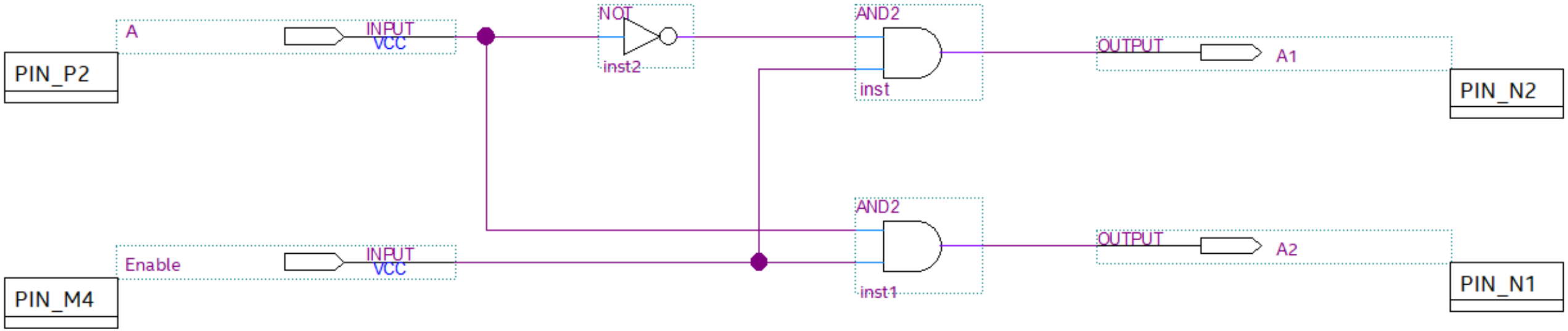

Development Board
ALTERA
MAX V
POWER
USB
BATTERY SUPPLY
BATT+
BATT-
24MHz
6MHz
I2C EEPROM
SPI EEPROM
LINEAR TECHNOLOGY
5V CONN
GND
GPIO
MOTOR 1
CTRL
GND
FB_B
ALL
FB_A
VAR VCCIO
MAX V
TRPNMLKJHGFEDCBA
1.2V
1.5V
1.8V
VAR VCCIO
MAX SPK
ALL
GND
LED1
LED0
PB1
PB0
CAPACITOR SENSE
MOTOR 2
3.3V CONN
GND

- **Enable** input when low both outputs, **A1** and **A2**, will always be low regards what the input state is for input **A**.
- When the **Enable** input is high output **A1** will be the invert of **Input** and output **A2** will be the same as the **Input**.



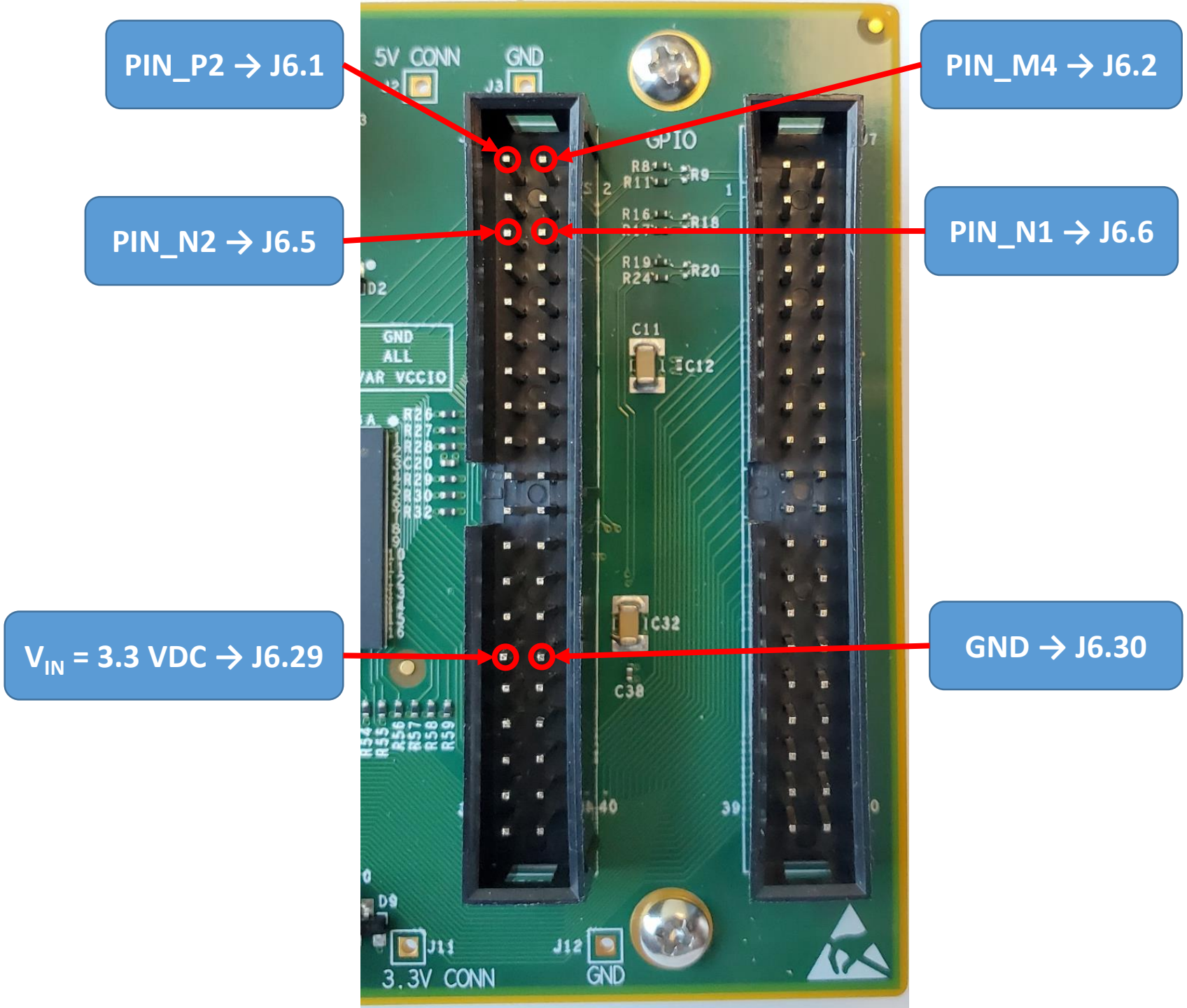
Node Name	Direction	Location	I/O Bank	Fitter Location	I/O Standard	Reserved	Current Strength	Differential Pair	Strict Preservation
in A	Input	PIN_P2	1	PIN_P2	3.3-V LVTTL		16mA (default)		
out A1	Output	PIN_N2	1	PIN_N2	3.3-V LVTTL		16mA (default)		
out A2	Output	PIN_N1	1	PIN_N1	3.3-V LVTTL		16mA (default)		
in Enable	Input	PIN_M4	1	PIN_M4	3.3-V LVTTL		16mA (default)		

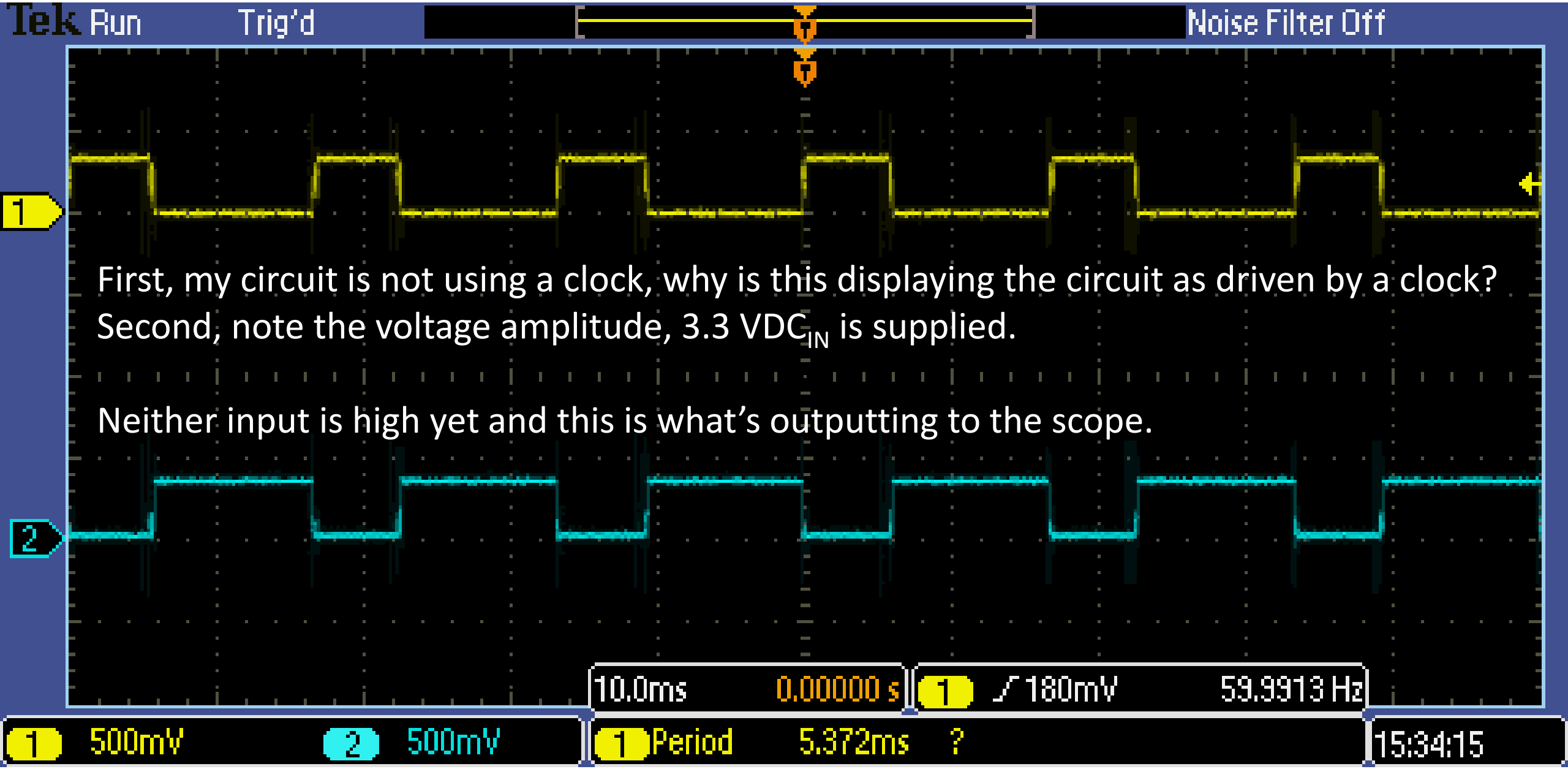
Table 2–8. GPIO Header A Schematic Signal Names and Functions (Part 1 of 2)

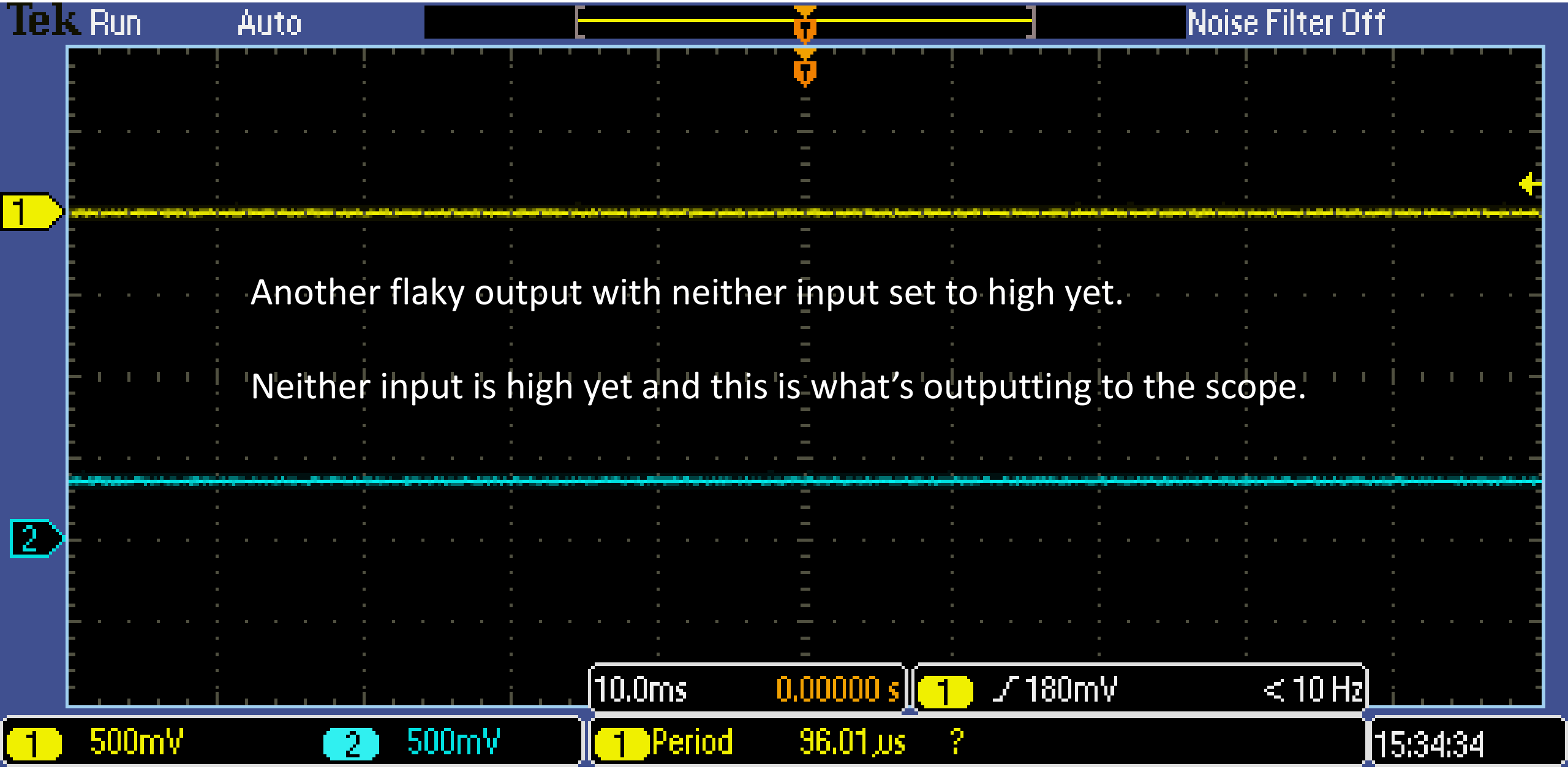
Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J6.1	GPIO connector A pin	AGPIO_1		P2
J6.2	GPIO connector A pin	AGPIO_2		M4
J6.3	GPIO connector A pin	AGPIO_3		L4
J6.4	GPIO connector A pin	AGPIO_4		N3
J6.5	GPIO connector A pin	AGPIO_5	3.3-V	N2
J6.6	GPIO connector A pin	AGPIO_6		N1
J6.7	GPIO connector A pin	AGPIO_7		M3
J6.8	GPIO connector A pin	AGPIO_8		M2
J6.9	GPIO connector A pin	AGPIO_9		M1
J6.10	GPIO connector A pin	AGPIO_10		L3
J6.11	Power	5VIN_CONN	5-V	—
J6.12	Ground	GND	—	—
J6.13	GPIO connector A pin	AGPIO_11		L1
J6.14	GPIO connector A pin	AGPIO_12		L2
J6.15	GPIO connector A pin	AGPIO_13		K2
J6.16	GPIO connector A pin	AGPIO_14		K3
J6.17	GPIO connector A pin	AGPIO_15		J3
J6.18	GPIO connector A pin	AGPIO_16		K1
J6.19	GPIO connector A pin	AGPIO_17		J1
J6.20	GPIO connector A pin	AGPIO_18		J2
J6.21	GPIO connector A pin	AGPIO_19	3.3-V	H2
J6.22	GPIO connector A pin	AGPIO_20		H3
J6.23	GPIO connector A pin	AGPIO_21		G3
J6.24	GPIO connector A pin	AGPIO_22		H1
J6.25	GPIO connector A pin	AGPIO_23		G1
J6.26	GPIO connector A pin	AGPIO_24		G2
J6.27	GPIO connector A pin	AGPIO_25		F2
J6.28	GPIO connector A pin	AGPIO_26		F3
J6.29	Power	3.3VIN_CONN		—
J6.30	Ground	GND	—	—

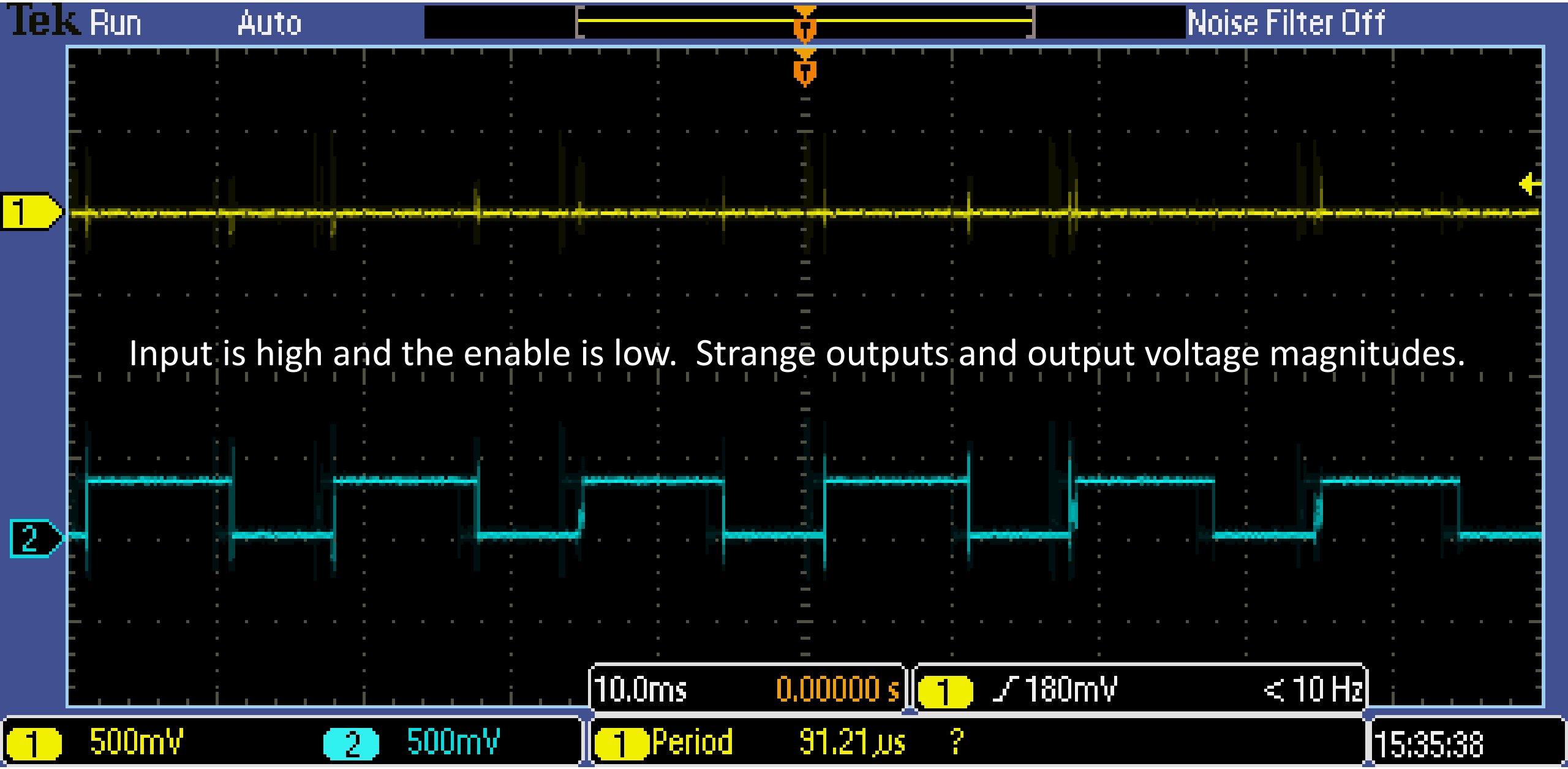
Table 2–8. GPIO Header A Schematic Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	MAX V CPLD Device Pin Number
J6.31	GPIO connector A pin	AGPIO_27	3.3-V	E3
J6.32	GPIO connector A pin	AGPIO_28		F1
J6.33	GPIO connector A pin	AGPIO_29		E1
J6.34	GPIO connector A pin	AGPIO_30		E2
J6.35	GPIO connector A pin	AGPIO_31		D2
J6.36	GPIO connector A pin	AGPIO_32		D3
J6.37	GPIO connector A pin	AGPIO_33		C3
J6.38	GPIO connector A pin	AGPIO_34		D1
J6.39	GPIO connector A pin	AGPIO_35		E4
J6.40	GPIO connector A pin	AGPIO_36		C2


PIN_P2 → J6.1
PIN_M4 → J6.2
PIN_N2 → J6.5
PIN_N1 → J6.6
V_{IN} = 3.3 VDC → J6.29
GND → J6.30
5V CONN
GND
GPIO
3.3V CONN
GND


Tek Run Trig'd Noise Filter Off
1
First, my circuit is not using a clock, why is this displaying the circuit as driven by a clock?
Second, note the voltage amplitude, 3.3 VDC$_{IN}$ is supplied.
Neither input is high yet and this is what's outputting to the scope.
2
10.0ms 0.00000 s
1 ∕ 180mV 59.9913 Hz
1 500mV 2 500mV
1 Period 5.372ms ?
15:34:15


Tek Run Auto Noise Filter Off
Another flaky output with neither input set to high yet.
Neither input is high yet and this is what's outputting to the scope.
10.0ms 0.00000 s
1 ∕ 180mV < 10 Hz
1 500mV 2 500mV
1 Period 96.01 µs ?
15:34:34


Tek Run Auto
Noise Filter Off
1
2
Input is high and the enable is low. Strange outputs and output voltage magnitudes.
10.0ms 0.00000 s
1 180mV
< 10 Hz
1 500mV
2 500mV
1 Period 91.21 µs ?
15:35:38

With the correct input and enable bit patterns this should be the output pattern. Alternating flip-flopping output states. Not the case and note again the output amplitude. Not sure how this correct output came about for state-changes and has not been reproducible.