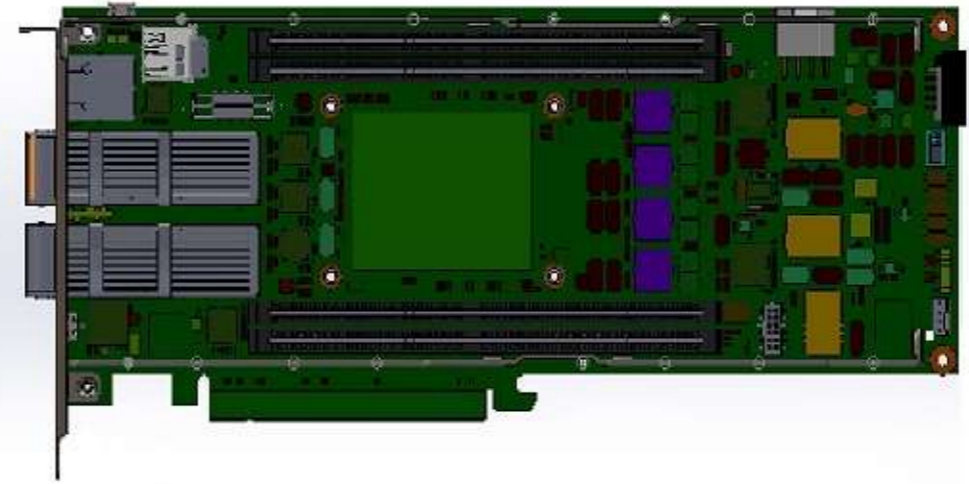


REV	DATE	PAGES	DESCRIPTION
A	11 / 12 / 2017	All	Initial

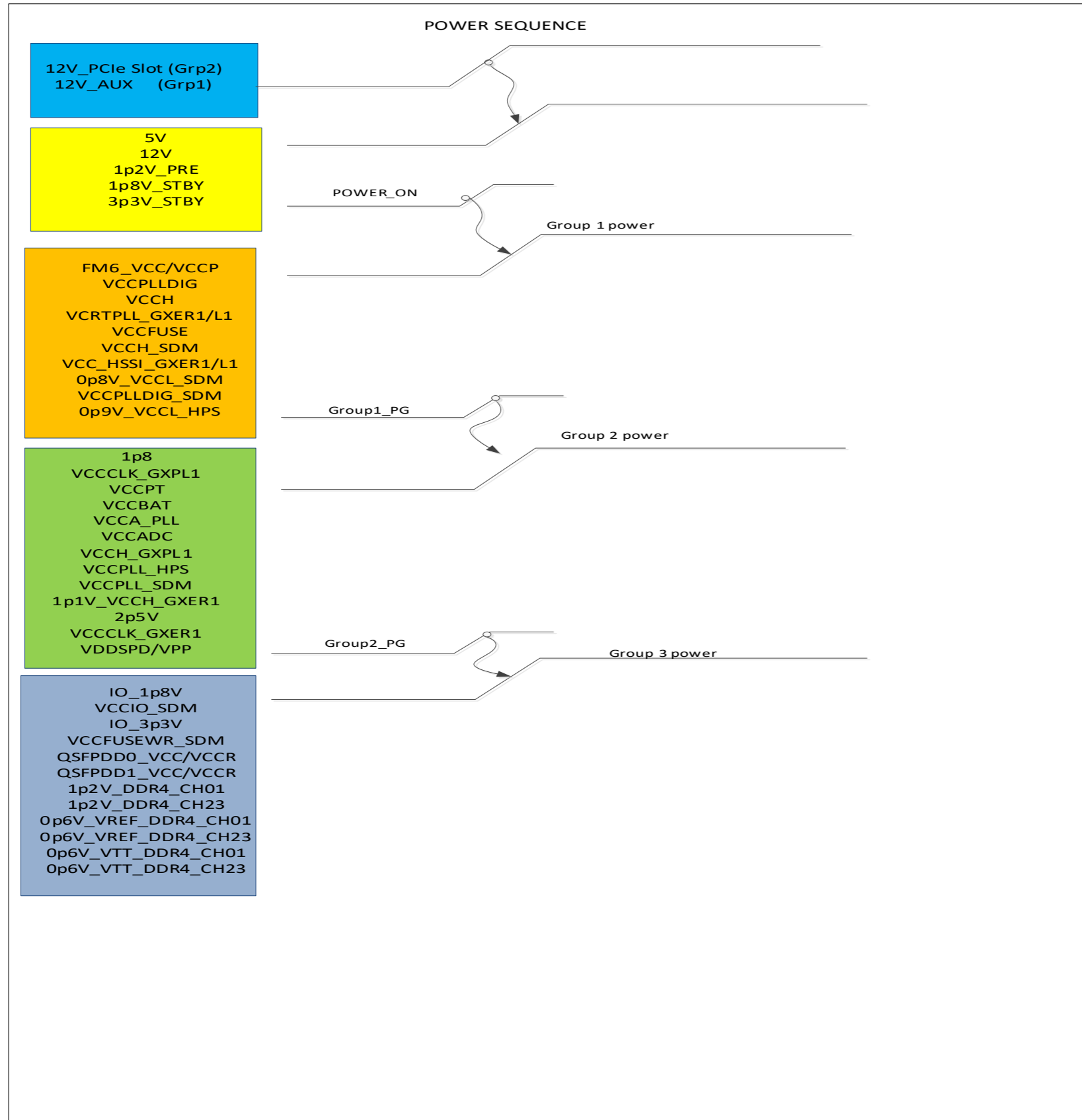
PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Rev. History	39	Clock 2
2	Block Diagram	40	I2C and PMBUS
3	Power Tree	41	LEDs and PushButtons
4	Power Sequence Timing	42	LEDs for QSFPDD
5	Clock Tree Diagram	43	MAX10 - USB Blaster II -1
6	I2C Diagram	44	MAX10 - USB Blaster II -2
7	JTAG Diagram	45	BLANK
8	DDR4_DDR4 Pin Map	46	MAX10 Power Control -1
9	DDR4/DDRT Single DIMM CH0	47	MAX10 Power Control -2
10	FPGA BANK 3A	48	Power inputs
11	FPGA BANK 3B	49	PWR 12V to 5V
12	DDR4 Single DIMM CH1	50	PWR 12V to 3.3V
13	FPGA BANK 3C	51	PWR VCC - 1
14	FPGA BANK 3D	52	PWR VCC - 2
15	DDR4/DDRT Single DIMM CH2	53	PWR 1p8V
16	FPGA BANK 2A	54	PWR - 0p8V_VCCL_SDM
17	FPGA BANK 2B	55	PWR - 0p8V_VCCL_HPS
18	DDR4/DDRT Single DIMM CH3	56	BLANK
19	FPGA BANK 2C	57	PWR - IO_1p8V
20	FPGA BANK 2D	58	PWR - VCC_HSSI
21	FPGA BANK 9A	59	PWR - 1p2V_VCCR
22	FPGA BANK 10A	60	PWR - 1p2V_DDR4_CH01
23	QSFPDD0	61	PWR - 1p2V_DDR4_CH23
24	QSFPDD1	62	PWR - 0p6V_VTT/VREF
25	PCIe End Point Edge Connector	63	PWR - 2p5V
26	FPGA Config SDM	64	PWR - 1p1V_VCCH_GXER1
27	FPGA BANK HPS	65	PWR - Decoupling Caps 1
28	ETH PHY	66	PWR - Decoupling Caps 2
29	UART		
30	Micro SD		
31	eMMC		
32	FPGA BANK NC DNU		
33	FPGA Power 1		
34	FPGA Power 2		
35	FPGA Gnd 1		
36	FPGA Gnd 2		
37	FPGA Gnd 3		
38	Clock 1		

Board BOM : K57065 Rev01



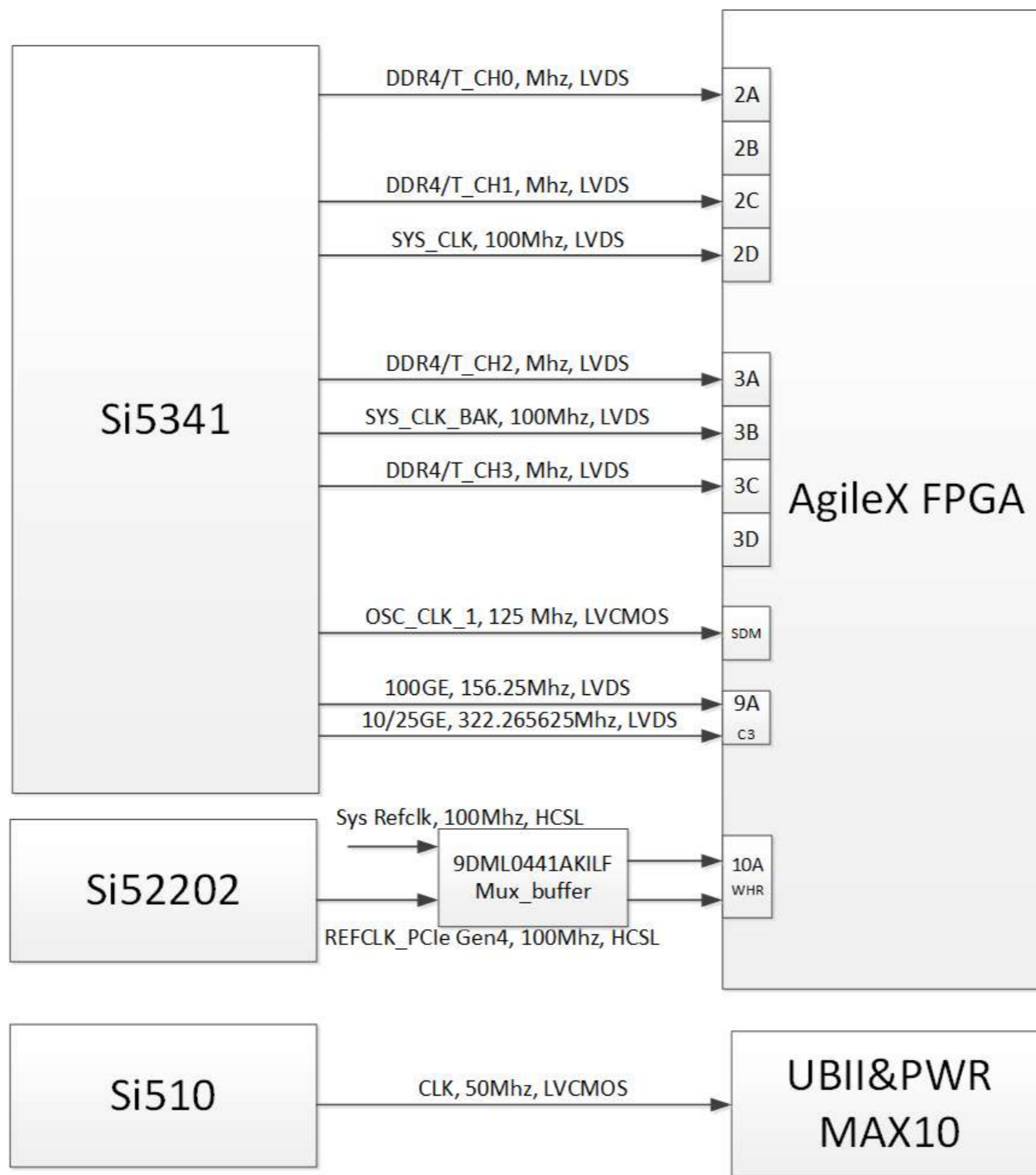
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Thursday, May 07, 2020	Sheet 1 of 66

Power Sequence Timing



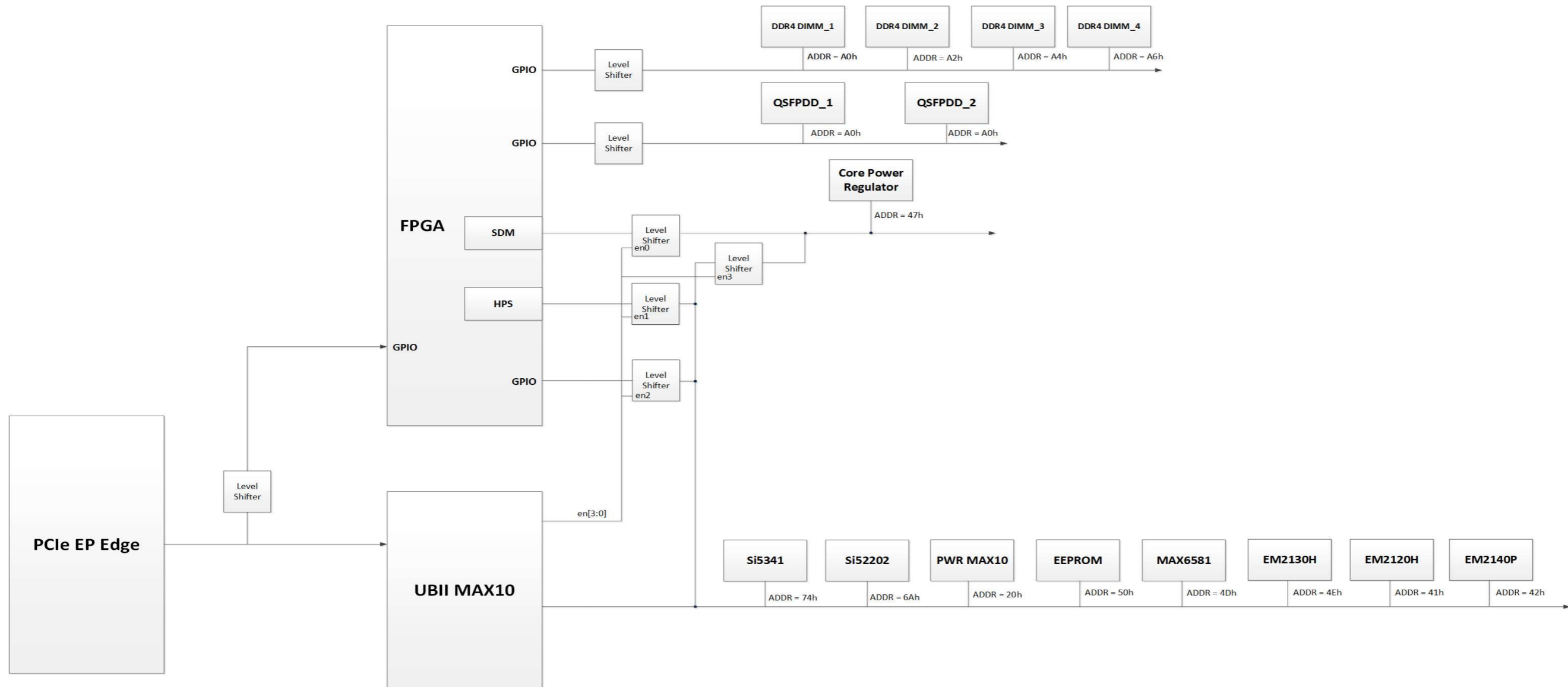
Intel Corporation, 101 Innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 4 of 66

Clock Tree



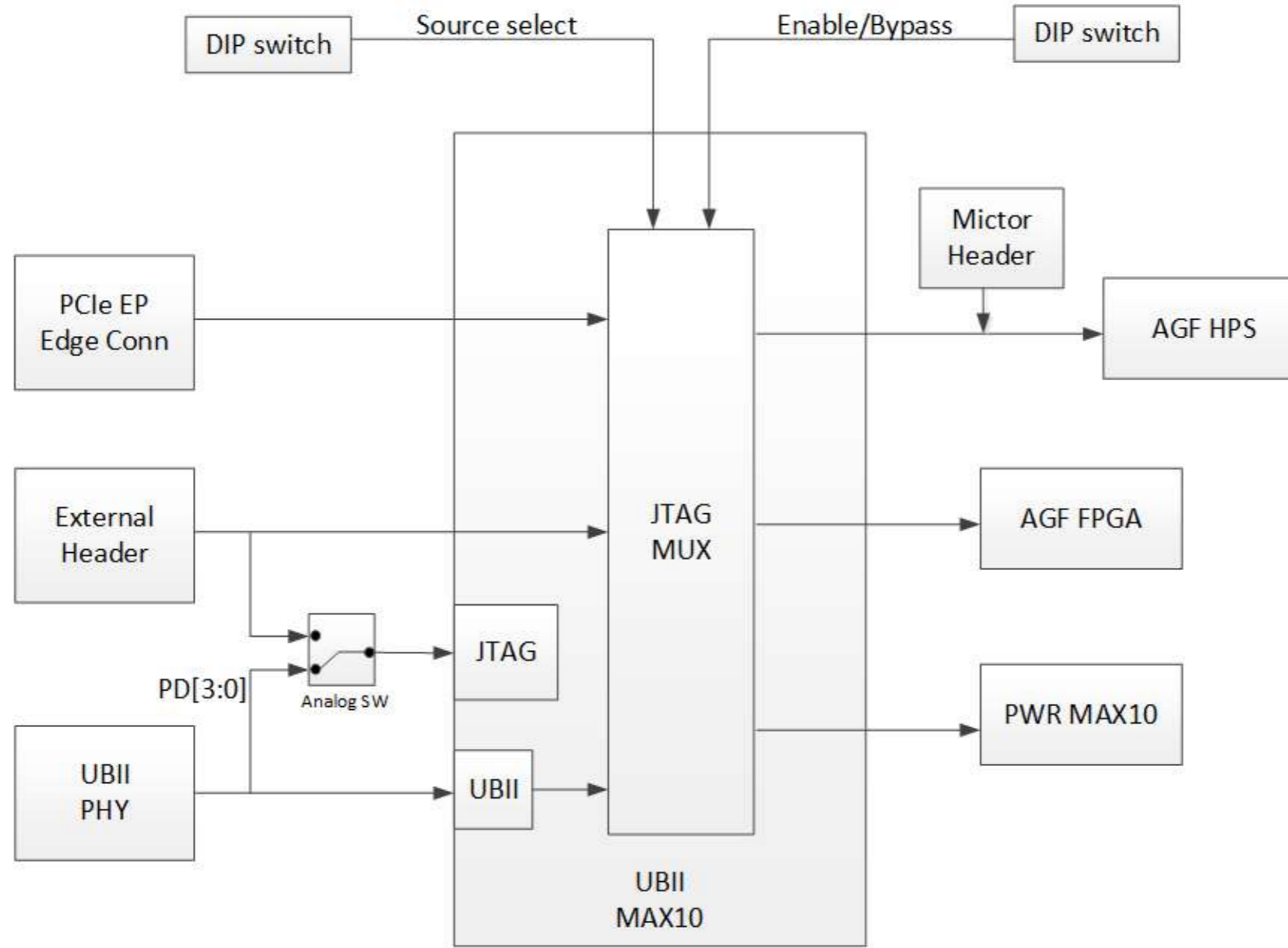
Intel Corporation, 101 Innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 5 of 66

I2C Diagram



Intel Corporation, 101 Innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 6 of 66

JTAG Block Diagram



Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 7 of 66

DDR4/DDR-T DIMM Pin Map

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	12V	145	12V	38	DQ24	182	VSS	75	CLK0#	219	CLK1#	108	DQ40	252	VSS
2	VSS	146	VREFCA	39	VSS	183	DQ25	76	VDD	220	VDD	109	VSS	253	DQ41
3	DQ4	147	VSS	40	DQS12	184	VSS	77	VTT	221	VTT	110	DQS14	254	VSS
4	VSS	148	DQ5	41	DQS12#	185	DQS3#	KEY				111	DQS14#	255	DQS5#
5	DQ0	149	VSS	42	VSS	186	DQS3					112	VSS	256	DQS5
6	VSS	150	DQ1	43	DQ30	187	VSS					113	DQ46	257	VSS
7	DQS0	151	VSS	44	VSS	188	DQ31					114	VSS	258	DQ47
8	DQSQ#	152	DQS0#	45	DQ26	189	VSS	78	EVENT	222	PARITY	115	DQ42	259	VSS
9	VSS	153	DQS0	46	VSS	190	DQ27	79	A0	223	VDD	116	VSS	260	DQ43
10	DQ6	154	VSS	47	CB4	191	VSS	80	VDD	224	BA1	117	DQ52	261	VSS
11	VSS	155	DQ7	48	VSS	192	CB5	81	BA0	225	A10	118	VSS	262	DQ53
12	DQ2	156	VSS	49	CB0	193	VSS	82	RAS#/A16	226	VDD	119	DQ48	263	VSS
13	VSS	157	DQ3	50	VSS	194	CB1	83	VDD	227	RFU	120	VSS	264	DQ49
14	DQ12	158	VSS	51	DQS17	195	VSS	84	CS0#	228	WE#/A14	121	DQS15	265	VSS
15	VSS	159	DQ13	52	DQS17#	196	DQS8#	85	VDD	229	VDD	122	DQS15#	266	DQS6#
16	DQ8	160	VSS	53	VSS	197	DQS8	86	CAS#/A15	230	SAVE#	123	VSS	267	DQS6
17	VSS	161	DQ9	54	CB6	198	VSS	87	ODT0	231	VDD	124	DQ54	268	VSS
18	DQS10	162	VSS	55	VSS	199	CB7	88	VDD	232	A13	125	VSS	269	DQ55
19	DQS10#	163	DQS1#	56	CB2	200	VSS	89	CS1#	233	VDD	126	DQ50	270	VSS
20	VSS	164	DQS1	57	VSS	201	CB3	90	VDD	234	A17	127	VSS	271	DQ51
21	DQ14	165	VSS	58	RESET#	202	VSS	91	ODT1	235	C2	128	DQ60	272	VSS
22	VSS	166	DQ15	59	VDD	203	CKE1	92	VDD	236	VDD	129	VSS	273	DQ61
23	DQ10	167	VSS	60	CKE0	204	VDD	93	C0	237	C1	130	DQ56	274	VSS
24	VSS	168	DQ11	61	VDD	205	RFU	94	VSS	238	SA2	131	VSS	275	DQ57
25	DQ20	169	VSS	62	ACT#	206	VDD	95	DQ36	239	VSS	132	DQS16	276	VSS
26	VSS	170	DQ21	63	BG0	207	BG1	96	VSS	240	DQ37	133	DQS16#	277	DQS7#
27	DQ16	171	VSS	64	VDD	208	ALERT#	97	DQ32	241	VSS	134	VSS	278	DQS7
28	VSS	172	DQ17	65	A12	209	VDD	98	VSS	242	DQ33	135	DQ62	279	VSS
29	DQS11	173	VSS	66	A9	210	A11	99	DQS13	243	VSS	136	VSS	280	DQ63
30	DQS11#	174	DQS2#	67	VDD	211	A7	100	DQS13#	244	DQS4#	137	DQ58	281	VSS
31	VSS	175	DQS2	68	A8	212	VDD	101	VSS	245	DQS4	138	VSS	282	DQ59
32	DQ22	176	VSS	69	A6	213	A5	102	DQ38	246	VSS	139	SA0	283	VSS
33	VSS	177	DQ23	70	VDD	214	A4	103	VSS	247	DQ39	140	SA1	284	VDDSPD
34	DQ18	178	VSS	71	A3	215	VDD	104	DQ34	248	VSS	141	SCL	285	SDA
35	VSS	179	DQ19	72	A1	216	A2	105	VSS	249	DQ35	142	VPP	286	VPP
36	DQ28	180	VSS	73	VDD	217	VDD	106	DQ44	250	VSS	143	VPP	287	VPP
37	VSS	181	DQ29	74	CLK0	218	CLK1	107	VSS	251	DQ45	144	RFU	288	VPP

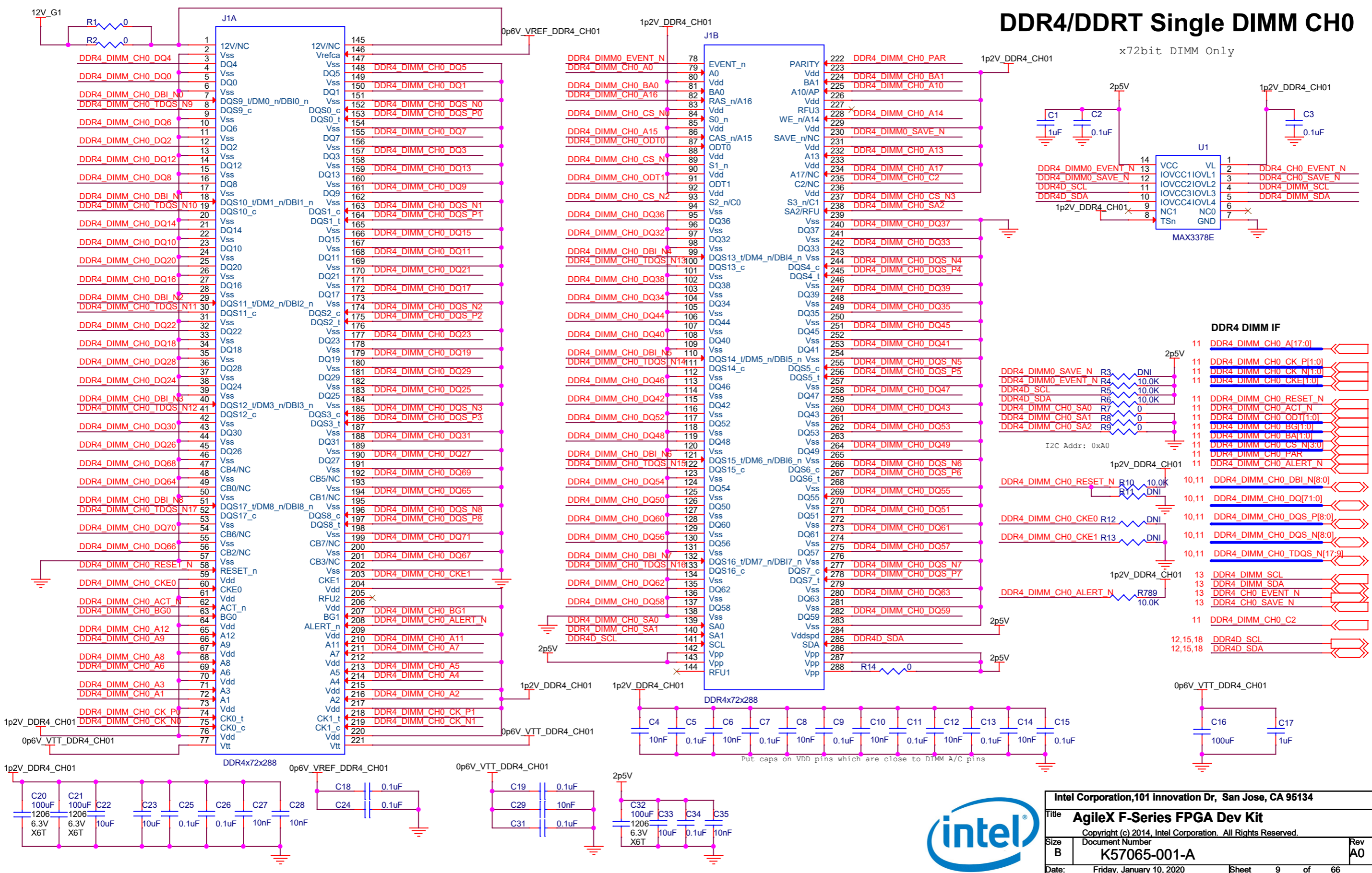
DDR-T DIMM Pin Map is Identical to standard DDR4 DIMM Pin Map except the DDR-T protocol repurposes five of these pins:

- CS1# (pin 89) : Grant, GNT# <0> Input
- CKE1 (pin 203) : Request, REQ# <0> Output
- ODT1 (pin 91) : Error, ERR# Output
- CLK1 (pin 218):Early Read ID, ERID<0> Output
- CLK1# (pin 219):Early Read ID, ERID<1> Output



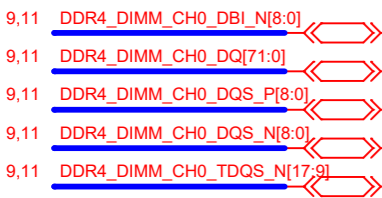
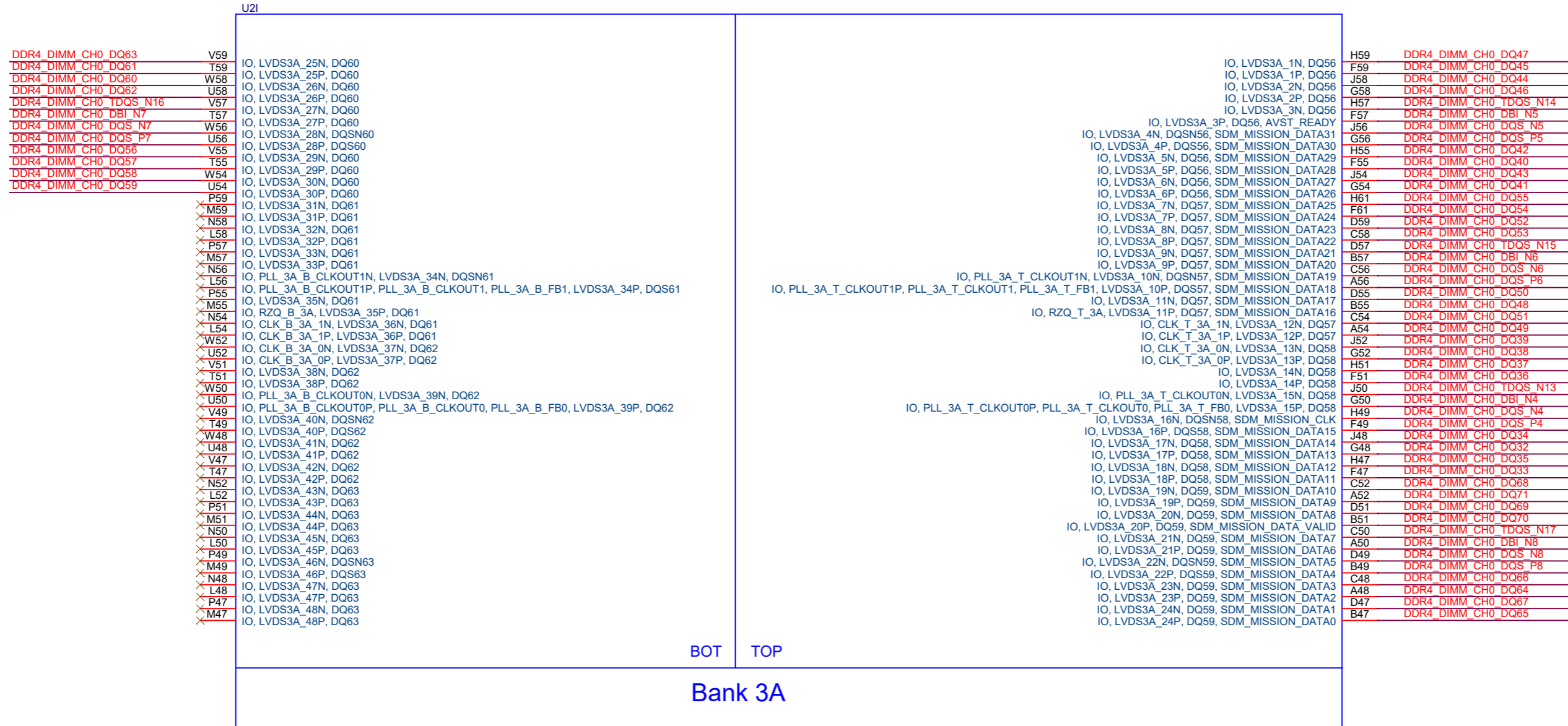
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Rev
Friday, January 10, 2020	A0
Sheet 8 of 66	

DDR4/DDRT Single DIMM CH0



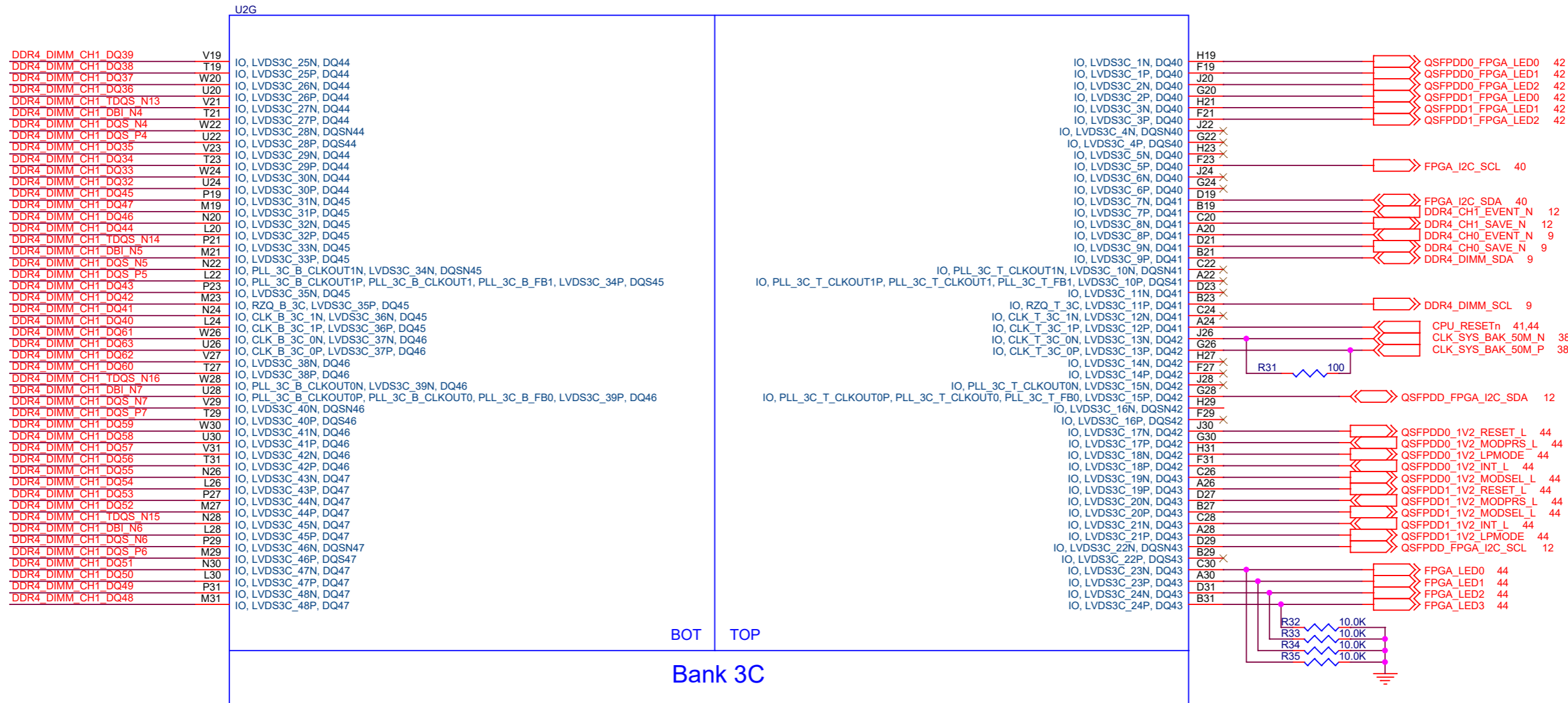
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	9 of 66
Rev	A0

DDR4/T CH0 INTERFACE -- FPGA SIDE 3A



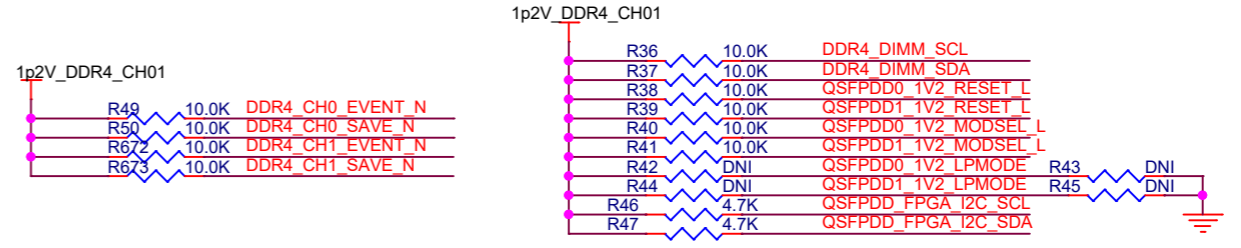
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	10 of 66
Rev	A0

DDR4 DIMM CH1 Interface - FPGA Side 3C



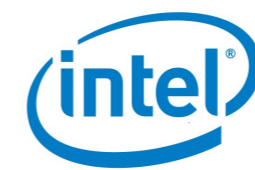
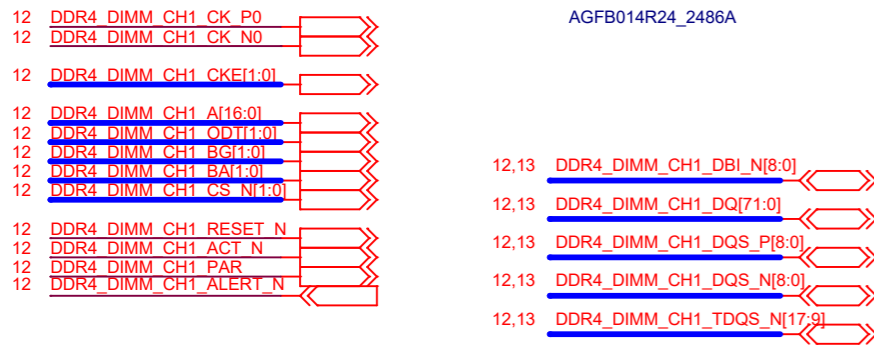
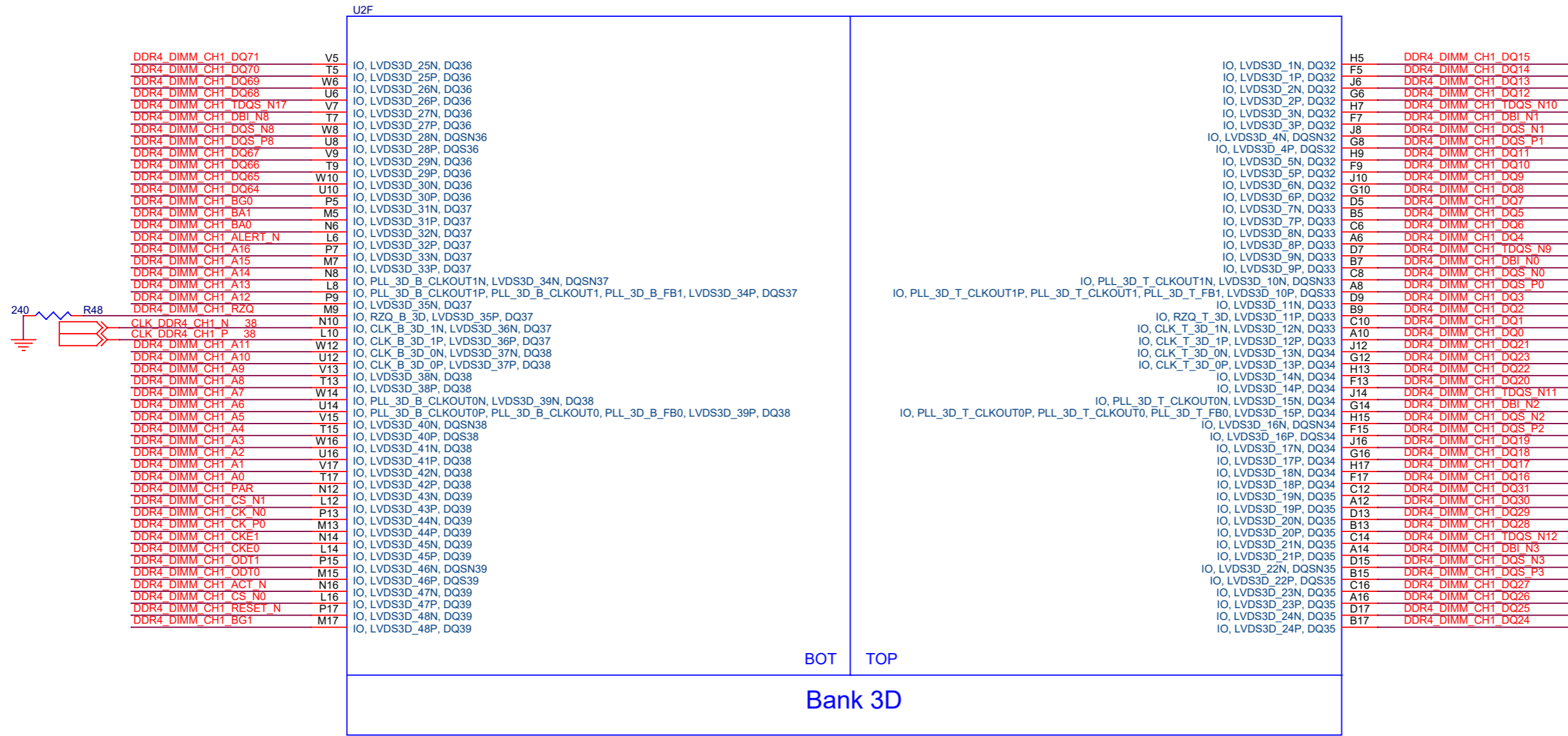
AGFB014R24_2486A

- 12,14 DDR4_DIMM_CH1_DBI_N[8:0]
- 12,14 DDR4_DIMM_CH1_DQ[71:0]
- 12,14 DDR4_DIMM_CH1_DQS_P[8:0]
- 12,14 DDR4_DIMM_CH1_DQS_N[8:0]
- 12,14 DDR4_DIMM_CH1_TDQS_N[17:9]



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	13 of 66
Rev	A0

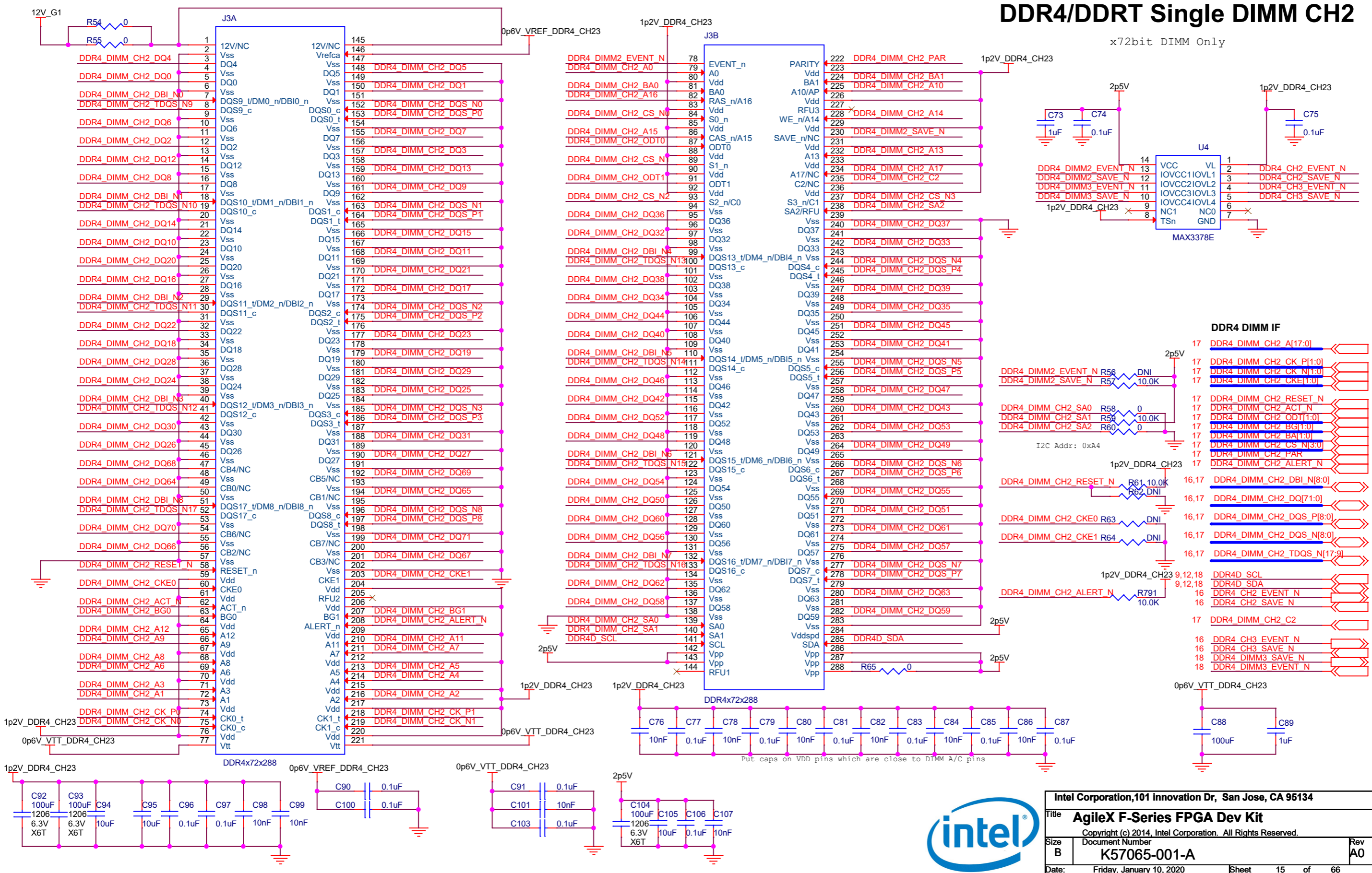
DDR4 CH1 Interface - FPGA Side 3D



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	14 of 66
Rev	A0

DDR4/DDRT Single DIMM CH2

x72bit DIMM Only



Intel Corporation, 101 innovation Dr, San Jose, CA 95134

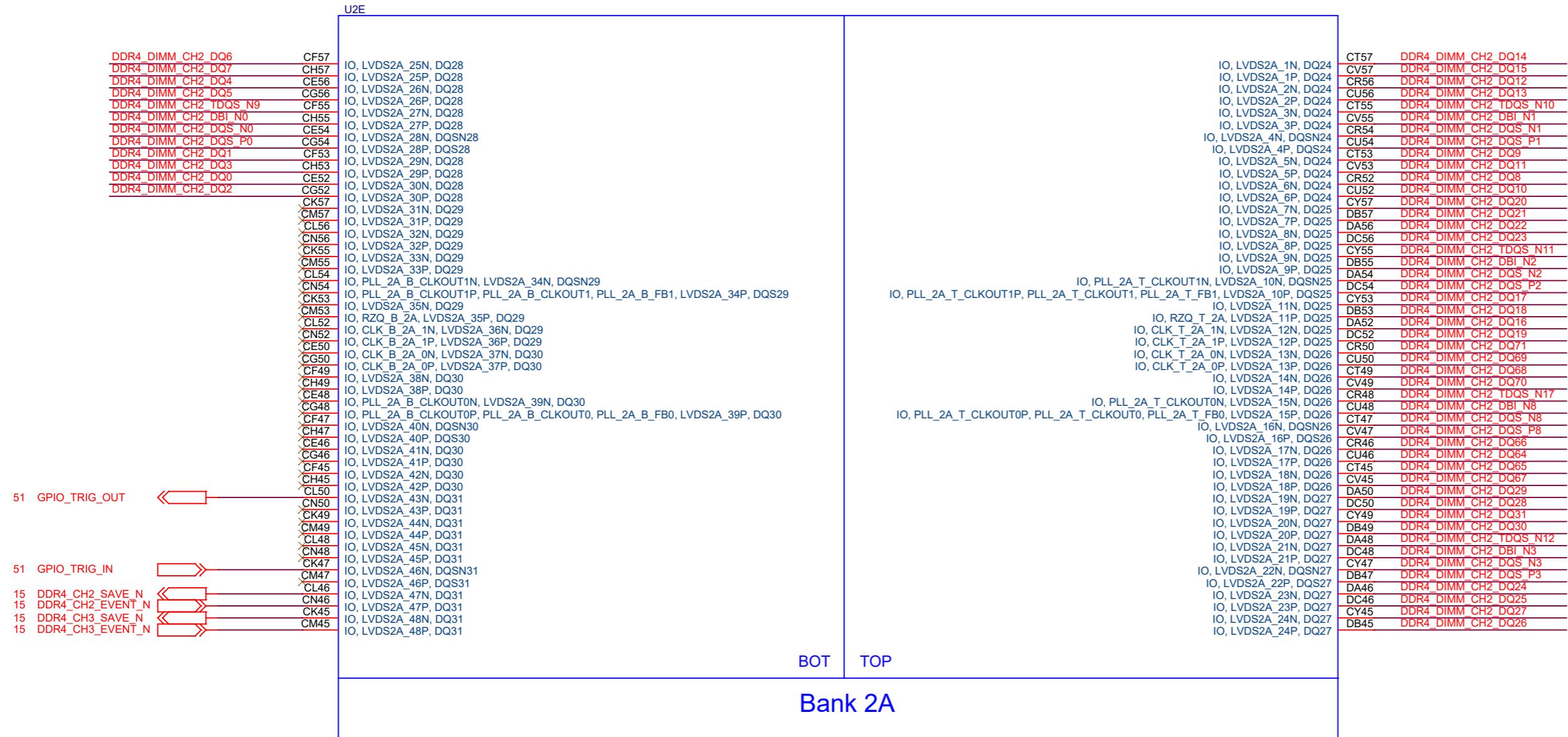
Title: **AgileX F-Series FPGA Dev Kit**

Copyright (c) 2014, Intel Corporation. All Rights Reserved.

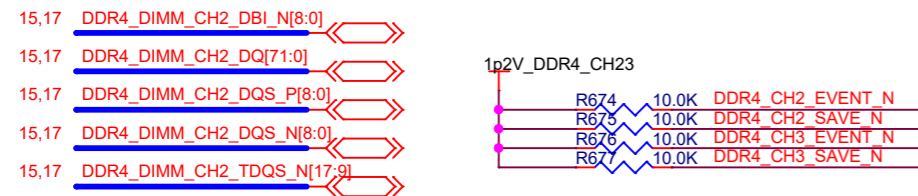
Size: B Document Number: **K57065-001-A** Rev: **A0**

Date: Friday, January 10, 2020 Sheet: 15 of 66

DDR4/T CH2 INTERFACE -- FPGA SIDE 2A

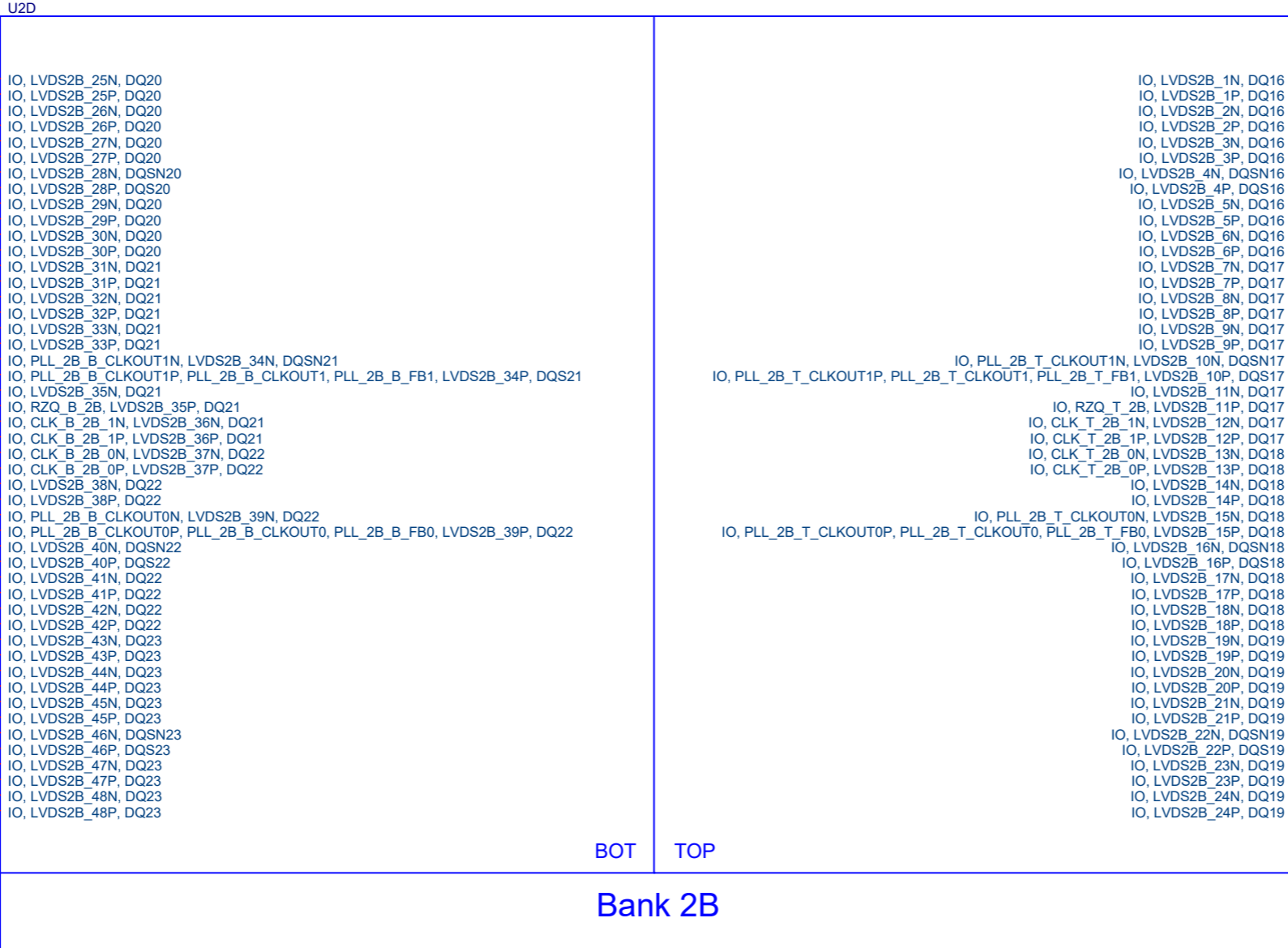


AGFB014R24_2486A



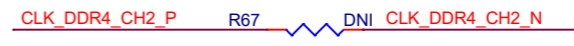
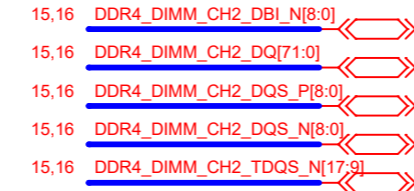
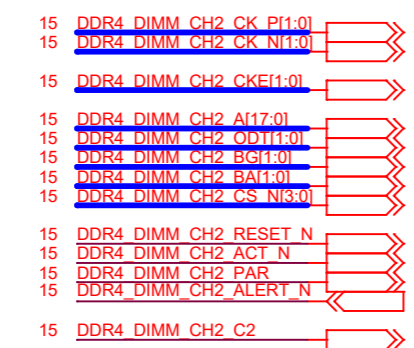
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	16 of 66
Rev	A0

DDR4/T CH2 INTERFACE -- FPGA SIDE 2B



DDRT:ERID2	DDR4_DIMM_CH2_CK_N1	CF43
DDRT:ERID0	DDR4_DIMM_CH2_CK_P1	CH43
DDRT:NC	DDR4_DIMM_CH2_ALERT_N	CE42
		CF41
		CH41
		CE40
		CG40
		CF39
DDRT:C3	DDR4_DIMM_CH2_C2	CH39
DDRT:C2	DDR4_DIMM_CH2_CS_N3	CE38
DDRT:C1	DDR4_DIMM_CH2_CS_N2	CG38
	DDR4_DIMM_CH2_BG0	CK43
	DDR4_DIMM_CH2_BA1	CM43
	DDR4_DIMM_CH2_BA0	CL42
	DDR4_DIMM_CH2_A17	CN42
	DDR4_DIMM_CH2_A16	CK41
	DDR4_DIMM_CH2_A15	CM41
	DDR4_DIMM_CH2_A14	CL40
	DDR4_DIMM_CH2_A13	CN40
	DDR4_DIMM_CH2_A12	CK39
	DDR4_DIMM_CH2_RZQ	CM39
	CLK_DDR4_CH2_N_38	CL38
	CLK_DDR4_CH2_P_38	CN38
	DDR4_DIMM_CH2_A11	CE36
	DDR4_DIMM_CH2_A10	CG36
	DDR4_DIMM_CH2_A9	CF35
	DDR4_DIMM_CH2_A8	CH35
	DDR4_DIMM_CH2_A7	CE34
	DDR4_DIMM_CH2_A6	CG34
	DDR4_DIMM_CH2_A5	CF33
	DDR4_DIMM_CH2_A4	CH33
	DDR4_DIMM_CH2_A3	CE32
	DDR4_DIMM_CH2_A2	CG32
	DDR4_DIMM_CH2_A1	CF31
	DDR4_DIMM_CH2_A0	CH31
	DDR4_DIMM_CH2_PAR	CL36
DDRT:GNT0	DDR4_DIMM_CH2_CS_N1	CN36
	DDR4_DIMM_CH2_CK_N0	CK35
	DDR4_DIMM_CH2_CK_P0	CM35
DDRT:REQ	DDR4_DIMM_CH2_CKE1	CL34
	DDR4_DIMM_CH2_CKE0	CN34
DDRT:ERR	DDR4_DIMM_CH2_ODT1	CK33
	DDR4_DIMM_CH2_ODT0	CM33
	DDR4_DIMM_CH2_ACT_N	CL32
	DDR4_DIMM_CH2_CS_N0	CN32
	DDR4_DIMM_CH2_RESET_N	CK31
	DDR4_DIMM_CH2_BG1	CM31

AGFB014R24_2486A



CT43	DDR4_DIMM_CH2_DQ39
CV43	DDR4_DIMM_CH2_DQ37
CR42	DDR4_DIMM_CH2_DQ38
CU42	DDR4_DIMM_CH2_DQ36
CT41	DDR4_DIMM_CH2_TDQS_N13
CV41	DDR4_DIMM_CH2_DBI_N4
CR40	DDR4_DIMM_CH2_DQS_N4
CU40	DDR4_DIMM_CH2_DQS_P4
CT39	DDR4_DIMM_CH2_DQ32
CV39	DDR4_DIMM_CH2_DQ33
CR38	DDR4_DIMM_CH2_DQ35
CU38	DDR4_DIMM_CH2_DQ34
CY43	DDR4_DIMM_CH2_DQ47
DB43	DDR4_DIMM_CH2_DQ45
DA42	DDR4_DIMM_CH2_DQ46
DC42	DDR4_DIMM_CH2_DQ44
CY41	DDR4_DIMM_CH2_TDQS_N14
DB41	DDR4_DIMM_CH2_DBI_N5
DA40	DDR4_DIMM_CH2_DQS_N5
DC40	DDR4_DIMM_CH2_DQS_P5
CY39	DDR4_DIMM_CH2_DQ40
DB39	DDR4_DIMM_CH2_DQ41
DA38	DDR4_DIMM_CH2_DQ43
DC38	DDR4_DIMM_CH2_DQ42
CR36	DDR4_DIMM_CH2_DQ63
CU36	DDR4_DIMM_CH2_DQ61
CT35	DDR4_DIMM_CH2_DQ62
CV35	DDR4_DIMM_CH2_DQ60
CR34	DDR4_DIMM_CH2_TDQS_N16
CU34	DDR4_DIMM_CH2_DBI_N7
CT33	DDR4_DIMM_CH2_DQS_N7
CV33	DDR4_DIMM_CH2_DQS_P7
CR32	DDR4_DIMM_CH2_DQ56
CU32	DDR4_DIMM_CH2_DQ57
CT31	DDR4_DIMM_CH2_DQ59
CV31	DDR4_DIMM_CH2_DQ58
DA36	DDR4_DIMM_CH2_DQ52
DC36	DDR4_DIMM_CH2_DQ53
CY35	DDR4_DIMM_CH2_DQ55
DB35	DDR4_DIMM_CH2_DQ54
DA34	DDR4_DIMM_CH2_TDQS_N15
DC34	DDR4_DIMM_CH2_DBI_N6
CY33	DDR4_DIMM_CH2_DQS_N6
DB33	DDR4_DIMM_CH2_DQS_P6
DA32	DDR4_DIMM_CH2_DQ48
DC32	DDR4_DIMM_CH2_DQ49
CY31	DDR4_DIMM_CH2_DQ51
DB31	DDR4_DIMM_CH2_DQ50

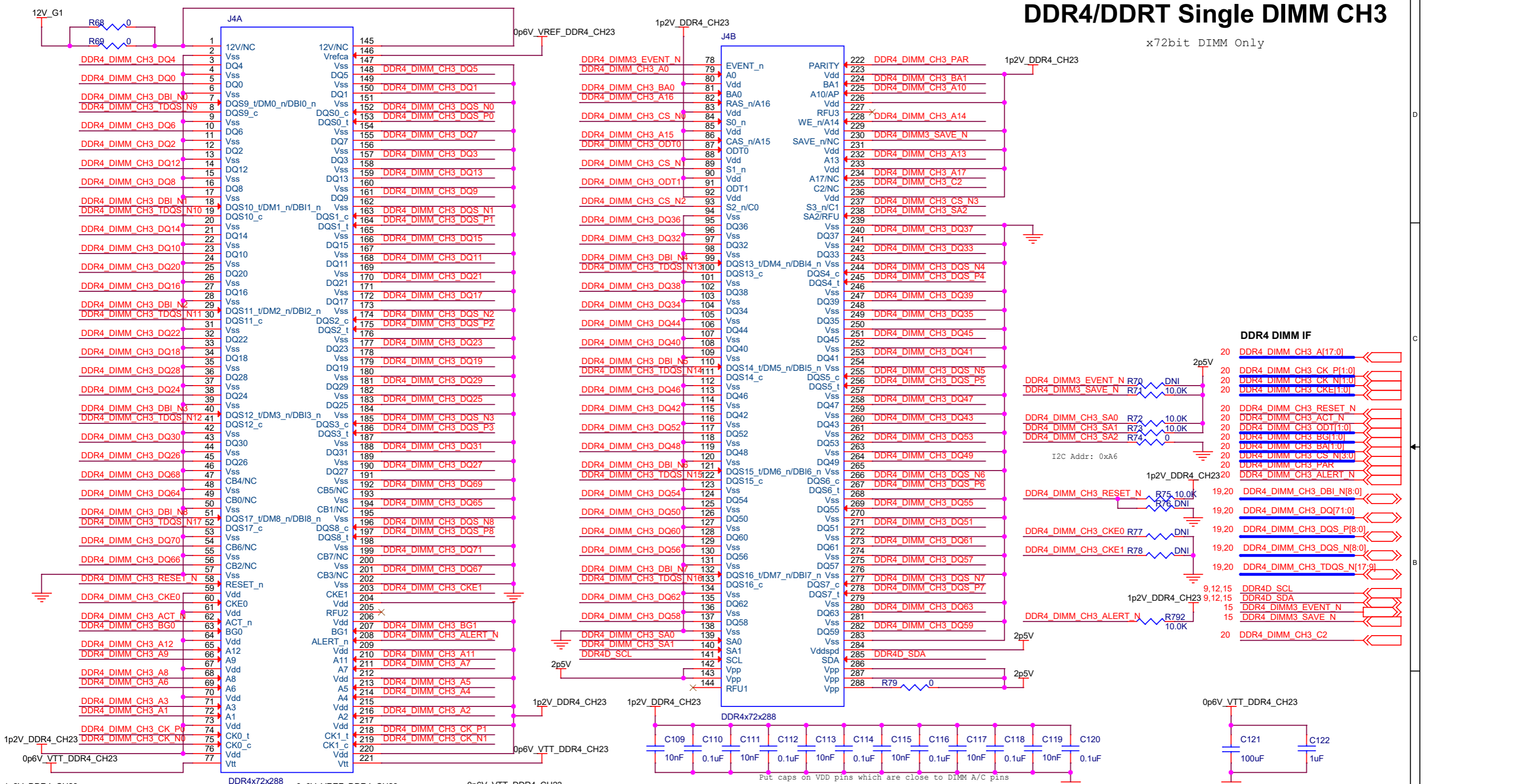
BOT TOP
Bank 2B



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	17 of 66
Rev	A0

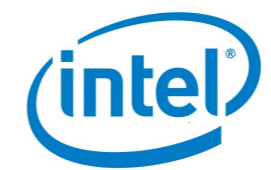
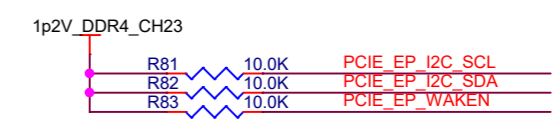
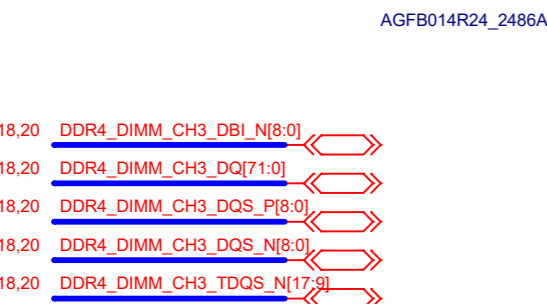
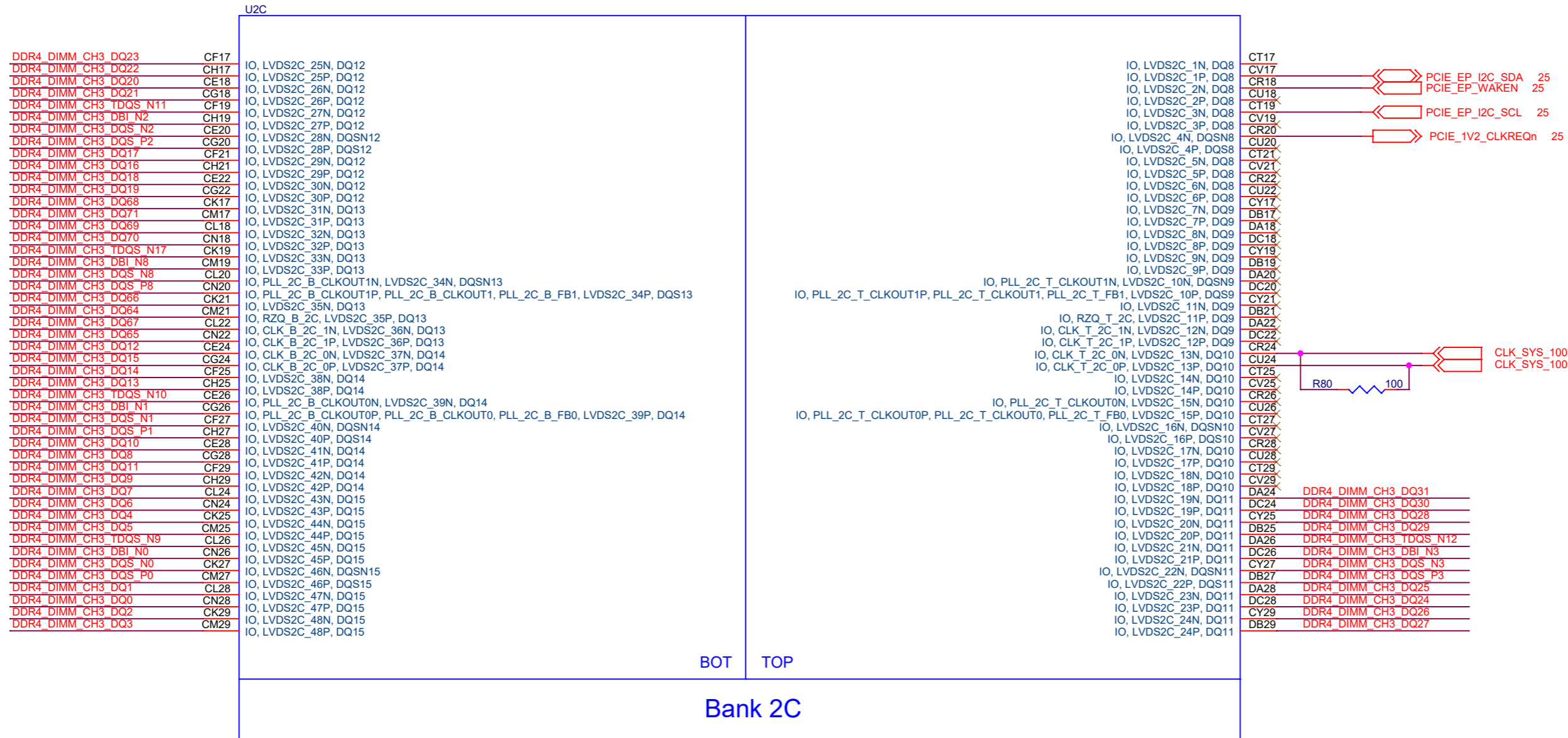
DDR4/DDRT Single DIMM CH3

x72bit DIMM Only



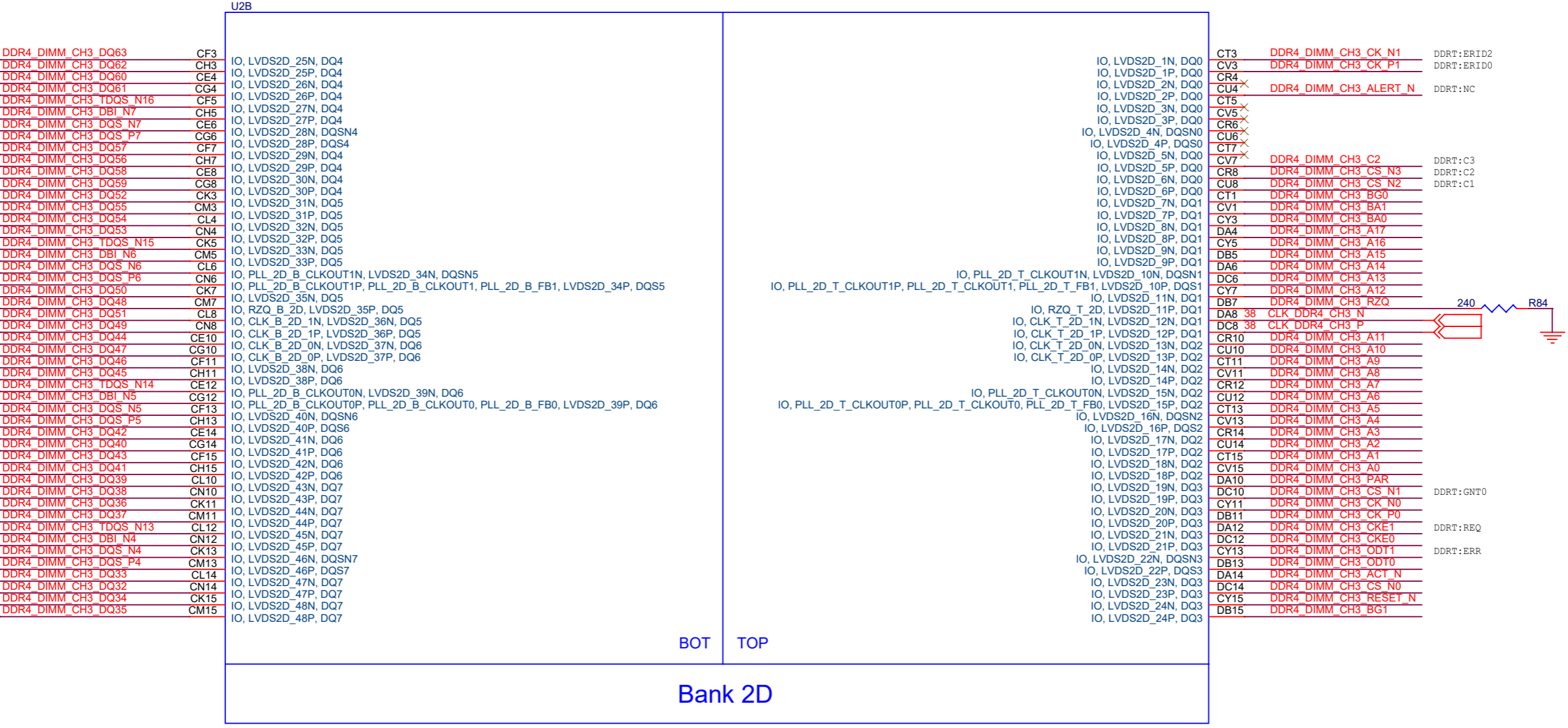
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 18	of 66

DDR4/T CH3 INTERFACE -- FPGA SIDE 2C

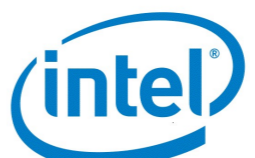
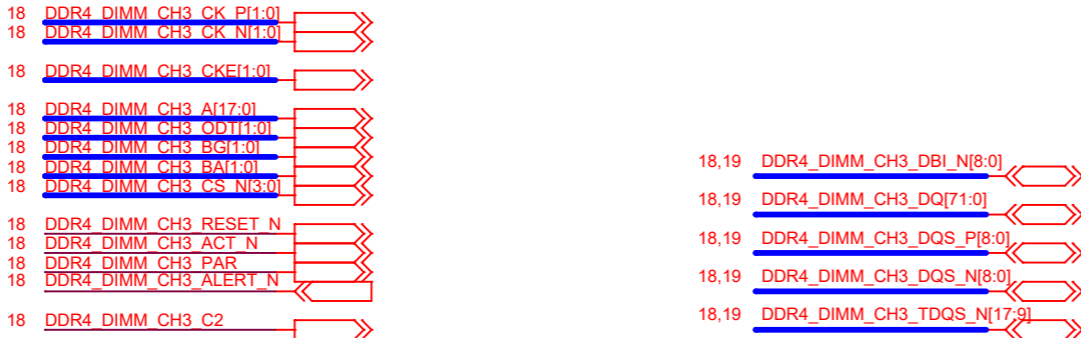


Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	19 of 66
Rev	A0

DDR4/T CH3 INTERFACE -- FPGA SIDE 2D

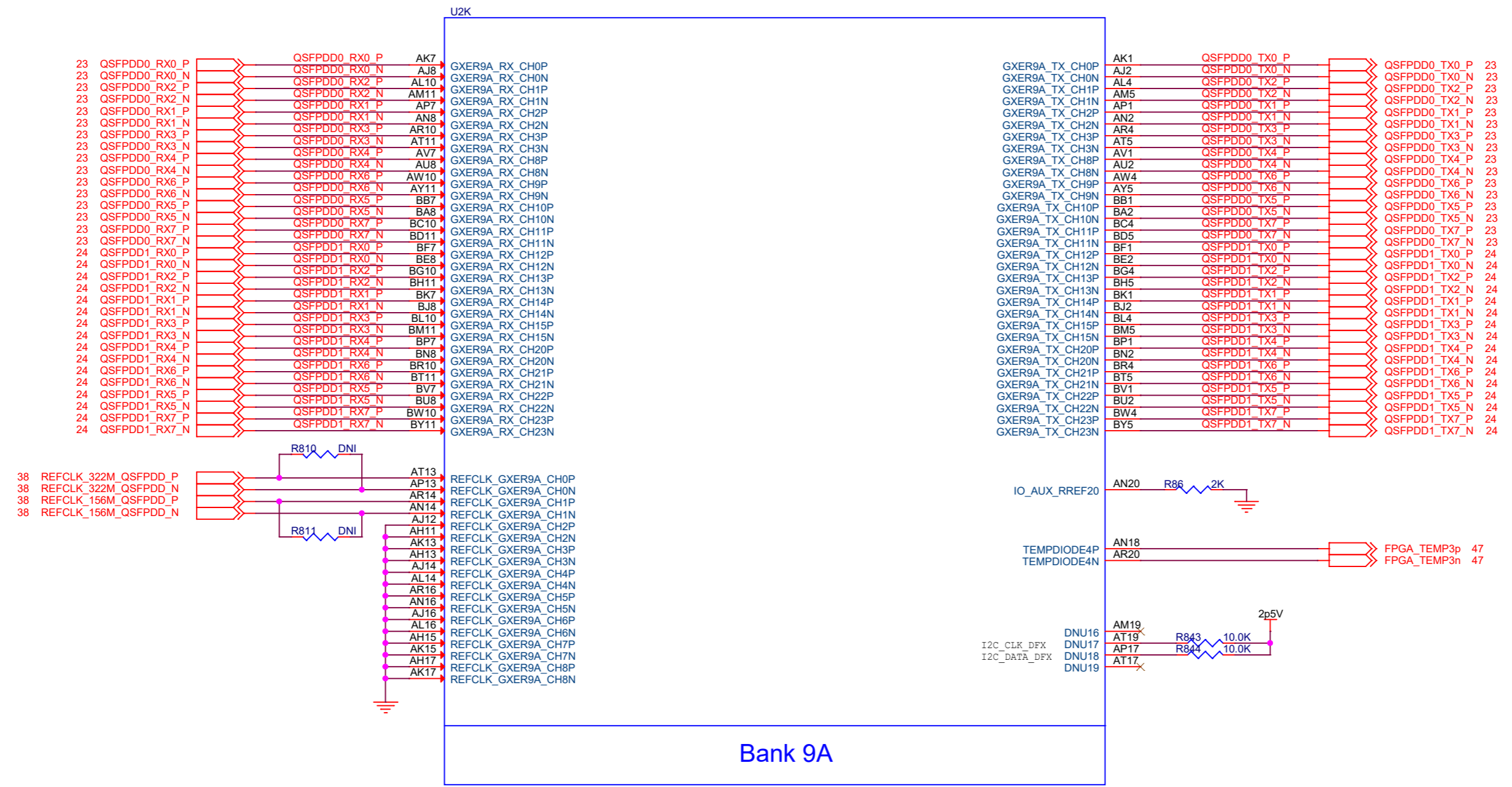


AGFB014R24_2486A



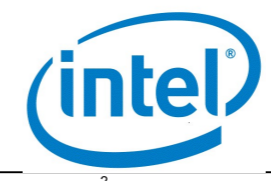
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 20	of 66

E-TILE BANK 9A



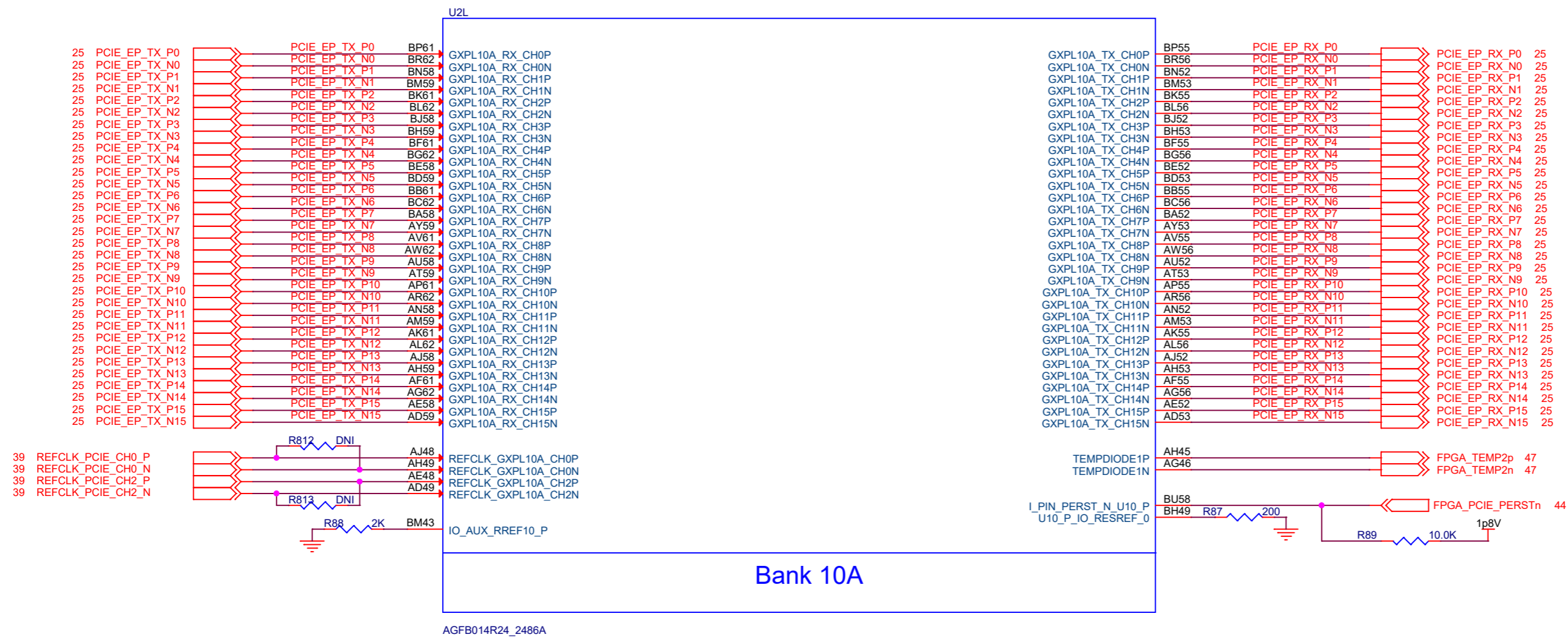
AGFB014R24_2486A

Bank 9A



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	21 of 66
Rev	A0

P-TILE BANK 10A



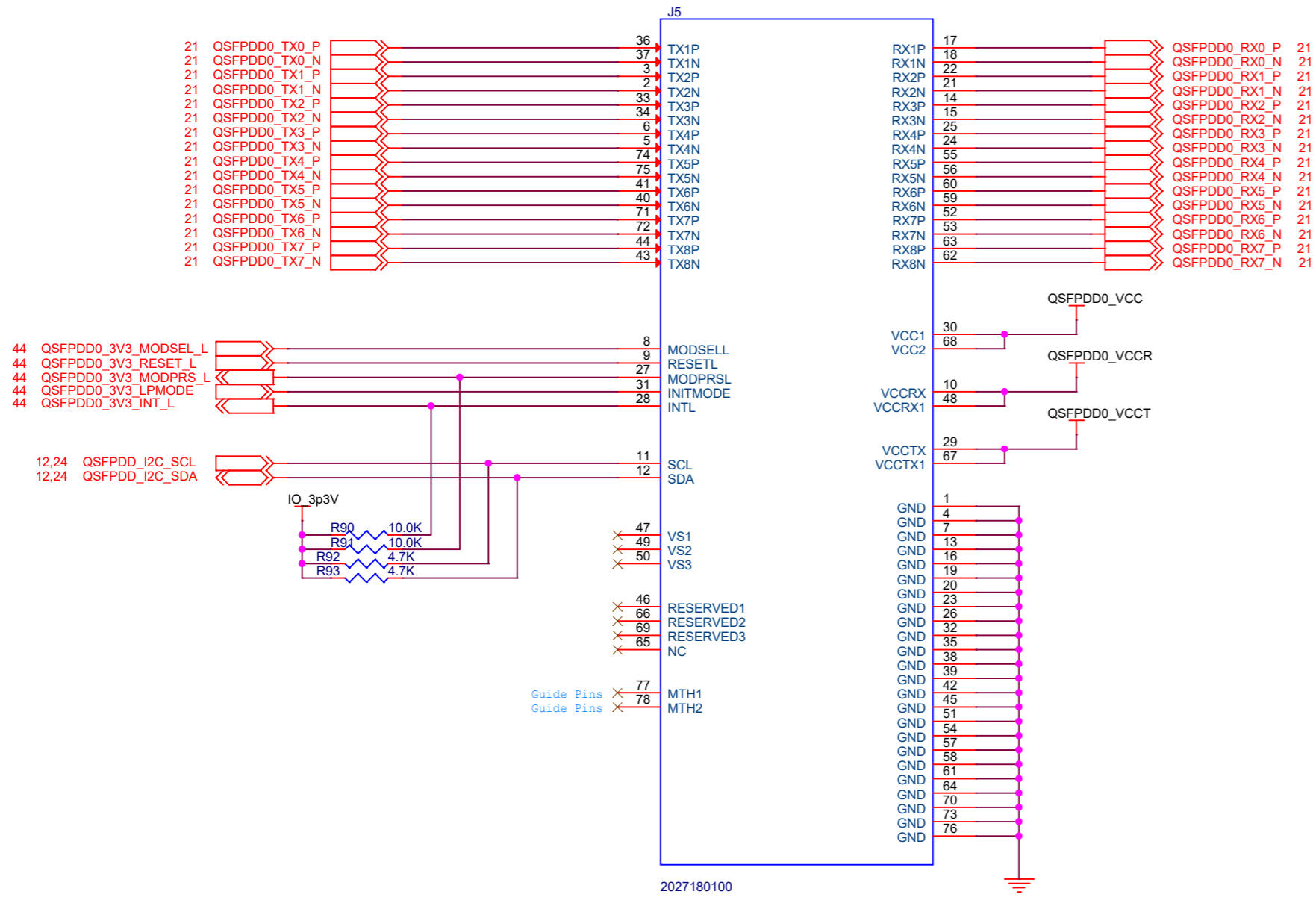
Bank 10A

AGFB014R24_2486A

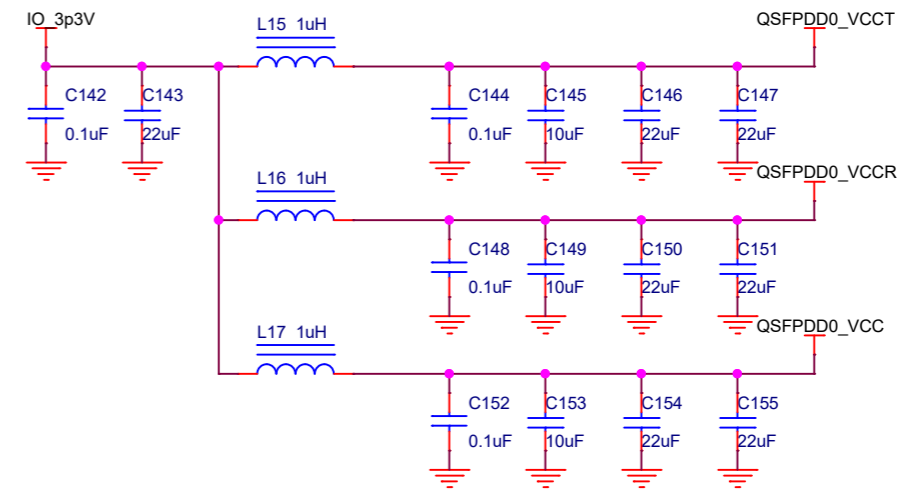


Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	22 of 66
Rev	A0

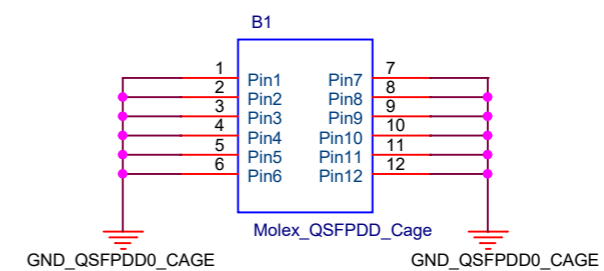
QSFPDD0



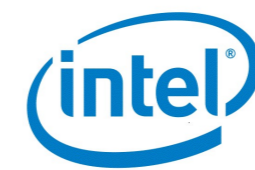
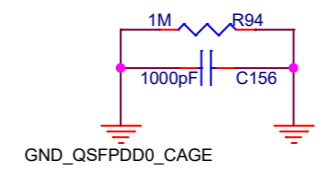
- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



Place close to QSFPDD Connector



MOLEX MPN 2031431355



Intel Corporation, 101 Innovation Dr., San Jose CA 95134 Copyright (c) 2016, Intel Corporation. All Rights Reserved.		
Title AgileX F-Series FPGA Dev Kit		
Size B	Document Number K57065-001-A	Rev A0
Date: Friday, January 10, 2020	Sheet 1	23 of 66

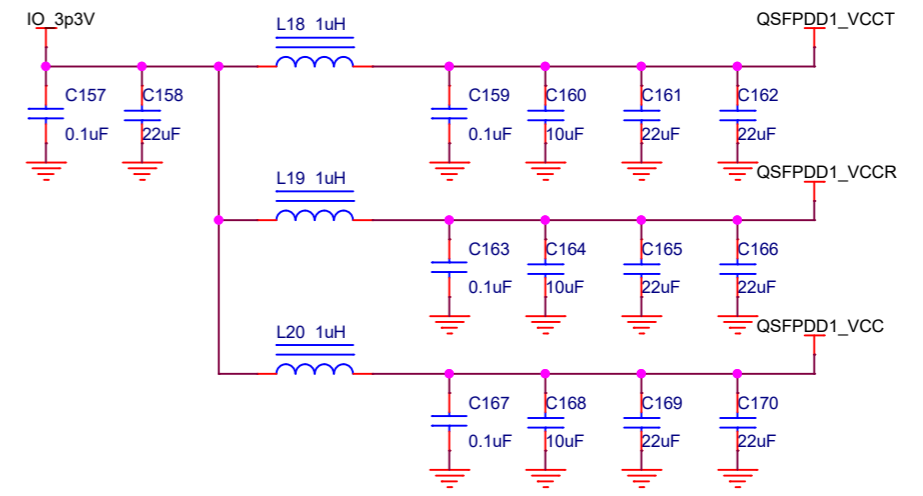
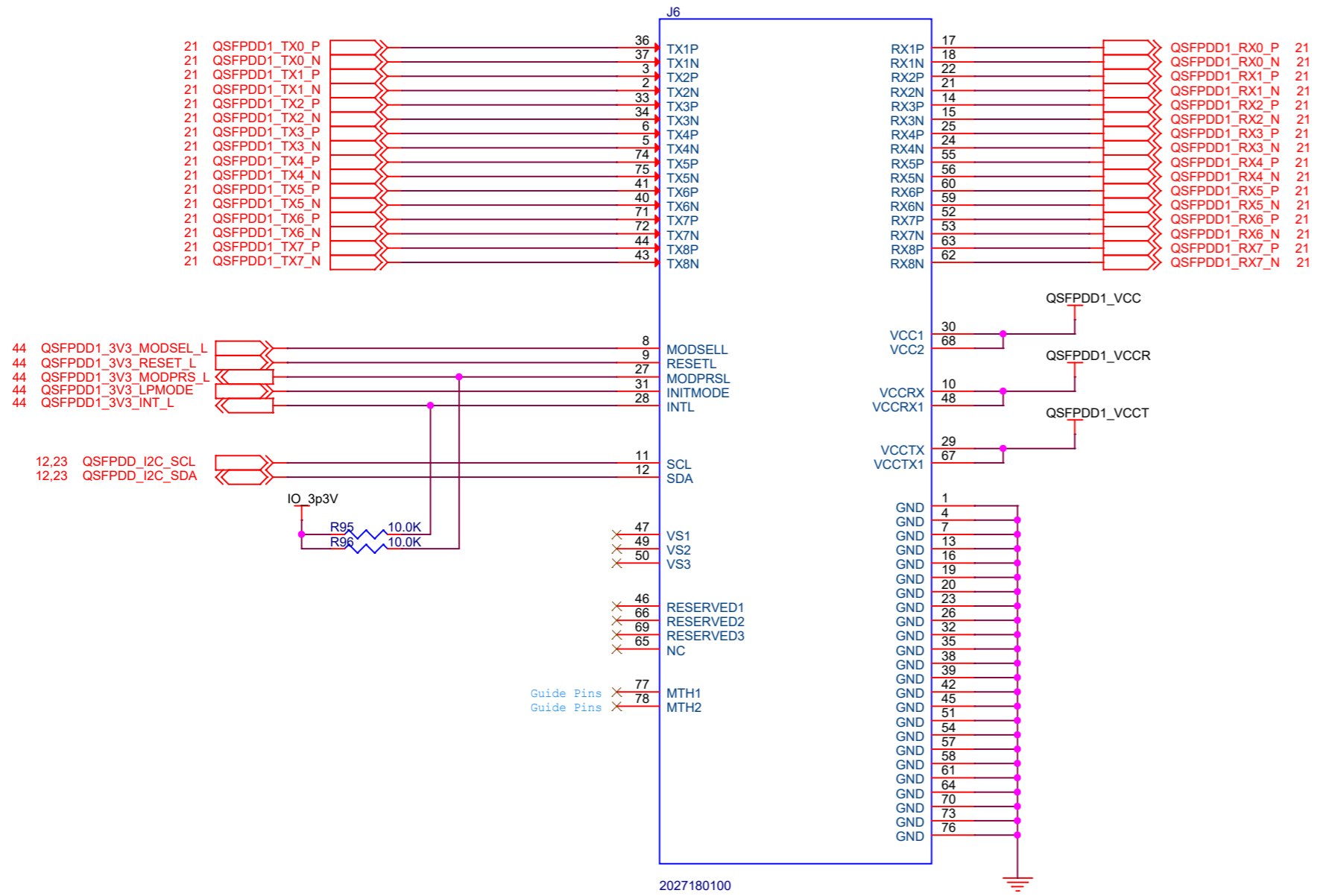
QSFPDD1

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

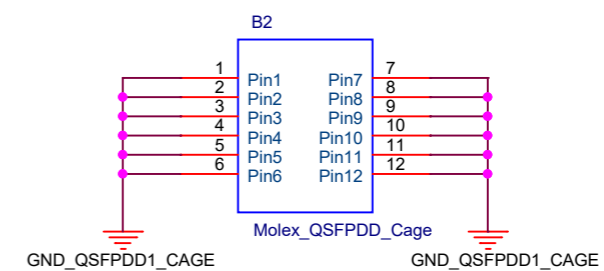
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

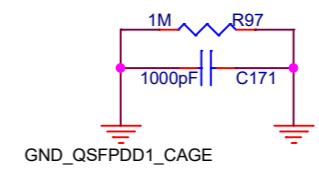
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



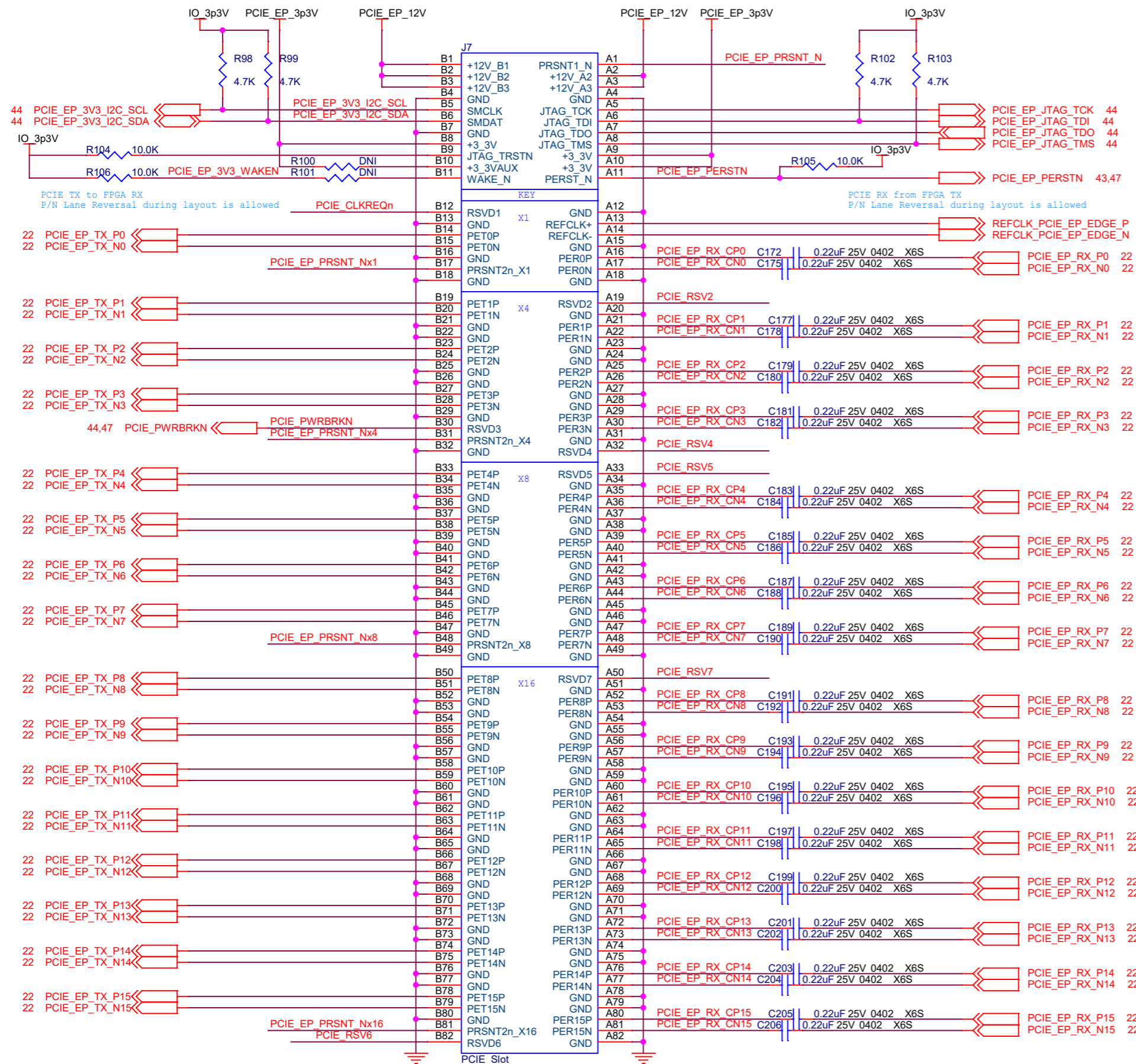
Place close to QSFPDD Connector



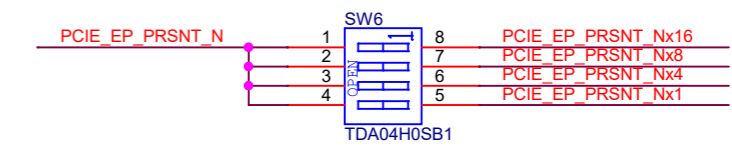
MOLEX MPN 2031431355



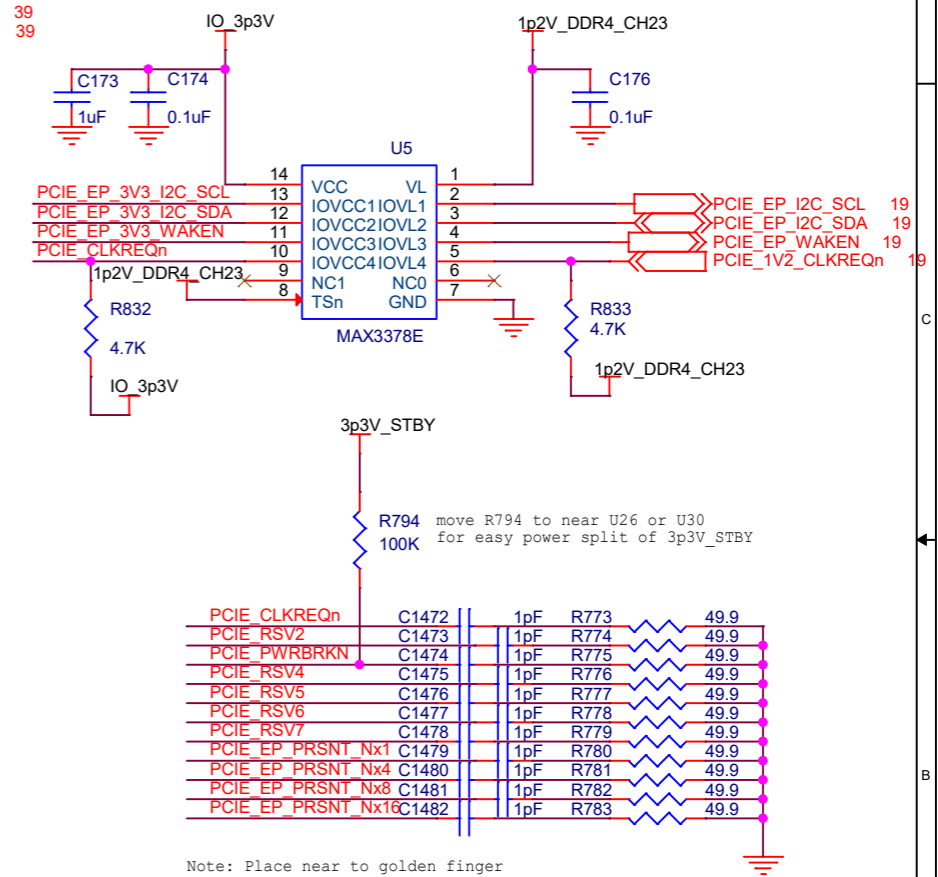
Intel Corporation, 101 Innovation Dr., San Jose CA 95134 Copyright (c) 2016, Intel Corporation. All Rights Reserved.		
Title AgileX F-Series FPGA Dev Kit		
Size B	Document Number K57065-001-A	Rev A0
Date: Friday, January 10, 2020	Sheet 1	of 66



PCIe Endpoint Edge Connector



Notes: Close --> select;
Open --> deselect



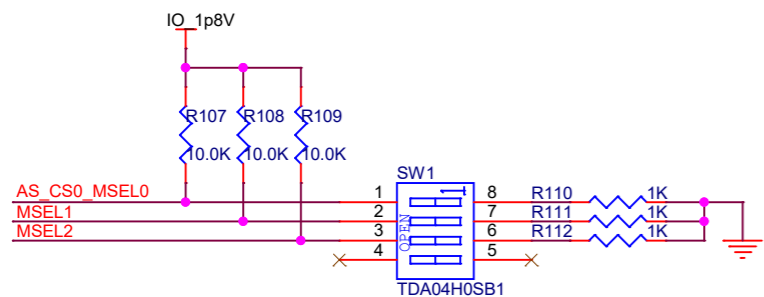
Note: Place near to golden finger

PCIe TX/RX signal naming convention with respect to CPU

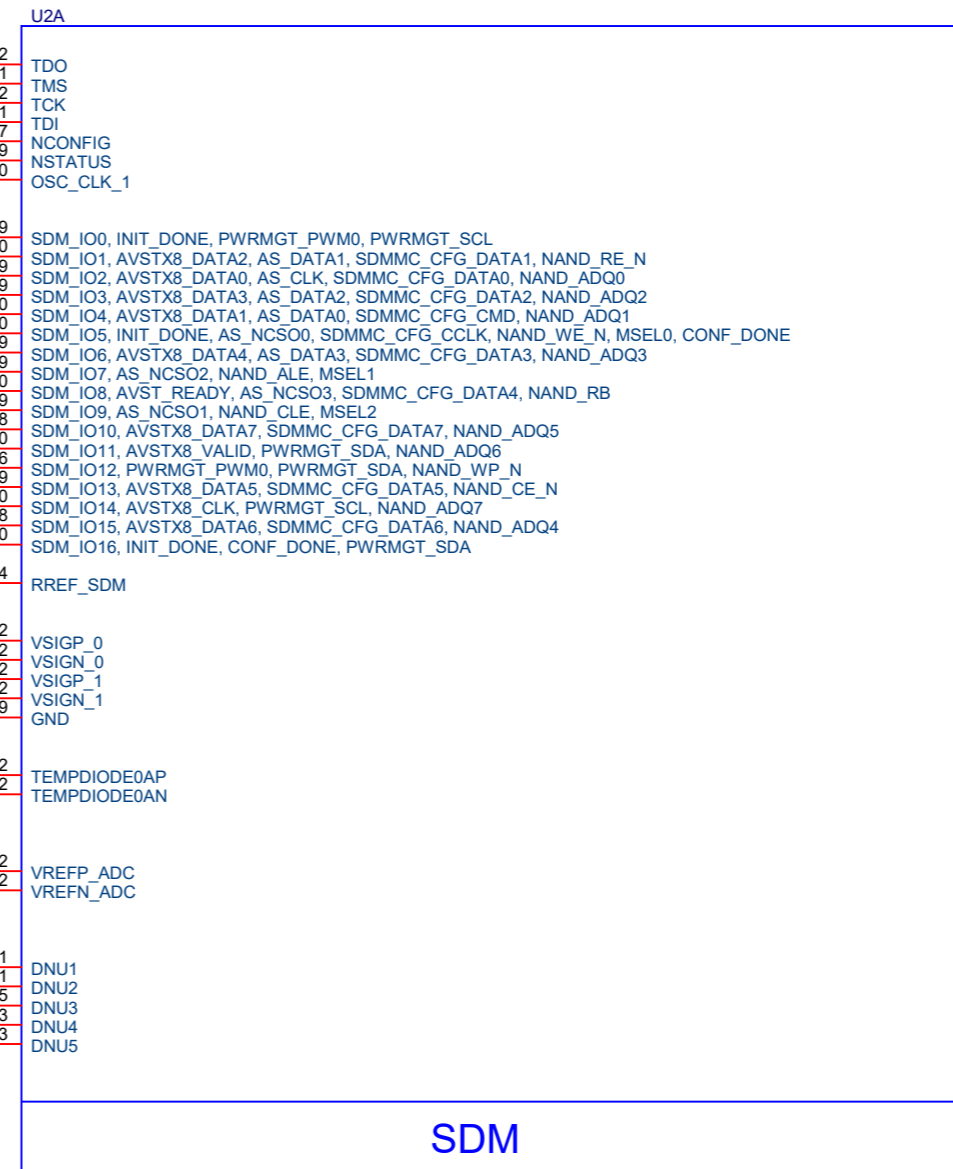
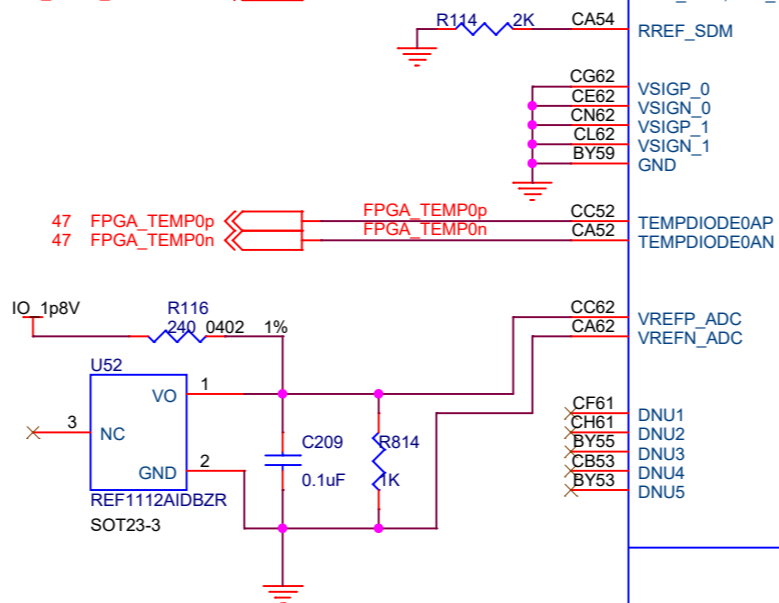
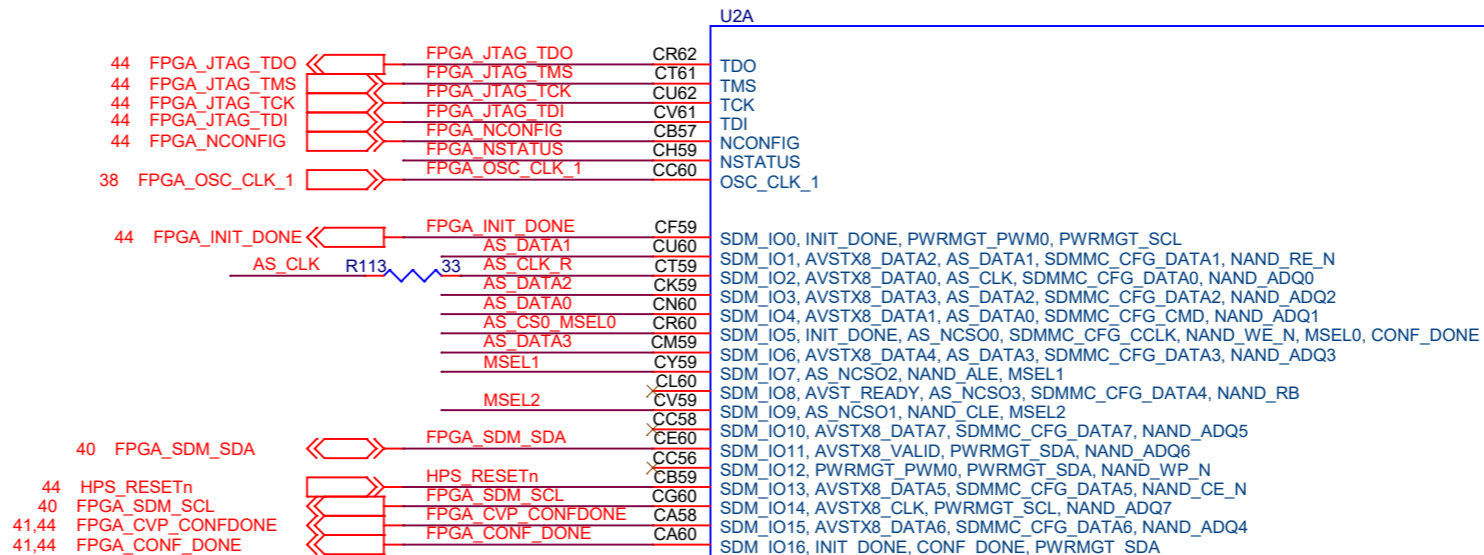
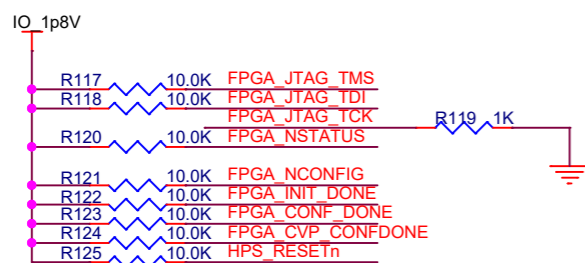
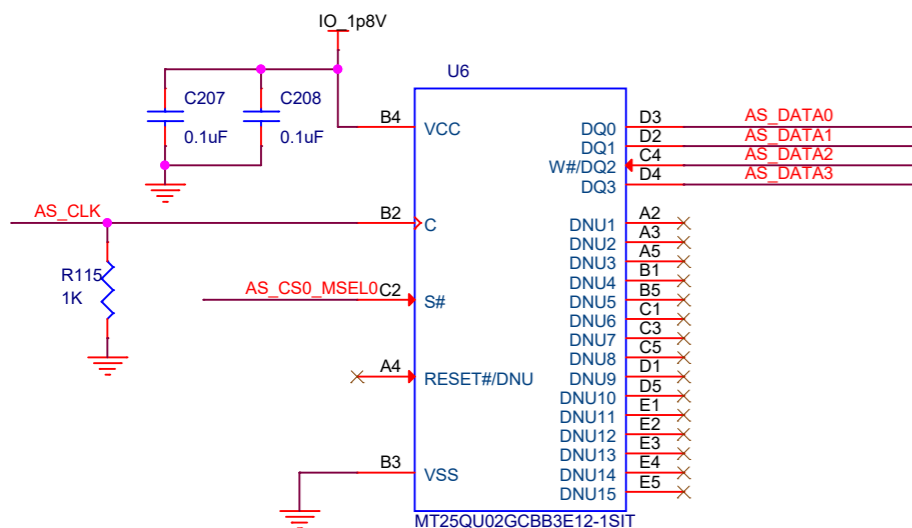



Intel Corporation, 101 Innovation Dr., San Jose CA 95134 Copyright (c) 2016, Intel Corporation. All Rights Reserved.		
Title AgileX F-Series FPGA Dev Kit		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 25 of 66

SDM & Configuration



Config_Mode	MSEL2	MSEL1	MSEL0
AS_FAST	0	0	1
AS_NORMAL	0	1	1

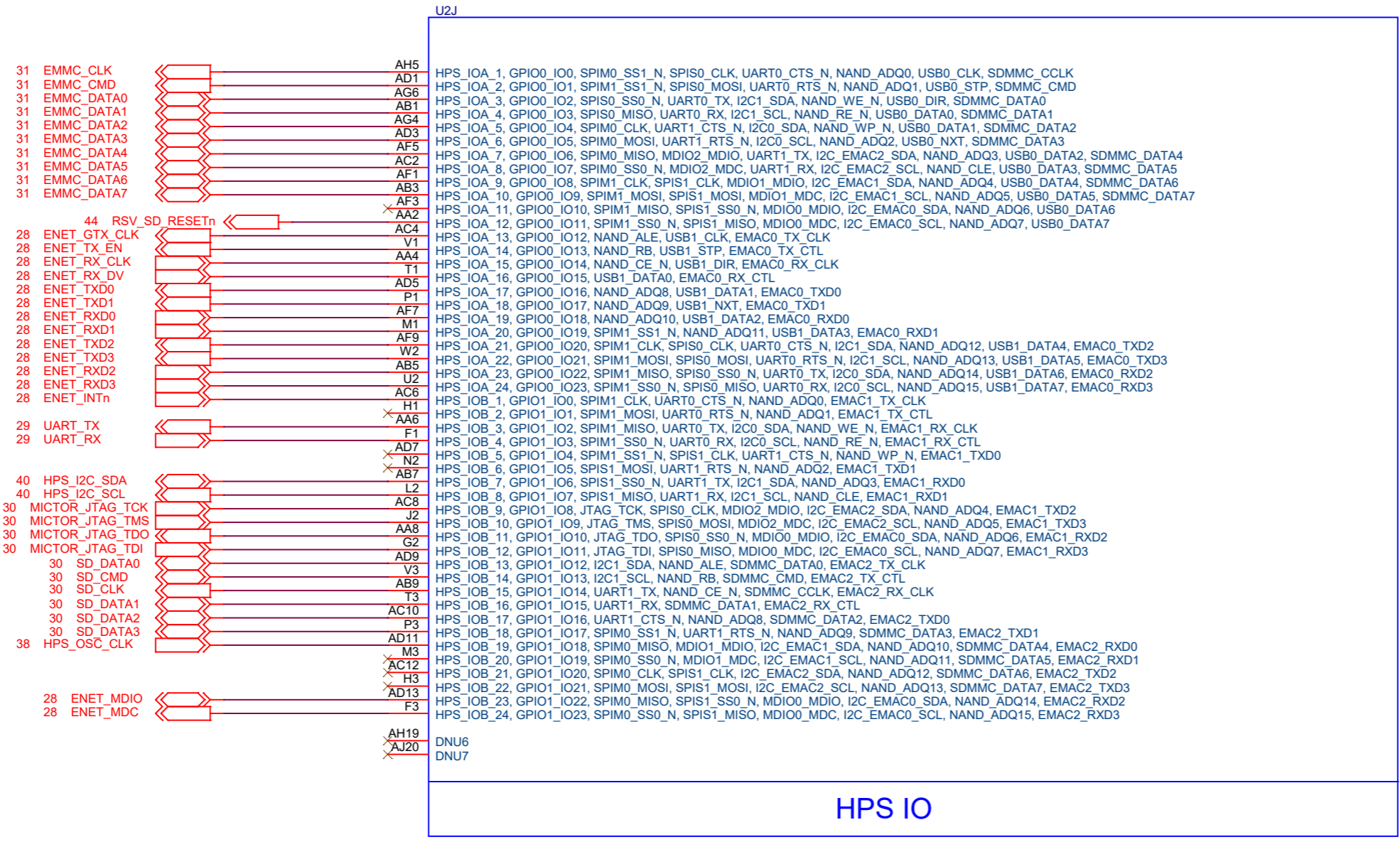
Intel Corporation, 101 innovation Dr, San Jose, CA 95134

Title **AgileX F-Series FPGA Dev Kit**

Copyright (c) 2014, Intel Corporation. All Rights Reserved.

Size B Document Number **K57065-001-A** Rev **A0**

Date: Friday, January 10, 2020 Sheet 26 of 66

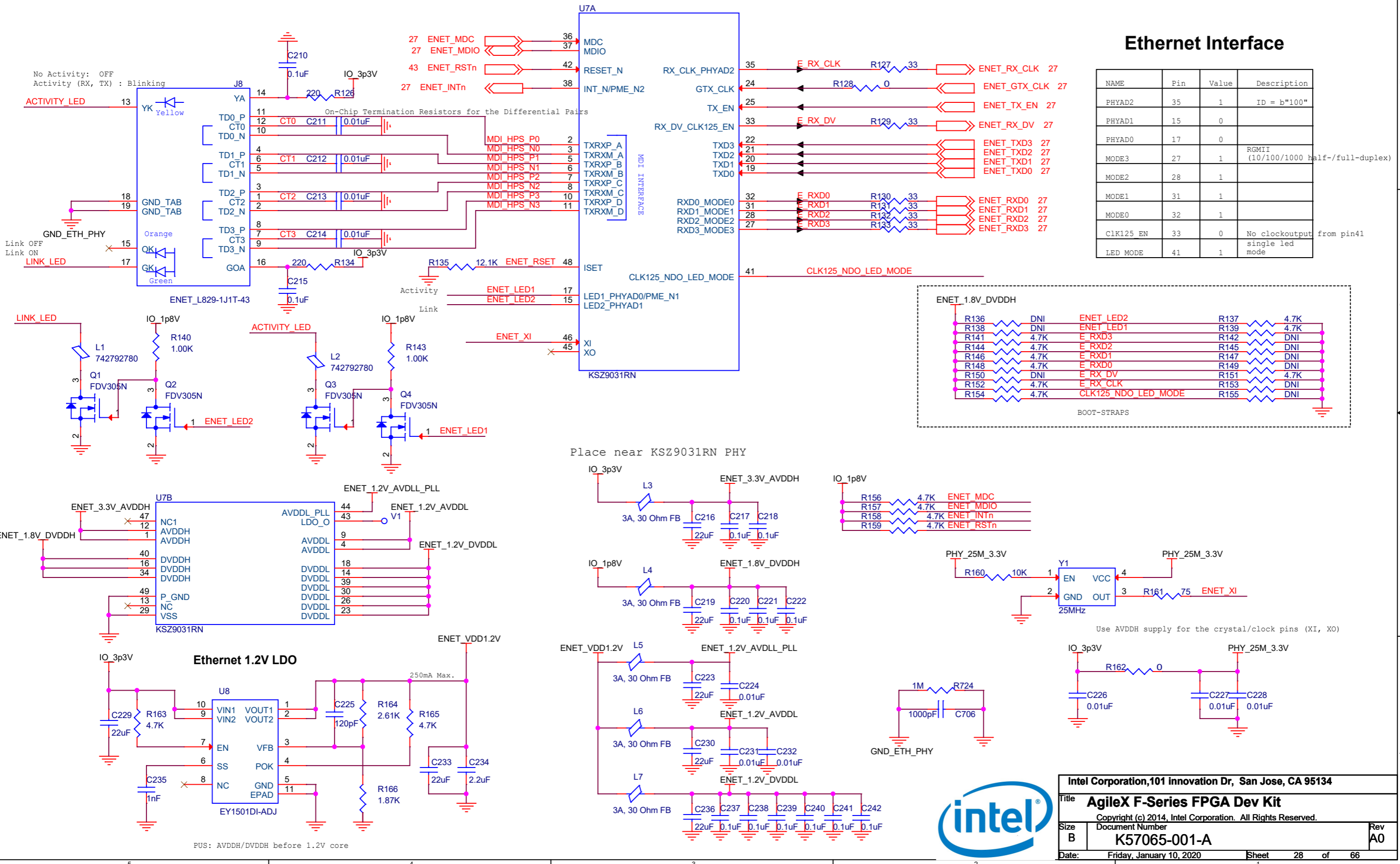


AGFB014R24_2486A



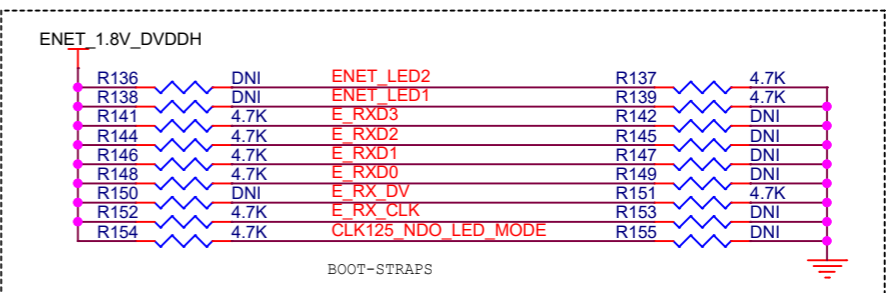
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 27 of 66

10/100/1000 Ethernet - HPS

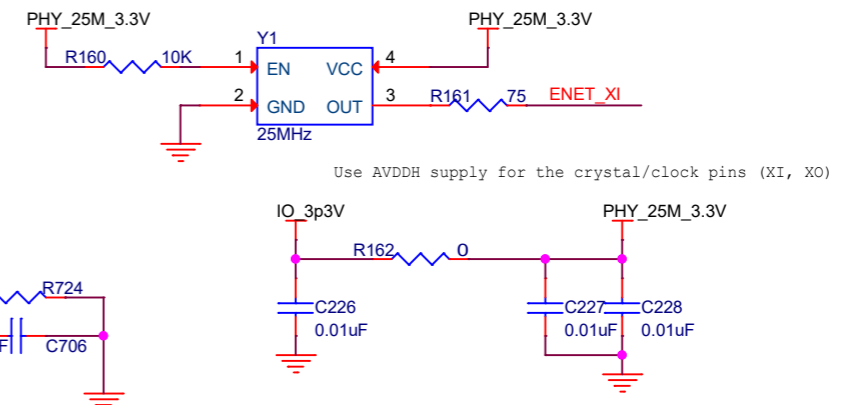
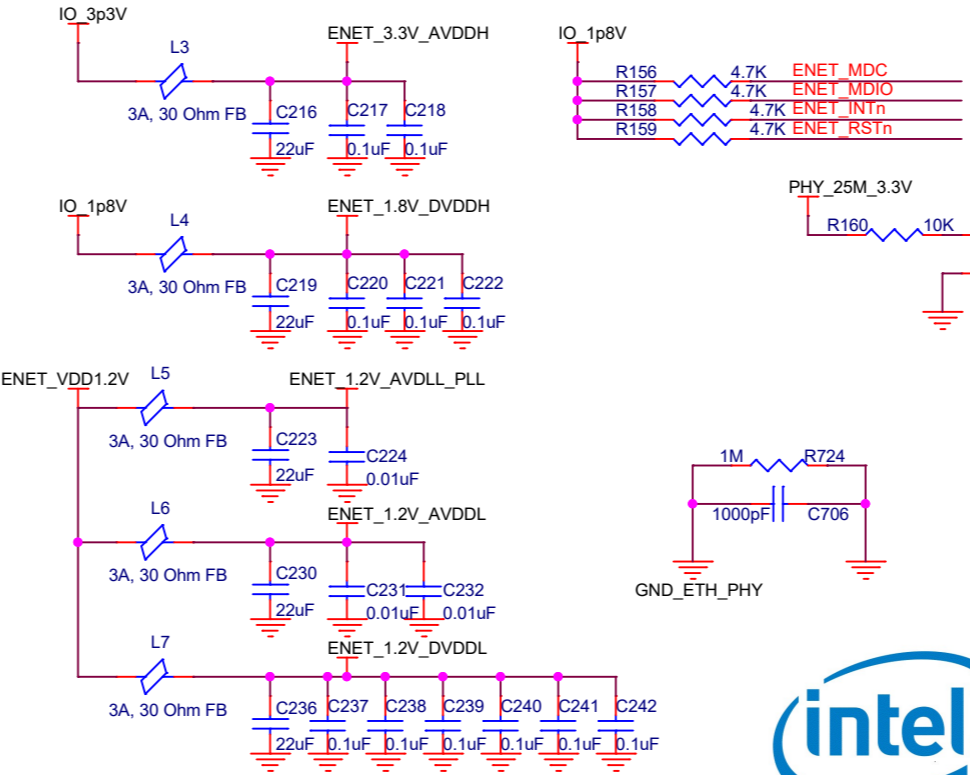


Ethernet Interface

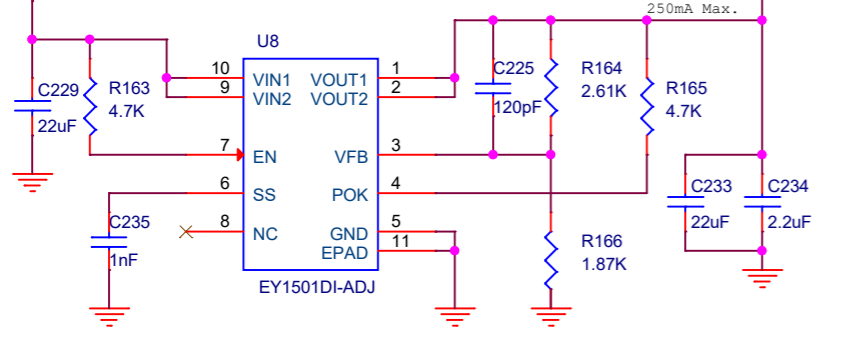
NAME	Pin	Value	Description
PHYAD2	35	1	ID = b"100"
PHYAD1	15	0	
PHYAD0	17	0	
MODE3	27	1	RGMI (10/100/1000 half-/full-duplex)
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
CLK125_EN	33	0	No clockoutput from pin41
LED MODE	41	1	single led mode



Place near KCS9031RN PHY



Ethernet 1.2V LDO



PUS: AVDDH/DVDDH before 1.2V core



Intel Corporation, 101 innovation Dr, San Jose, CA 95134

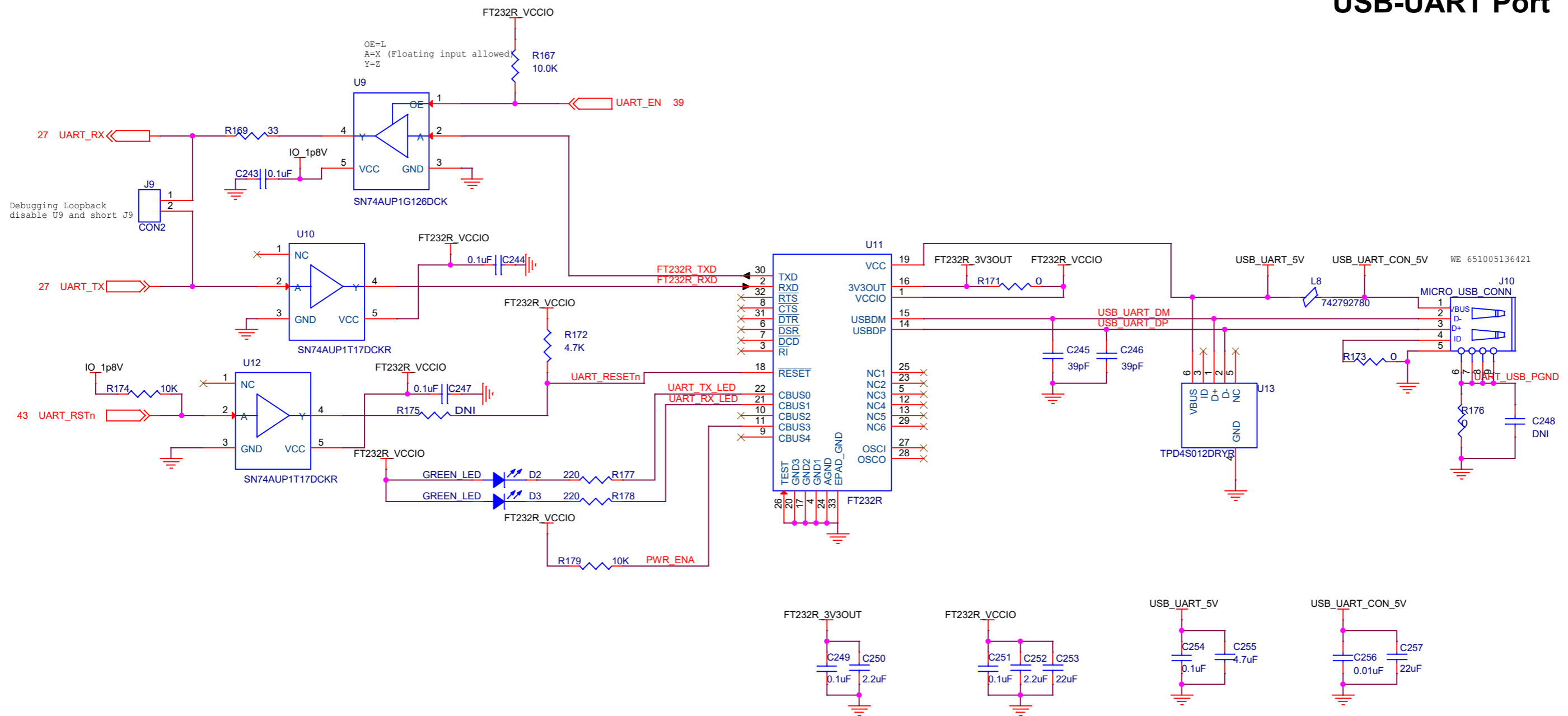
Title: **AgileX F-Series FPGA Dev Kit**

Copyright (c) 2014, Intel Corporation. All Rights Reserved.

Size: B Document Number: **K57065-001-A** Rev: **A0**

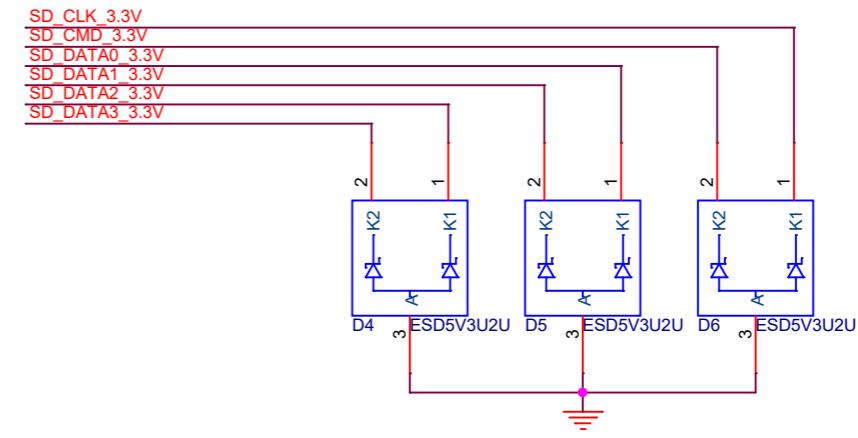
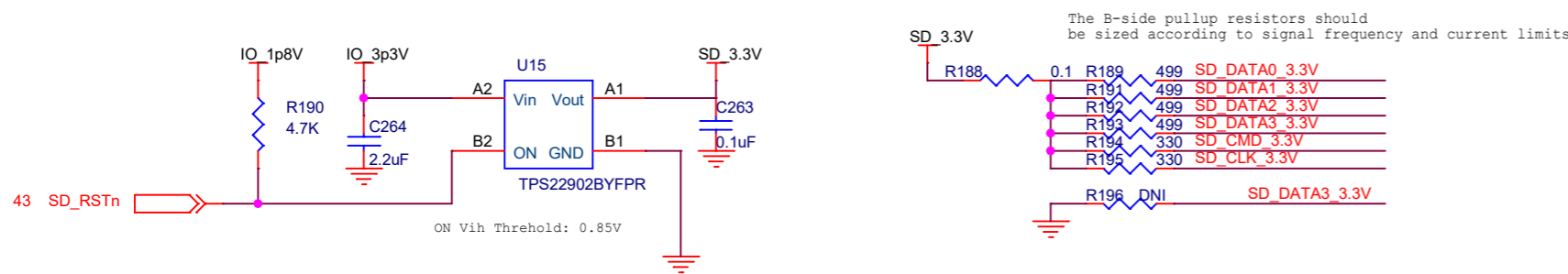
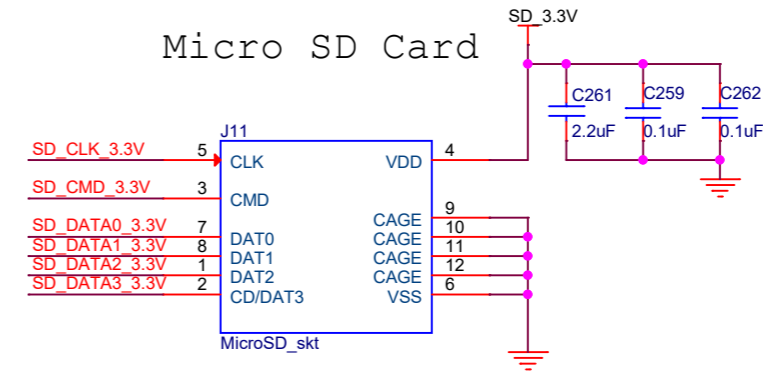
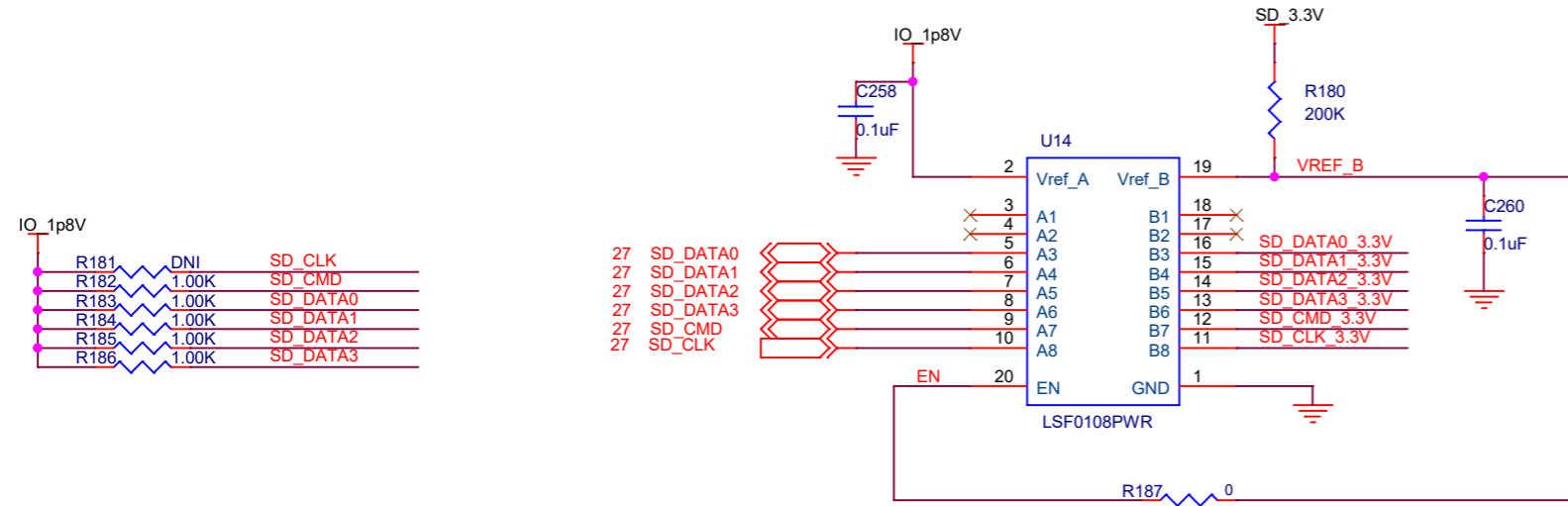
Date: Friday, January 10, 2020 Sheet: 28 of 66

USB-UART Port

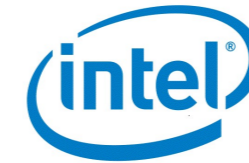
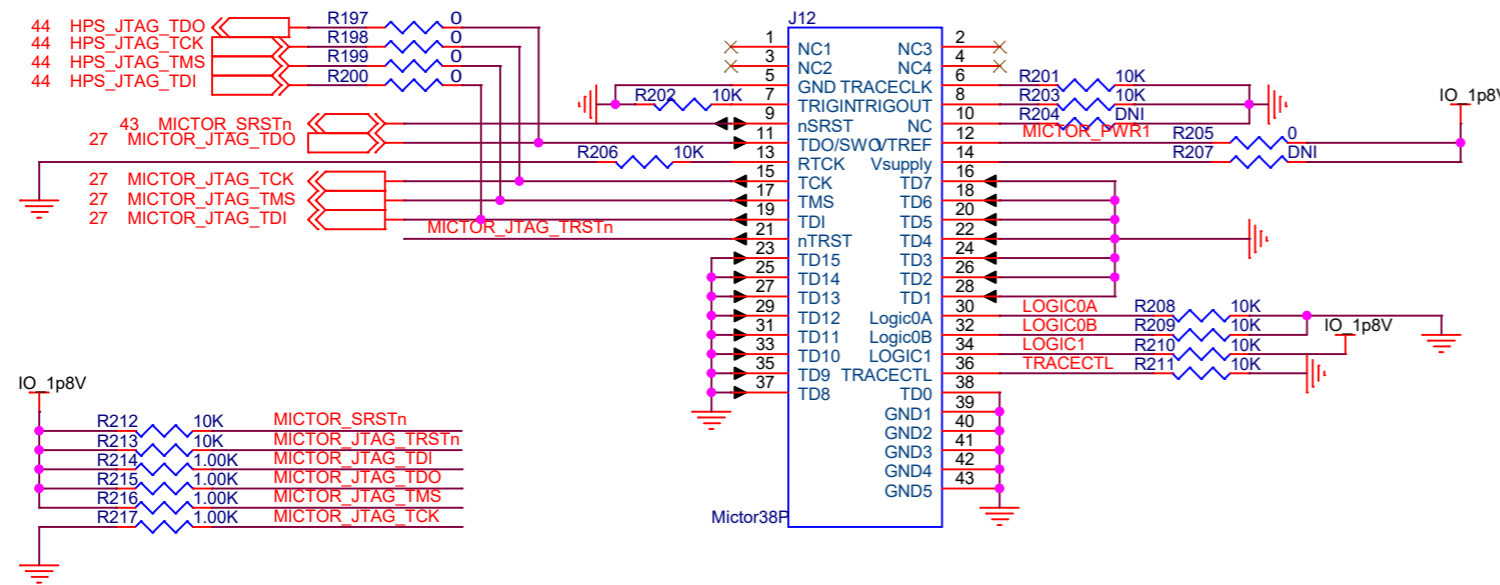


Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	29 of 66
Rev	A0

MicroSD Card

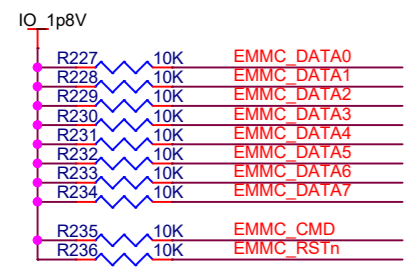
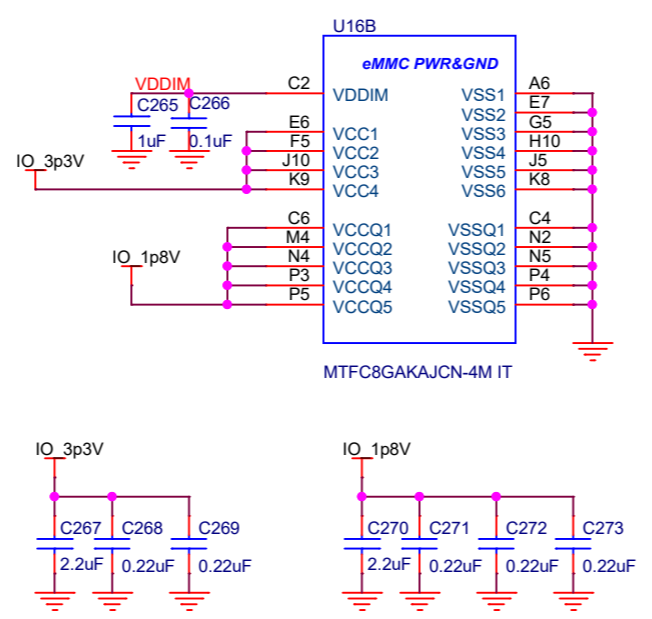
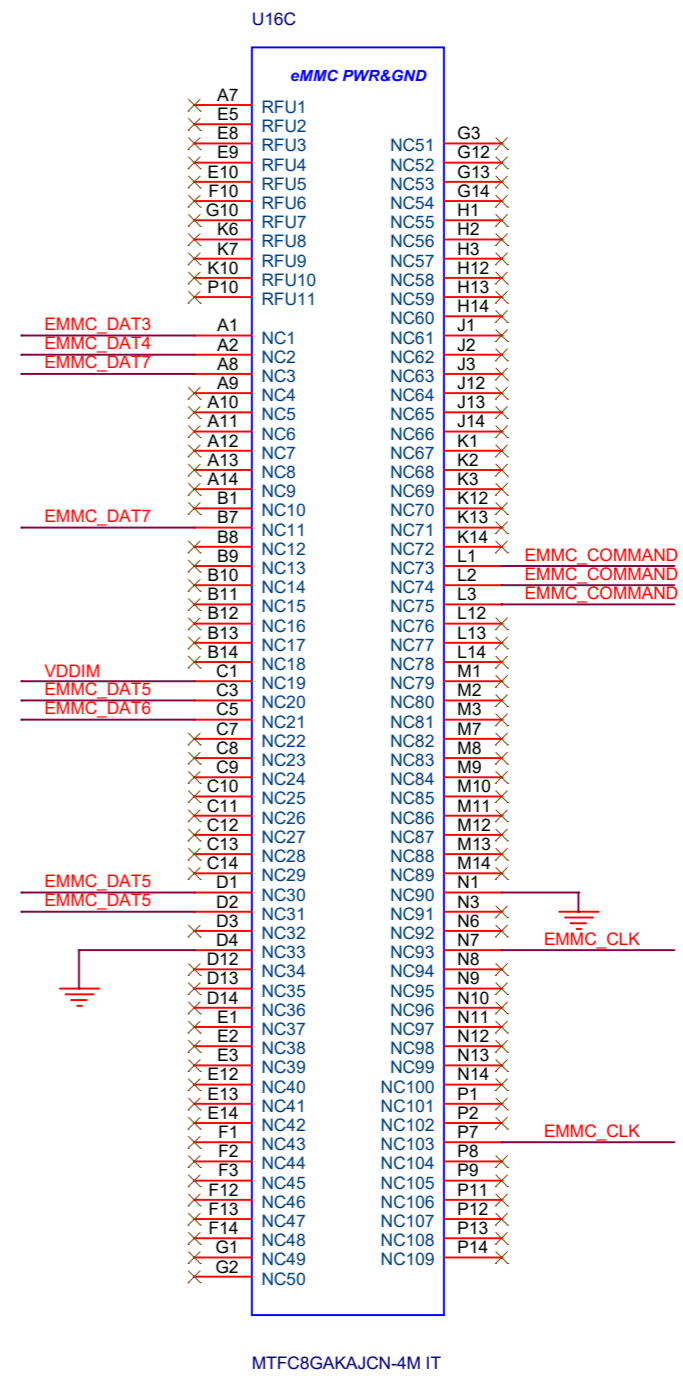
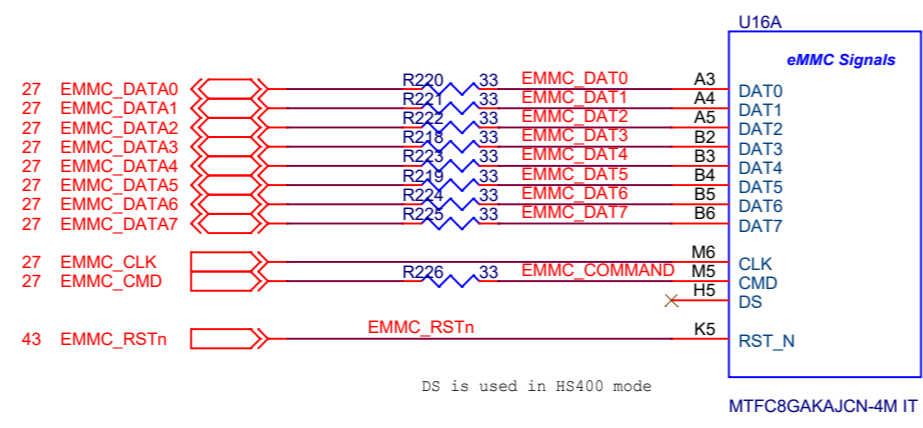


IEC61000-4-2 (ESD): ± 20 kV (air / contact)
 IEC61000-4-4 (EFT): ±50 A (5/50 ns)
 IEC61000-4-5 (surge): ±3 A (8/20 μs)



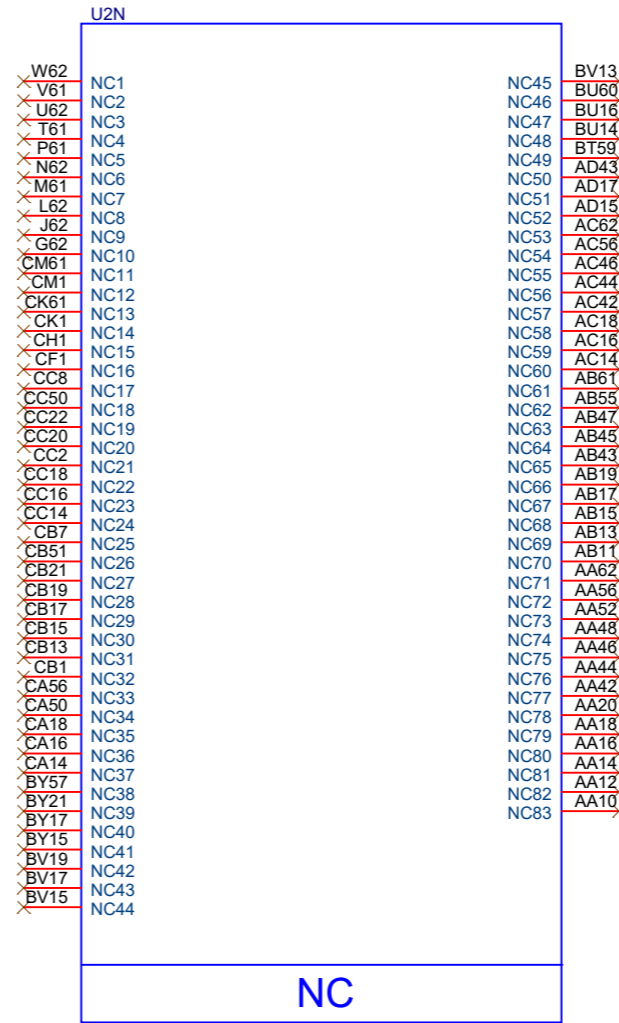
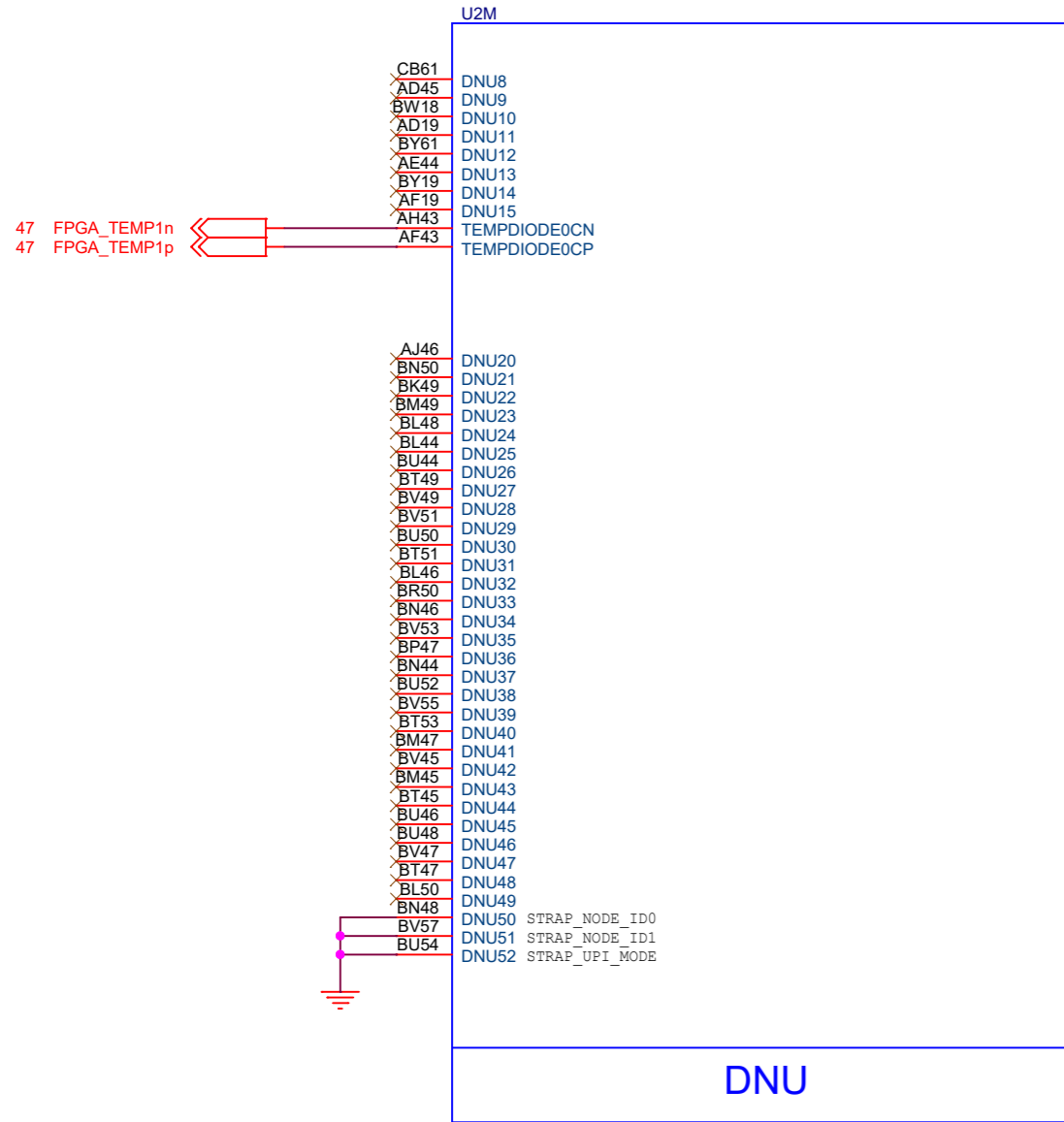
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 1	30 of 66

eMMC



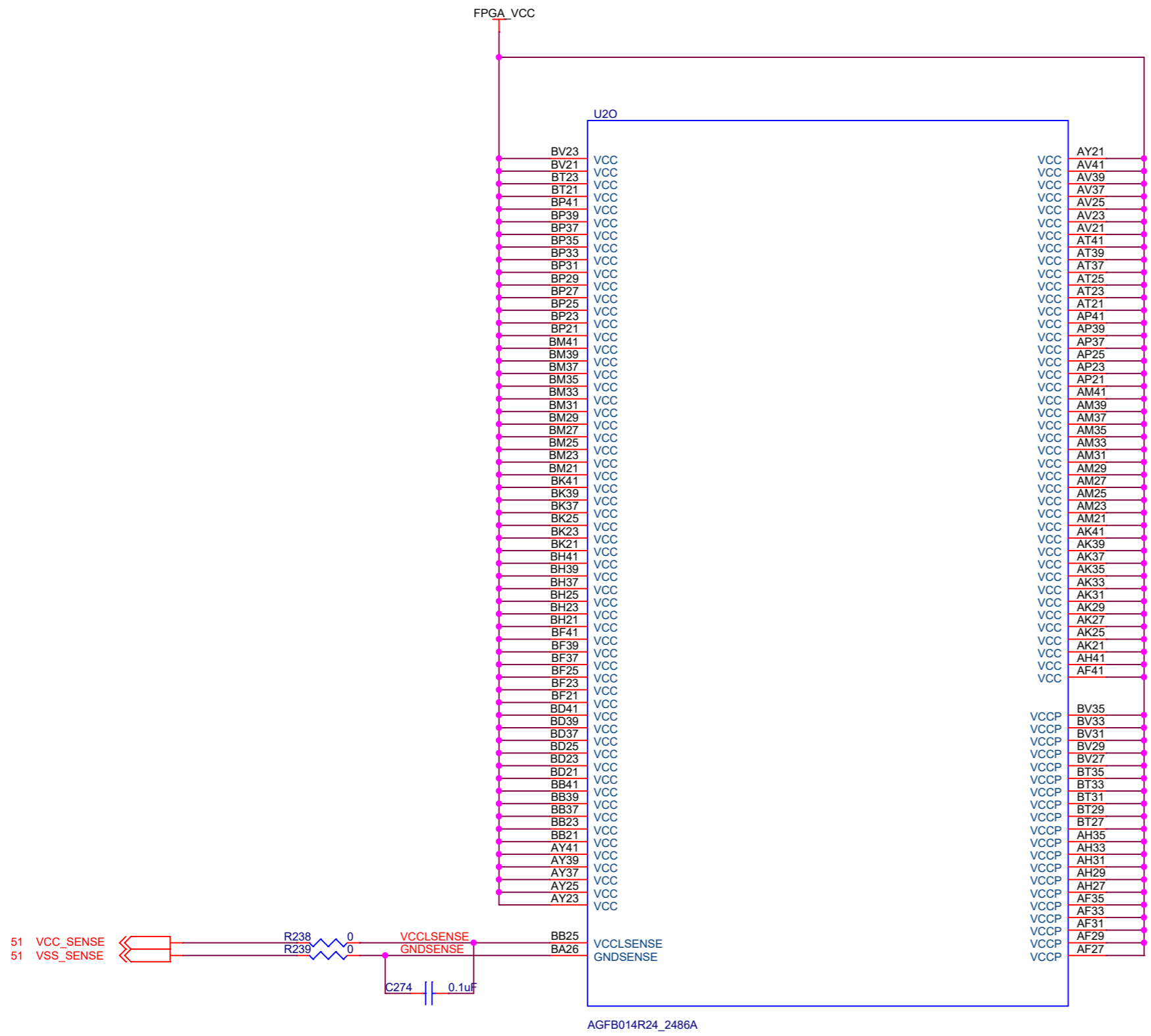
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 31 of 66

Bank NC/DNU

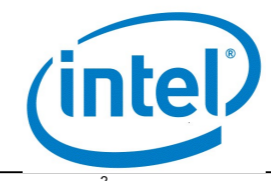


Intel Corporation, 101 Innovation Dr., San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 32 of 66

FPGA Power 1

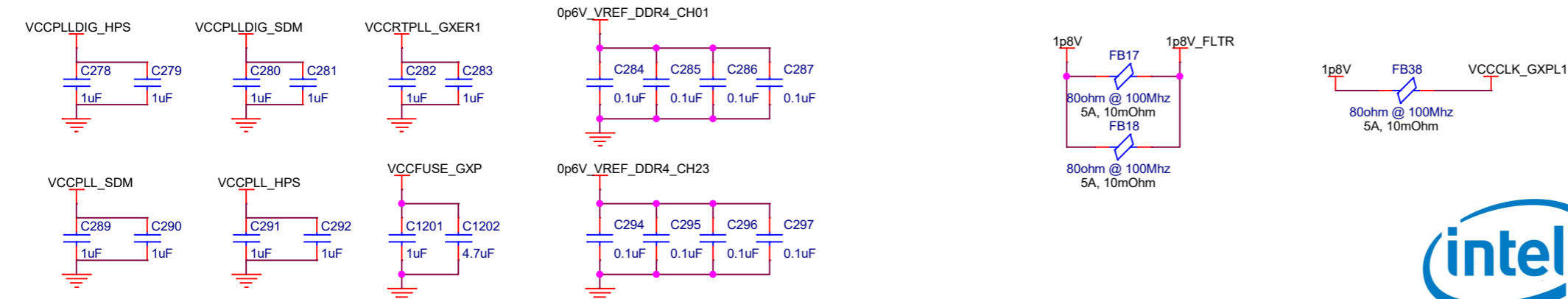
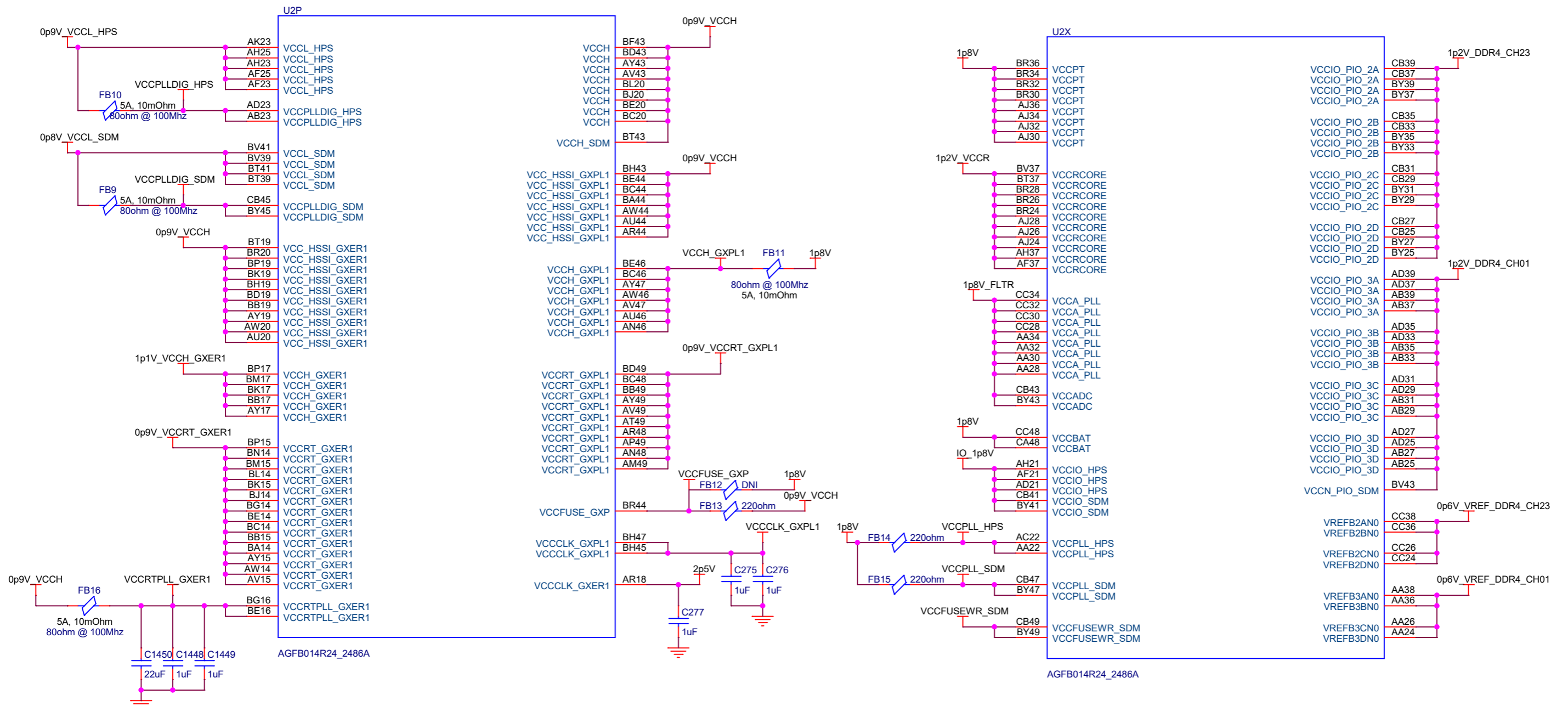


AGFB014R24_2486A



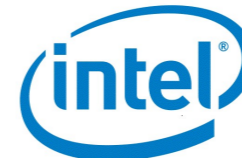
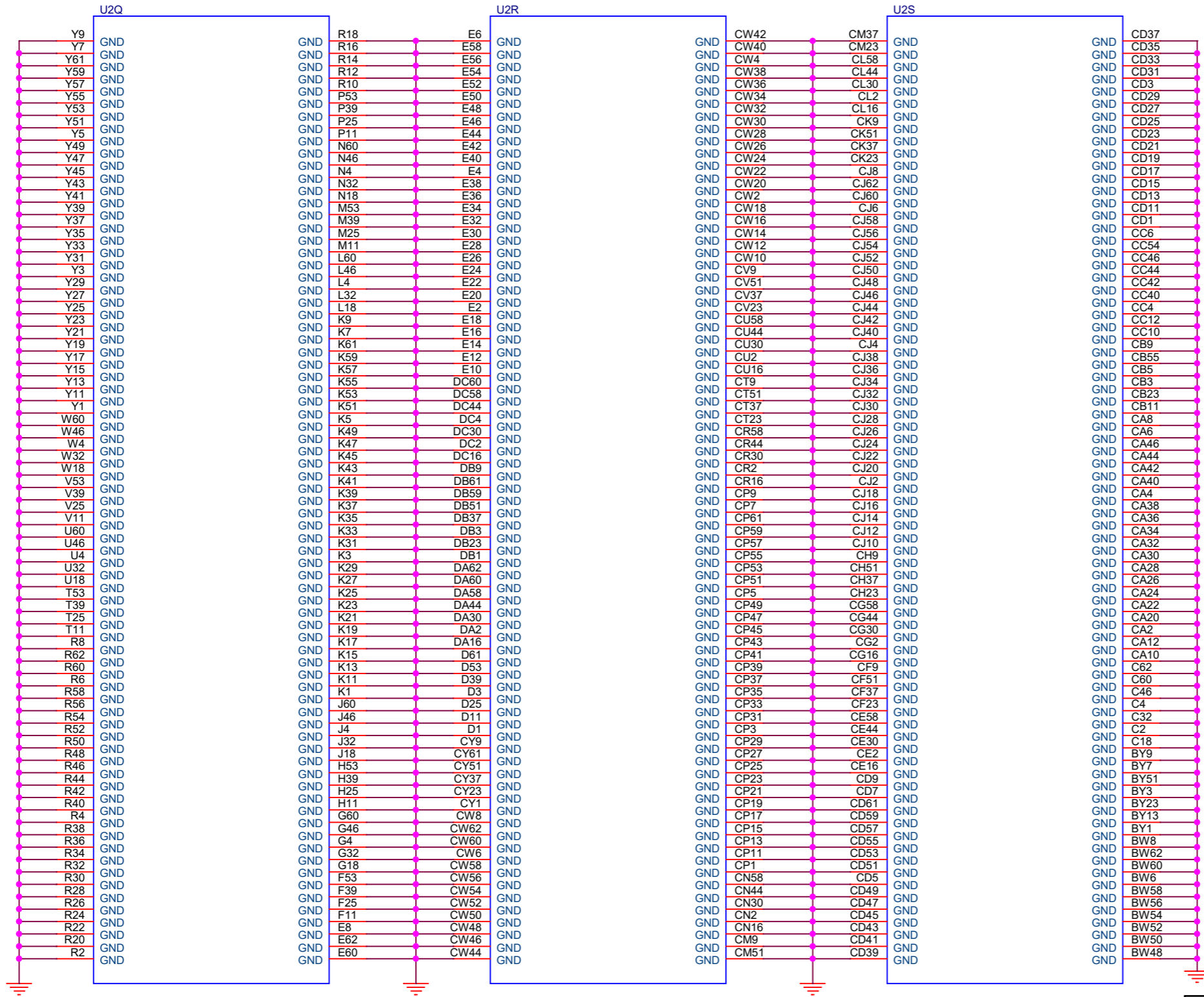
Intel Corporation, 101 Innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 33 of 66

FPGA Power 2



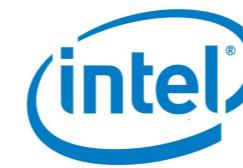
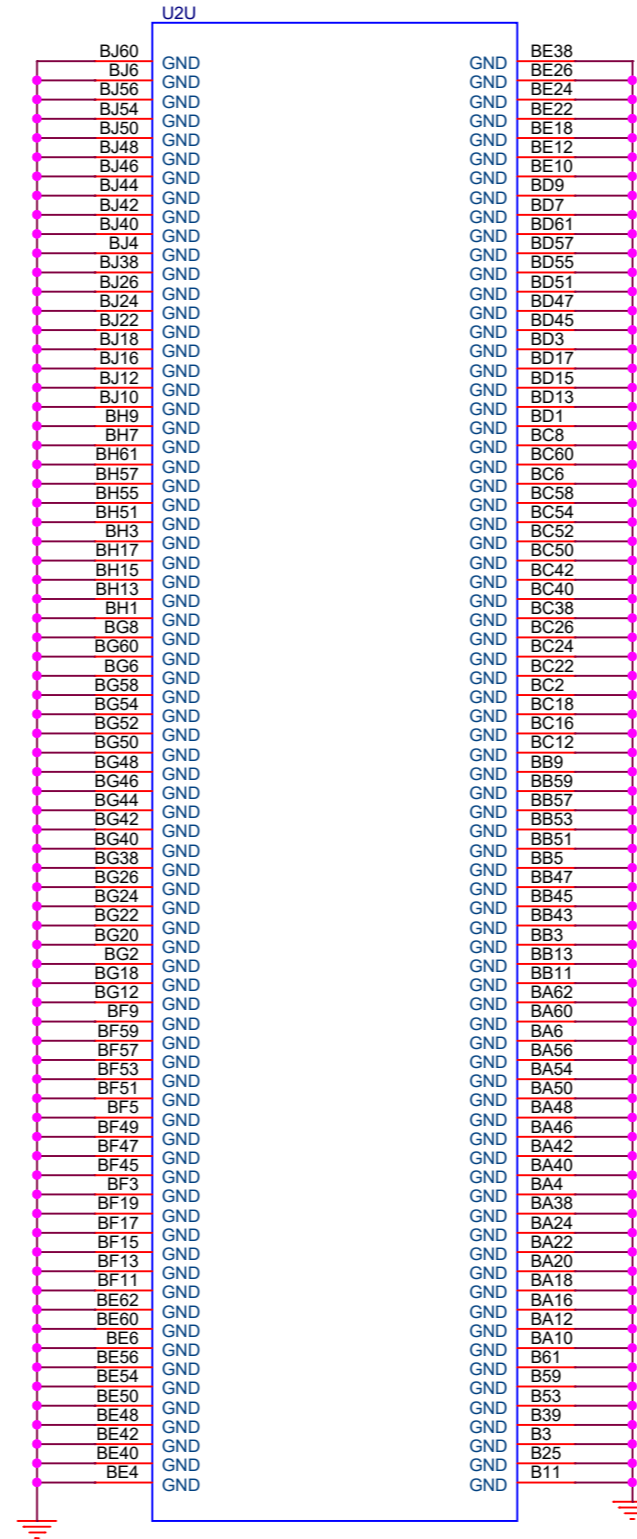
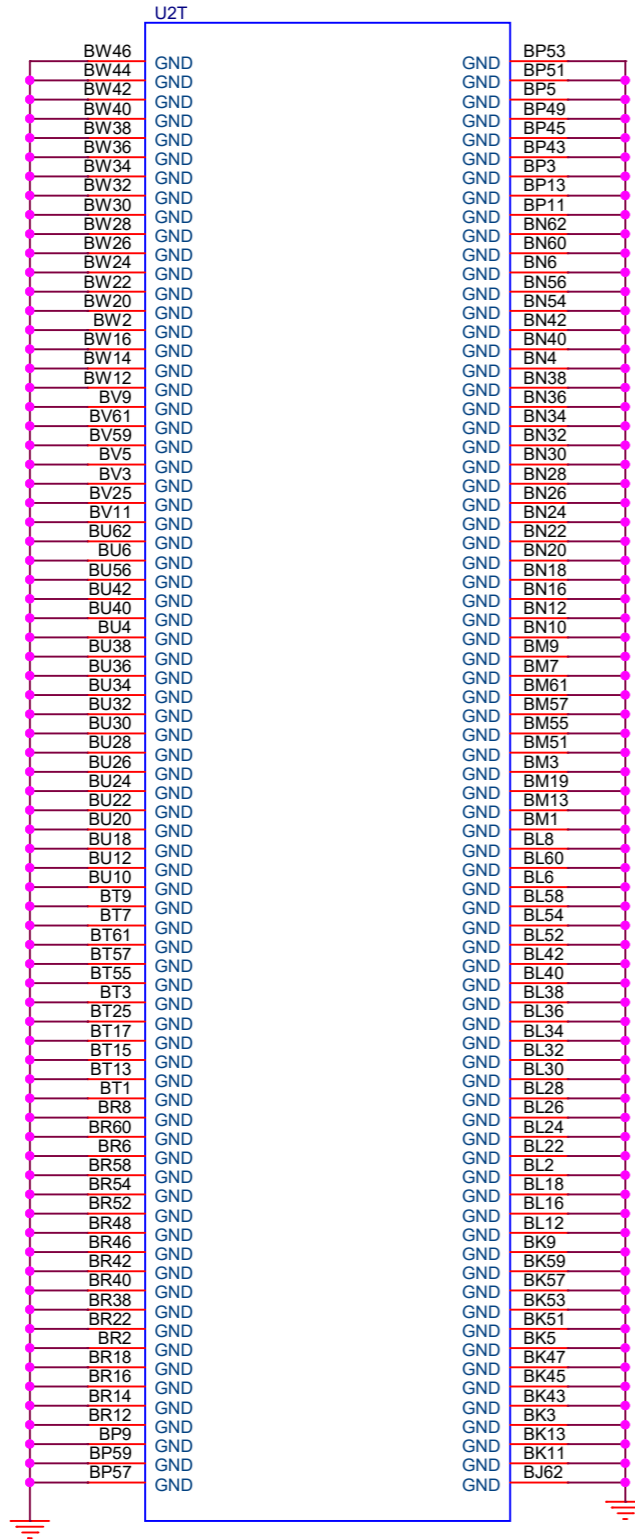
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date Friday, January 10, 2020	Rev A0
Sheet 1	34 of 66

FPGA GND 1



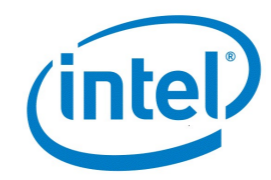
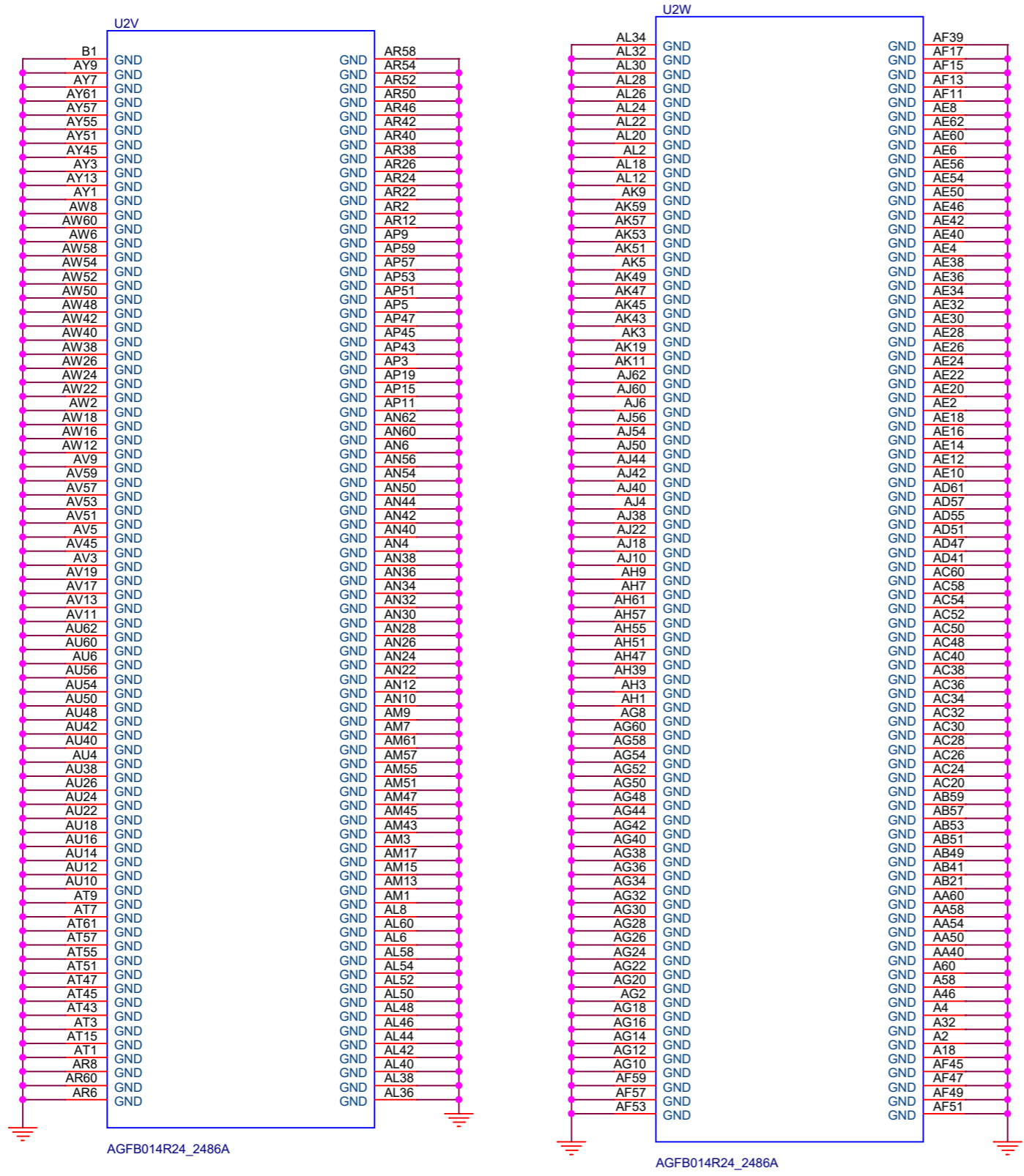
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 35 of 66

FPGA GND 2



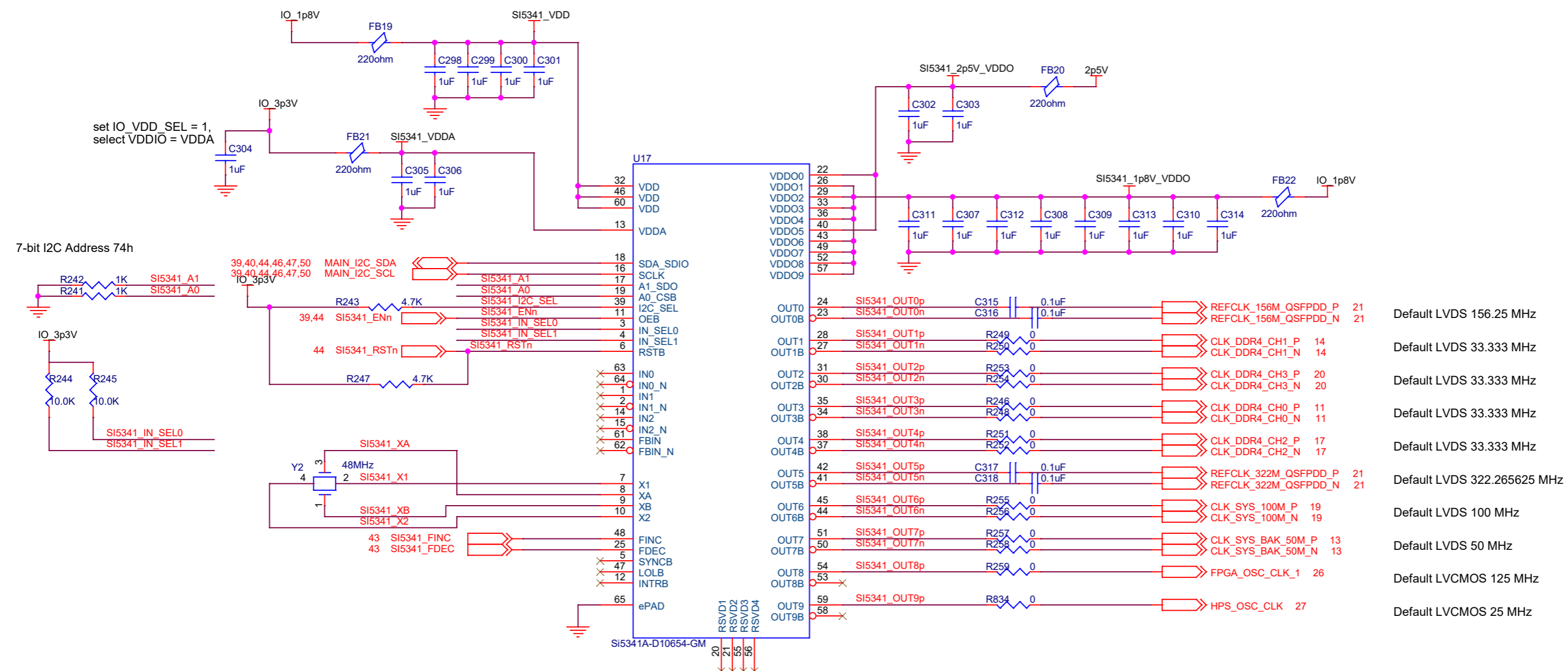

Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 36 of 66

FPGA GND 3



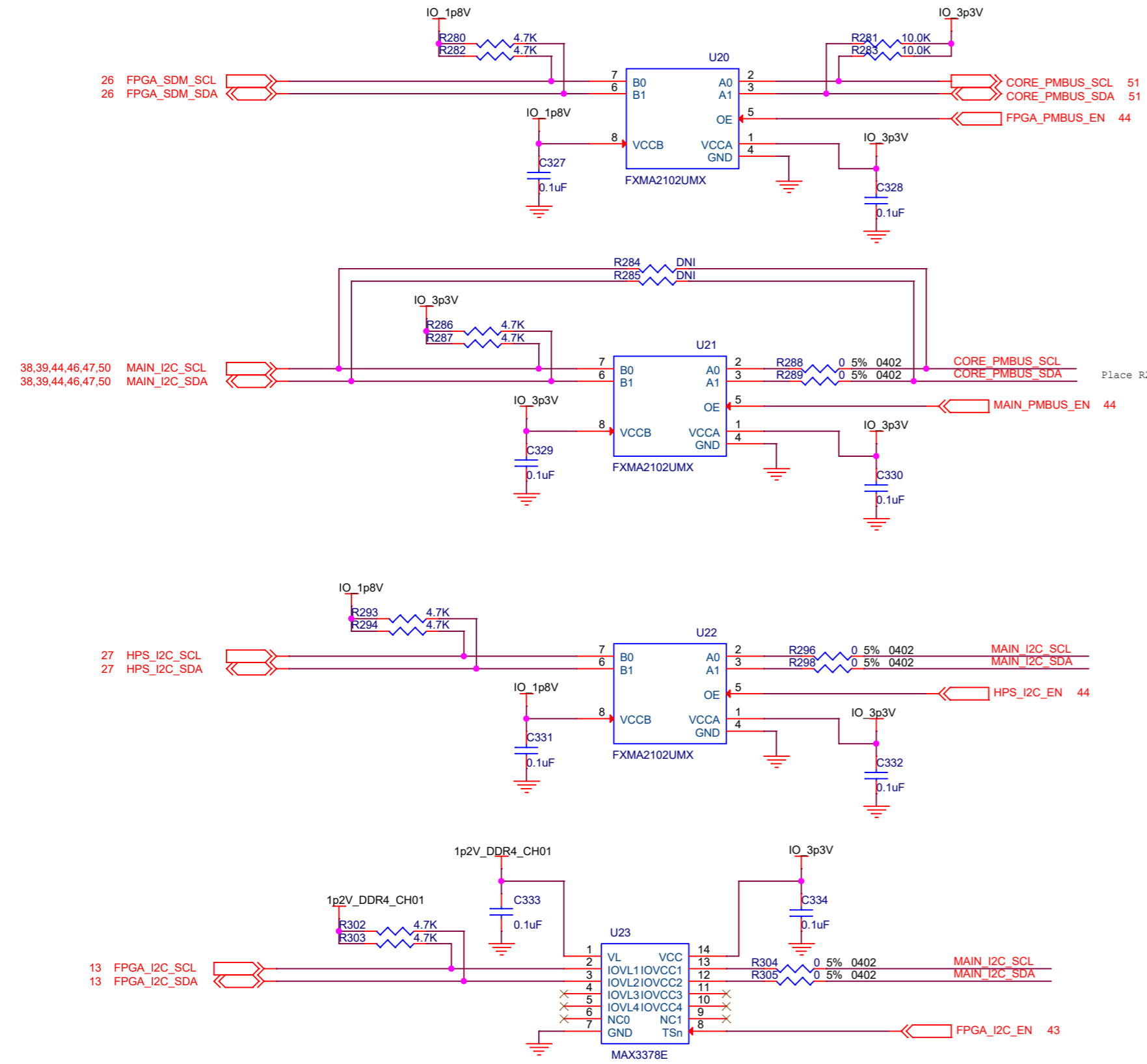
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 37 of 66

Clock 1

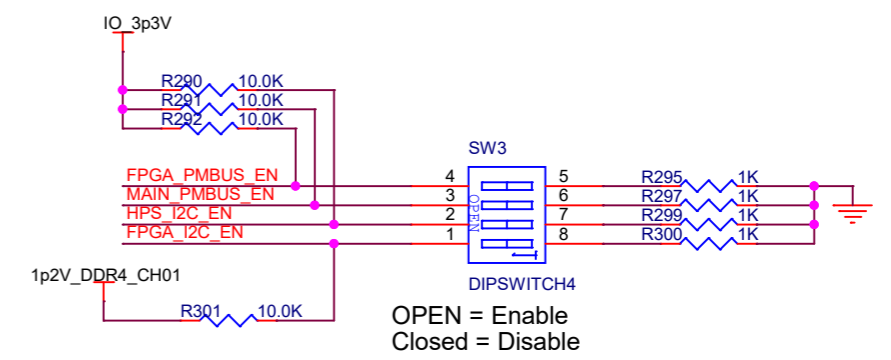



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	38 of 66
Rev	A0

I2C And PMBUS

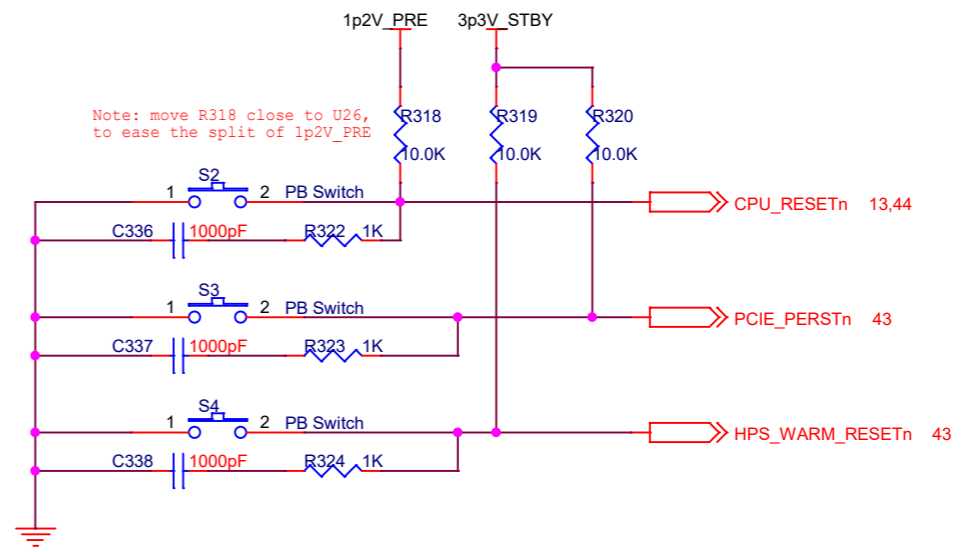
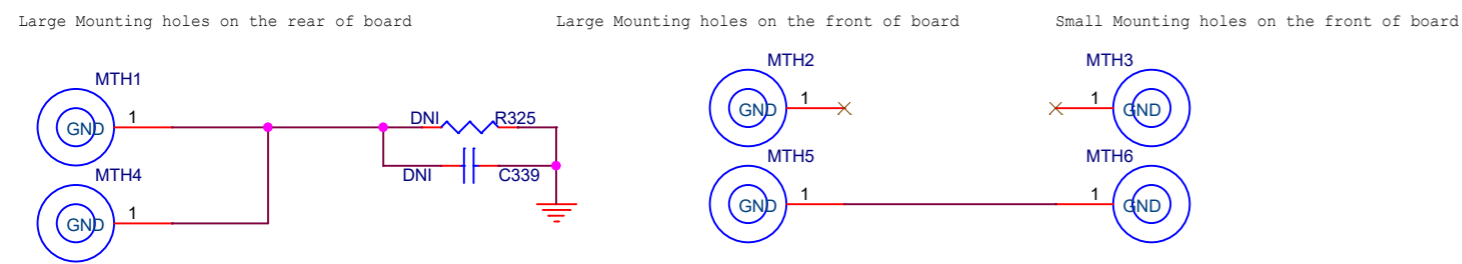
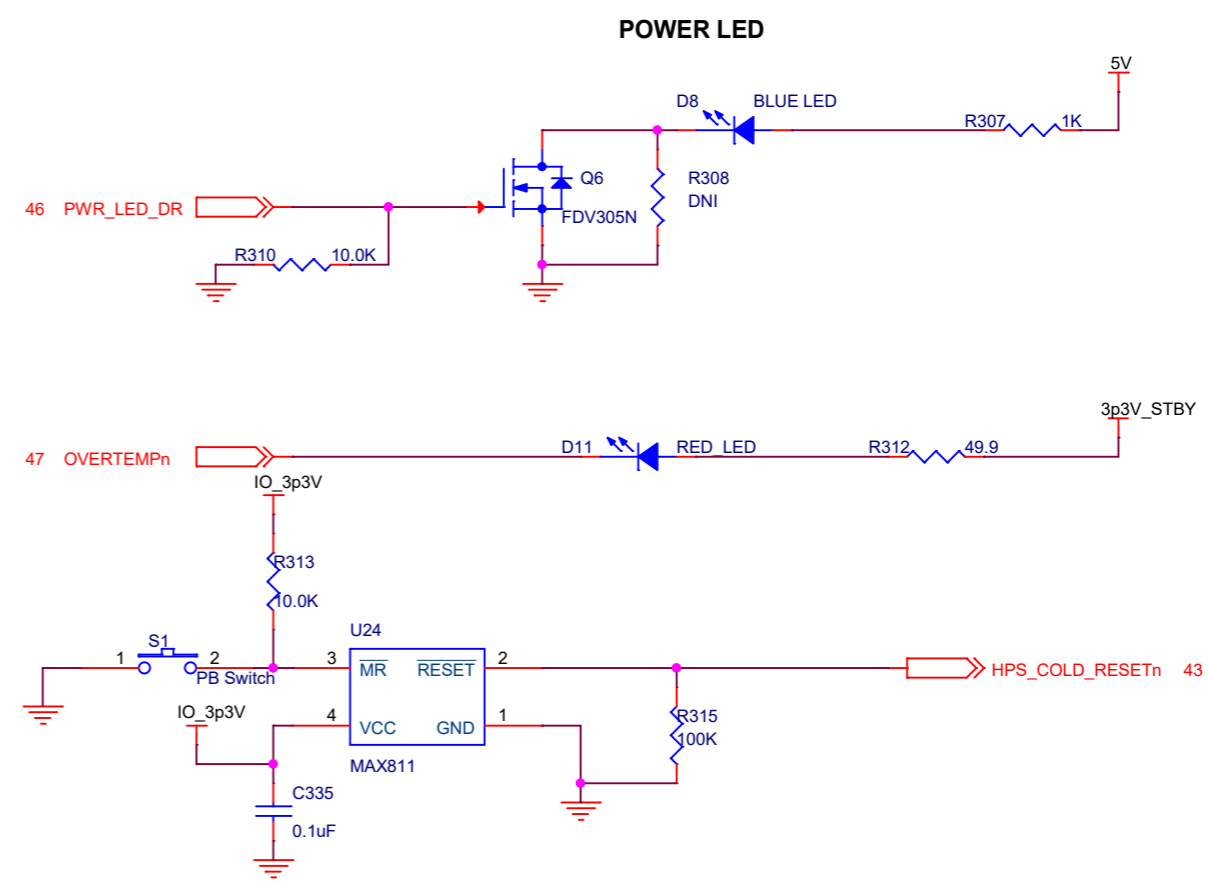
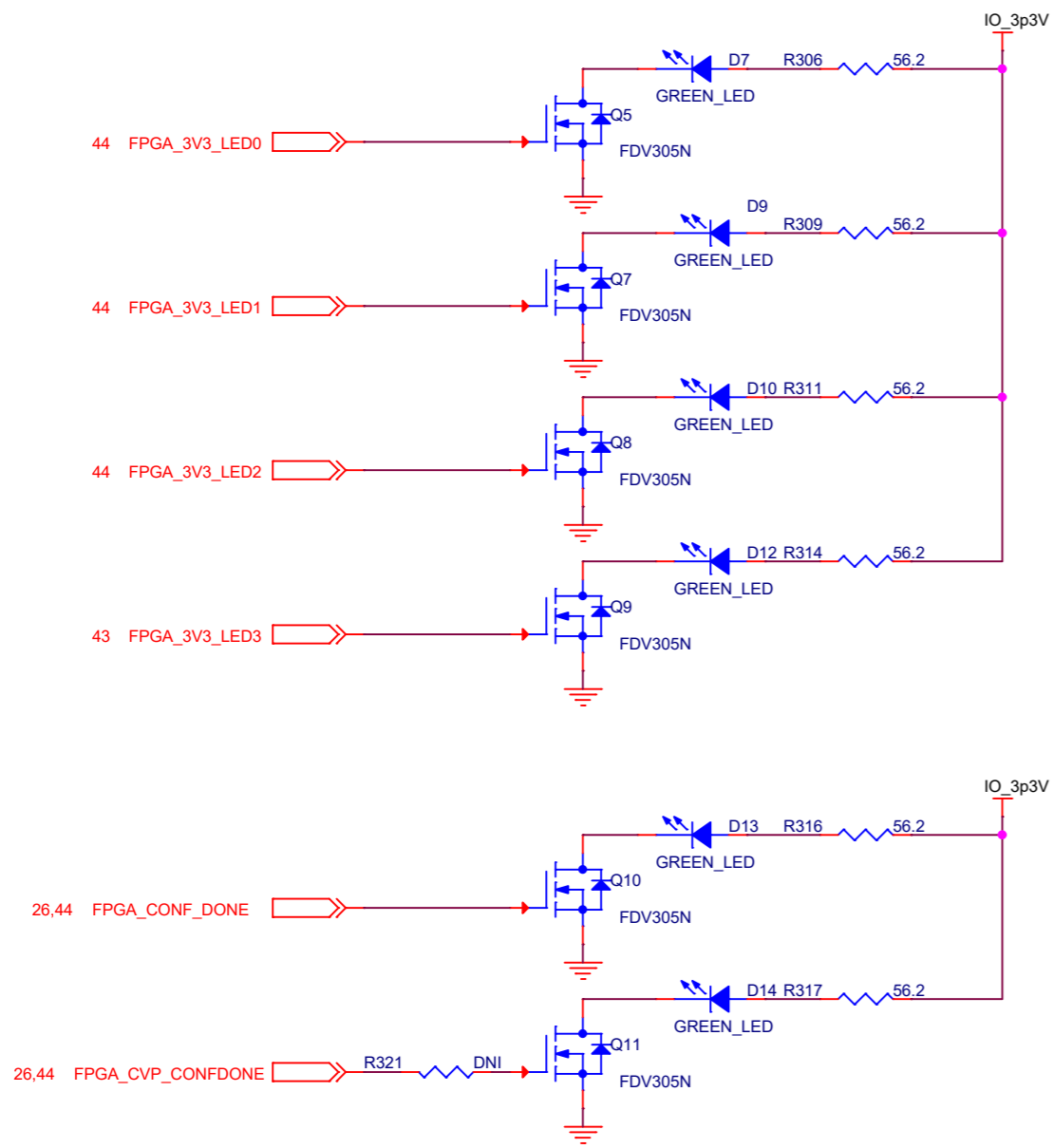


Place R288, R289 near to U20



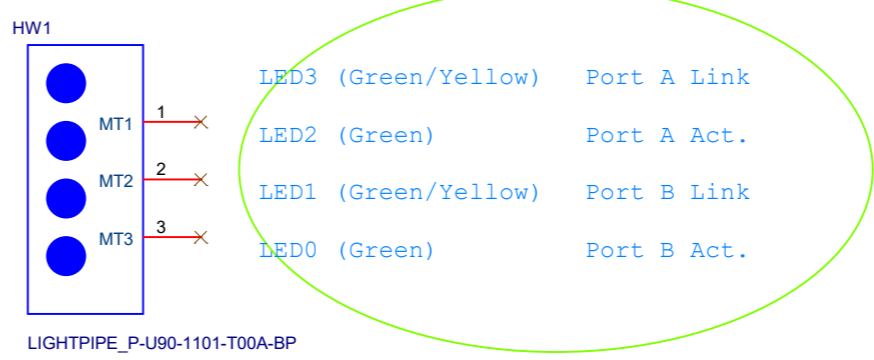
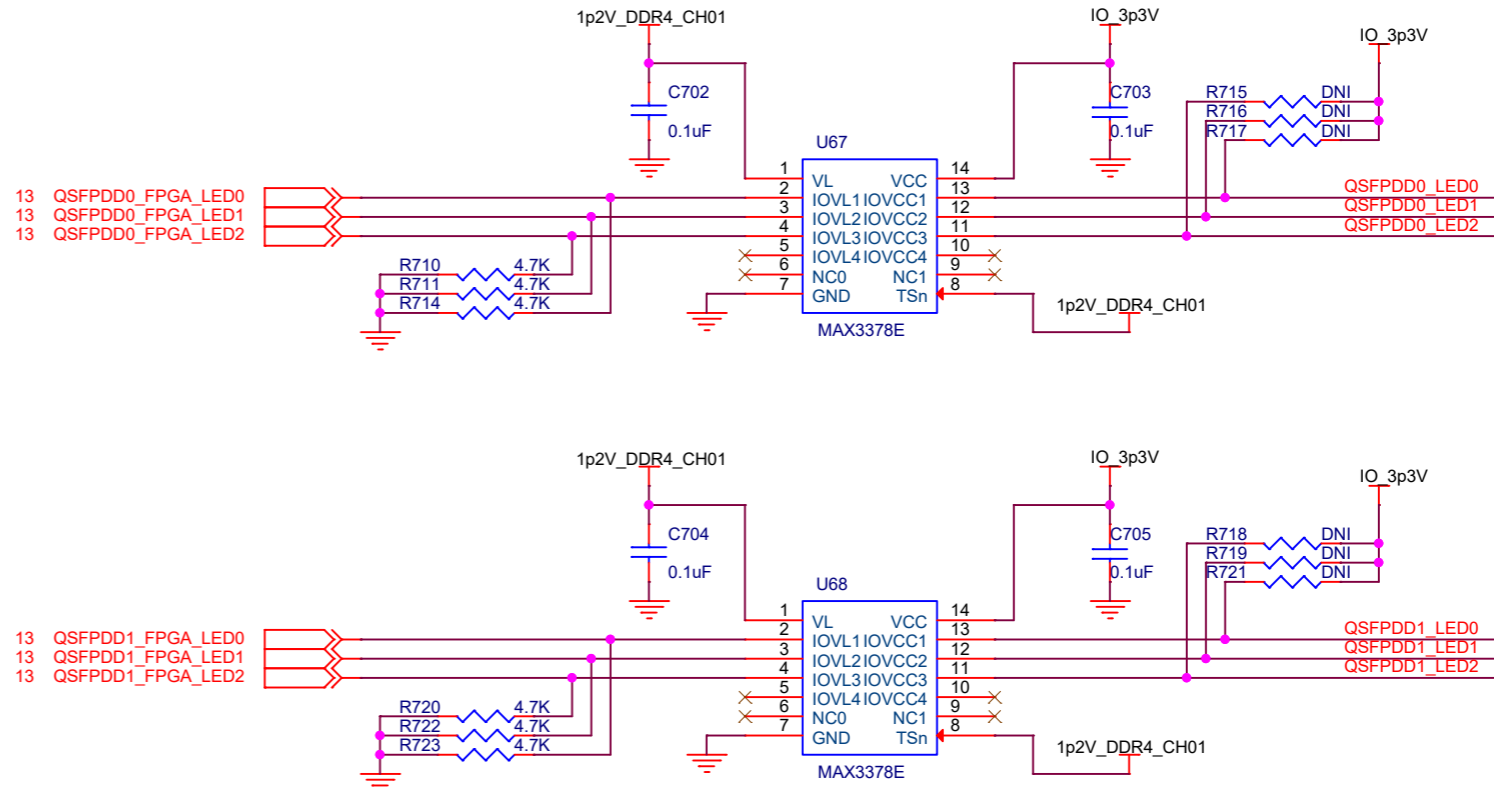
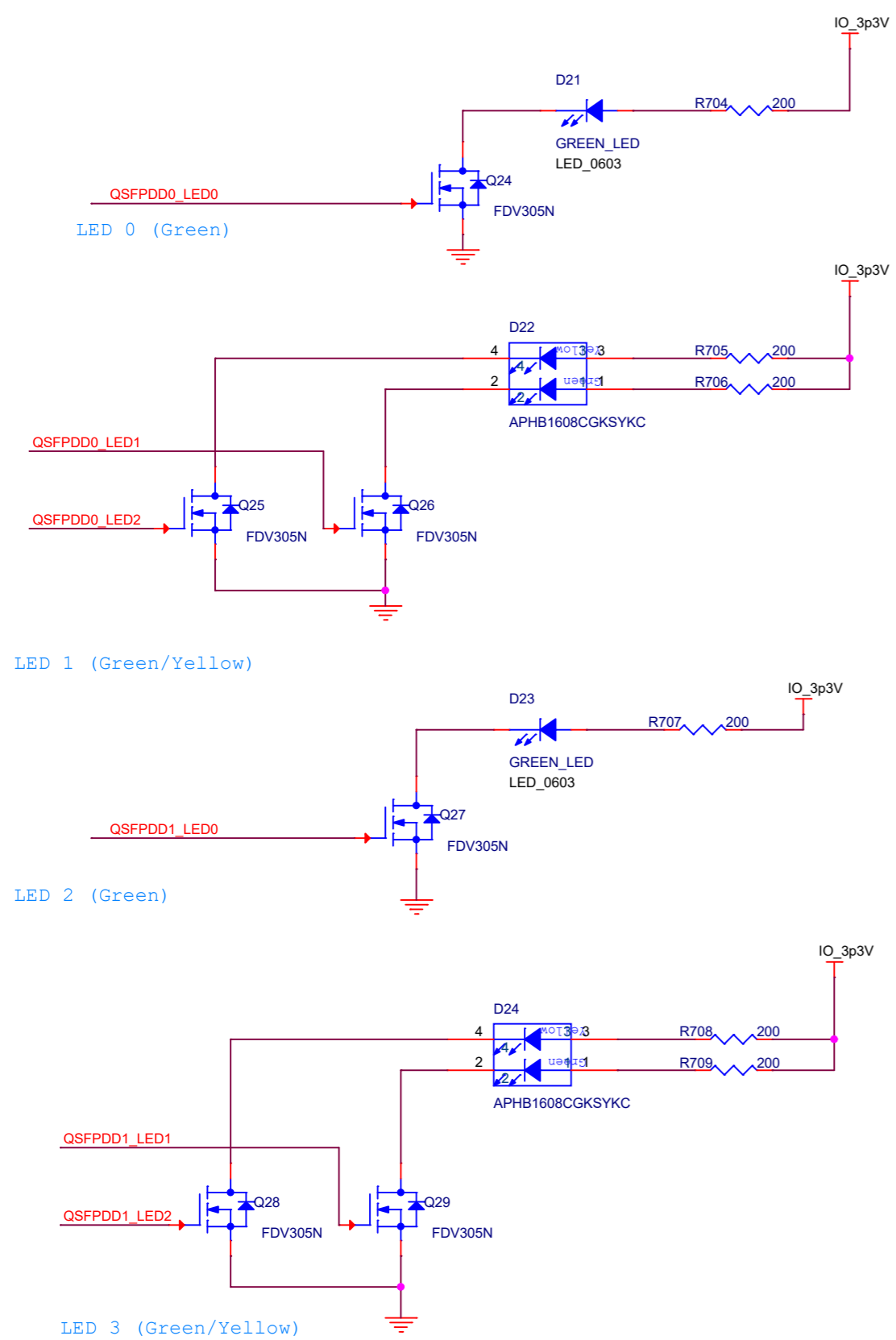
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 40	of 66

LEDs And PushButtons



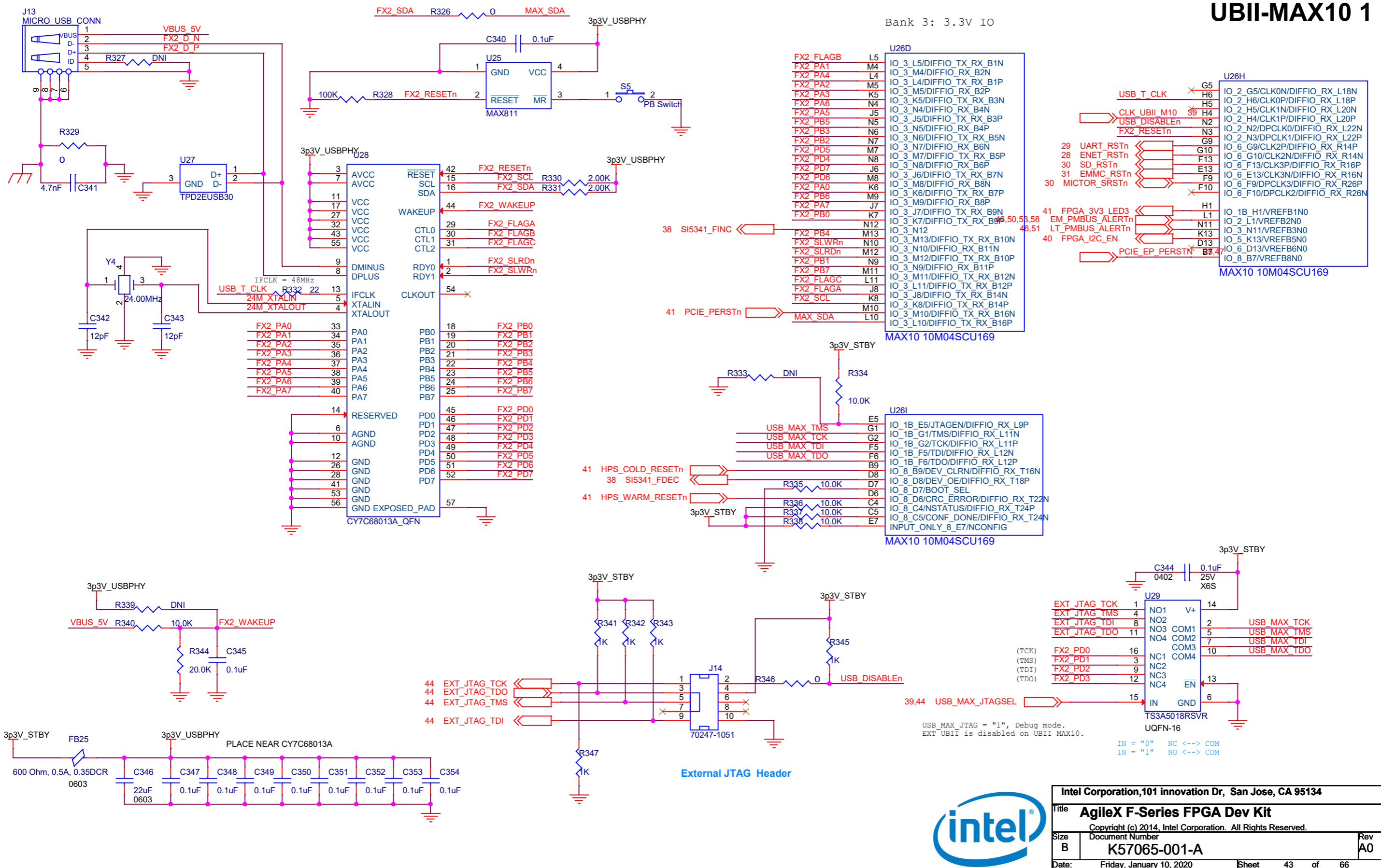
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 41	of 66

QSFPDD LED



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Sheet 42 of 66
	Rev A0

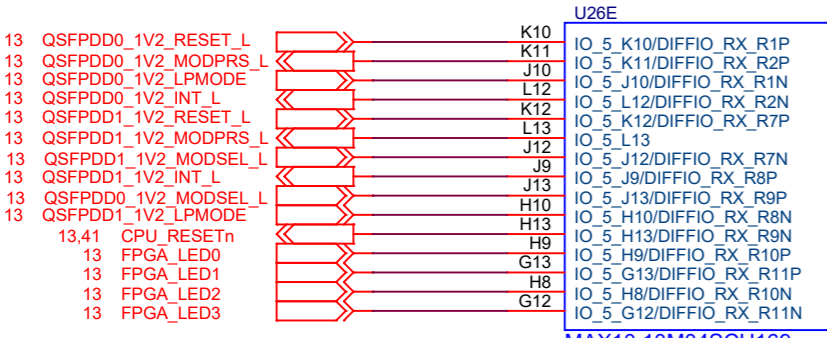
UBII-MAX10 1



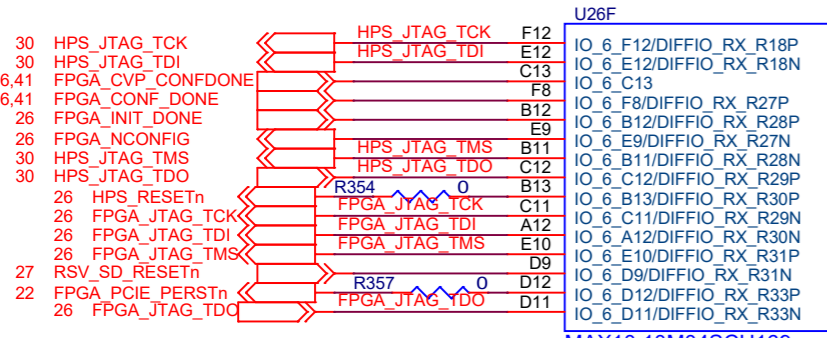
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	43 of 66
Rev	A0

UBII-MAX10 2

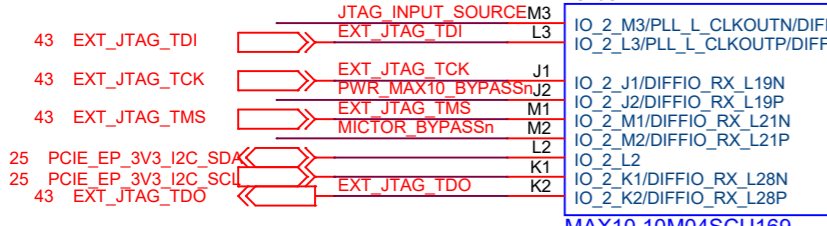
Bank 5: 1.2V IO



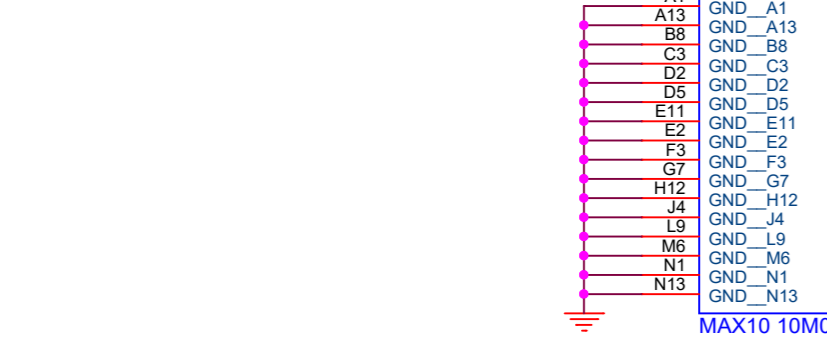
Bank 6: 1.8V IO



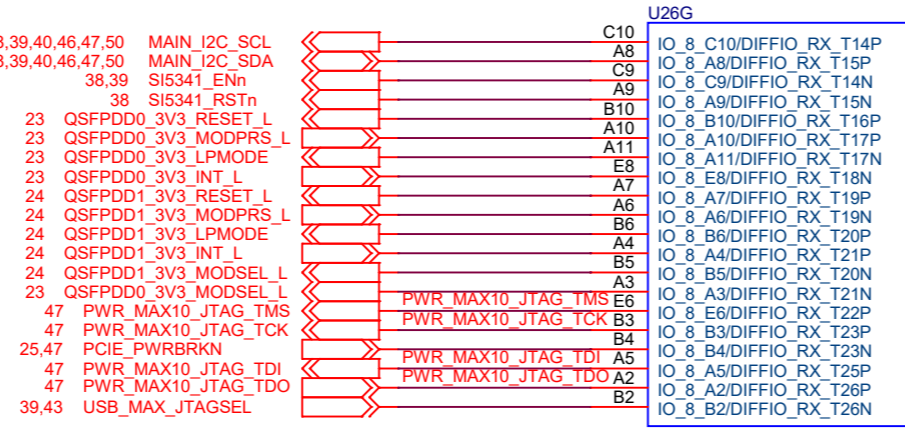
Bank 2: 3.3V IO



Bank 1A/1B: 3.3V IO

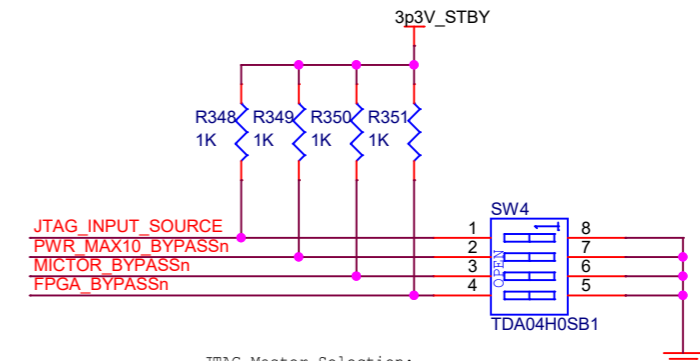
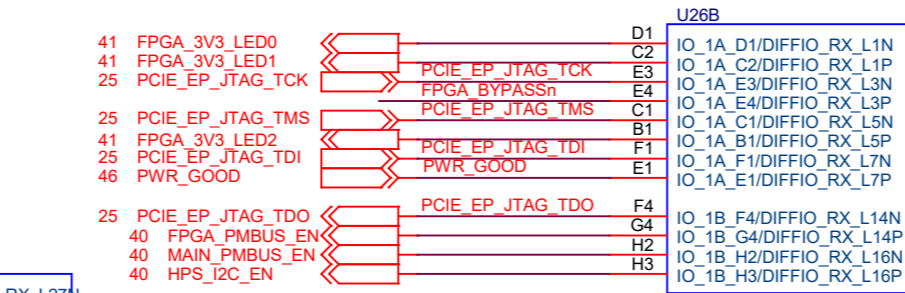


Bank 8: 3.3V IO



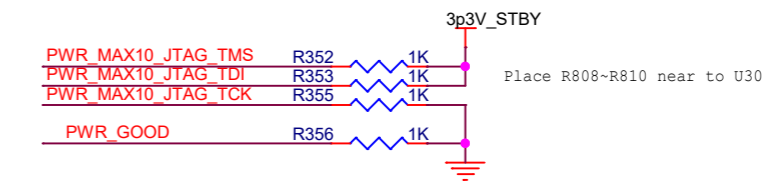
USB_MAX_JTAG = "1", Debug mode.
EXT_UBII is disabled on UBII MAX10.

Bank 1A/1B: 3.3V IO

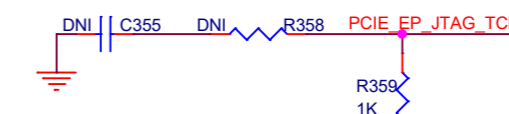
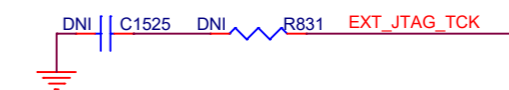


JTAG Master Selection:
USB_DISABLEn = 0: External JTAG
USB_DISABLEn = 1: On-Board UBII/PCie EP Edge
JTAG_INPUT_SOURCE = 0: PCie EP edge
JTAG_INPUT_SOURCE = 1: On-Board UBII

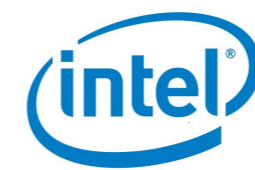
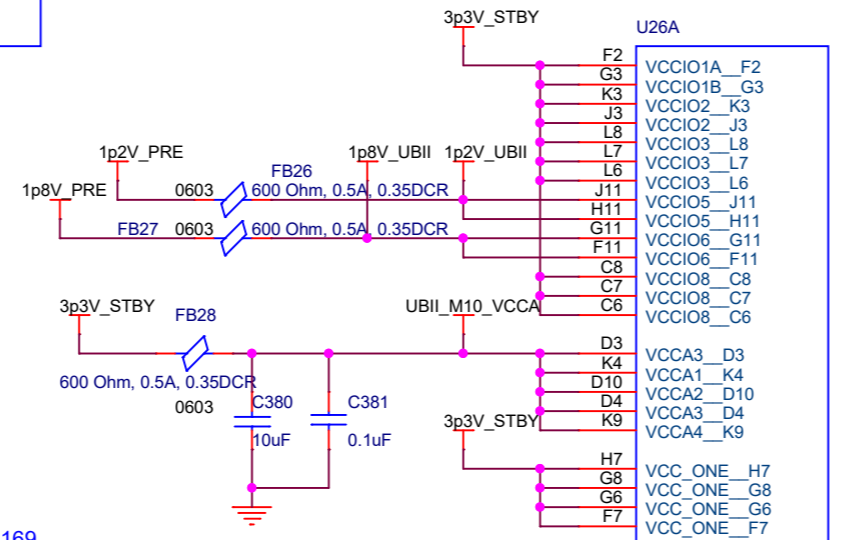
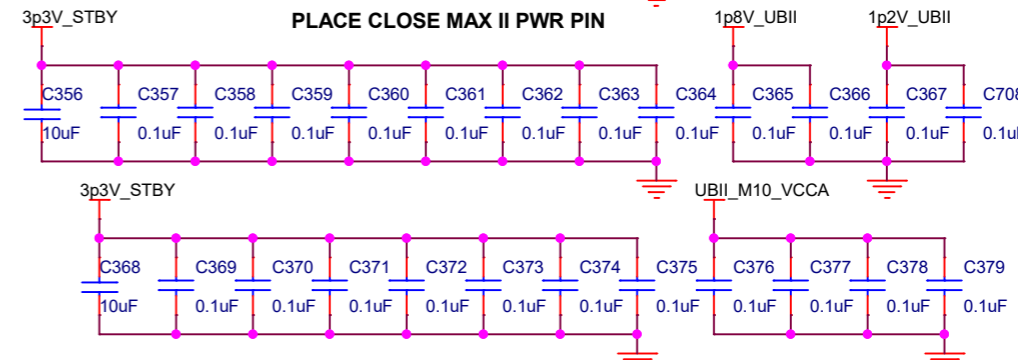
JTAG Chain:
SW4_2/3/4 = Low : Bypass
SW4_2/3/4 = High: Enable



Place R808-R810 near to U30



PLACE CLOSE MAX II PWR PIN



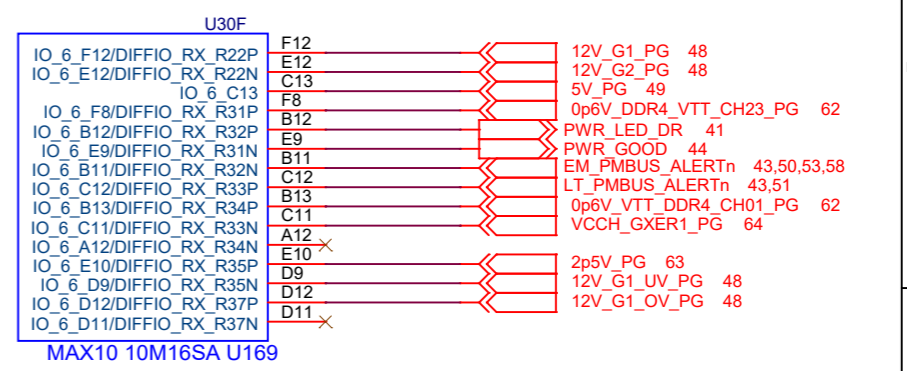
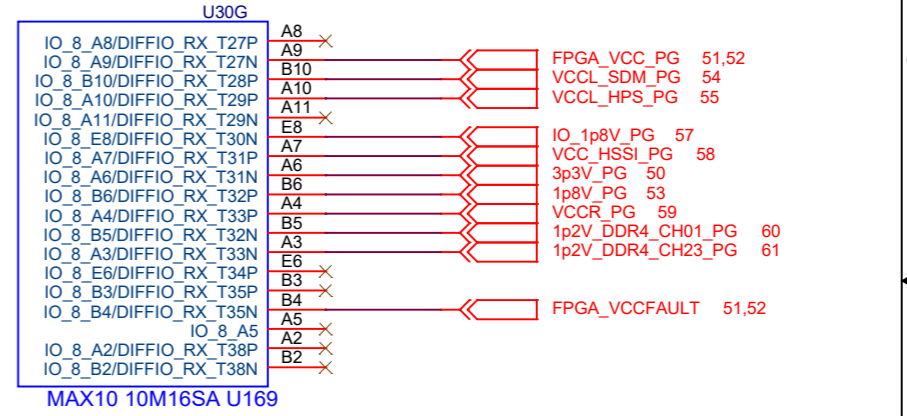
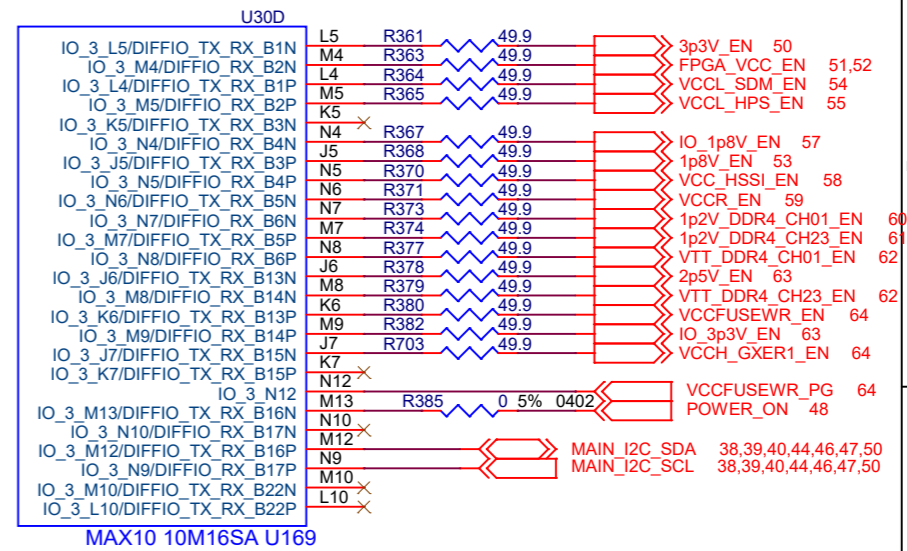
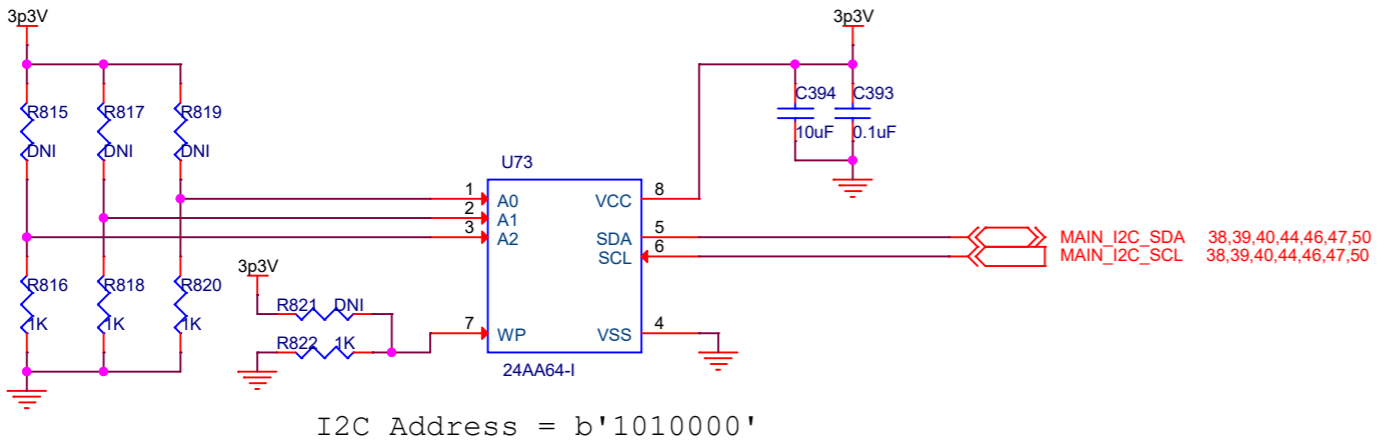
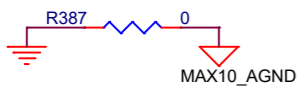
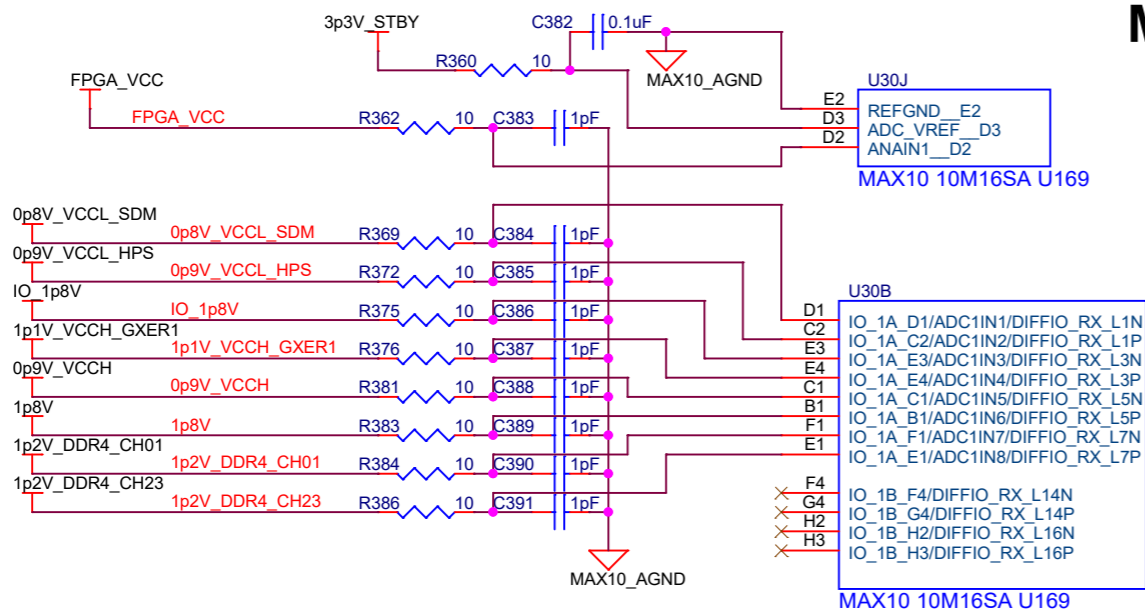
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 44	of 66

BLANK



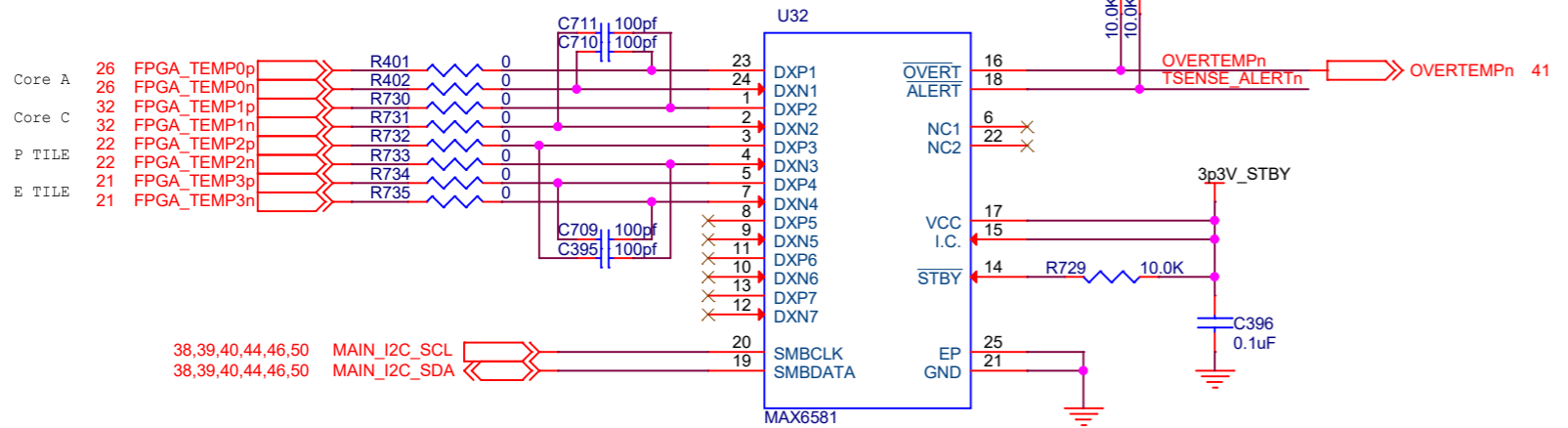
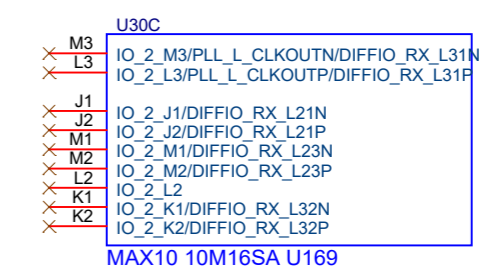
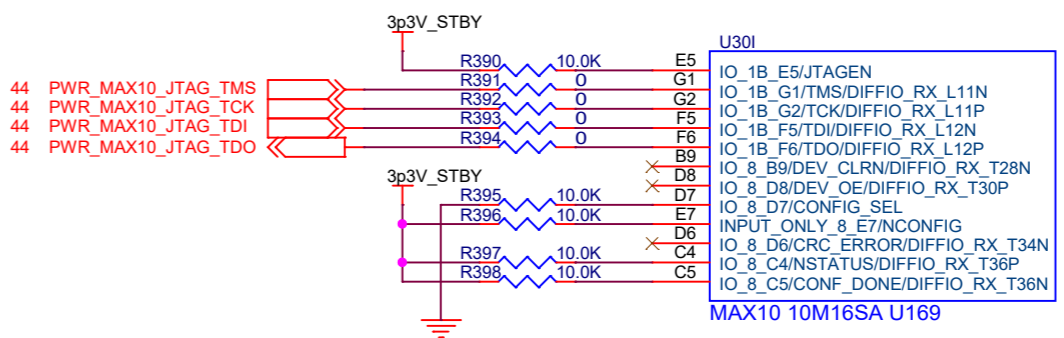
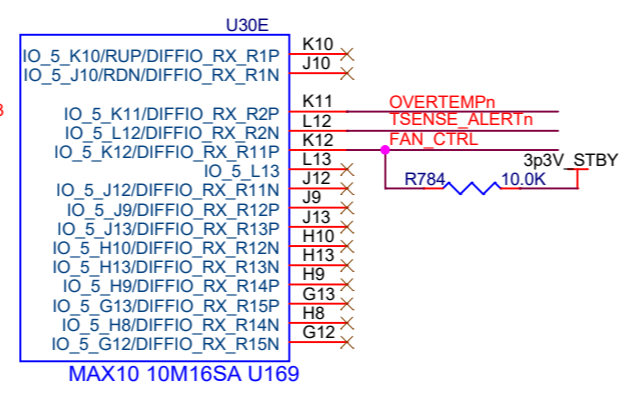
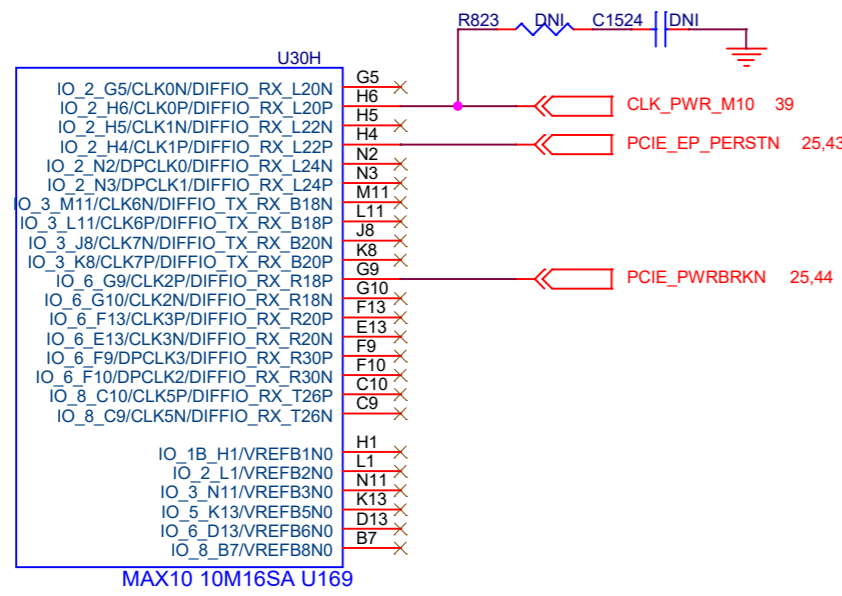
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 45 of 66

MAX 10 PWR Manager 1

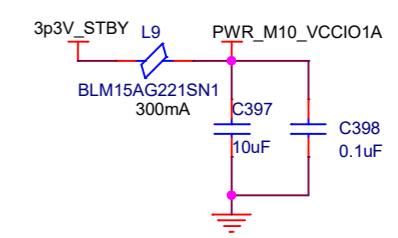
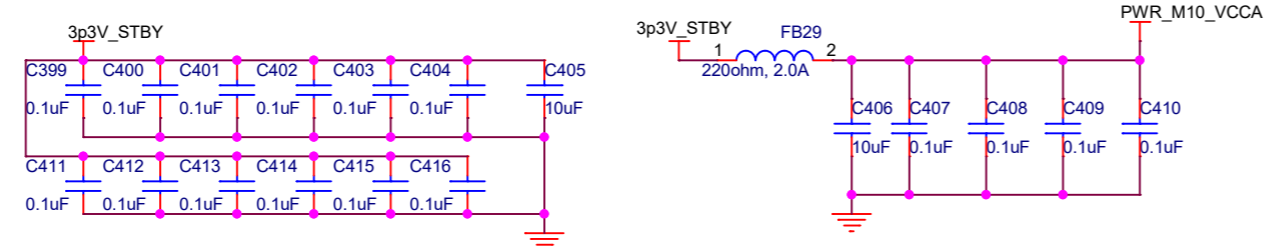
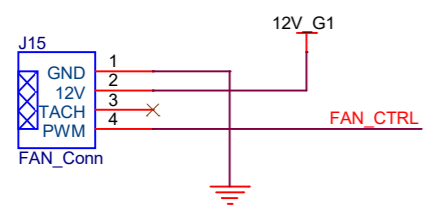
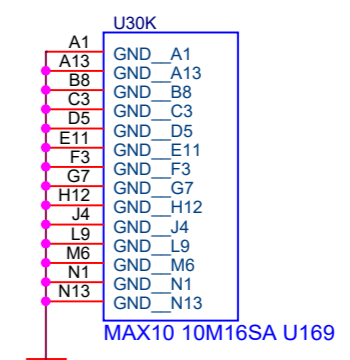
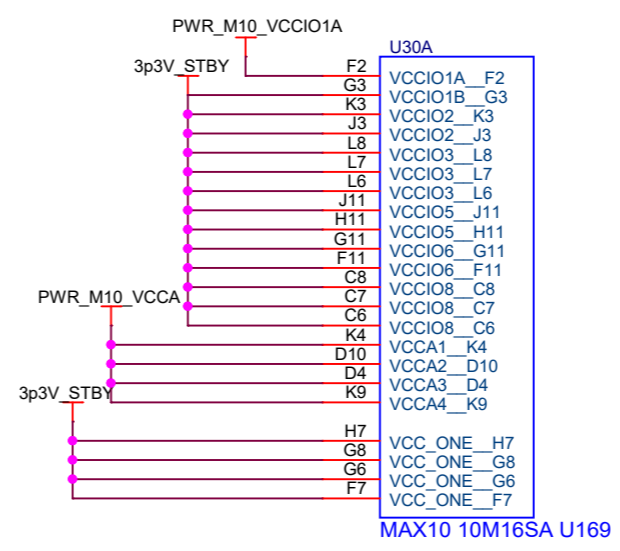


Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size	Document Number
B	K57065-001-A
Date:	Friday, January 10, 2020
Sheet	46 of 66
Rev	A0

MAX10 PWR Manager 2

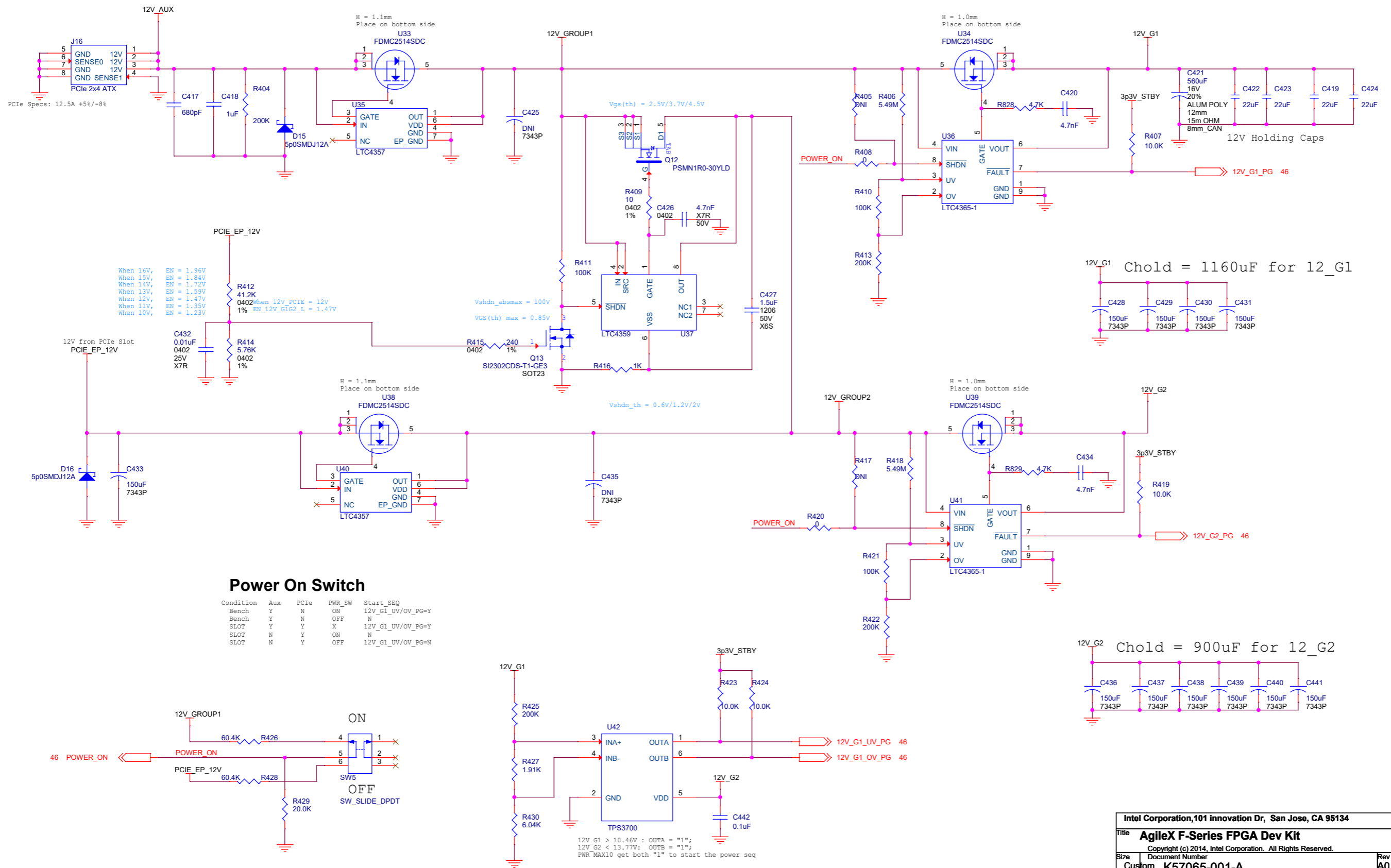


I2C ADDR = 4D
Board Temp Sensor



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 47	of 66

Power - Select Power Input



Power On Switch

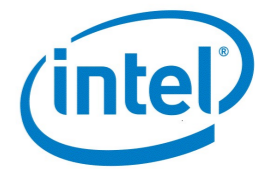
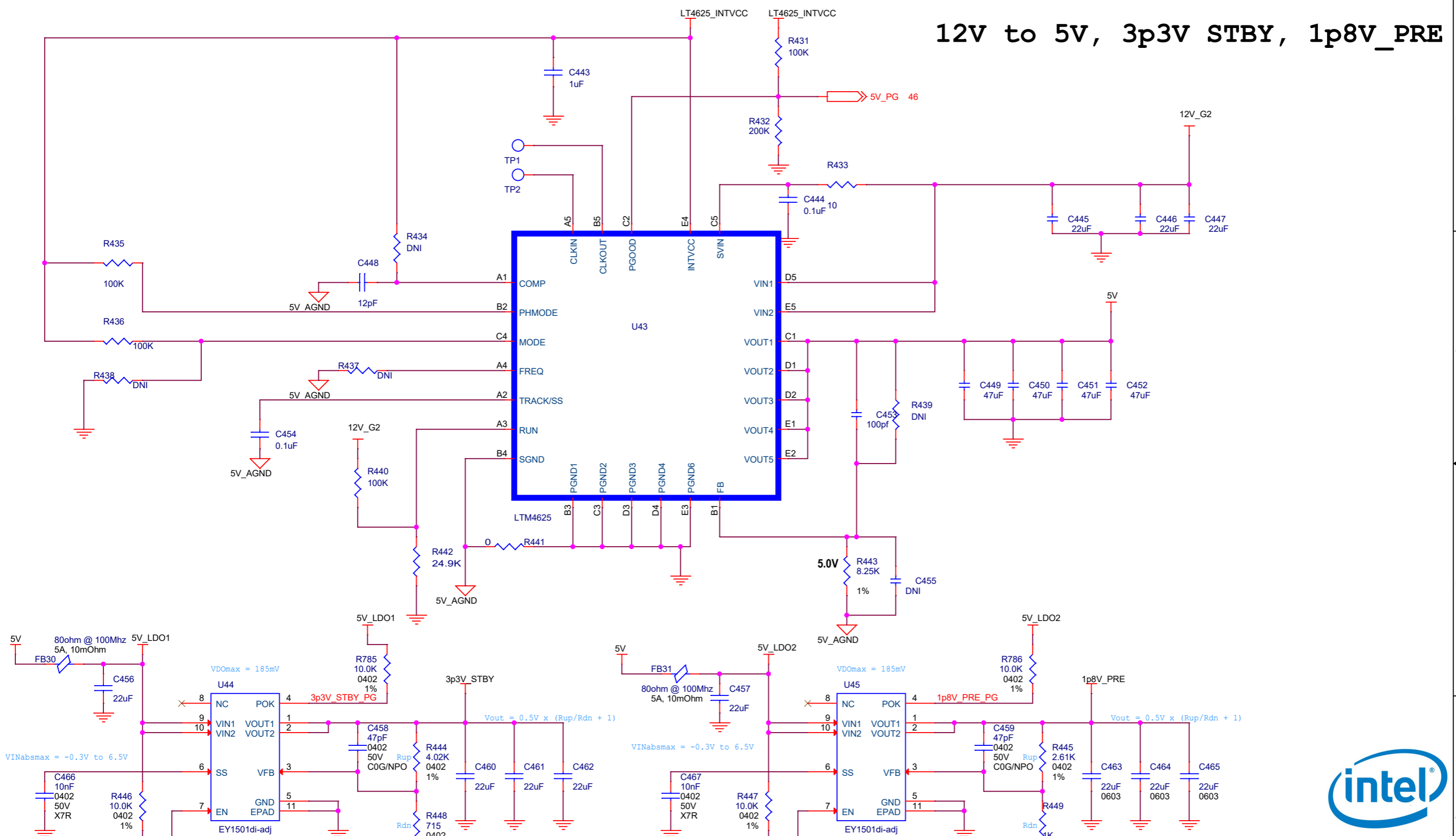
Condition	Aux	PCIe	PWR_SW	Start_SEQ
Bench	Y	N	ON	12V_G1_UV/OV_PG=Y
Bench	Y	N	OFF	N
SLOT	Y	Y	X	12V_G1_UV/OV_PG=Y
SLOT	N	Y	ON	N
SLOT	N	Y	OFF	12V_G1_UV/OV_PG=N

12V_G1 > 10.46V : OUTA = "1";
 12V_G2 < 13.77V: OUTB = "1";
 PWR MAX10 get both "1" to start the power seq

Intel Corporation, 101 Innovation Dr., San Jose, CA 95134			
Title: AgileX F-Series FPGA Dev Kit			
Copyright (c) 2014, Intel Corporation. All Rights Reserved.			
Size	Document Number	Rev	
Custom	K57065-001-A	A0	
Date:	Friday, January 10, 2020	Sheet	48 of 66

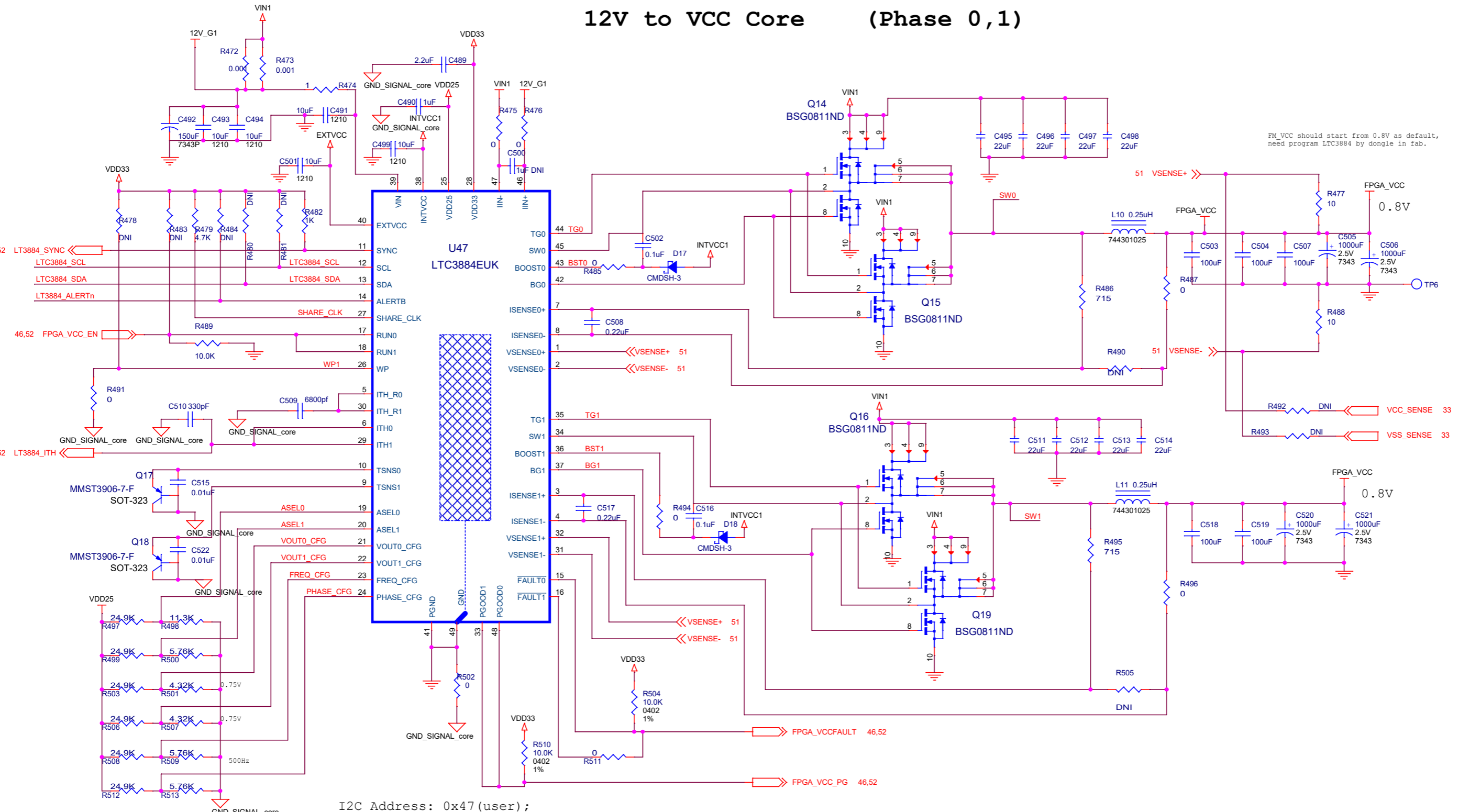


12V to 5V, 3p3V STBY, 1p8V_PRE



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Sheet 49 of 66
	Rev A0

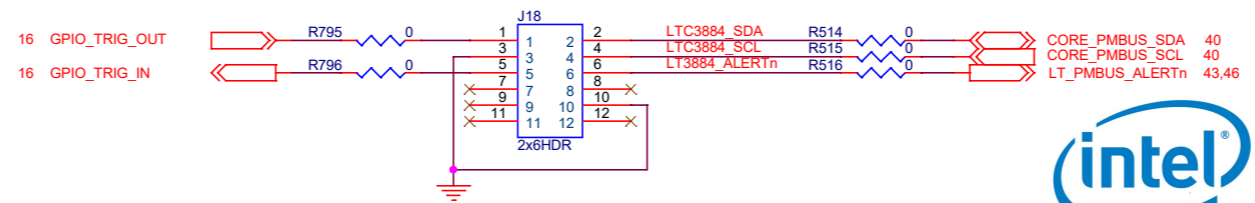
12V to VCC Core (Phase 0,1)



I2C Address: 0x47(user);
0x5A/5B (LTC3884 Global addr)

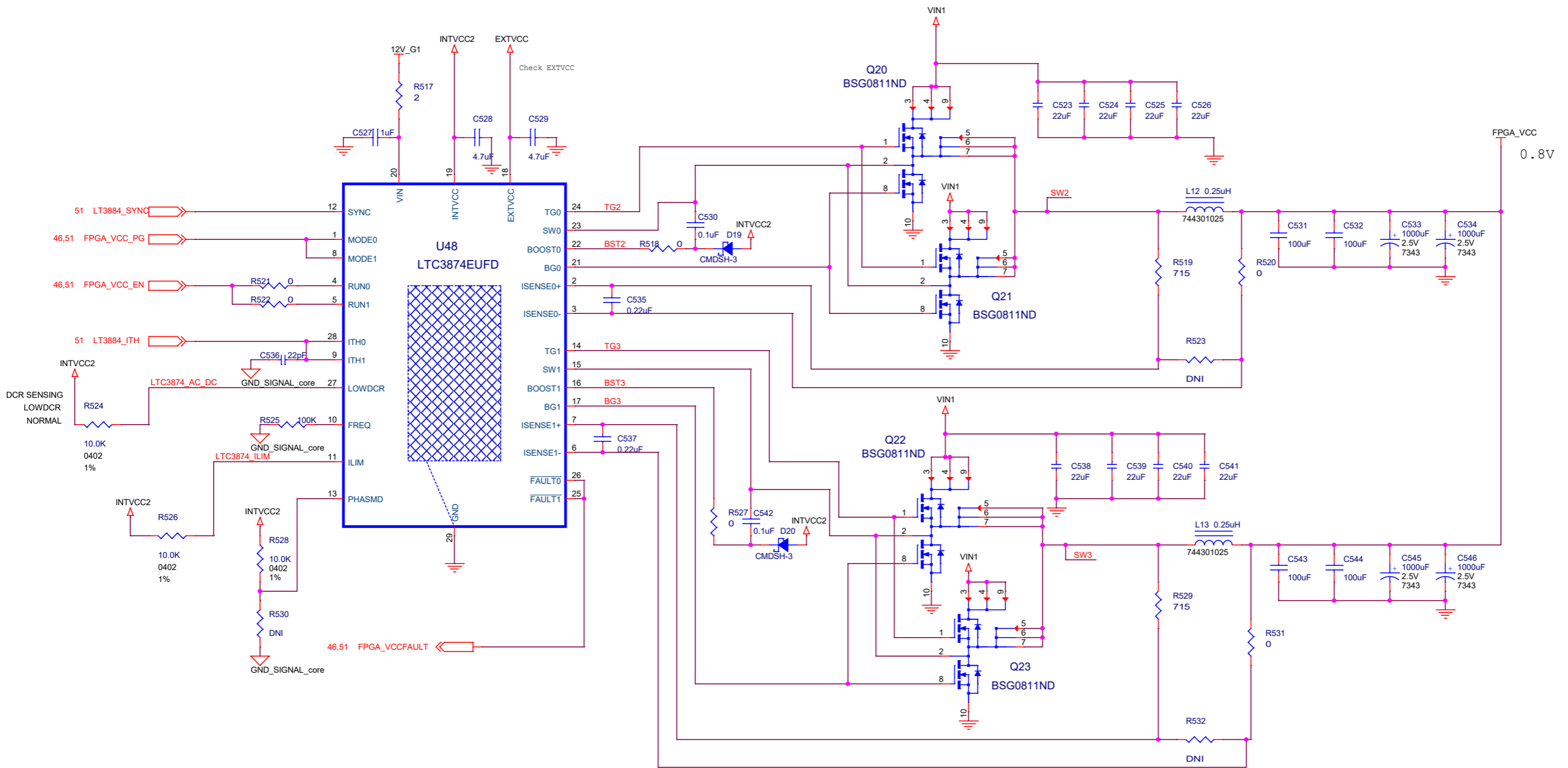
Check Phase define
Need 0.8V core voltage

FM_VCC should start from 0.8V as default,
need program LTC3884 by dongle in fab.



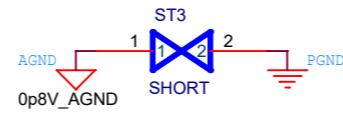
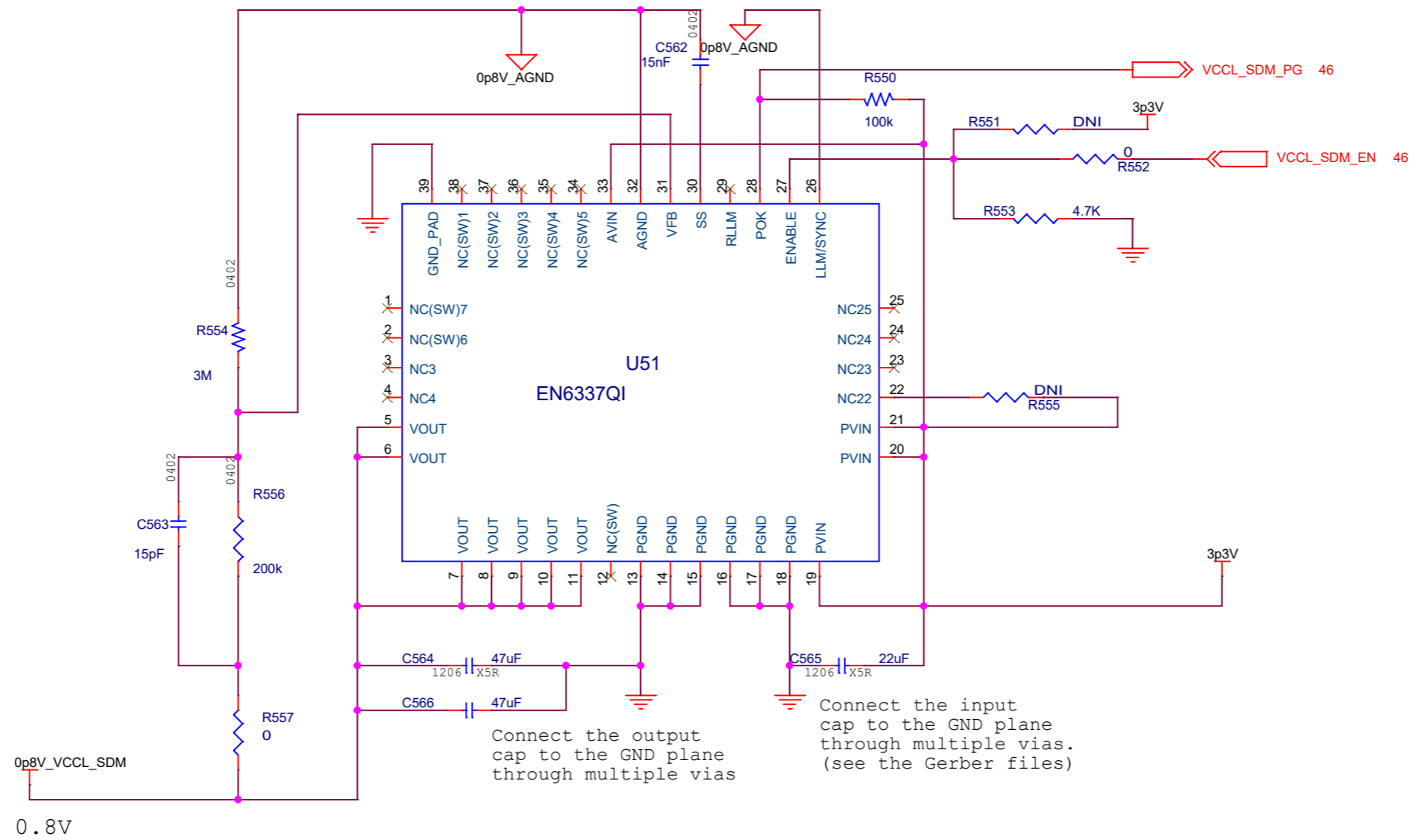
Intel Corporation, 101 Innovation Dr., San Jose, CA 95134	
Title: AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size: Document Number	Rev: A0
Custom: K57065-001-A	
Date: Friday, January 10, 2020	Sheet: 51 of 66

12V to VCC Core (Phase 2,3)



Intel Corporation, 101 Innovation Dr., San Jose, CA 95134	
Title: AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size: Custom	Document Number: K57065-001-A
Date: Friday, January 10, 2020	Rev: A0
Sheet 52 of 66	

PWR - 0p8V_VCCL_SDM



PLACE Output decoupling caps close to the device. Connect AGND and PGND at the point of cap GND connection.



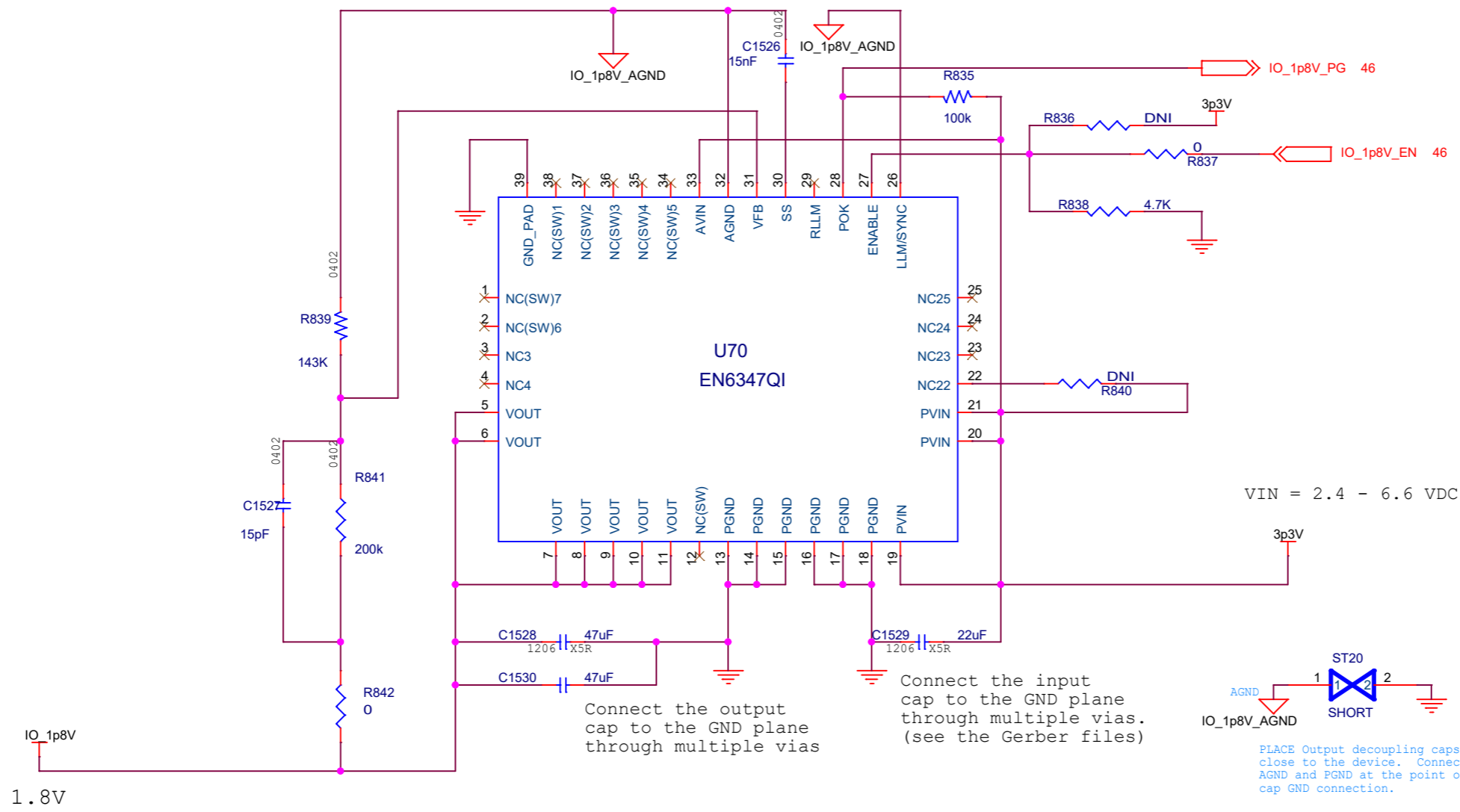
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size B	Document Number K57065-001-A	Rev A0
Date: Friday, January 10, 2020	Sheet 54	of 66

BLANK



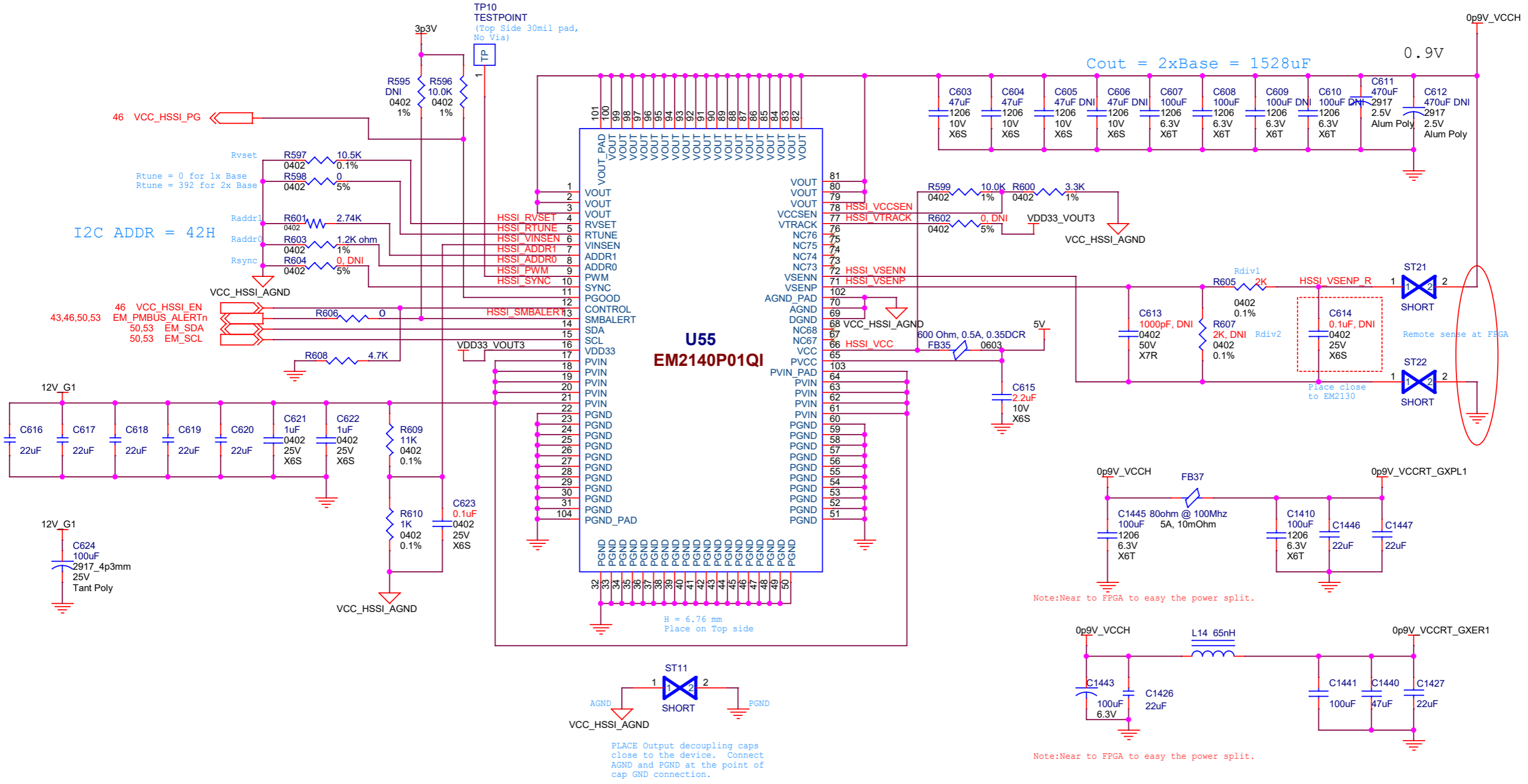
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title	AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 56 of 66

PWR - IO_1p8V



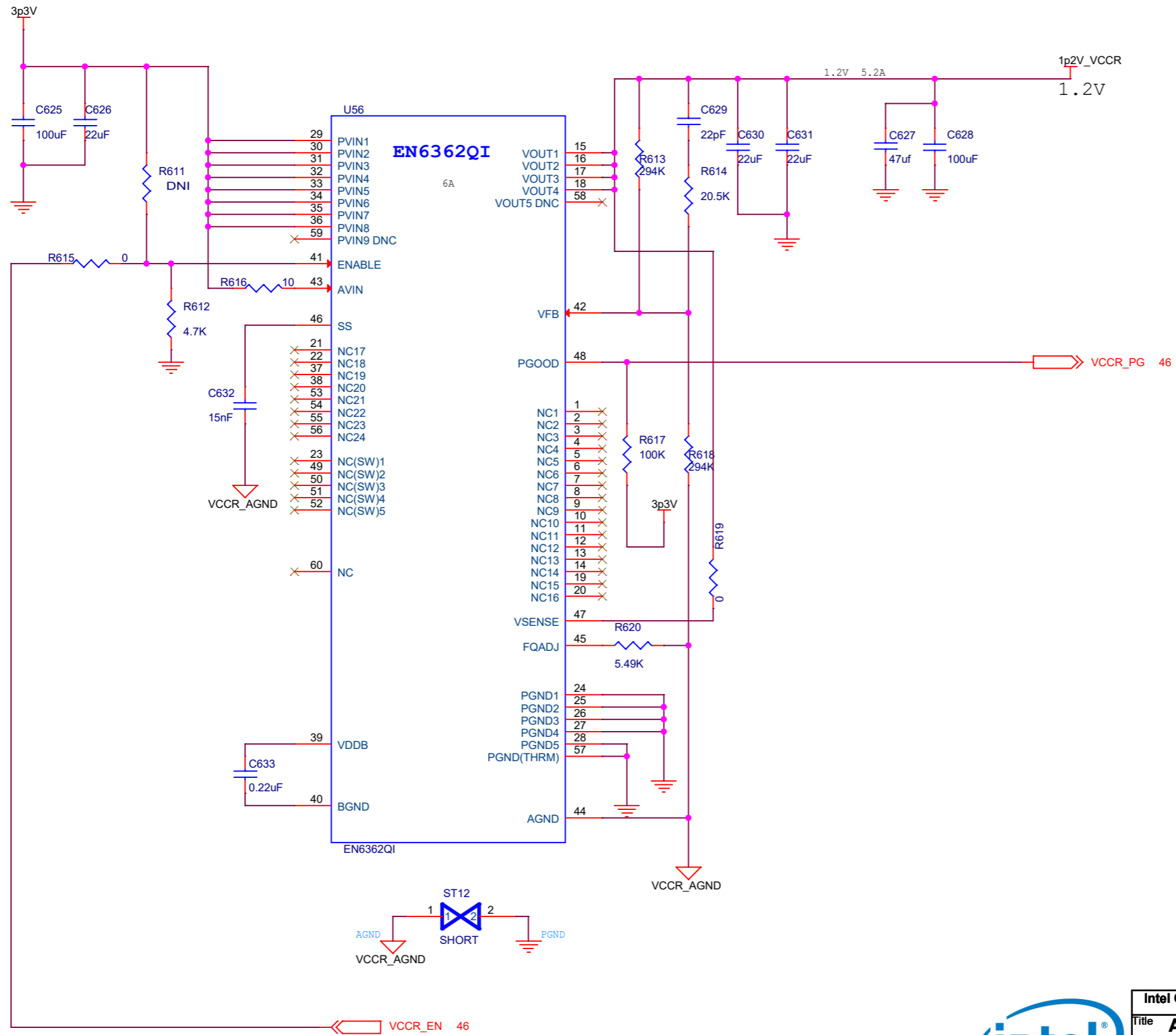
Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 57	of 66

PWR - VCC_HSSI_GXER1/VCC_HSSI_GXPL1



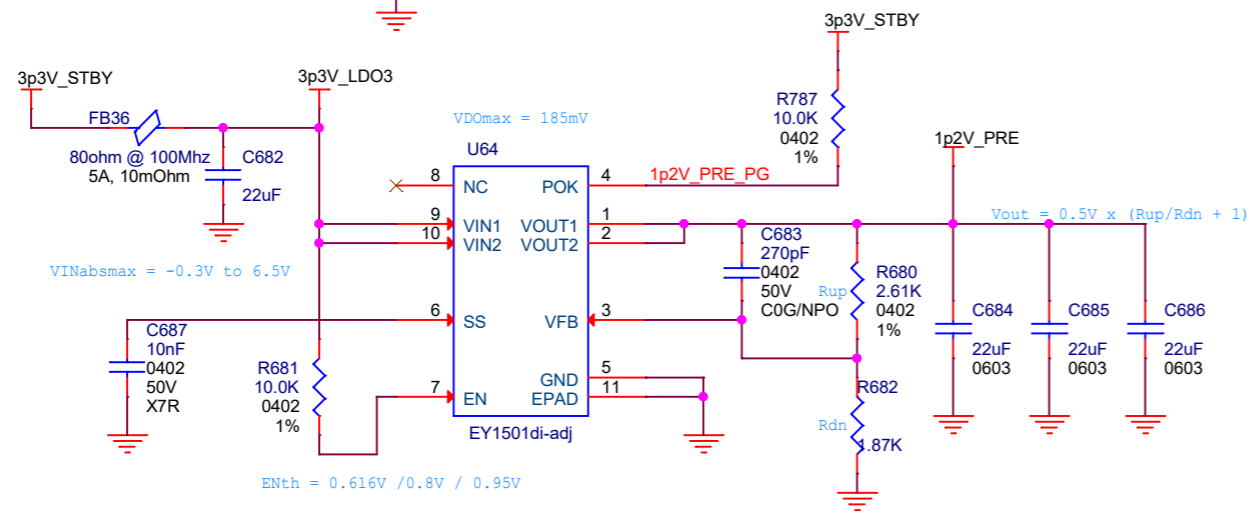
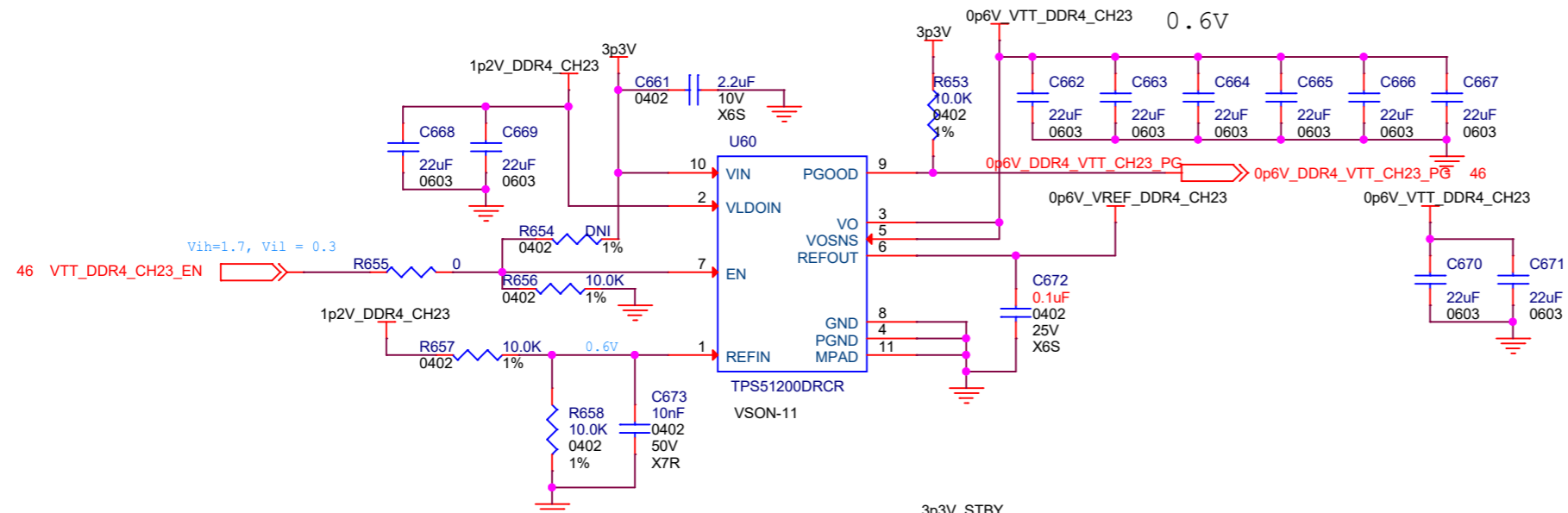
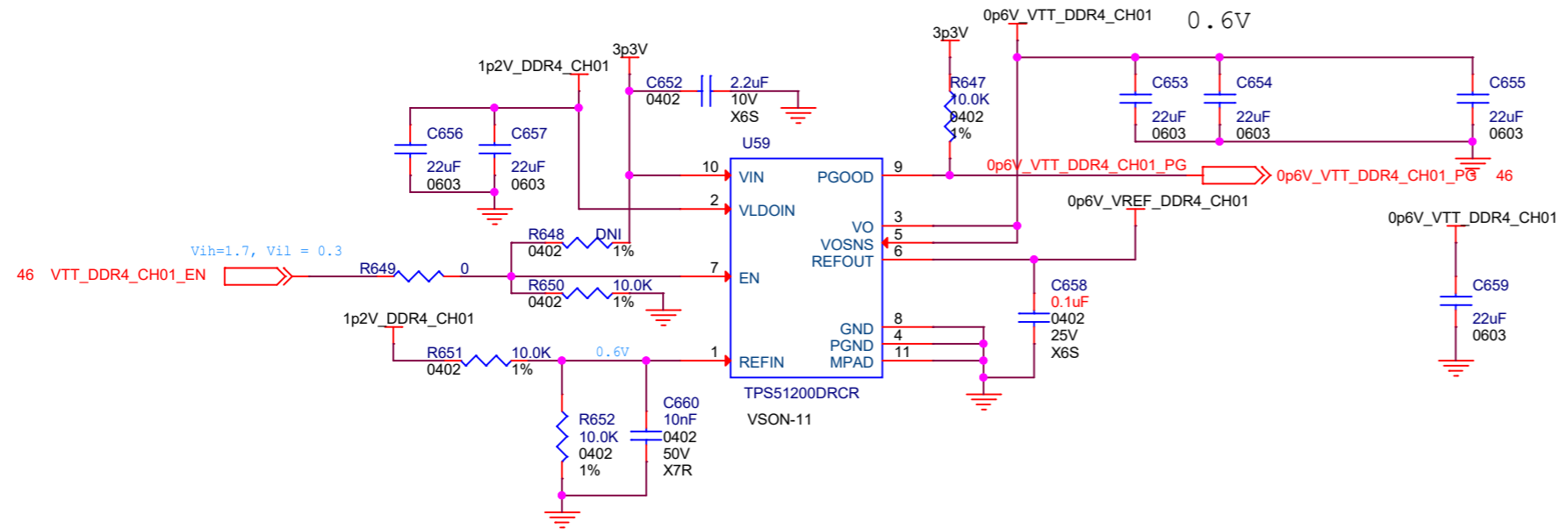
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 58 of 66

PWR - 1p2V VCCR



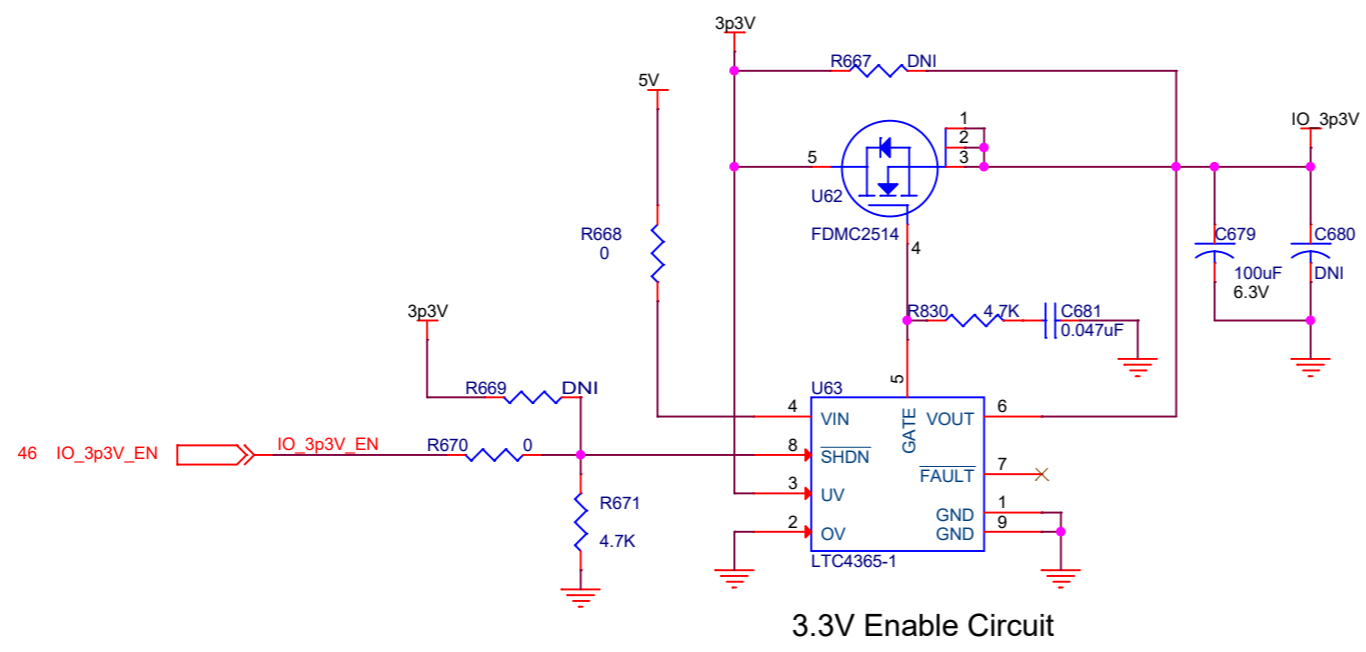
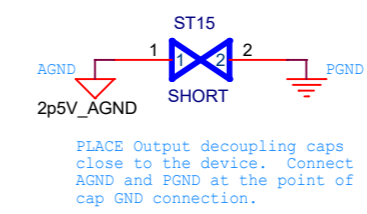
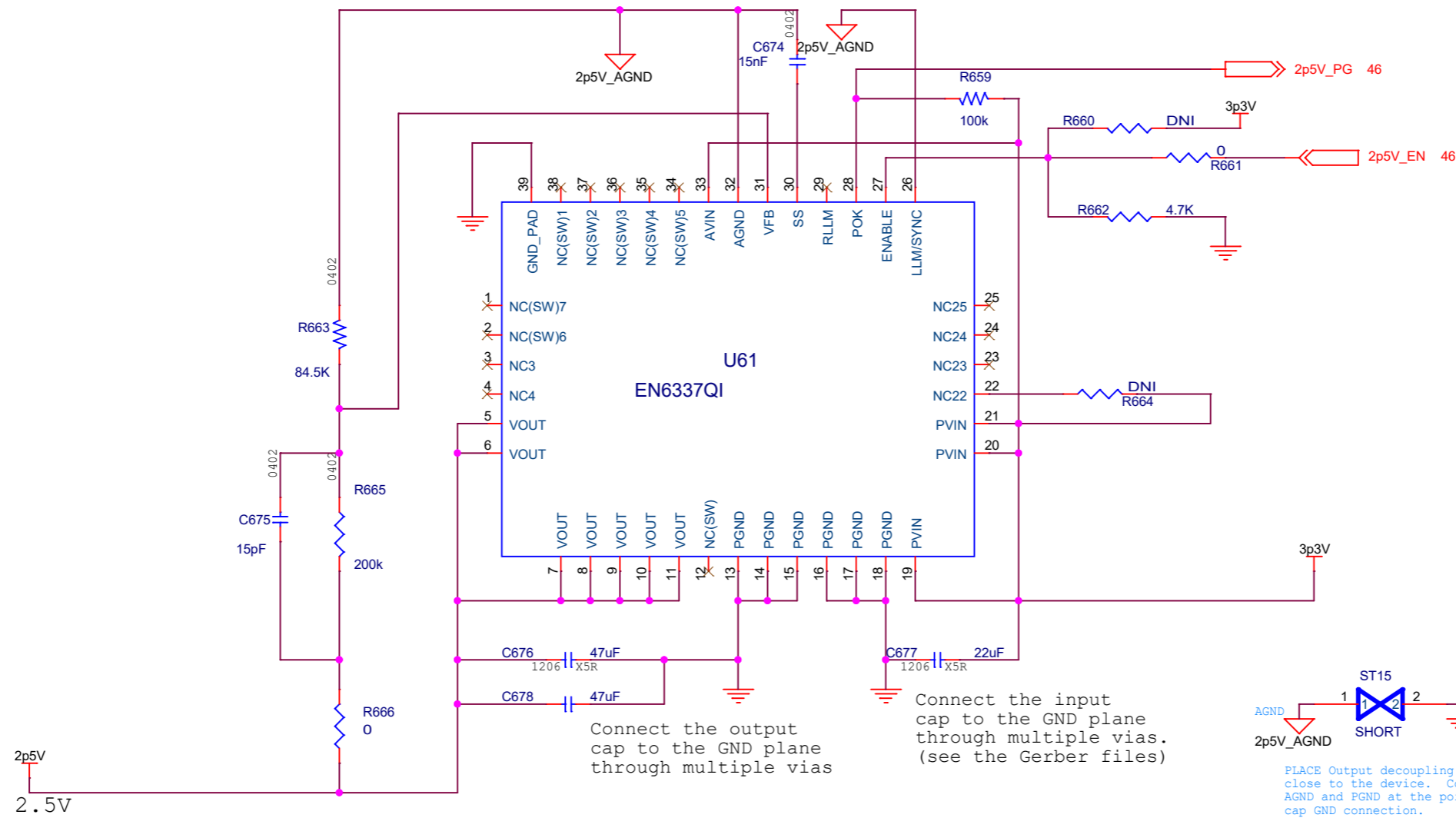
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 59 of 66

PWR - DDR4 VREF/VTT

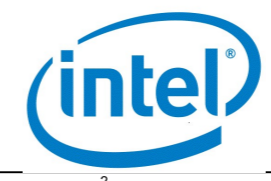


Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 62 of 66

PWR - 2p5V

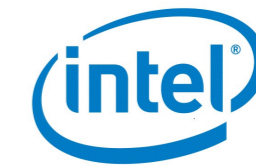
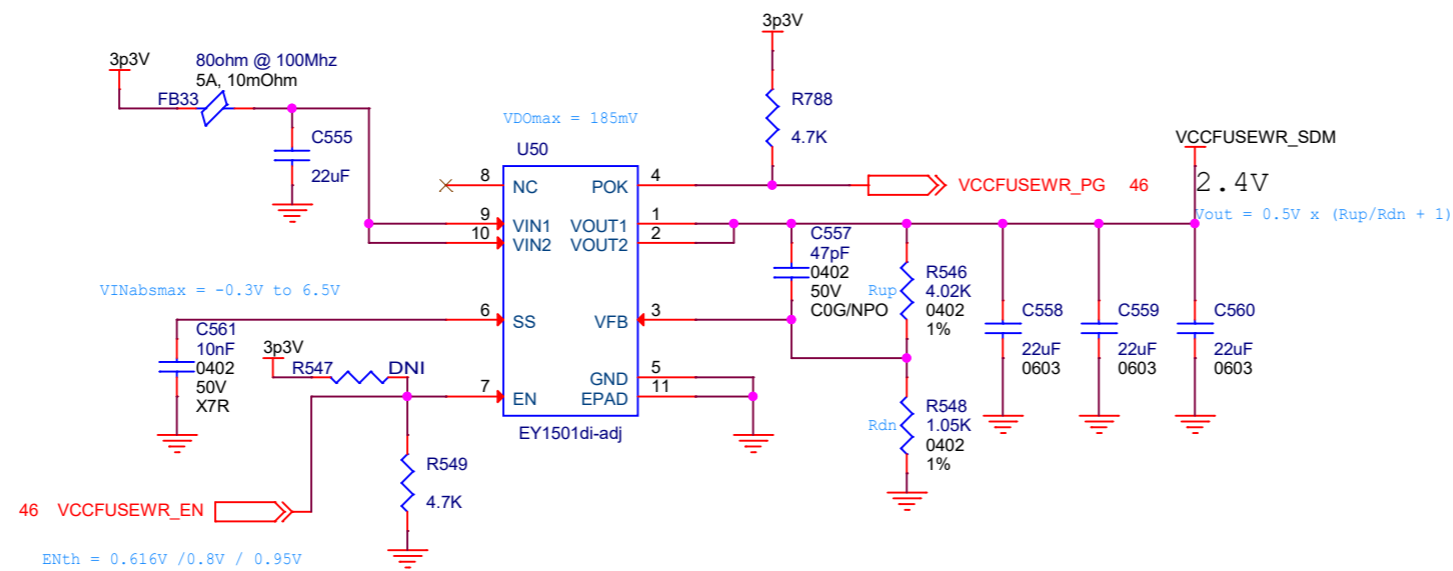
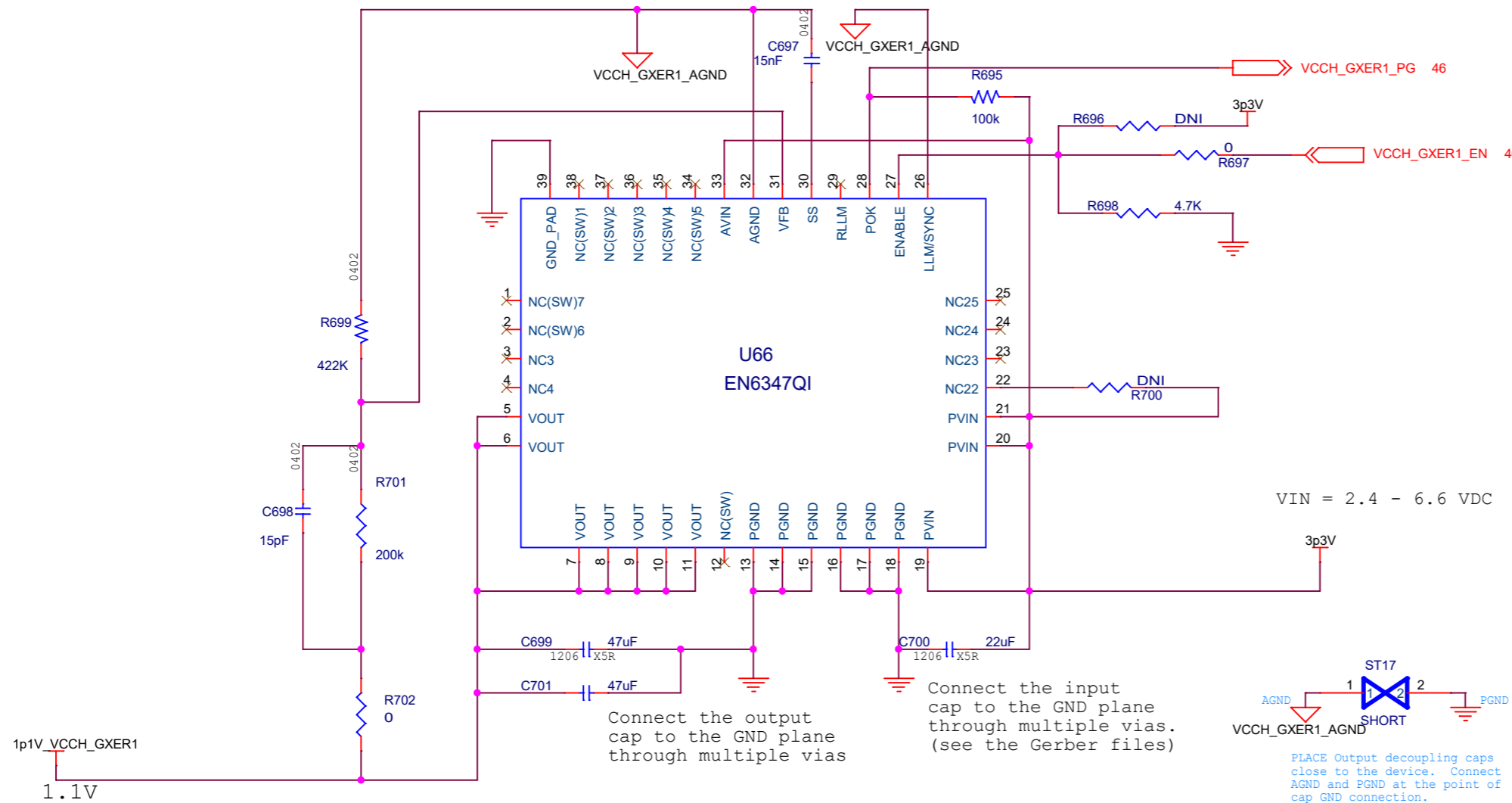


3.3V Enable Circuit

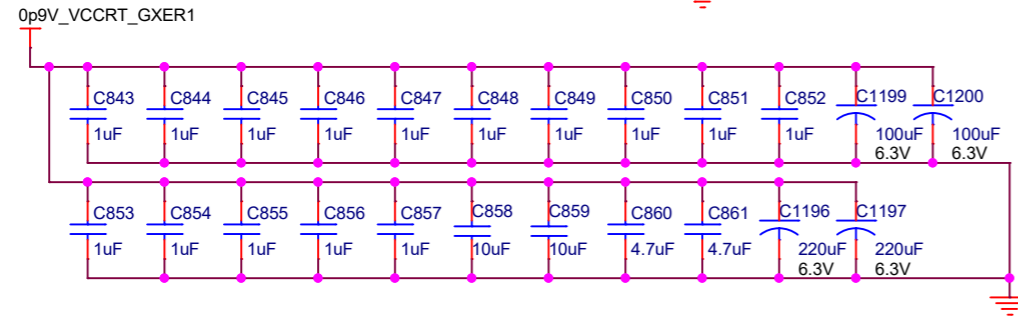
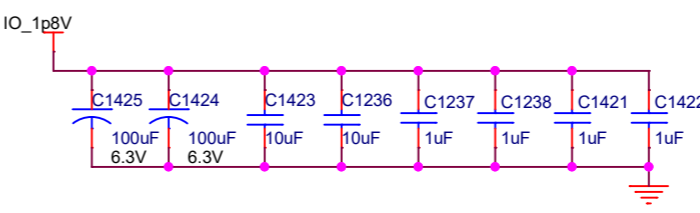
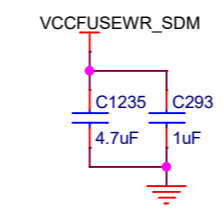
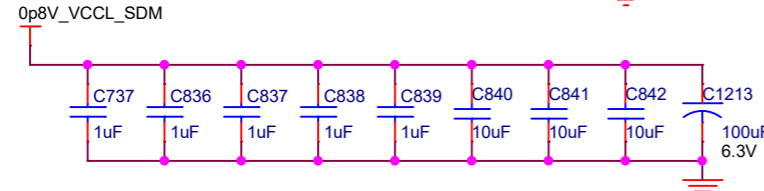
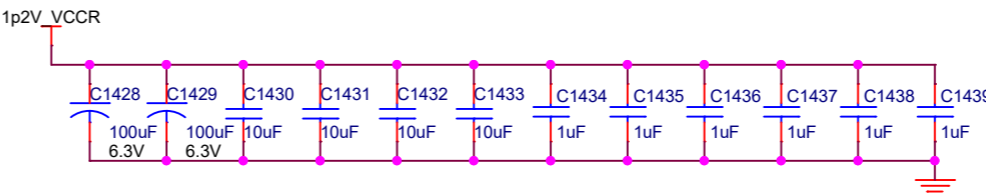
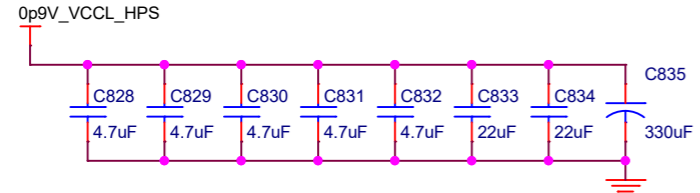
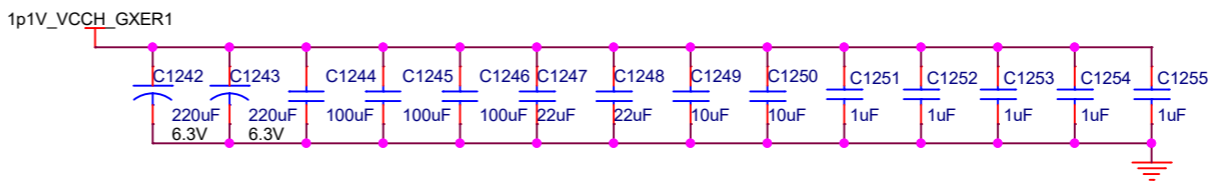
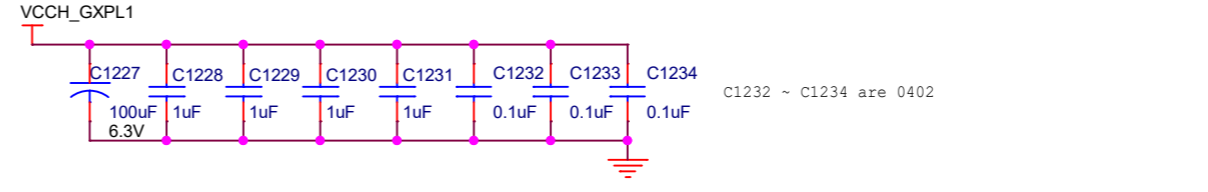
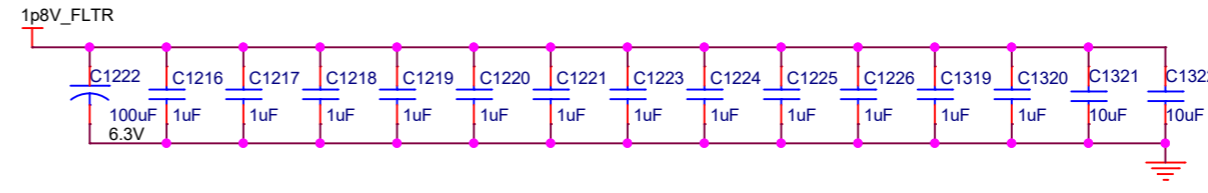
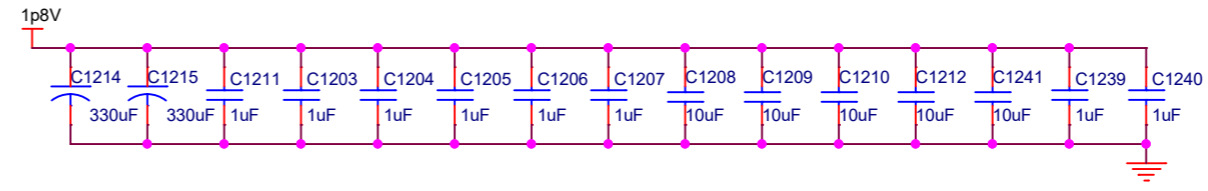
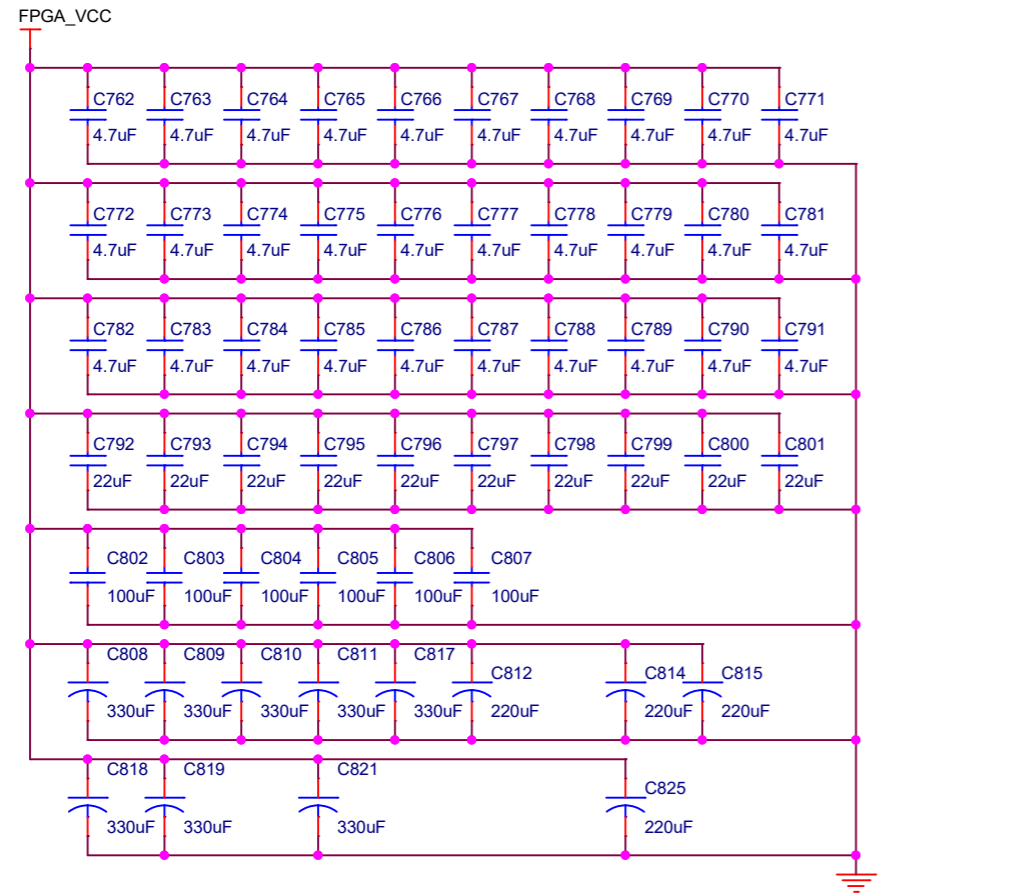


Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 63 of 66

PWR - 1p1V VCCH_GXER1 VCCFUSEWR_SDM



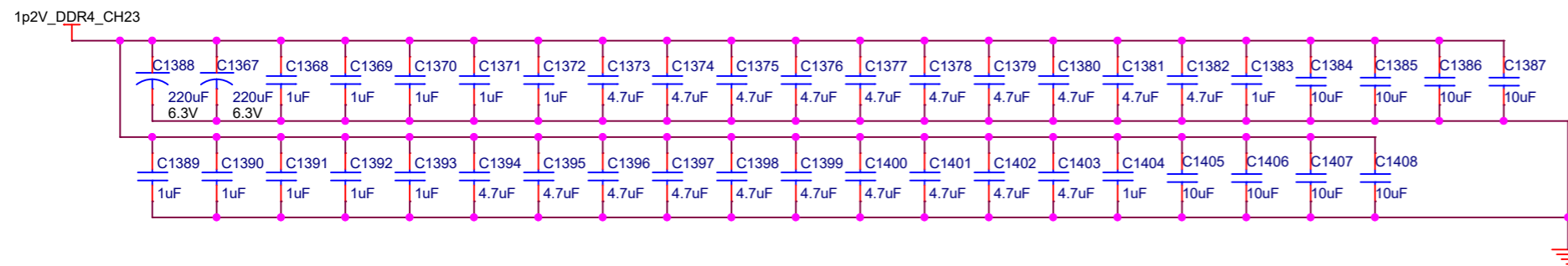
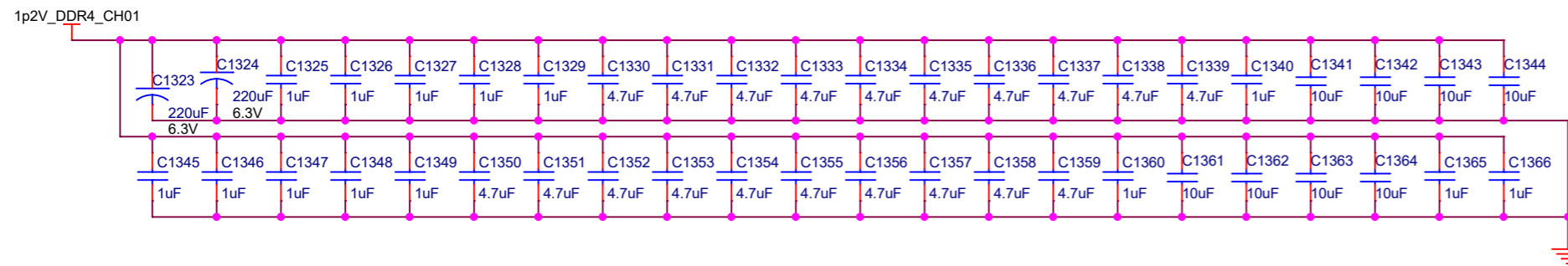
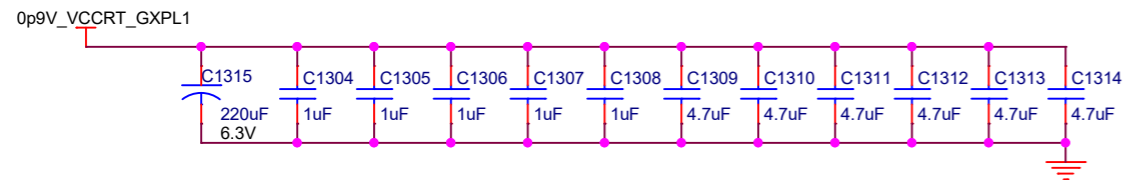
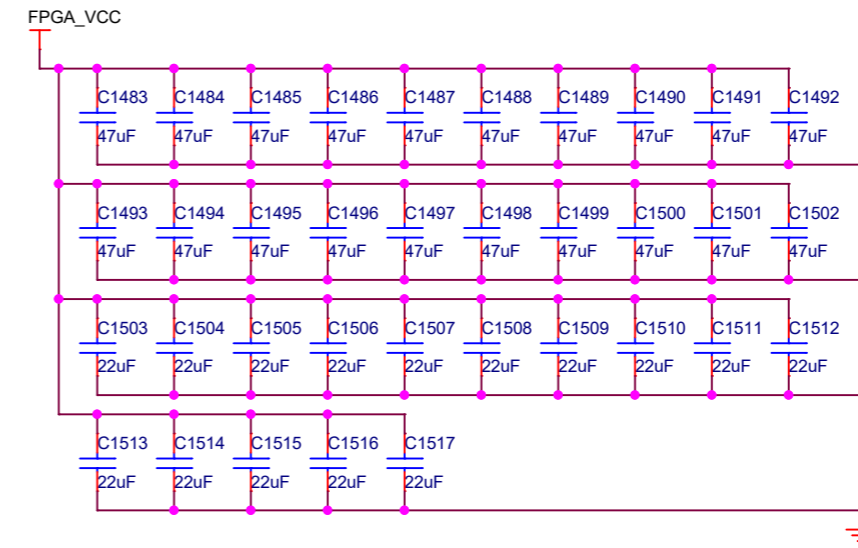
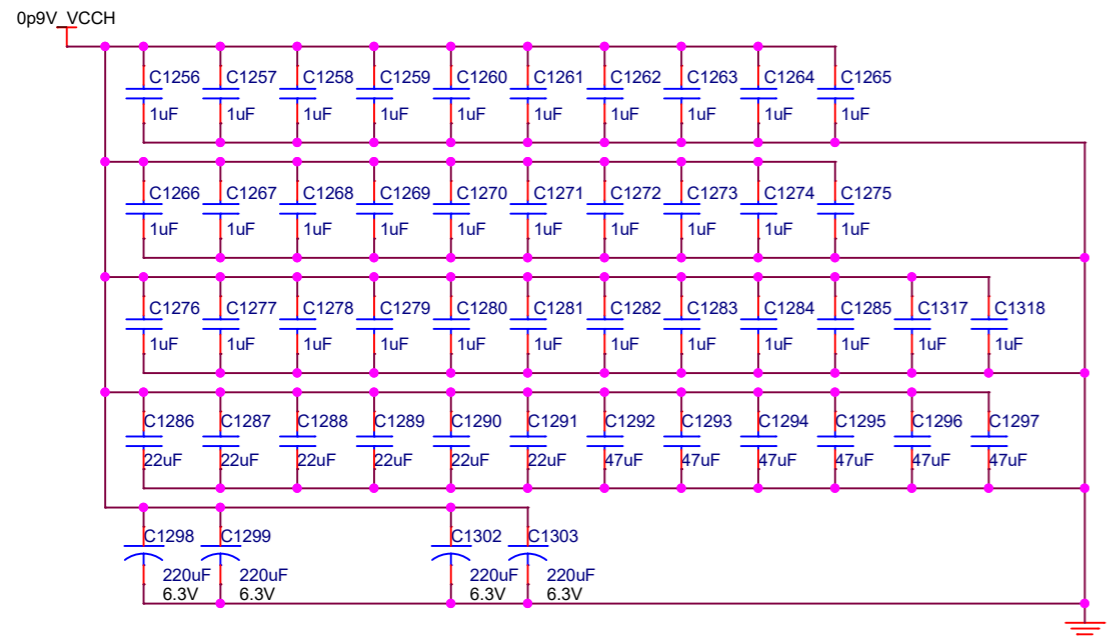
Intel Corporation, 101 innovation Dr, San Jose, CA 95134		
Title AgileX F-Series FPGA Dev Kit		
Copyright (c) 2014, Intel Corporation. All Rights Reserved.		
Size	Document Number	Rev
B	K57065-001-A	A0
Date:	Friday, January 10, 2020	Sheet 64 of 66



1 100uF + 1 10uF near to FPGA HPS area, 1 100uF+1 10uF near to FPGA SDM area



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Sheet 65 of 66
	Rev A0



Intel Corporation, 101 innovation Dr, San Jose, CA 95134	
Title AgileX F-Series FPGA Dev Kit	
Copyright (c) 2014, Intel Corporation. All Rights Reserved.	
Size B	Document Number K57065-001-A
Date: Friday, January 10, 2020	Rev A0
Sheet 66	of 66