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(13) 5CSE_4A_B44_N
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(13) 5CSE_4A_B44_P
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(13) 5CSE_4A_B46_P
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(13) 5CSE_4A_B77_P
(13) 5CSE_4A_B78_P
(13) 5CSE_4A_B80_N
(13) 5CSE_4A_B80_P

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to BTB

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5CSE_4A_B42_N AF13
5CSE_4A_B41_P AG8
5CSE_4A_B42_P AG13
5CSE_4A_B43_N U13
5CSE_4A_B44_N AH8
5CSE_4A_B43_P U14
5CSE_4A_B44_P AG9
5CSE_4A_B45_N AH9
5CSE_4A_B46_N AE15
5CSE_4A_B45_P AG10
5CSE_4A_B46_P AF15
5CSE_4A_B48_N AH11
5CSE_4A_B48_P AG11
5CSE_4A_B50_N AG16
5CSE_4A_B49_P AH12
5CSE_4A_B50_P AF17
5CSE_4A_B51_N V13
5CSE_4A_B52_N AH13
5CSE_4A_B51_P W14
5CSE_4A_B52_P AG14
5CSE_4A_B53_N AH14
5CSE_4A_B54_N AE17
5CSE_4A_B53_P AG15
5CSE_4A_B54_P AD17
5CSE_4A_B56_N AH16
5CSE_4A_B56_P AH17
5CSE_4A_B58_N AD19
5CSE_4A_B57_P AF18
5CSE_4A_B58_P AE19
5CSE_4A_B59_N AH18
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5CSE_4A_B59_P AA19
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5CSE_4A_B62_N AD20
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5CSE_4A_B78_P AF25
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(13) 5CSE_3B_CLK0_N
(13) 5CSE_3B_CLK0_P
(13) 5CSE_3B_B37_N
(13) 5CSE_3B_B37_P
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(13) 5CSE_3B_B26_N
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(13) 5CSE_3B_B30_N
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(13) 5CSE_3B_B30_P
(13) 5CSE_3B_B32_N
(13) 5CSE_3B_B32_P
(13) 5CSE_3B_B33_N
(13) 5CSE_3B_B34_N
(13) 5CSE_3B_B33_P
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(13) 5CSE_3B_B35_N
(13) 5CSE_3B_B36_N
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(13) 5CSE_3B_B36_P
(13) 5CSE_3B_B38_N
(13) 5CSE_3B_B38_P
(13) 5CSE_3B_B40_N
(13) 5CSE_3B_B40_P

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to BTB

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5CSE_3B_CLK0_P V11
5CSE_3B_B37_N AH4
5CSE_3B_B37_P AG5
5CSE_3A_B8_P AD5
5CSE_3B_B25_N AF4
5CSE_3B_B26_N AE9
5CSE_3B_B25_P AE4
5CSE_3B_B26_P AD10
5CSE_3B_B27_N U11
5CSE_3B_B28_N AF8
5CSE_3B_B27_P T11
5CSE_3B_B28_P AE7
5CSE_3B_B29_N AF9
5CSE_3B_B30_N AE11
5CSE_3B_B29_P AE8
5CSE_3B_B30_P AD11
5CSE_3B_B32_N AF6
5CSE_3B_B32_P AF5
5CSE_3B_B33_N AG6
5CSE_3B_B34_N AF10
5CSE_3B_B33_P AF7
5CSE_3B_B34_P AF11
5CSE_3B_B35_N T12
5CSE_3B_B36_N AH2
5CSE_3B_B35_P T13
5CSE_3B_B36_P AH3
5CSE_3B_B38_N AD12
5CSE_3B_B38_P AE12
5CSE_3B_B40_N AH5
5CSE_3B_B40_P AH6

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to BTB

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(13) 5CSE_5B_B22_P
(13) 5CSE_5B_B22_N
(13) 5CSE_5B_B23_P
(13) 5CSE_5B_B23_N
(13) 5CSE_5A_B4_P
(13) 5CSE_5A_B4_N
(13) 5CSE_5A_B6_P
(13) 5CSE_5A_B6_N
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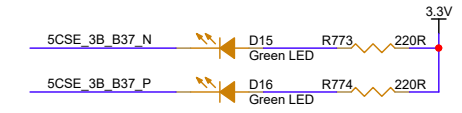
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5CSE_5A_B4_P Y17
5CSE_5A_B4_N Y18
5CSE_5A_B6_P Y16
5CSE_5A_B6_N W15
5CSE_5A_B7_P AA24
5CSE_5A_B8_P V16
5CSE_5A_B7_N AA23
5CSE_5A_B8_N V15

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IO_3B_W11/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B31N
IO_3B_V11/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B31P
IO_3B_AH4/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B37N/DQ3B
IO_3B_AG5/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B37P/DQ3B
IO_3A_AD5/DIFFIO_TX_B8P/DQ1B
IO_3B_AF4/DIFFIO_TX_B25N
IO_3B_AE9/DIFFIO_RX_B28N/DQ2B
IO_3B_AE4/DIFFIO_TX_B25P/DQ2B
IO_3B_AD10/DIFFIO_RX_B26P/DQ2B
IO_3B_U11/DIFFIO_RX_B27N/DQSN2B
IO_3B_AF8/DIFFIO_TX_B28N/DQ2B
IO_3B_T11/DIFFIO_RX_B27P/DQ2B
IO_3B_AE7/DIFFIO_TX_B28P
IO_3B_AF9/DIFFIO_TX_B29N/DQ2B
IO_3B_AE11/DIFFIO_RX_B30N/DQ2B
IO_3B_AE8/DIFFIO_TX_B29P/DQ2B
IO_3B_AD11/DIFFIO_RX_B30P/DQ2B
IO_3B_AF6/DIFFIO_TX_B32N/DQ2B
IO_3B_AF5/DIFFIO_TX_B32P/DQ2B
IO_3B_AC6/DIFFIO_TX_B33N
IO_3B_AF10/DIFFIO_RX_B34N/DQ3B
IO_3B_AF7/DIFFIO_TX_B33P/DQ3B
IO_3B_AF11/DIFFIO_RX_B34P/DQ3B
IO_3B_T12/DIFFIO_RX_B35N/DQSN3B
IO_3B_AH2/DIFFIO_TX_B36N/DQ3B
IO_3B_T13/DIFFIO_RX_B35P/DQ3B
IO_3B_AH3/DIFFIO_TX_B36P
IO_3B_AD12/DIFFIO_RX_B38N/DQ3B
IO_3B_AE12/DIFFIO_TX_B38P/DQ3B
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IO_3B_AH6/DIFFIO_TX_B40P/DQ3B

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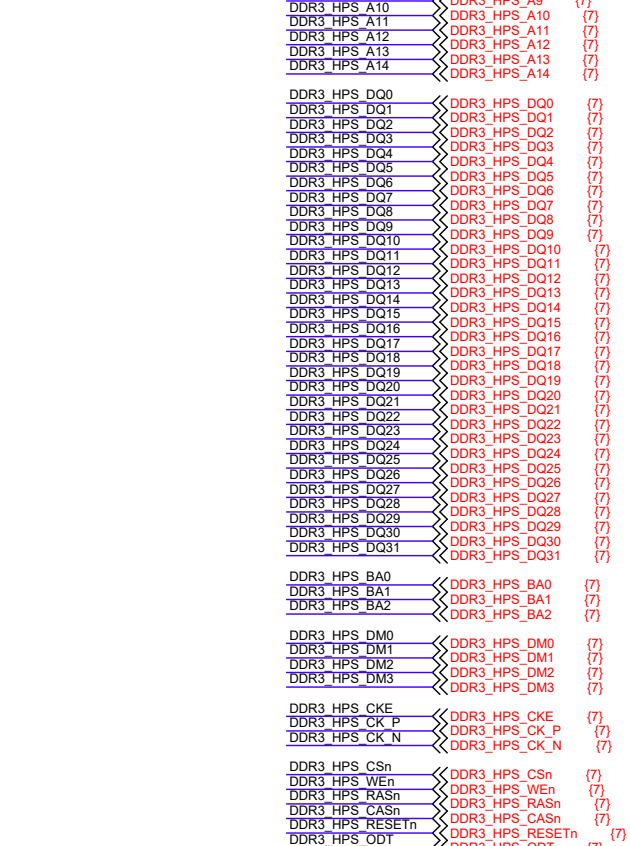
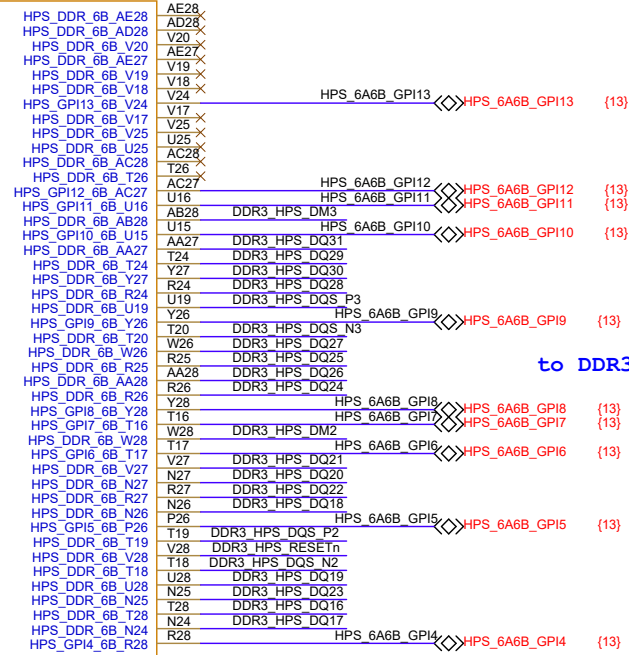
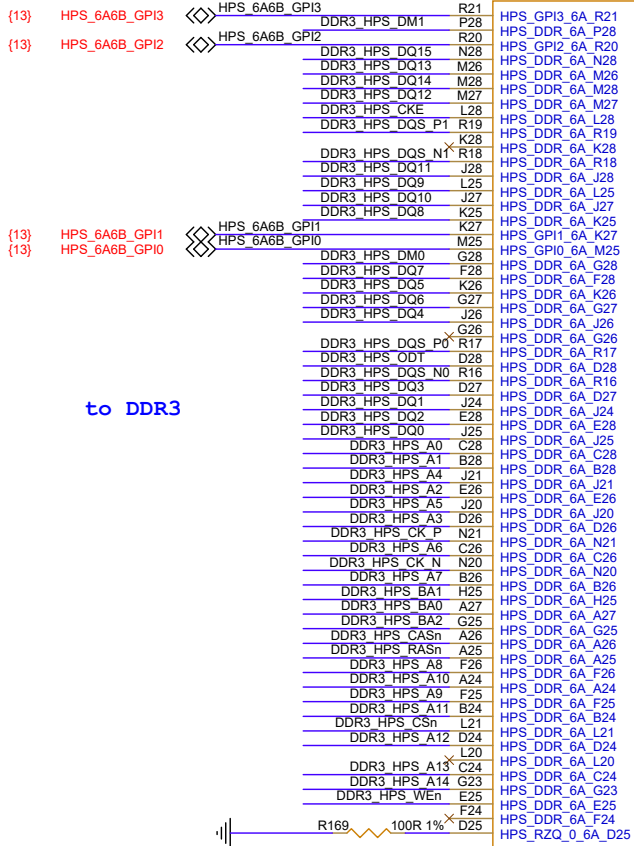
P1-4

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IO_5B_AB28/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R22P
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IO_5B_Y24/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P
IO_5B_W24/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N
IO_5A_Y17/DIFFIO_RX_R4P/DQ1R
IO_5A_Y18/DIFFIO_RX_R4N/DQ1R
IO_5A_Y16/DIFFIO_RX_R6P/DQ51R
IO_5A_W15/DIFFIO_RX_R6N/DQSN1R
IO_5A_AA24/DIFFIO_TX_R7P/DQ1R
IO_5A_V16/DIFFIO_RX_R8P/DQ1R
IO_5A_AA23/DIFFIO_TX_R7N
IO_5A_V15/DIFFIO_RX_R8N/DQ1R

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Title		
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DDR3 HPS_A0	DDR3_HPS_A0	(7)
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DDR3 HPS_A2	DDR3_HPS_A2	(7)
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DDR3 HPS_A4	DDR3_HPS_A4	(7)
DDR3 HPS_A5	DDR3_HPS_A5	(7)
DDR3 HPS_A6	DDR3_HPS_A6	(7)
DDR3 HPS_A7	DDR3_HPS_A7	(7)
DDR3 HPS_A8	DDR3_HPS_A8	(7)
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DDR3 HPS_CSn	DDR3_HPS_CSn	(7)
DDR3 HPS_WEn	DDR3_HPS_WEn	(7)
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DDR3 HPS_CASn	DDR3_HPS_CASn	(7)
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DDR3 HPS_DQS_P0	DDR3_HPS_DQS_P0	(7)
DDR3 HPS_DQS_N0	DDR3_HPS_DQS_N0	(7)
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Date:	Friday, December 18, 2020	Sheet 2 of 13

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 (5,13) JTAG_FPGA_TDO << JTAG FPGA TDO
 (13) JTAG_HPS_TRST << JTAG HPS TRST
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 (3,8,13) HPS_nPOR << HPS nPOR

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 (13) SPIS0_MISO
 (13) SPIS0_SS0
 (13) HPS_7A_IO5
 (13) HPS_7A_IO6

(13) SPIM0_CLK
 (13) SPIM0_MOSI
 (13) SPIM0_MISO
 (13) SPIM0_SS0
 (13) UART0_RX
 (13) UART0_TX
 (13) I2C0_SDA
 (13) I2C0_SCL
 (13) CAN0_RX
 (13) CAN0_TX

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 (9) NAND_D6 << NAND D6
 (9) NAND_D5 << NAND D5
 (9) NAND_D4 << NAND D4
 (9) NAND_D3 << NAND D3
 (9) NAND_D2 << NAND D2
 (9) NAND_D1 << NAND D1
 (9) NAND_D0 << NAND D0

(9) NAND_RnB << NAND RnB
 (9) NAND_nRE << NAND nRE
 (9) NAND_nCE << NAND nCE
 (9) NAND_nWP << NAND nWP

(9) NAND_CLE << NAND CLE
 (9) NAND_ALE << NAND ALE
 (9) NAND_nWE << NAND nWE

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 (8) QSPI_IO2 << QSPI IO2
 (8) QSPI_IO3 << QSPI IO3

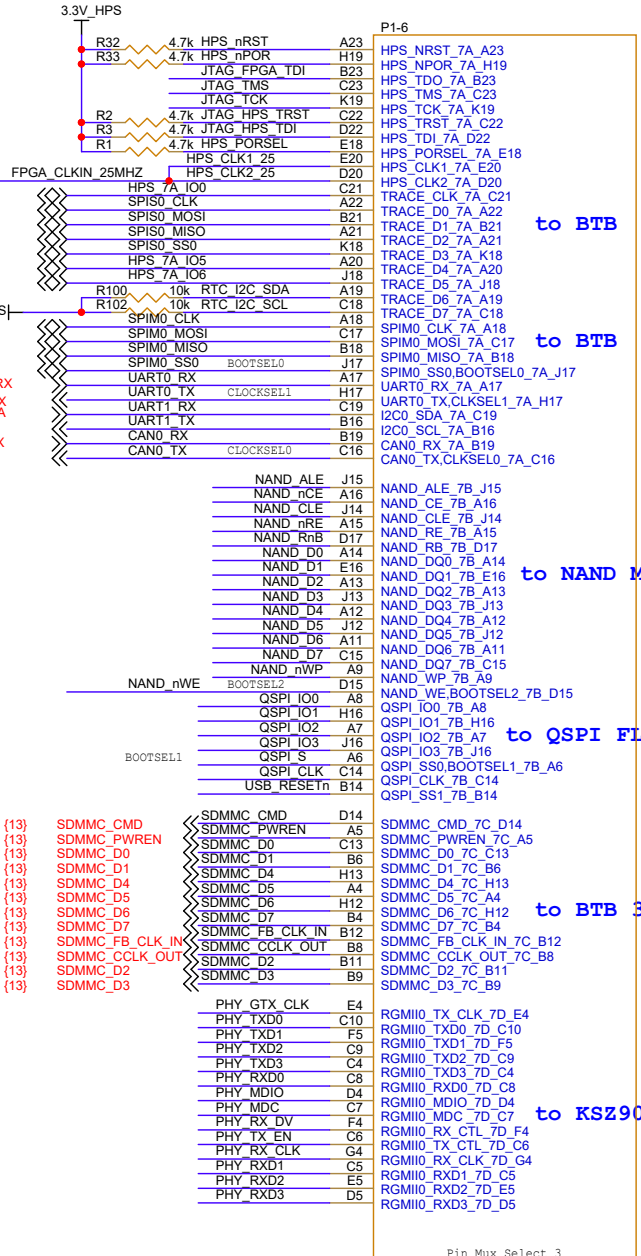
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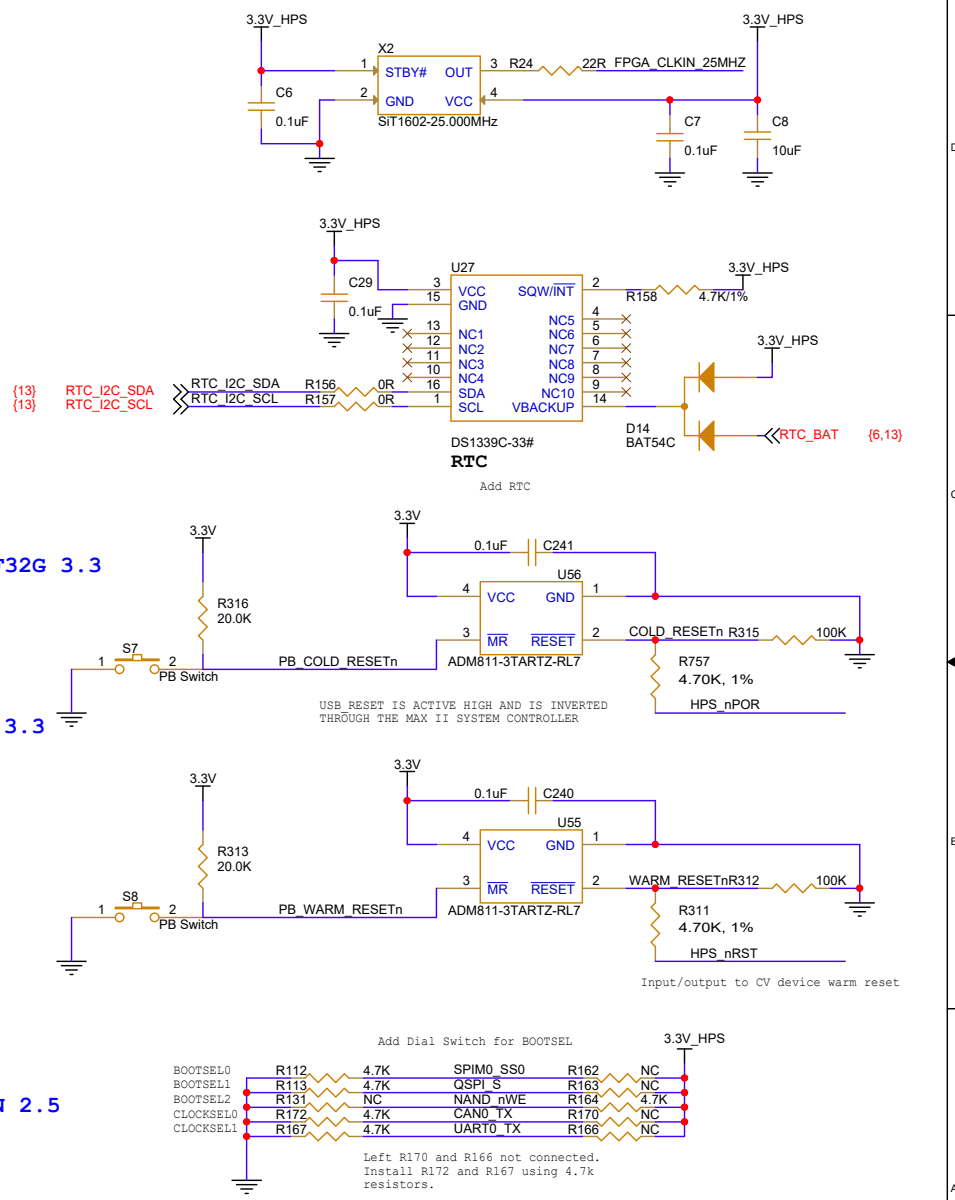
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 (10) PHY_RX_CLK << PHY RX_CLK
 (10) PHY_RX_DV << PHY RX_DV

(10) PHY_TXD0 << PHY TXD0
 (10) PHY_TXD1 << PHY TXD1
 (10) PHY_TXD2 << PHY TXD2
 (10) PHY_TXD3 << PHY TXD3
 (10) PHY_GTX_CLK << PHY GTX_CLK
 (10) PHY_TX_CLK << PHY TX_CLK
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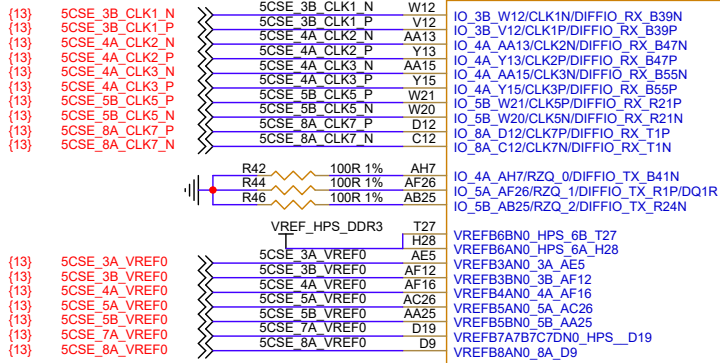


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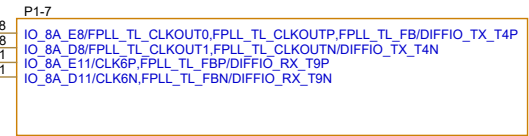
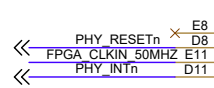
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Size	Document Number	Rev
B	FPGA Bank 7, JTAG, SDRAM, RGMII, NAND, QSPI etc	V1.0
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to BTB

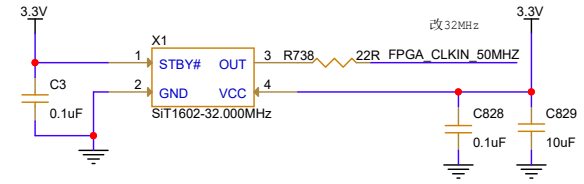


CycloneV 5CSEMA6U23
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{10} PHY_RESETn
 {10} PHY_INTn

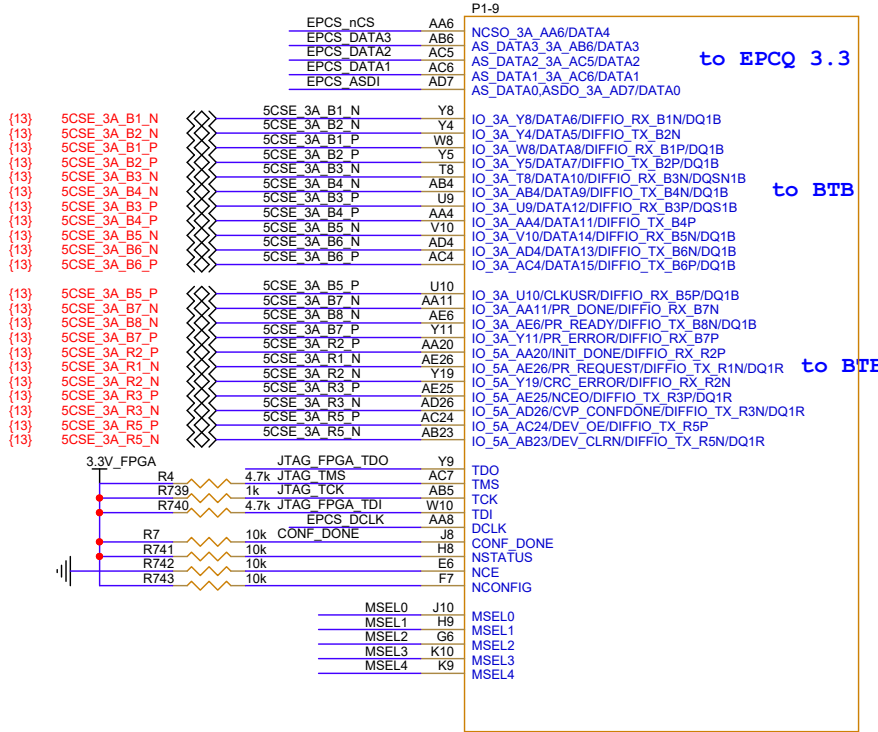


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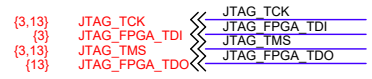


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Size B	Document Number FPGA Bank 8 and Clock and Clock Generator	Rev V1.0
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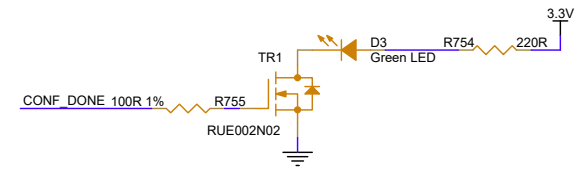
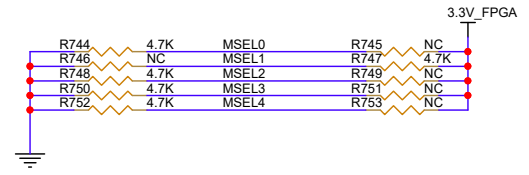
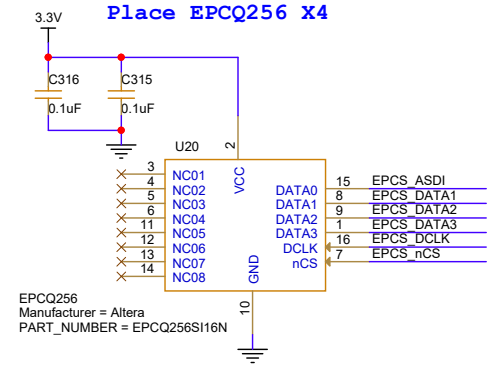
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to EPCQ 3.3

to BTB

to BTB



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Size	Document Number	Rev
B	FPGA Configuration and EPCS	V1.0
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P1-11

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A3	GND_A3	K14	K14
AA1	GND_AA1	K16	K16
AA17	GND_AA17	K20	K20
AA2	GND_AA2	K2	K2
AA3	GND_AA3	K4	K4
AA9	GND_AA9	K8	K8
AB1	GND_AB1	L1	L1
AB2	GND_AB2	L10	L10
AB24	GND_AB24	L13	L13
AB27	GND_AB27	L15	L15
AB3	GND_AB3	L17	L17
AC1	GND_AC1	L19	L19
AC2	GND_AC2	L2	L2
AC3	GND_AC3	L24	L24
AD14	GND_AD14	L27	L27
AD22	GND_AD22	L3	L3
AD25	GND_AD25	L5	L5
AD3	GND_AD3	L8	L8
AD6	GND_AD6	L9	L9
AD8	GND_AD8	L10	L10
AE1	GND_AE1	M10	M10
AE16	GND_AE16	M11	M11
AE18	GND_AE18	M14	M14
AE2	GND_AE2	M16	M16
AE3	GND_AE3	M20	M20
AF11	GND_AF11	M3	M3
AF2	GND_AF2	M8	M8
AF24	GND_AF24	M1	M1
AG1	GND_AG1	N1	N1
AG17	GND_AG17	N13	N13
AG2	GND_AG2	N15	N15
AG27	GND_AG27	N17	N17
AG3	GND_AG3	N19	N19
AG7	GND_AG7	N2	N2
AH10	GND_AH10	N4	N4
AH20	GND_AH20	N5	N5
B15	GND_B15	N8	N8
B17	GND_B17	N10	N10
B20	GND_B20	N11	N11
B22	GND_B22	N12	N12
B25	GND_B25	N13	N13
B27	GND_B27	N14	N14
B3	GND_B3	N15	N15
B5	GND_B5	N16	N16
B7	GND_B7	N17	N17
C1	GND_C1	N18	N18
C11	GND_C11	N19	N19
C2	GND_C2	N20	N20
C3	GND_C3	P1	P1
D10	GND_D10	P10	P10
D13	GND_D13	P11	P11
D16	GND_D16	P12	P12
D21	GND_D21	P13	P13
D3	GND_D3	P14	P14
E1	GND_E1	P15	P15
E19	GND_E19	P16	P16
E2	GND_E2	P17	P17
E23	GND_E23	P18	P18
E24	GND_E24	P19	P19
E27	GND_E27	P20	P20
E3	GND_E3	P21	P21
E9	GND_E9	P22	P22
F1	GND_F1	P23	P23
F2	GND_F2	P24	P24
F3	GND_F3	P25	P25
G1	GND_G1	P26	P26
G2	GND_G2	P27	P27
G3	GND_G3	P28	P28
H11	GND_H11	P29	P29
H15	GND_H15	P30	P30
H20	GND_H20	P31	P31
H24	GND_H24	P32	P32
H27	GND_H27	P33	P33
H3	GND_H3	P34	P34
H4	GND_H4	P35	P35
H5	GND_H5	P36	P36
H6	GND_H6	P37	P37
J1	GND_J1	P38	P38
J2	GND_J2	P39	P39
J3	GND_J3	P40	P40
J5	GND_J5	P41	P41
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K11	GND_K11	P44	P44

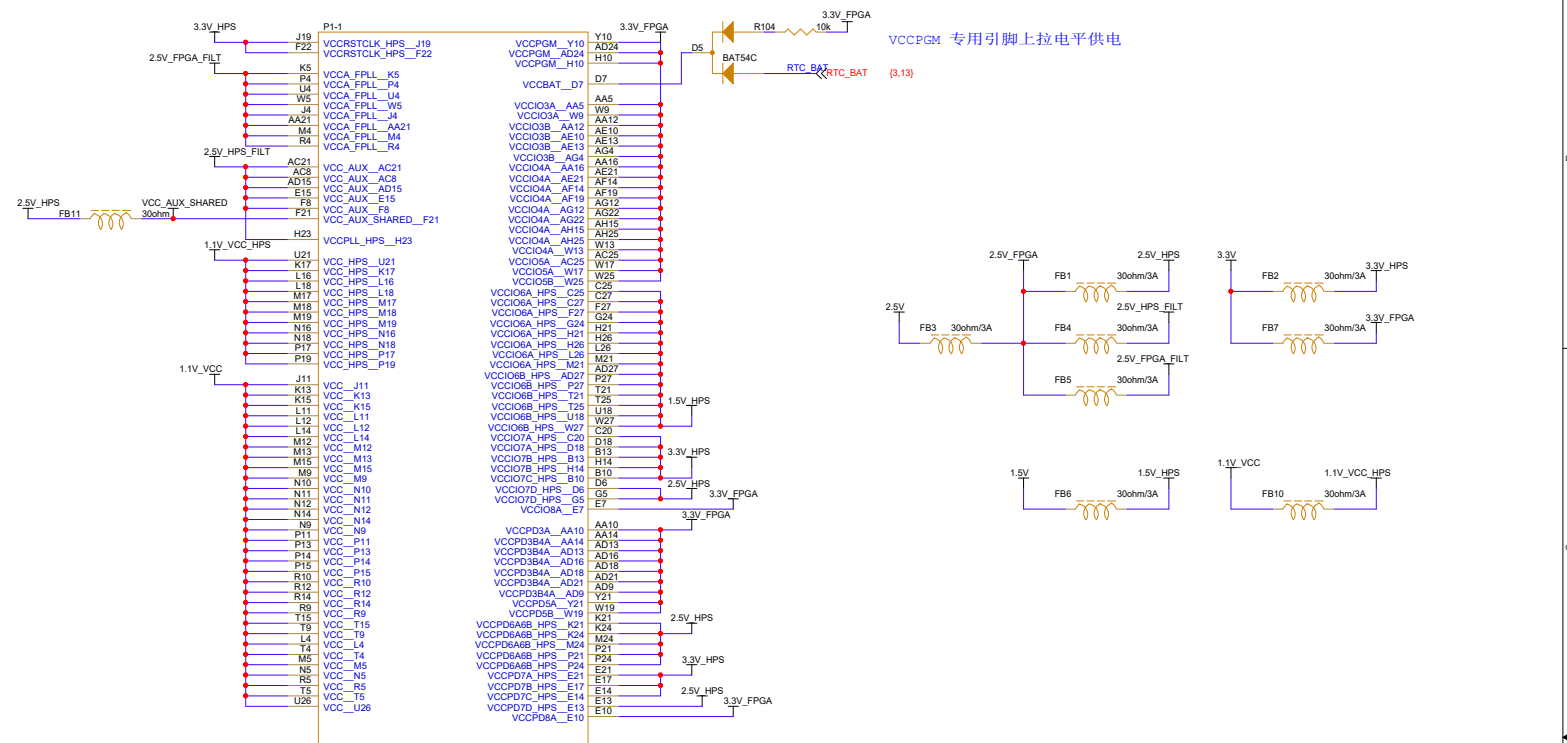
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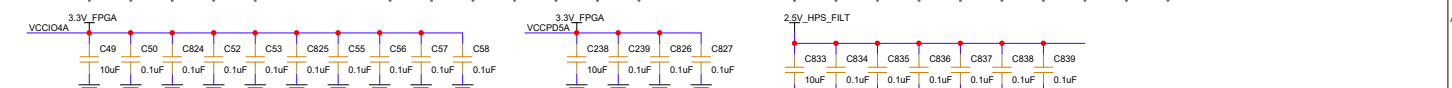
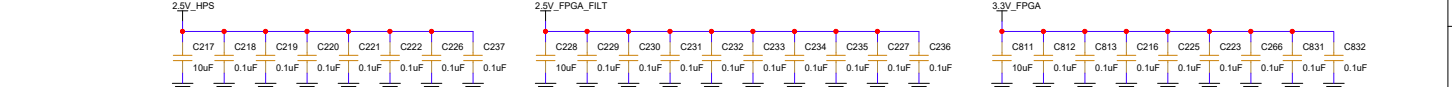
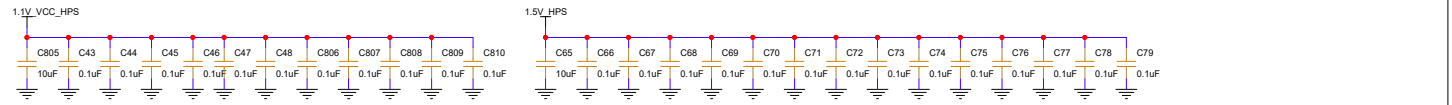
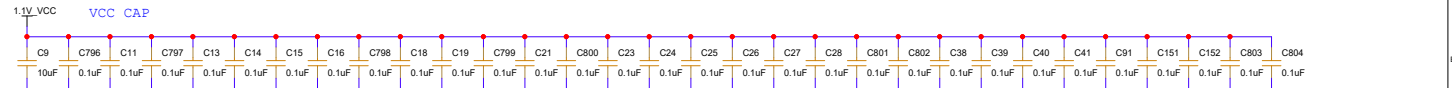
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AE14	DNJ_AE14
B2	DNJ_B2
D1	DNJ_D1
D2	DNJ_D2
D23	DNJ_D23
E12	DNJ_E12
H1	DNJ_H1
H2	DNJ_H2
M1	DNJ_M1
M2	DNJ_M2
T1	DNJ_T1
T2	DNJ_T2
U8	DNJ_U8
Y1	DNJ_Y1
Y2	DNJ_Y2

R756 2K B1
RREF_TL_B1

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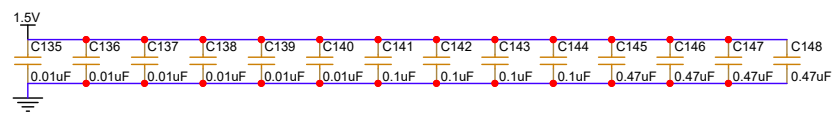
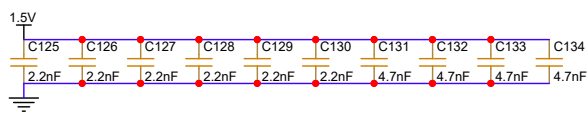
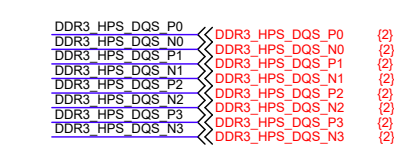
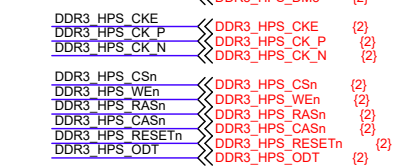
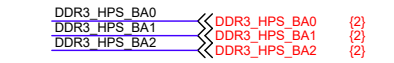
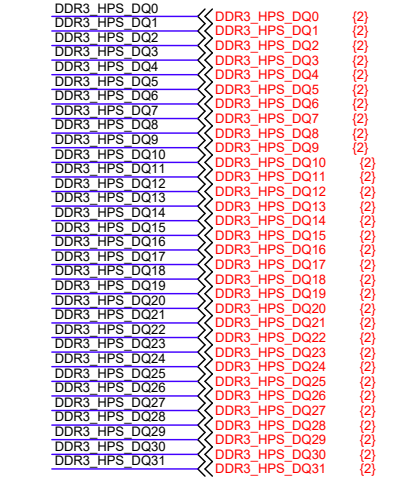
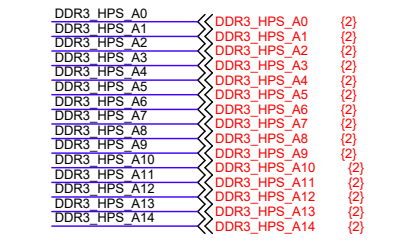
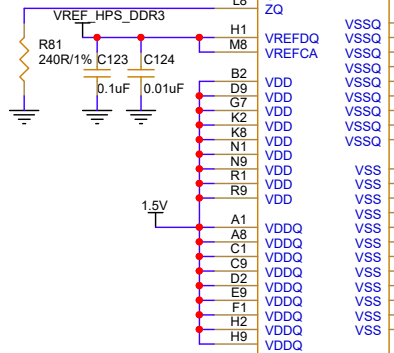
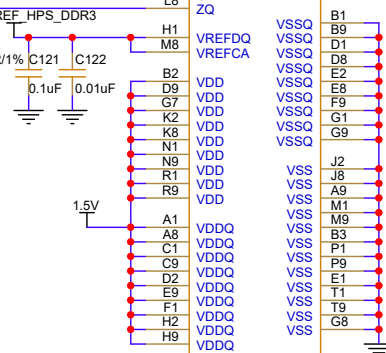
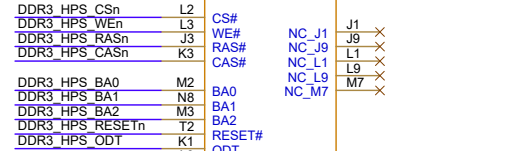
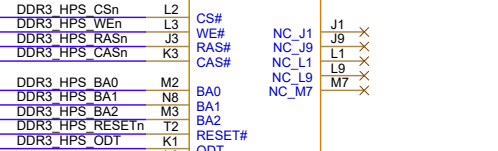
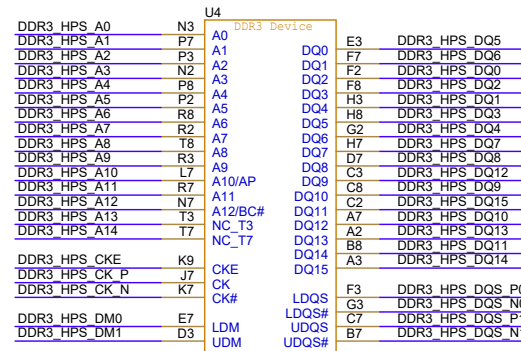
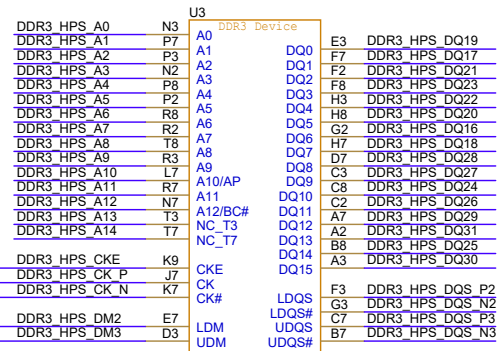
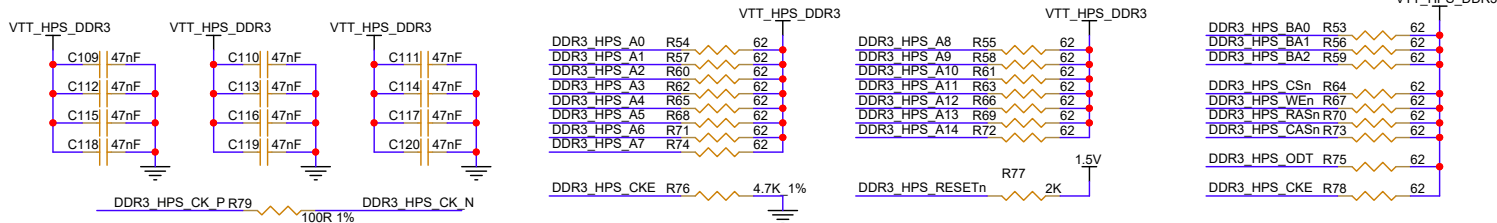
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BANK 3B 4A 5A调整电平

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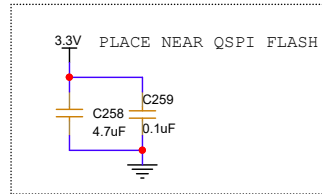
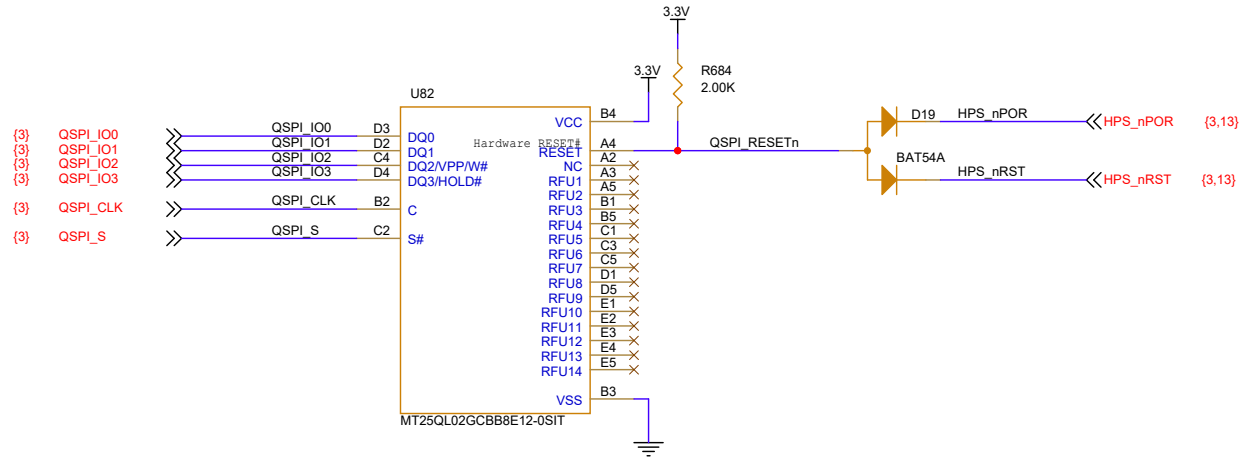
DDR3 SDRAM



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QSPI Flash

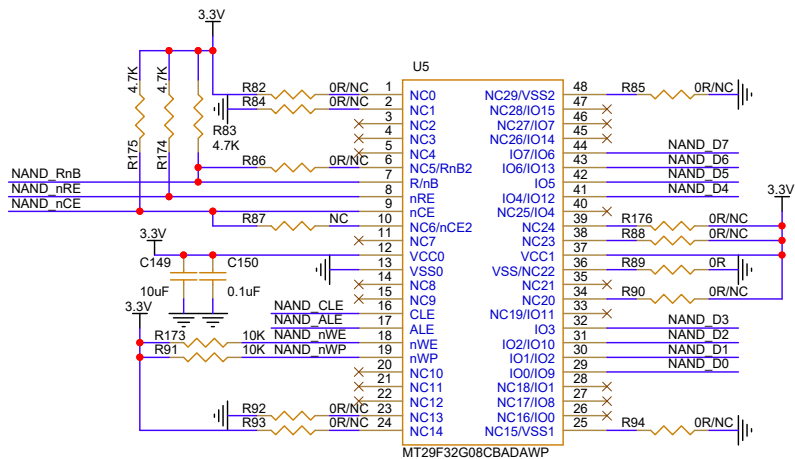
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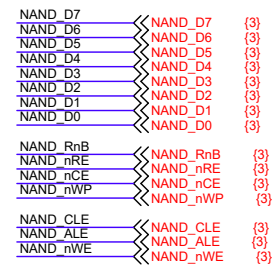
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NAND FLASH

Placce CAP



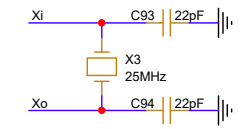
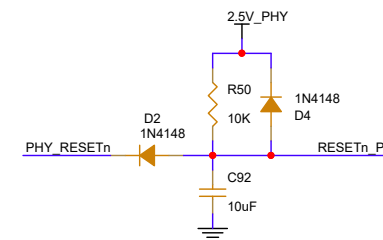
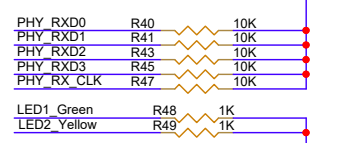
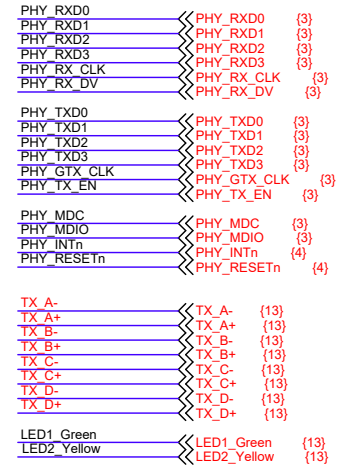
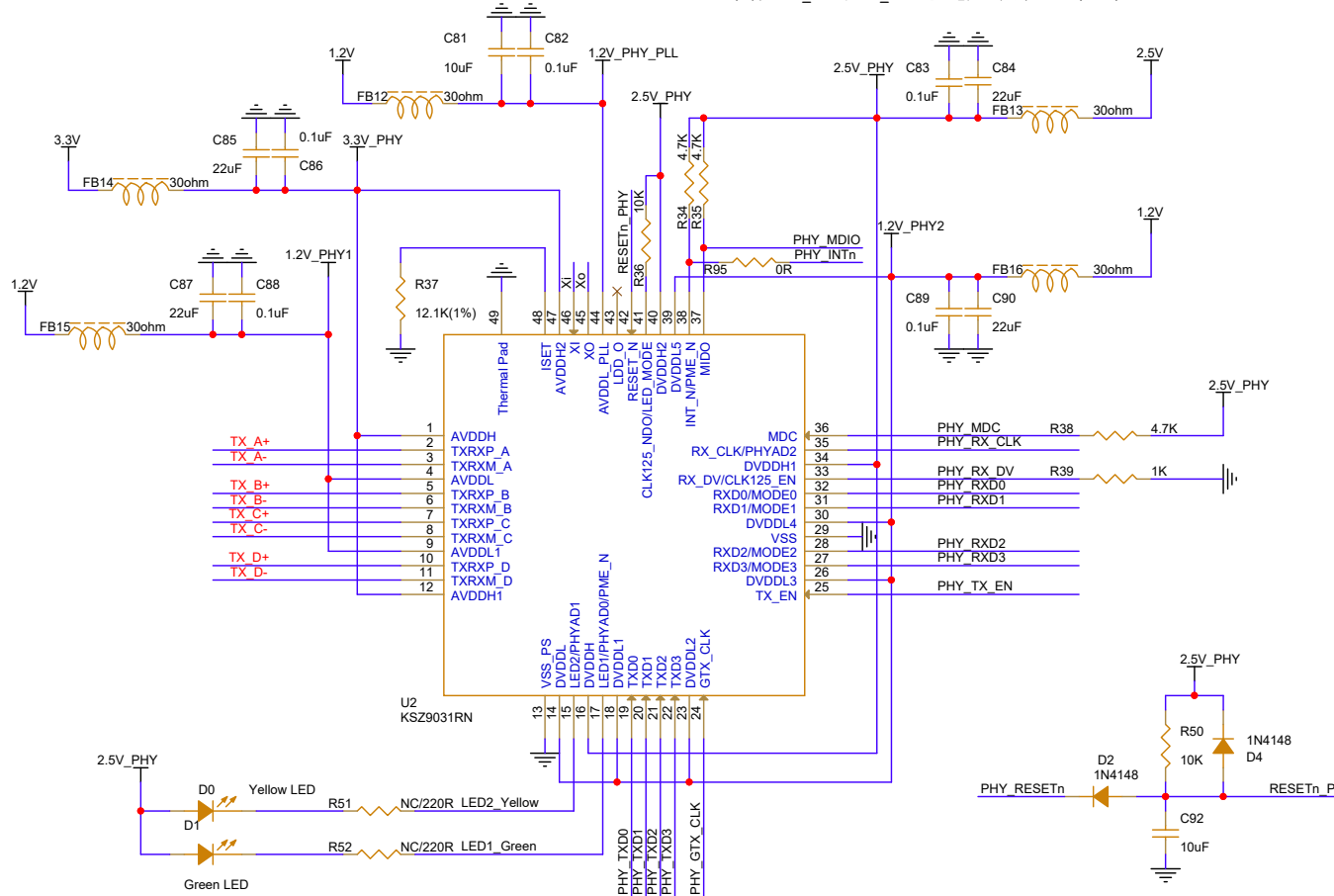
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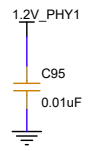
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B	Conector	V1.0	
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10/100/1000M Ethernet

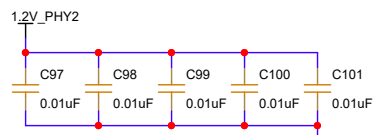
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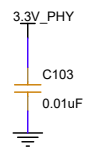
Docouple Capcittance
place near pin4, pin9;



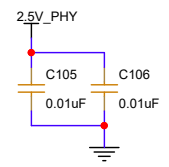
Docouple Capcittance
place near pin14, pin18, pin23, pin26, pin30, pin39;



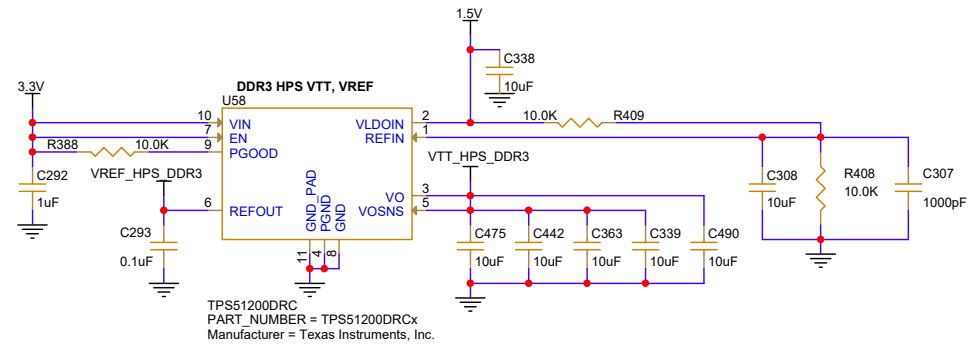
Docouple Capcittance
place near pin1, pin12, pin47;



Docouple Capcittance
place near pin16, pin34, pin40;

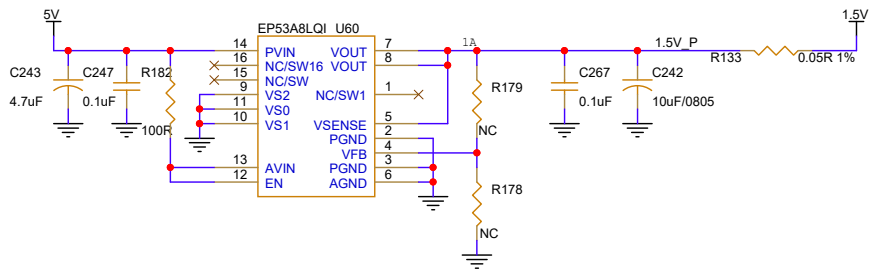
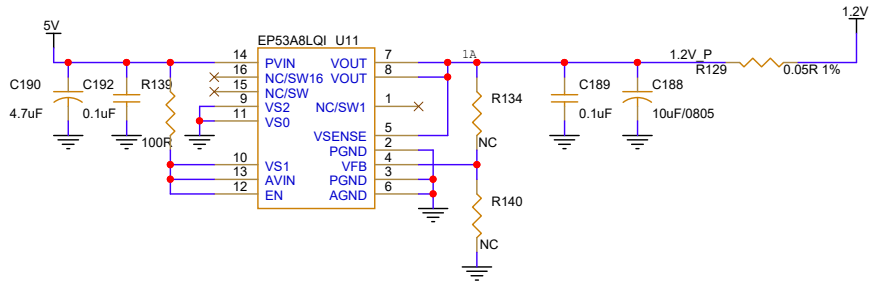
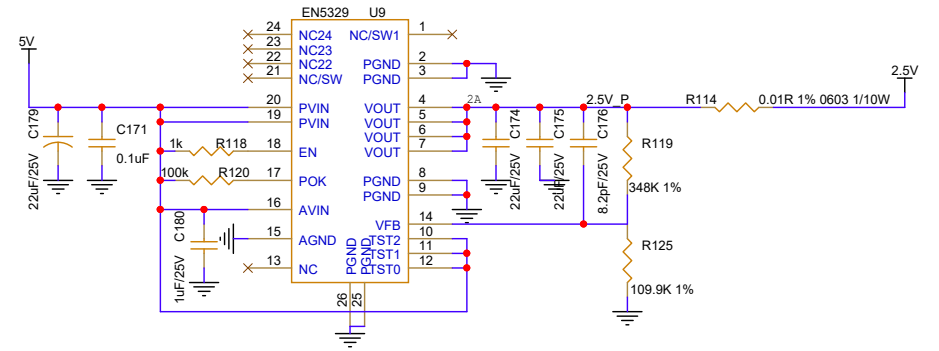
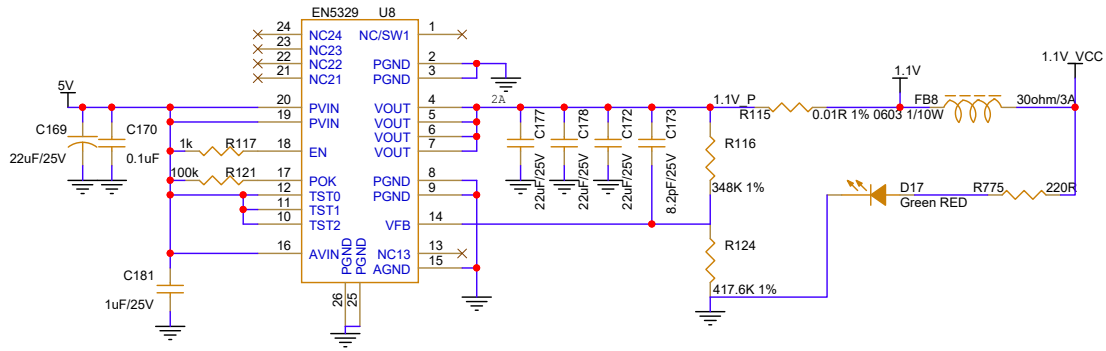


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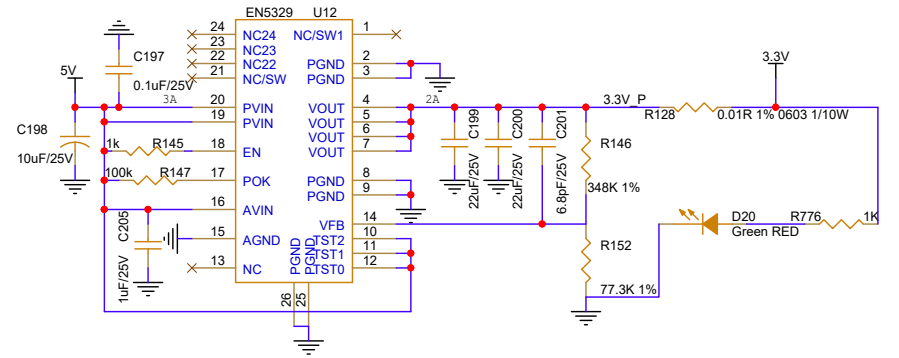


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B	<Doc>	V1.0
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分压 $V_{out} = 0.6v (1+R_a/R_b)$



分压或确定值 $V_{out} = 0.6v (1+R_a/R_b)$



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<Title>		
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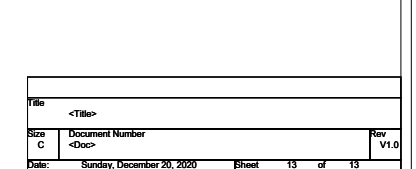
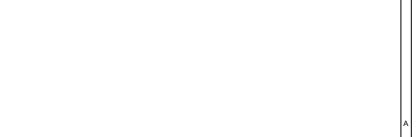
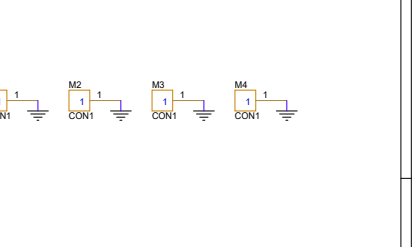
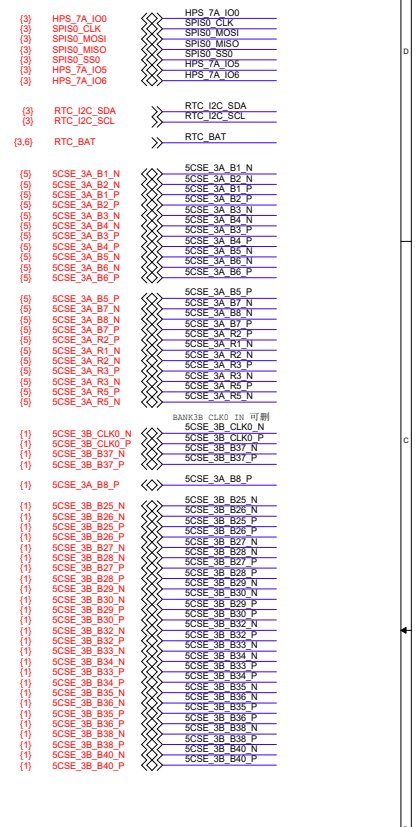
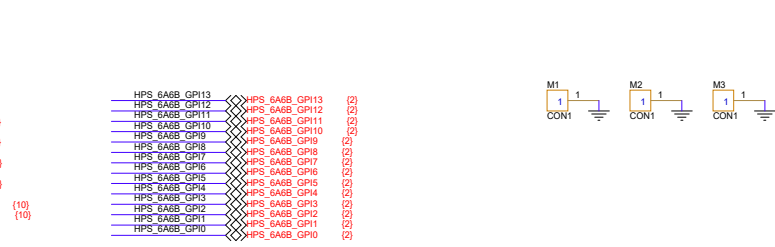
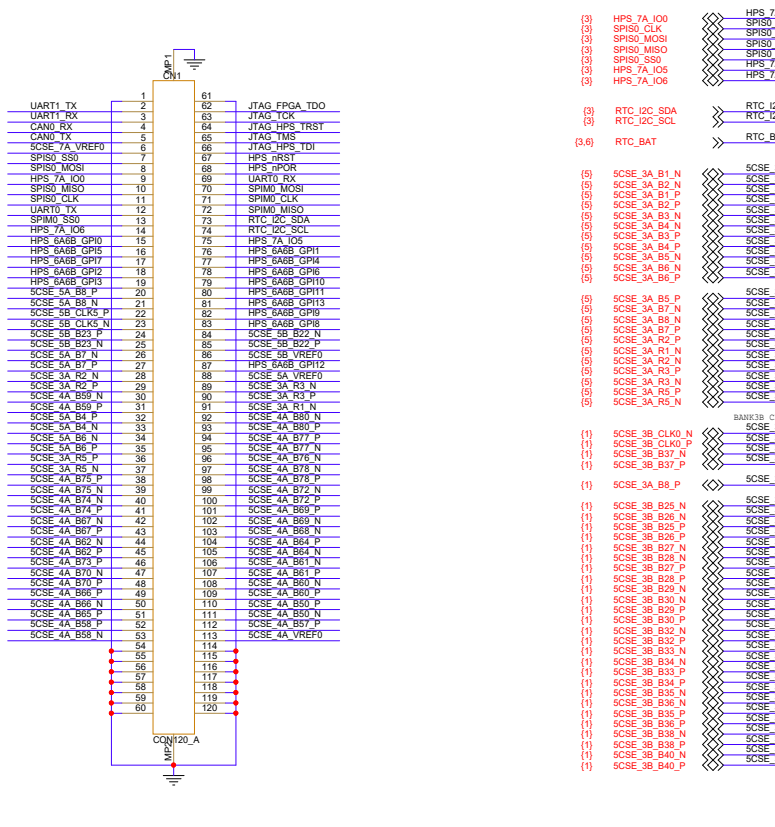
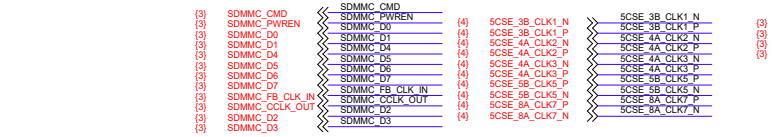
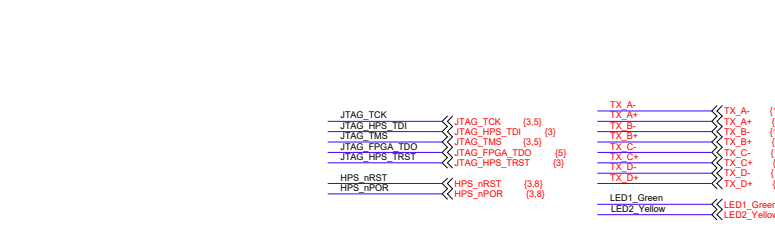
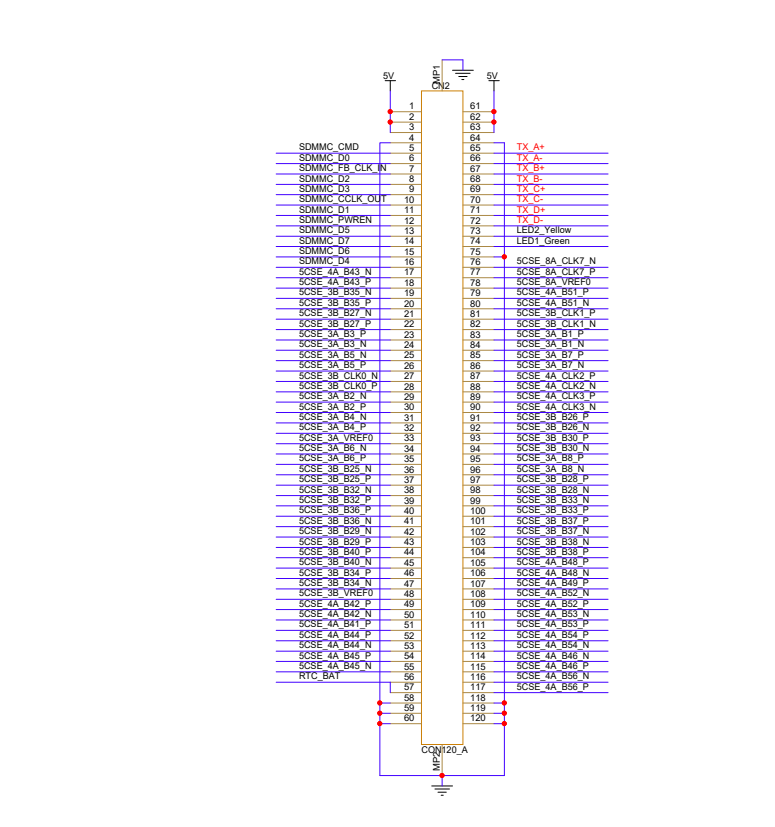
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(1)	SCSE_4A_B61_P	SCSE_4A_B61_P
(1)	SCSE_4A_B61_N	SCSE_4A_B61_N
(1)	SCSE_4A_B62_P	SCSE_4A_B62_P
(1)	SCSE_4A_B62_N	SCSE_4A_B62_N
(1)	SCSE_4A_B63_P	SCSE_4A_B63_P
(1)	SCSE_4A_B63_N	SCSE_4A_B63_N
(1)	SCSE_4A_B64_P	SCSE_4A_B64_P
(1)	SCSE_4A_B64_N	SCSE_4A_B64_N
(1)	SCSE_4A_B65_P	SCSE_4A_B65_P
(1)	SCSE_4A_B65_N	SCSE_4A_B65_N
(1)	SCSE_4A_B66_P	SCSE_4A_B66_P
(1)	SCSE_4A_B66_N	SCSE_4A_B66_N
(1)	SCSE_4A_B67_P	SCSE_4A_B67_P
(1)	SCSE_4A_B67_N	SCSE_4A_B67_N
(1)	SCSE_4A_B68_P	SCSE_4A_B68_P
(1)	SCSE_4A_B68_N	SCSE_4A_B68_N
(1)	SCSE_4A_B69_P	SCSE_4A_B69_P
(1)	SCSE_4A_B69_N	SCSE_4A_B69_N
(1)	SCSE_4A_B70_P	SCSE_4A_B70_P
(1)	SCSE_4A_B70_N	SCSE_4A_B70_N
(1)	SCSE_4A_B71_P	SCSE_4A_B71_P
(1)	SCSE_4A_B71_N	SCSE_4A_B71_N
(1)	SCSE_4A_B72_P	SCSE_4A_B72_P
(1)	SCSE_4A_B72_N	SCSE_4A_B72_N
(1)	SCSE_4A_B73_P	SCSE_4A_B73_P
(1)	SCSE_4A_B73_N	SCSE_4A_B73_N
(1)	SCSE_4A_B74_P	SCSE_4A_B74_P
(1)	SCSE_4A_B74_N	SCSE_4A_B74_N
(1)	SCSE_4A_B75_P	SCSE_4A_B75_P
(1)	SCSE_4A_B75_N	SCSE_4A_B75_N
(1)	SCSE_4A_B76_P	SCSE_4A_B76_P
(1)	SCSE_4A_B76_N	SCSE_4A_B76_N
(1)	SCSE_4A_B77_P	SCSE_4A_B77_P
(1)	SCSE_4A_B77_N	SCSE_4A_B77_N
(1)	SCSE_4A_B78_P	SCSE_4A_B78_P
(1)	SCSE_4A_B78_N	SCSE_4A_B78_N
(1)	SCSE_4A_B79_P	SCSE_4A_B79_P
(1)	SCSE_4A_B79_N	SCSE_4A_B79_N
(1)	SCSE_4A_B80_P	SCSE_4A_B80_P
(1)	SCSE_4A_B80_N	SCSE_4A_B80_N

(1)	SCSE_3B_B22_P	SCSE_3B_B22_P
(1)	SCSE_3B_B22_N	SCSE_3B_B22_N
(1)	SCSE_3B_B23_P	SCSE_3B_B23_P
(1)	SCSE_3B_B23_N	SCSE_3B_B23_N
(1)	SCSE_5A_B4_P	SCSE_5A_B4_P
(1)	SCSE_5A_B4_N	SCSE_5A_B4_N
(1)	SCSE_5A_B6_P	SCSE_5A_B6_P
(1)	SCSE_5A_B6_N	SCSE_5A_B6_N
(1)	SCSE_5A_B7_P	SCSE_5A_B7_P
(1)	SCSE_5A_B7_N	SCSE_5A_B7_N
(1)	SCSE_5A_B8_P	SCSE_5A_B8_P
(1)	SCSE_5A_B8_N	SCSE_5A_B8_N

(4)	SCSE_3A_VREF0	SCSE_3A_VREF0
(4)	SCSE_3B_VREF0	SCSE_3B_VREF0
(4)	SCSE_4A_VREF0	SCSE_4A_VREF0
(4)	SCSE_5A_VREF0	SCSE_5A_VREF0
(4)	SCSE_6B_VREF0	SCSE_6B_VREF0
(4)	SCSE_7A_VREF0	SCSE_7A_VREF0
(4)	SCSE_8A_VREF0	SCSE_8A_VREF0

(3)	SDMMC_CMD	SDMMC_CMD
(3)	SDMMC_PWRN	SDMMC_PWRN
(3)	SDMMC_D0	SDMMC_D0
(3)	SDMMC_D1	SDMMC_D1
(3)	SDMMC_D4	SDMMC_D4
(3)	SDMMC_D5	SDMMC_D5
(3)	SDMMC_D6	SDMMC_D6
(3)	SDMMC_D7	SDMMC_D7
(3)	SDMMC_D1	SDMMC_FB_CLK_IN
(3)	SDMMC_CCLK_OUT	SDMMC_CCLK_OUT
(3)	SDMMC_D2	SDMMC_D2
(3)	SDMMC_D3	SDMMC_D3

(4)	SCSE_3B_CLK1_N	SCSE_3B_CLK1_N
(4)	SCSE_3B_CLK1_P	SCSE_3B_CLK1_P
(4)	SCSE_4A_CLK2_N	SCSE_4A_CLK2_N
(4)	SCSE_4A_CLK2_P	SCSE_4A_CLK2_P
(4)	SCSE_4A_CLK3_N	SCSE_4A_CLK3_N
(4)	SCSE_4A_CLK3_P	SCSE_4A_CLK3_P
(4)	SCSE_5B_CLK5_N	SCSE_5B_CLK5_N
(4)	SCSE_5B_CLK5_P	SCSE_5B_CLK5_P
(4)	SCSE_8A_CLK7_N	SCSE_8A_CLK7_N
(4)	SCSE_8A_CLK7_P	SCSE_8A_CLK7_P



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