-- Refer to page 43 of the audio codec datasheet and the schematic
-- on p. 38 of DE1 User's manual. CSB is tied to ground so the 7-bit base address is
-- b0011010 + 0 R/W' = 0x34.
-- The registers are initialized as follows:

-- Register 0, 00h (Left Line In):
-- disable simultaneous load, disable mute, left line in is high
-- Hence, data to be sent through i2c: 0x34001A
-- Note that .MIF file contents are specified in unsigned decimal, hence .mif data is 3407898

-- Register 1, 02h (Right Line In):
-- disable simultaneous load, disable mute, right line in is high
-- Hence data to be sent through i2c : 0x34021A .mif data: 3408410

-- Register 2, 04h (Left Headphone Out):
-- disable simultaneous load, disable zero crossing detect, left headphone out is high
-- Hence data to be sent through i2c : 0x340479 .mif data: 3409017

-- Register 3, 06h (Right Headphone Out):
-- disable simultaneous load, disable zero crossing detect, right headphone out is high
-- Hence data to be sent through i2c : 0x340679 .mif data: 3409529

-- Register 4, 08h (Analogue Audio Path Control):
-- side tone attenuation to -6 dB, disable side tone, DAC select, disable bypass,
-- line input select to ADC,disable mic mute, disable mic boost
-- Hence data to be sent through i2c : 0x340810 .mif data: 3409936

-- Register 5, 0Ah (Digital Audio Path Control):
-- clear DC offset (high pass filter is enabled), disable soft mute, 48 KHz de-emphasis
-- control, enable high pass filter
-- Hence data to be sent through i2c : 0x340A06 .mif data: 3410438

-- Register 6, 0Ch (Power Down Control):
-- disable all power down modes
-- Hence data to be sent through i2c : 0x340C00 .mif data: 3410944

-- Register 7, 0Eh (Digital Audio Interface Format):
-- don't invert bit clock, slave mode, no channel swap, msb is
-- available on first bclk rising edge, 16 bits, msb-first, left-justified
-- Hence data to be sent through i2c : 0x340E01 .mif data: 3411457

-- Register 8, 10h (Digital Audio Interface Format):
-- clockout is core clock, core clock is MCLK, ADC/DAC sample rate control is 48 KHz
-- with a 18.432 MHz MCLK (384 fs, in normal mode)
-- Hence data to be sent through i2c : 0x341002 .mif data: 3411970

-- Register 9, 12h (turn on interface):
-- activate interface
-- Hence data to be sent through i2c : 0x341201 .mif data: 3412481