

# Questa Sim Error

QuestaIntel Starter FPGA Edition-64 2023.3

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

Library

Name	Type	Path
220model	Library	SMODEL_TECH/./intel/vhdl/220model
220model_ver	Library	SMODEL_TECH/./intel/verilog/220model
altera	Library	SMODEL_TECH/./intel/vhdl/altera
altera_Insim	Library	SMODEL_TECH/./intel/vhdl/altera_Insim
altera_Insim_ver	Library	SMODEL_TECH/./intel/verilog/altera_In...
altera_mf	Library	SMODEL_TECH/./intel/vhdl/altera_mf
altera_mf_ver	Library	SMODEL_TECH/./intel/verilog/altera_mf
altera_ver	Library	SMODEL_TECH/./intel/verilog/altera
arriai	Library	SMODEL_TECH/./intel/vhdl/arriai
arriai_hssi	Library	SMODEL_TECH/./intel/vhdl/arriai_hssi
arriai_hssi_ver	Library	SMODEL_TECH/./intel/verilog/arriai_hssi
arriai_pcie_hip	Library	SMODEL_TECH/./intel/vhdl/arriai_pcie...
arriai_pcie_hip_ver	Library	SMODEL_TECH/./intel/verilog/arriai_pc...
arriai_ver	Library	SMODEL_TECH/./intel/verilog/arriai
arriaiIgz	Library	SMODEL_TECH/./intel/vhdl/arriaiIgz
arriaiIgz_hssi	Library	SMODEL_TECH/./intel/vhdl/arriaiIgz_hss
arriaiIgz_hssi_ver	Library	SMODEL_TECH/./intel/verilog/arriaiIgz_...
arriaiIgz_pcie_hip	Library	SMODEL_TECH/./intel/vhdl/arriaiIgz_pc...
arriaiIgz_pcie_hip_v...	Library	SMODEL_TECH/./intel/verilog/arriaiIgz_...
arriaiIgz_ver	Library	SMODEL_TECH/./intel/verilog/arriaiIgz
arriav	Library	SMODEL_TECH/./intel/vhdl/arriav
arriav_hssi_ver	Library	SMODEL_TECH/./intel/verilog/arriav_hssi
arriav_pcie_hip_ver	Library	SMODEL_TECH/./intel/verilog/arriav_pc...
arriav_ver	Library	SMODEL_TECH/./intel/verilog/arriav
arriavIgz	Library	SMODEL_TECH/./intel/vhdl/arriavIgz
arriavIgz_hssi	Library	SMODEL_TECH/./intel/vhdl/arriavIgz_hssi

Objects

Name	Value	Kind	Mode
------	-------	------	------

Fatal License Error

Unable to checkout a viewer license necessary for use of the Questa Intel Starter FPGA Edition graphical user interface. Vsim is closing.

OK

Transcript

```
# ** License Issue: License server does not support this feature (intelqsimstarter)
# ** License Issue: Invalid host. (/home/j/intelFPGA_lite/23.1std/licenses/LR-191993_License.dat)
# ** Error: Failure to checkout 'intelqsimstarter' license feature.
```

See video  
link guide  
shown on  
slide 12

Get Free license- Search FPGA and it should get you here. Select link I circled in yellow

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Intel Programmable Solutions Group is now Altera®, an Intel Company  
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in YouTube Facebook X

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An Intel Company

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 <p>Arria® Stratix® Agilex™ Cyclone® MAX®</p>	 <p>FPGA AI NIC, SmartNIC, IPU, and SoMs</p>	 <p>FPGA Development Tools</p>	 <p>intel. FPGA Development Kits</p>
FPGAs, SoC FPGAs, CPLDs	FPGA Acceleration Platforms and System-on-Modules (SoMs)	FPGA Design Software, Tools, Intel® Quartus® Prime Software	FPGA Development Kits

Go to the bottom of the next page and you should see licensing. Select the link

## Additional Resources



### Download

Get the complete suite of Altera® FPGA design tools.



### Licensing

Find out how to get a license file, set up a license, solve license problems, or change license information.



### Buy

Find local distributors that can help you in purchasing Altera® FPGA Software.



### Training

This page lists all the online and instructor-led courses currently available.

# Intel® FPGA Licensing Support Center

Information on license types, getting a license file, setting up a license file, and resolving license-related issues.

[Get Started](#)

[FAQs](#)

[Quick Links](#)

[NIC/Host/Guard ID](#)

## Get Started

Thank you for choosing Intel® as your technology partner. We are here to guide you through the licensing process and help you make the most of your FPGA experience. Whether you are new or an existing user, we will provide you with all the essential information to get started quickly.

### Step 1: License Key Required?

Check the software tool license requirement.

### Step 2: License Generation

Generate a license file from the [Intel® FPGA Self-Service Licensing Center](#).

Select this link



### Step 3: License Setup

Set up the license depending on the type of license used.

### Step 4: Debugging

Troubleshoot and debug any licensing issues.

Somewhere at these steps your prompted to create an account or profile specifically for a license

Cant help but feeling your voluntarily getting scammed with the details prompted For,,, ugh. Its legit though.

tel. PRODUCTS SUPPORT SOLUTIONS DEVELOPERS PARTNERS FOUNDRY

Intel® FPGA Self-Service Licensing Center

Home Licenses Computers and License Files Admins Sign up for Evaluation or No-Cost Licenses Reports Help

# Hi! Welcome to the new Licensing Center.

Try the new License Assistant

License Assistant

Thanks for chatting with

- Rehost and j licenses
- Renew and j licenses
- Create com license for yn license
- Create tem checkout licen floating lic
- End Ct

Type your message...

Select Product & Add Additional Details

Add Host & Generate License

Web Description	Maintenance Expiration ⓘ	Licen
<input type="checkbox"/> Intel® Quartus® Prime Software 90-Day Evaluation (Standard and Pro Editions) (License: EVALUATION-LIC)	2025-01-02	
<input type="checkbox"/> Agilex™ 5 E-Series FPGA Software Enablement (License: SW-AGILEX-5E)	2025-10-02	
<input checked="" type="checkbox"/> Questa*-Intel® FPGA Starter Edition (License: SW-QUESTA)	2025-10-02	
<input type="checkbox"/> Nios® V/m Microcontroller Intel® FPGA IP (License: IP-NIOSVM)	2025-10-02	
<input type="checkbox"/> Nios® V/g General Purpose Processor Intel® FPGA IP (License: IP-NIOSVG)	2025-10-02	

Scroll to the bottom of this page and select up to 2 seats, I guess. I just used 1.

<input type="checkbox"/> Discontinued – Intel® Quartus® II Software (License: SW-QUARTUS-WE-FIX)	2025-10-02
<input type="checkbox"/> Discontinued – MAX+PLUS® II Software (License: MAXPLUS2WEB)	2025-10-02

\*# of Seats ⓘ

1

Next

# Create a computer which your free license will be associated with

\* = Required Information

\* Computer Name

anyNamUwant

\* License Type

FIXED

[View all dependencies](#)

Active 



Redundant Server ID 1

Companion Computer ID 1 

Primary Admin

sumName

\* Computer Type

NIC ID

[View all dependencies](#)

\* Primary Computer ID

12 hex characters

See next slide for  
char's  
To place in this bloc

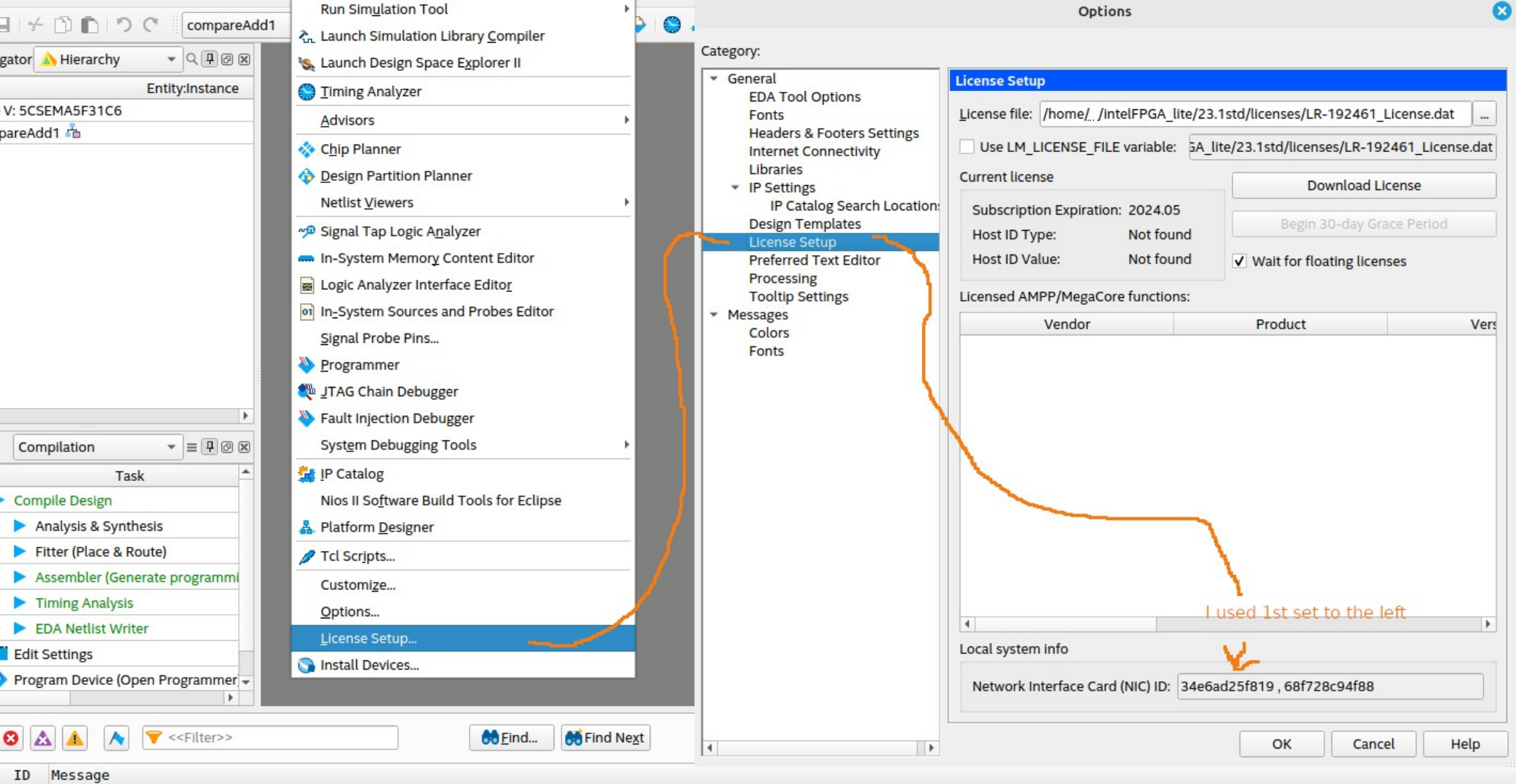
Temporary NIC ID

Redundant Server ID 2

Companion Computer ID 2 

Primary Admin Email

myEmail@anEmail.com







Add Host &amp; Generate License

### \* Generate License (Create a New Computer Or Choose an Existing Computer)

Choose an Existing Computer ⓘ

[View All Computers](#)

2

Create a New Computer ⓘ

1

+New Computer

3

\* I have read and agree to the terms of use of this license as listed below

Maintenance for this license is valid for 12 months from the date you sign up for this license. [Terms of Use](#)

Check this box if you don't want Intel to contact you for feedback. Your feedback helps us improve the product.

A license.data  
Will be emailed

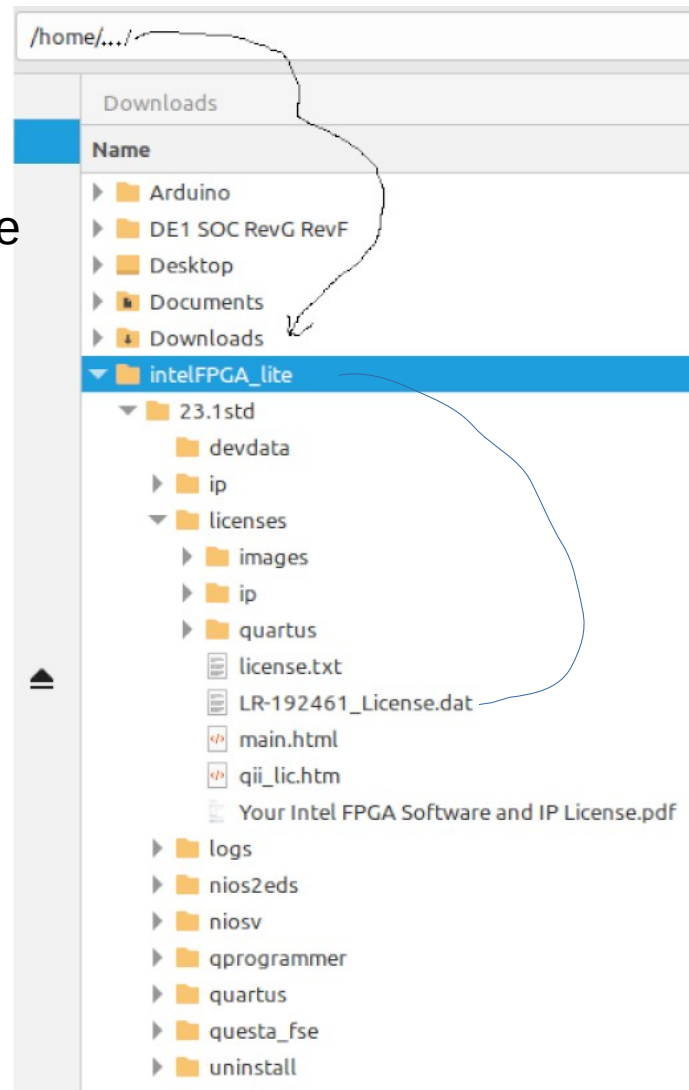
4

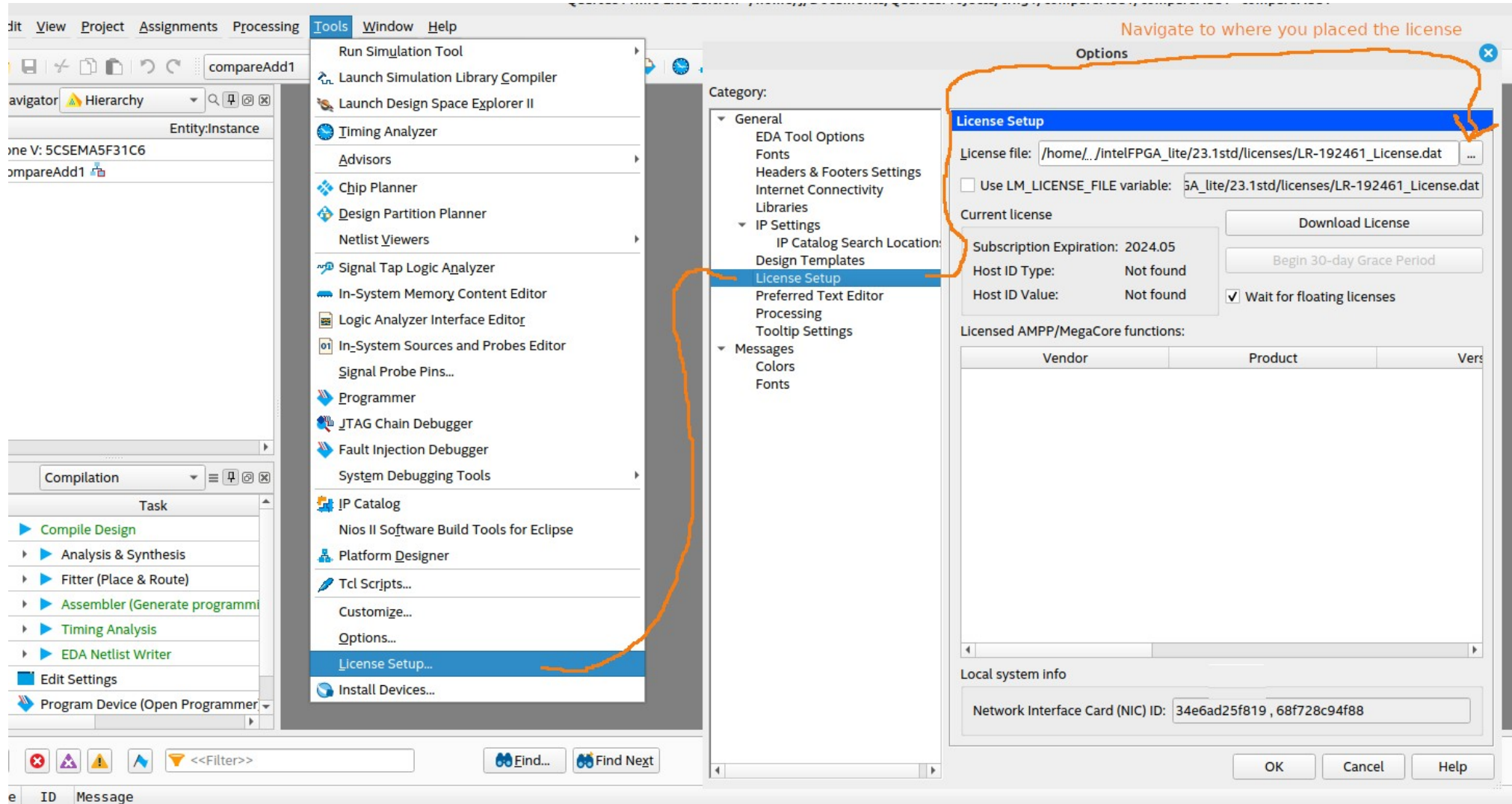
Back

Generate

I placed this license.dat  
File in the tree shown.

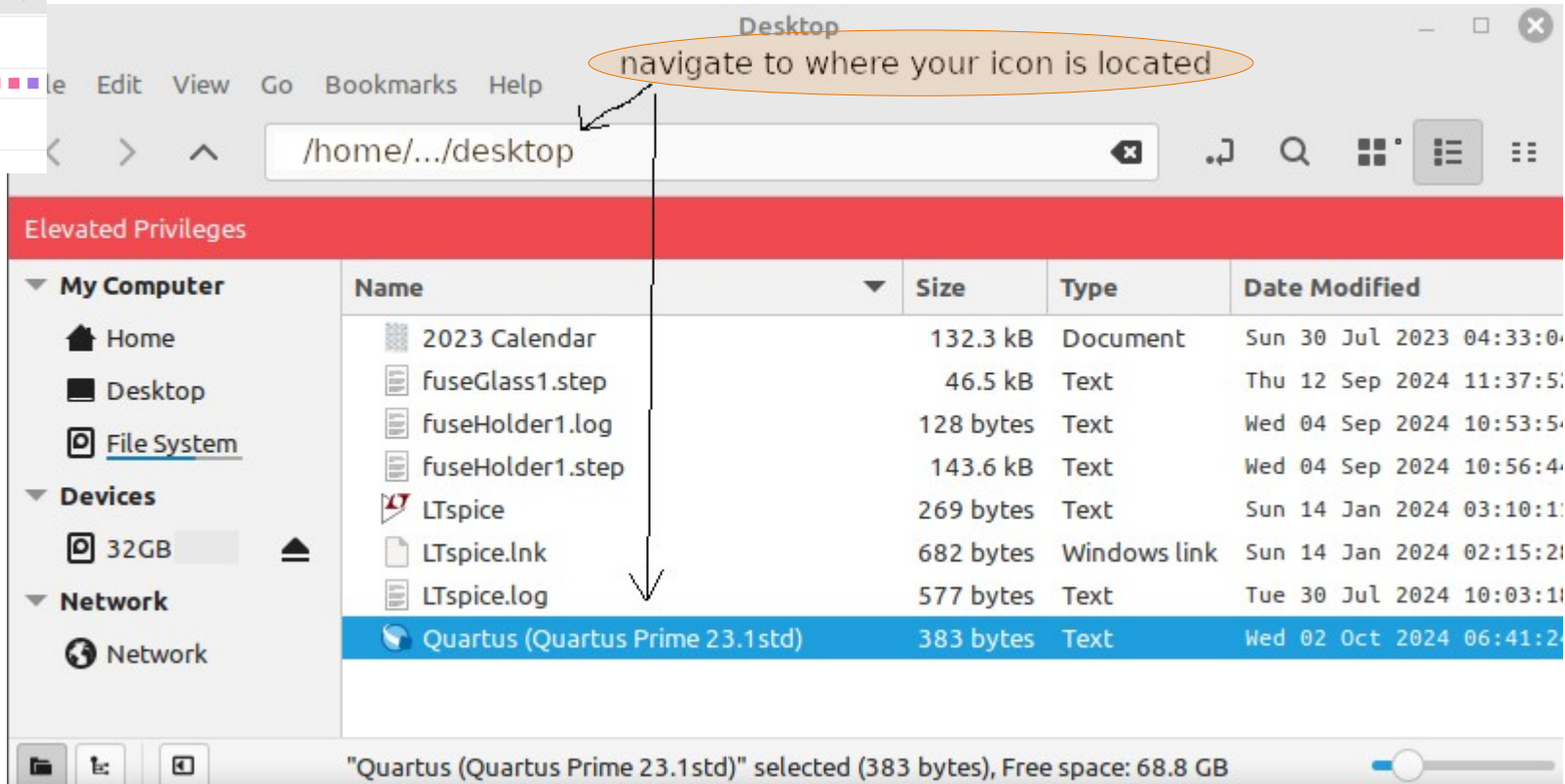
Not sure if it's required there  
But just seemed logical

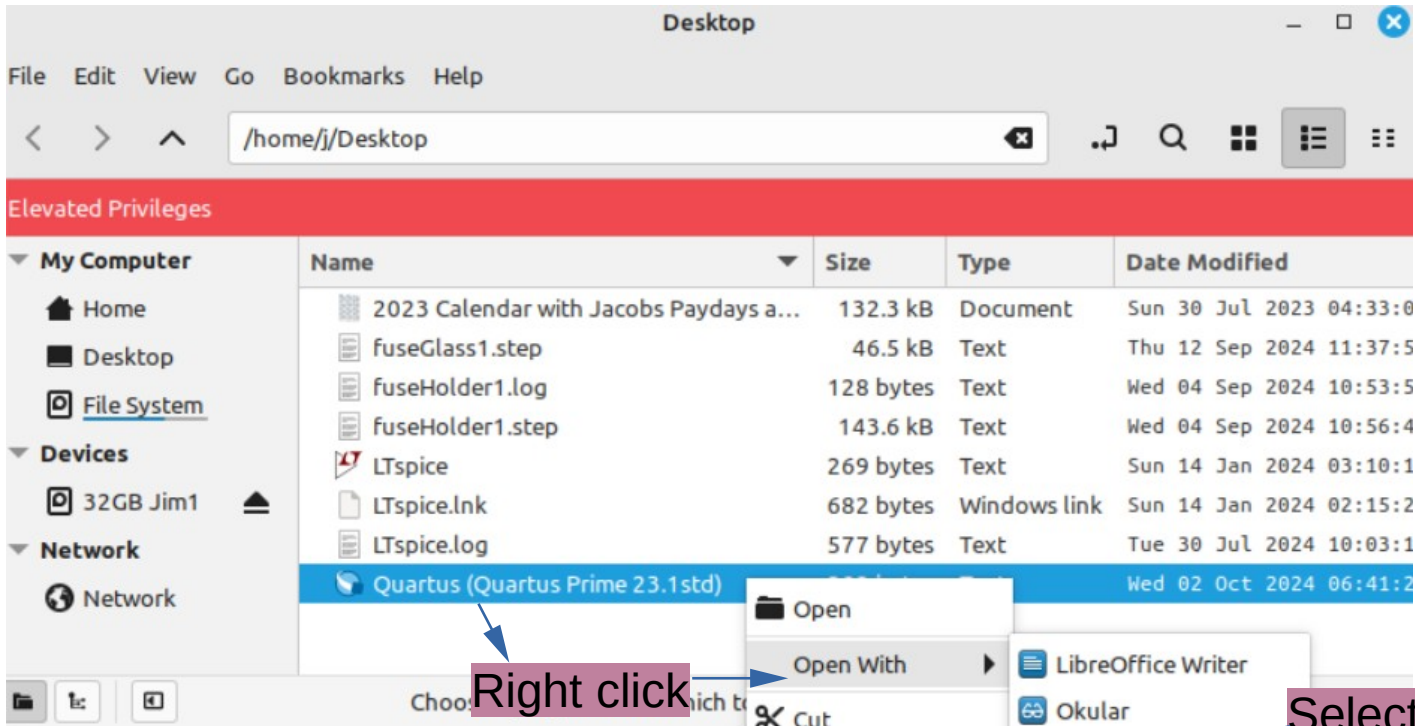




1 I opened as Root

2 **Set the environment.** This will open the waveform viewer since your license is now pointed to...





Right click

Select Text Editor Or similar



Elevated Privileges

Quartus (Quartus Prime 23.1std).desktop x

**[Desktop Entry]**

Type=Application

Version=0.9.4

Name=Quartus (Quartus Prime 23.1std)

Comment=Quartus (Quartus Prime 23.1std)

Icon=/home/ /intelFPGA\_lite/23.1std/quartus/adm/quartusii.png

Exec=env LM LICENSE FILE=/home/./intelFPGA\_lite/23.1std/licenses/LR-192461 License.dat /home/./intelFPGA\_lite/23.1std/quartus/bin/quartus --64bit

Terminal=false

Path=/home/./intelFPGA\_lite/23.1std

Add green line info, before what is in place already.  
Note there is a space between the two statements.  
Press "save"

space

Note your license

<https://www.intel.com/content/www/us/en/docs/programmable/683472/24-2/and-software-license.html>

Modified "env" instead in accordance with video link guide

### On Linux System

Run one of the following commands in a command prompt window:

```
export LM_LICENSE_FILE=<path to license>:$LM_LICENSE_FILE
```

```
setenv LM_LICENSE_FILE "<path_to_license_file>"
```

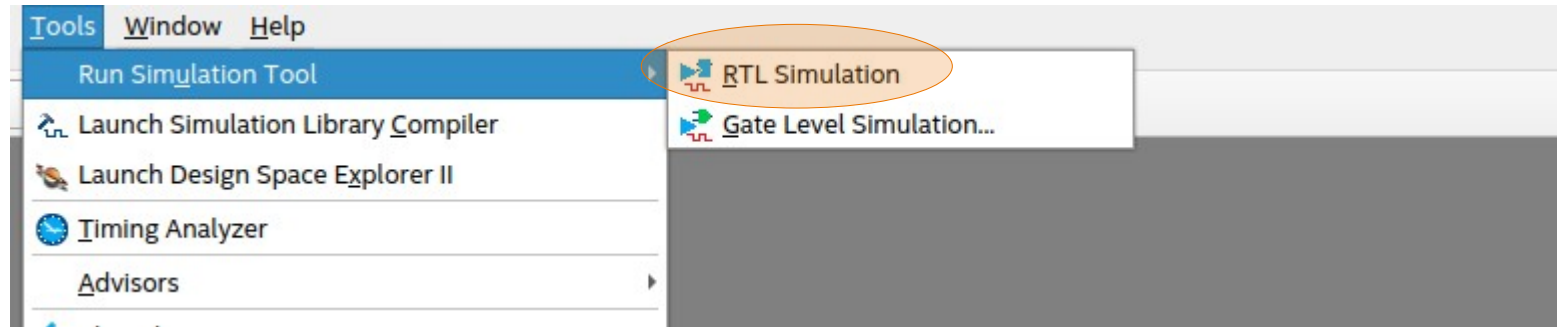
You can also set up the Questa\*-Intel® FPGA Edition software license using the Siemens EDA license daemon `mgcld`, which you can find in the `<Questa - Intel FPGA Edition installation directory>/` directory. Before starting the Questa\*-Intel® FPGA Edition software, set the `MGLS_LICENSE_FILE` environment variable to the location and file name of the Questa\*-Intel® FPGA Edition license file. For example:

```
MGLS_LICENSE_FILE (<Questa installation directory>/licenses/eda/license.dat)
```

or with the `<port>@<hostname>` notation, where `<port>` is the license port number and `<hostname>` is the license server's host name. For example, `1900@my_lic_server`.

This is the guide I followed (mostly):  
I found it very helpful

<https://www.youtube.com/watch?v=e5kHFiAVcRI>





File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

Library

Name	Type	Path
work	Library	rtl_work
220model	Library	\$MODEL_TECH/./intel/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./intel/verilog/220model
altera	Library	\$MODEL_TECH/./intel/vhdl/altera
altera_Insim	Library	\$MODEL_TECH/./intel/vhdl/altera_Insim
altera_Insim_ver	Library	\$MODEL_TECH/./intel/verilog/altera_In...
altera_mf	Library	\$MODEL_TECH/./intel/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./intel/verilog/altera_mf
altera_ver	Library	\$MODEL_TECH/./intel/verilog/altera
ariaii	Library	\$MODEL_TECH/./intel/vhdl/ariaii
ariaii_hssi	Library	\$MODEL_TECH/./intel/vhdl/ariaii_hssi
ariaii_hssi_ver	Library	\$MODEL_TECH/./intel/verilog/ariaii_hssi
ariaii_pcie_hip	Library	\$MODEL_TECH/./intel/vhdl/ariaii_pcie...
ariaii_pcie_hip_ver	Library	\$MODEL_TECH/./intel/verilog/ariaii_pc...
ariaii_ver	Library	\$MODEL_TECH/./intel/verilog/ariaii
ariaiigz	Library	\$MODEL_TECH/./intel/vhdl/ariaiigz
ariaiigz_hssi	Library	\$MODEL_TECH/./intel/vhdl/ariaiigz_hssi
ariaiigz_hssi_ver	Library	\$MODEL_TECH/./intel/verilog/ariaiigz_...
ariaiigz_pcie_hip	Library	\$MODEL_TECH/./intel/vhdl/ariaiigz_pc...
ariaiigz_pcie_hip_v...	Library	\$MODEL_TECH/./intel/verilog/ariaiigz_...
ariaiigz_ver	Library	\$MODEL_TECH/./intel/verilog/ariaiigz
ariav	Library	\$MODEL_TECH/./intel/vhdl/ariav
ariav_hssi_ver	Library	\$MODEL_TECH/./intel/verilog/ariav_hssi
ariav_pcie_hip_ver	Library	\$MODEL_TECH/./intel/verilog/ariav_pc...
ariav_ver	Library	\$MODEL_TECH/./intel/verilog/ariav

Objects

Name	Value	Kind	Mode
[Empty]			

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path	Class Info
[Empty]					

Transcript

```
#
#
# stdin: <EOF>
Questa>
```

<No Design Loaded>

VoilA!! your set