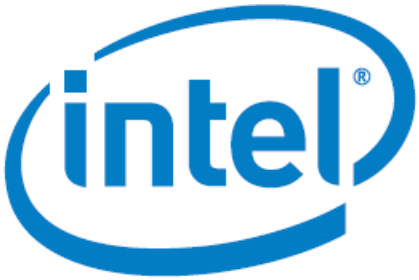


Nios II Processor Booting from CFI Flash on Cyclone V GX FPGA Development Kit

Date: 29 March 2017

Revision: 1.0

Introduction

This document demonstrates step-by-step instructions on how to boot a simple Hello World Nios II application from CFI flash using Cyclone V GX FPGA Development Kit.

Prerequisite

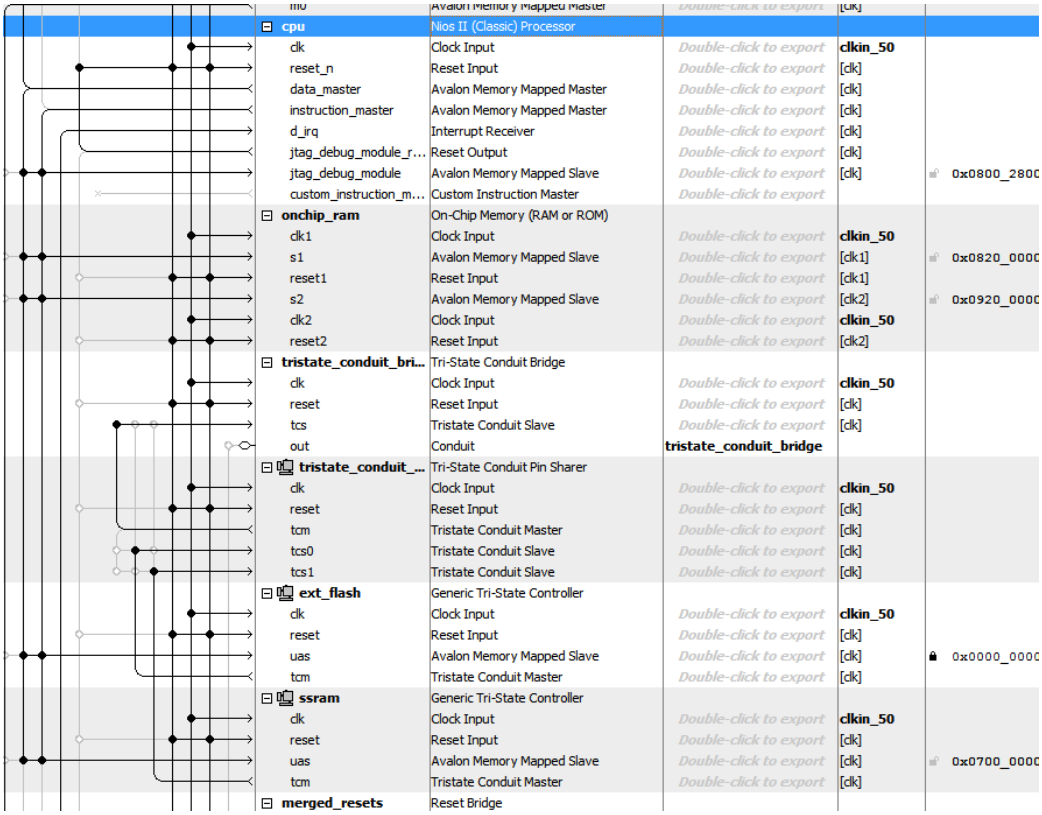
Before you start, download the Kit installation for Cyclone V GX FPGA Development Kit.

Related links:

- Avalon Tri-State Conduit Components User Guide
- Parallel Flash Loader IP Core User Guide
- Generic Nios II Booting Methods User Guide

Design Creation

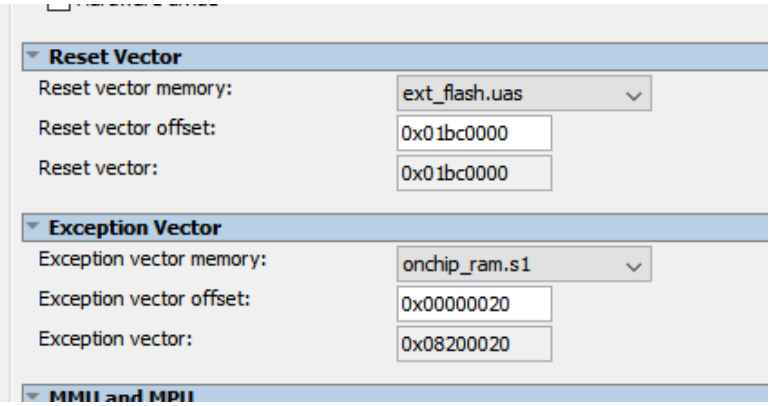
In this example, you do not have to create your hardware design from scratch, use the hardware design in "*<kit installation directory>/cycloneVGX_5cgxfc7df31es_fpga/examples/board_update_portal*". Ensure Generic Tri-State Controller and Tri-State Conduit Bridge are added in the Qsys system (c5gxfc7_fpga_bup_qsys.qsys). You may remove other unnecessary components such as TSE to simplify the design.



Qsys Setting

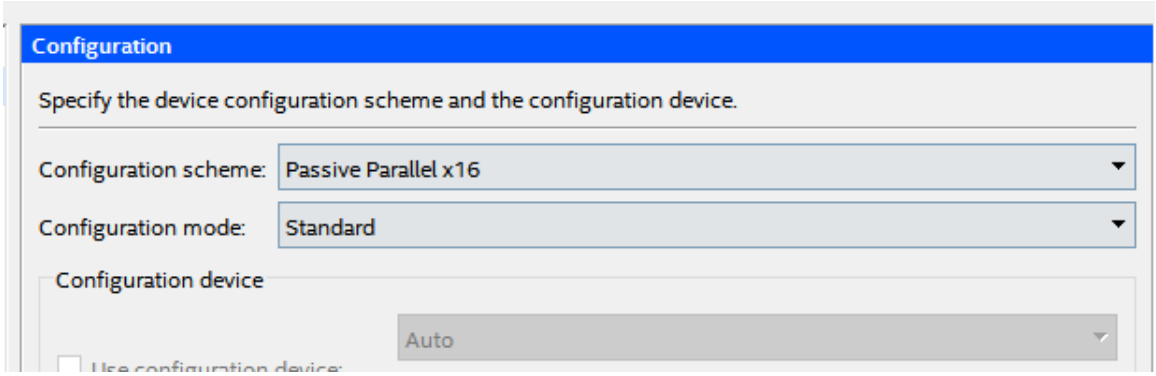
As we are using the Board Update Portal example, the factory hardware and software block in CFI flash will be replaced with new hardware and software blocks created here.

In Nios II Processor parameter editor, set the reset vector memory and exception vector memory as below:



Quartus Setting

The MSEL pins in Cyclone V GX development kit are defaulted to FPPx16 configuration scheme. In Quartus Prime software, set the configuration settings as below:



BSP Editor Setting

In Nios II SBT tool, create the Nios II processor HAL BSP based on the .sopcinfo created from Qsys generation. Refer to table below for BSP editor settings:

Boot Option	BSP Editor Setting: Linker Script	BSP Editor Seting: Settings.Advanced.hal.linker
Nios II processor application execute-in-place from CFI flash	• Set **.text** Linker Section to CFI flash • Set other Linker Sections (**.heap, .rwdata, .rodata, .bss, .stack**) to OCRAM/ External RAM	If the exception vector memory is set to OCRAM/ External RAM, enable the following settings: • allow_code_at_reset • enable_alt_load • enable_alt_load_copy_rodata • enable_alt_load_copy_rwdata • enable_alt_load_copy_exceptions If the exception vector memory is set to CFI flash, enable the following settings: • allow_code_at_reset • enable_alt_load • enable_alt_load_copy_rodata • enable_alt_load_copy_rwdata
Nios II processor application copied from CFI flash to RAM using boot copier	All Linker Sections are set to OCRAM/ External RAM	All settings are left unchecked

Application

1. In the Nios II SBT, create a new application using Hello World template.
2. Once the BSP editor settings configured, build the project and ELF file will be created.
3. Use **mem_init_generate** utility to generate FLASH file by selecting **Make Targets → Build**.
4. Launch **Nios II Command Shell**, use **nios2-elf-objcopy** utility to generate HEX file.

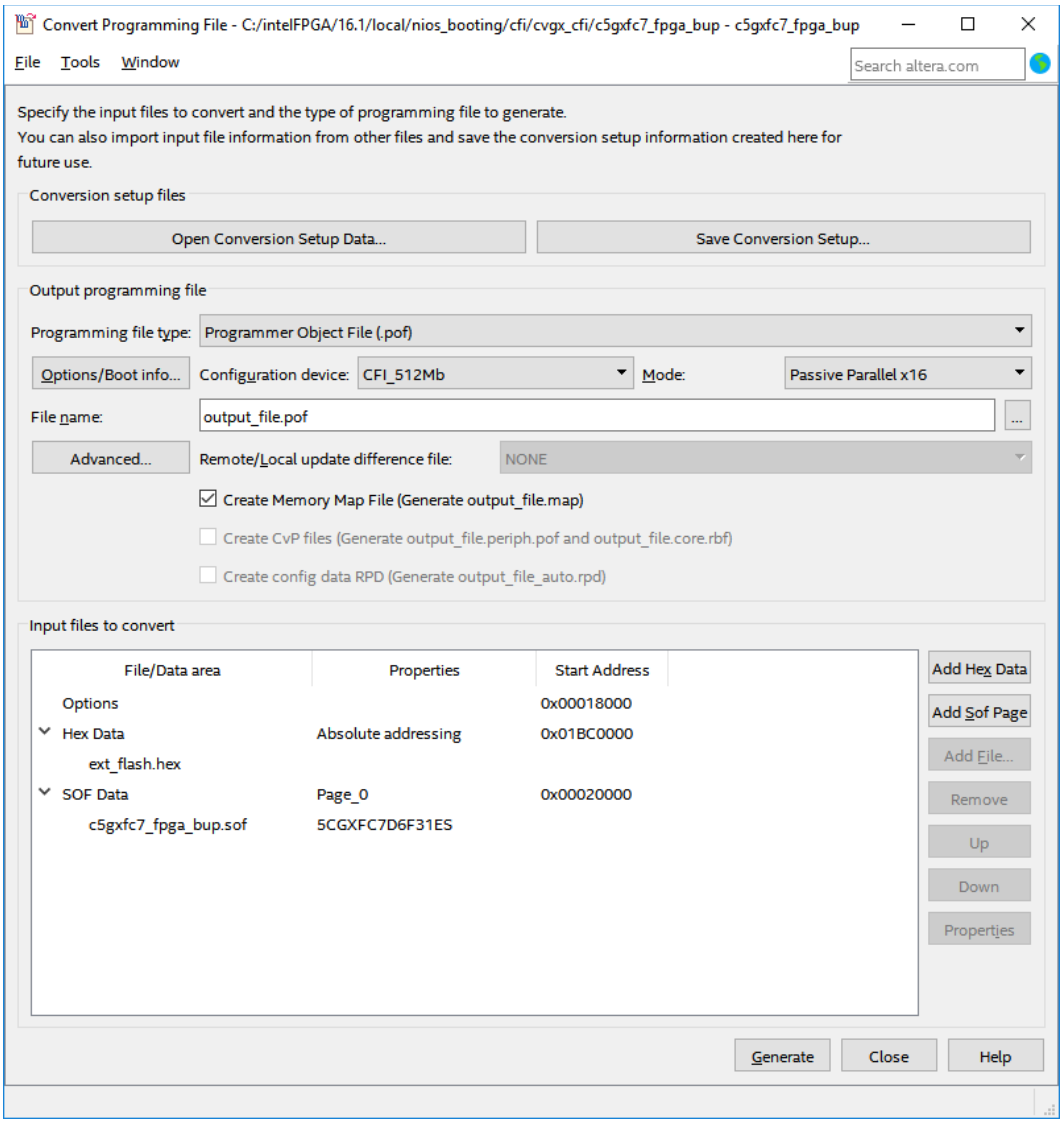
```
$ nios2-elf-objcopy --input-target srec --output-target ihex ext_flash.flash ext_flash.hex --verbose
copy from `ext_flash.flash' [srec] to `ext_flash.hex' [ihex]
```

Programming Files Generation

This example demonstration is using Board Update Portal design for the development kit, therefore you need to follow the CFI flash memory map as below:

Block Description	KB Size	Address Range
Unused	128	0x03FE.0000 - 03FF.FFFF
User software	28,800	0x023C.0000 - 03FD.FFFF
Factory software	8192	0x01BC.0000 - 023B.FFFF
zipfs (html, web content)	4096	0x017C.0000 - 01BB.FFFF
User hardware 2	8064	0x00FE.0000 - 017B.FFFF
User hardware 1	8064	0x0080.0000 - 00FD.FFFF
Factory hardware	8064	0x0002.0000 - 007F.FFFF
PFL option bits	32	0x0001.8000 - 0001.FFFF
Board information	32	0x0001.0000 - 0001.7FFF
Ethernet option bits	32	0x0000.8000 - 000.FFFF
User design reset vector	32	0x0000.0000 - 000.7FFF

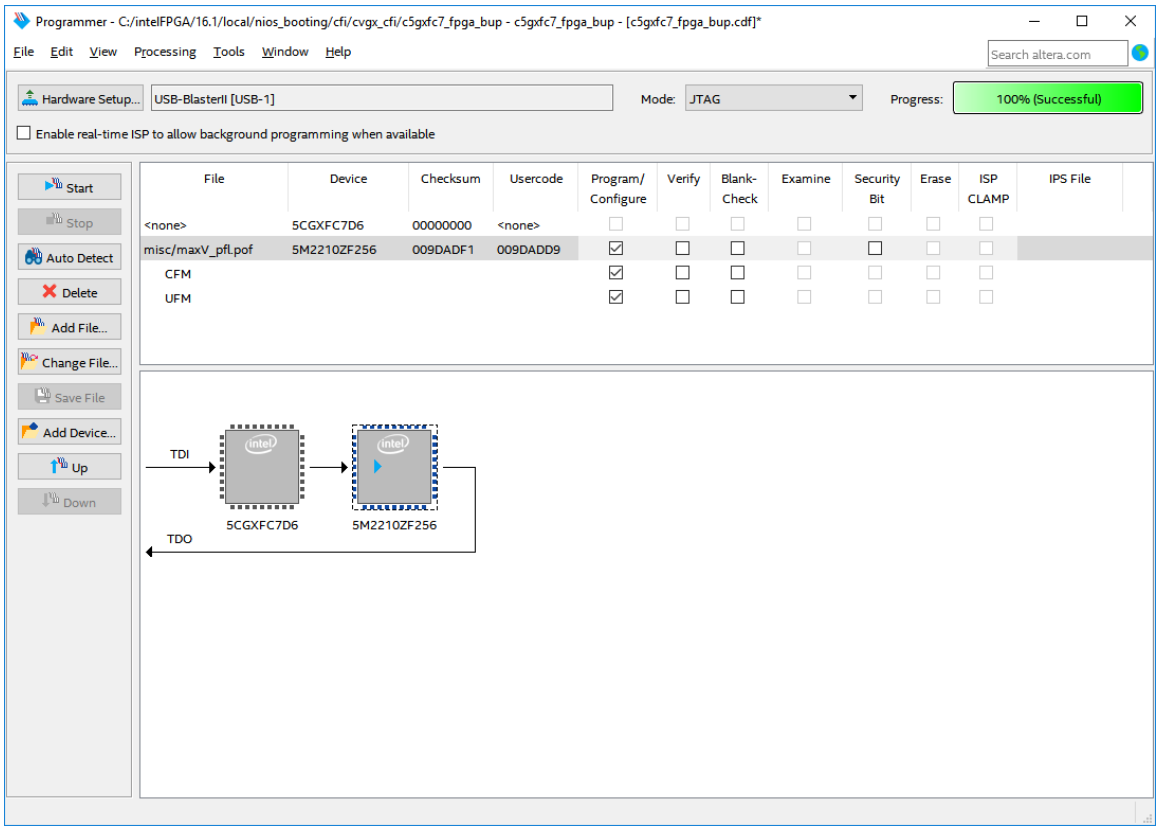
To generate the POF file, follow the configuration as below:



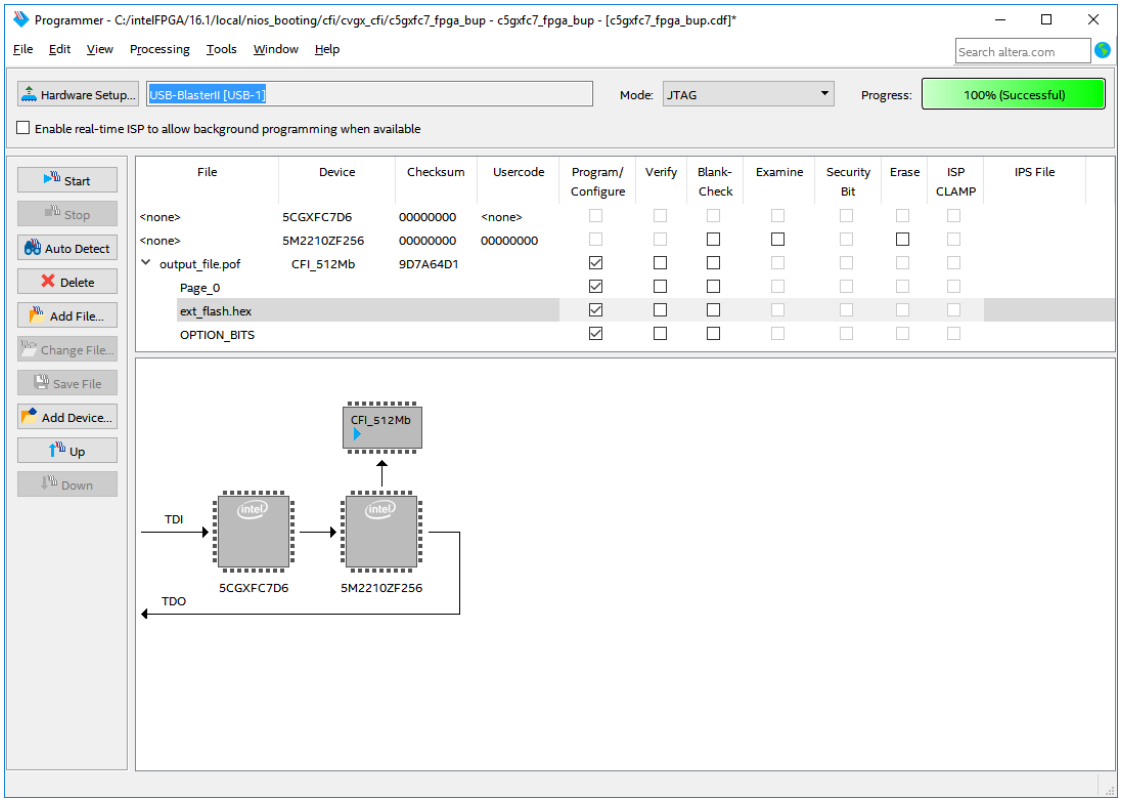
Programming CFI Flash

PFL IP core is required to program the CFI flash. A simple PFL design output file is available here.

1. Program the "**maxV_pfl.pof**" into the MAX V device.



2. Click **Auto Detect** and you should see **CFI_512Mb**.
3. Program the "**output_file.pof**" into the CFI flash.



4. Restore the MAX V design by programming the "**max5.pof**" in "*<kit installation directory>/cycloneVGX_5cgxfc7df31es_fpga/factory_recovery*".