

12G-SDI Audio Reference Design User Guide

Updated for Intel® Quartus® Prime Design Suite: **20.1**

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Chapter 1: Introduction

The 12G-SDI Audio Embed/Extract Reference Design provides an application example for embedding and de-embedding of digital audio data into a 12G-SDI video signal. Hereafter it is referred to as the Reference Design.

This User Guide describes the Reference Design, and any other necessary third-party components, with the goal that the user can quickly and easily evaluate audio over 4K video signals.

Features:

- Embedding of up to 32 audio pairs into SDI TX video signal
- Extracting of up to 32 audio pairs from SDI RX video signal
- Supports 12G-SDI standard
- Four instances of SDI Audio Embed block to embed up to 8 audio pairs each
- Thirty-two instances of SDI Audio Extract block (one per audio pair)
- Video for audio embedding provided by a Video Pattern Generator
- Received SDI video signal used for audio extraction only, no loopback
- Configuration and Status registers accessible through JTAG Master
- LED status and reset push button

The Reference Design comprises 2 main components:

1. Intel® Arria® 10 SoC Development Kit
 - The Development Kit Card hosts an Arria 10 SX SoC, two FMC connectors, power supplies, USB Blaster II, push buttons and LEDs.
2. Terasic* 12G SDI-FMC Daughter Card
 - The Terasic 12G SDI-FMC Daughter Card has multiple 12G SDI BNC connectors as well AES3id BNC connectors. This daughter card must be connected to the Arria 10 SX SoC Development Kit Card FMC-A connector.

Chapter 1: Requirements and Setup

This chapter provides details for the requirements and setup of the Reference Design.

1.1 Requirements

The reference design requires the following hardware and software to run the test:

- Intel Quartus® Prime Pro Edition version 20.1 software
- Intel Arria 10 SoC Development Kit
- 12G-SDI lab equipment with audio generation and decoding capabilities. This guide uses the Omnitek* Ultra 4K
- Terasic 12G SDI-FMC Daughter Card
- AES3 lab equipment. This guide uses the Tektronix* WFM-8300 with audio monitoring option
- 2 cables with a BNC connector in one end, and a 12G-SDI lab equipment compatible connector in the other end
- 2 cables with a BNC connector in one end, and an AES3 lab equipment compatible connector in the other end
- USB Type A to Micro USB cable for programming and debugging the FPGA

Related Information

[Quartus Software Download Page](#)

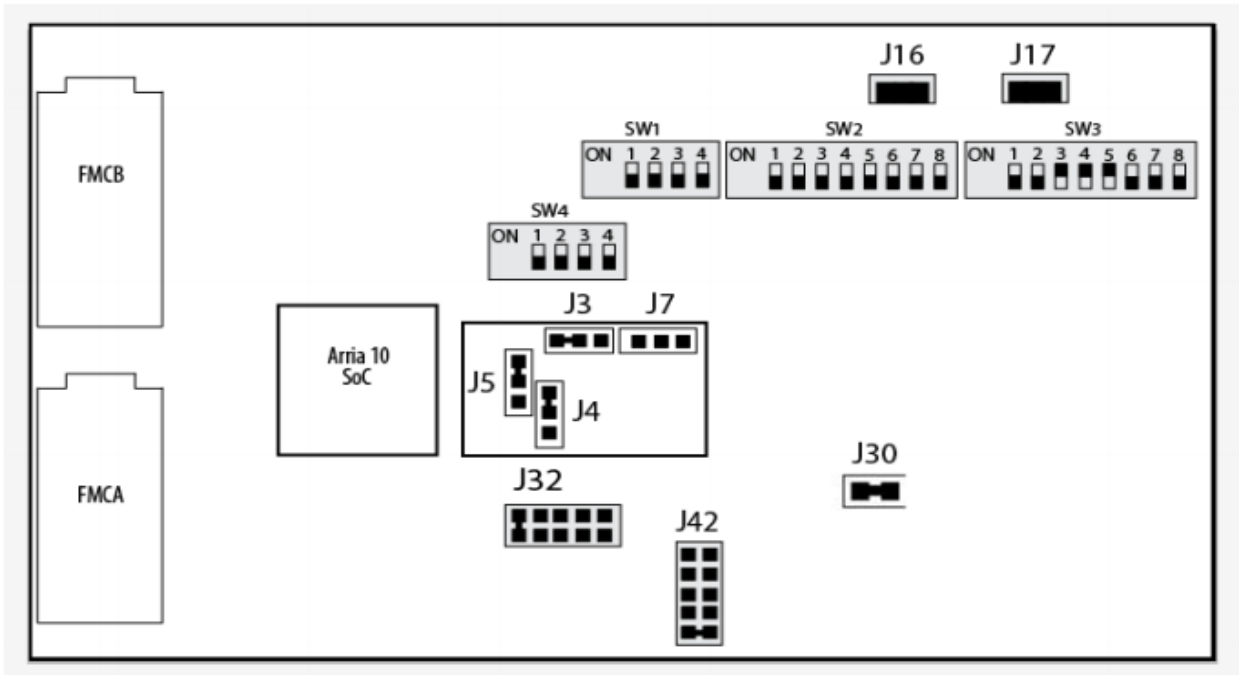
[Development Kits Page](#)

1.2 Reference Design Setup

This section describes the steps to setup the hardware to run the reference design. Figure 2-1 shows the Reference Design Block Diagram.

1. Configure Development Kit Board jumpers in factory default position, as illustrated in Figure 1-1.

Figure 1-1. Default switch and resistors settings on the Development Kit.



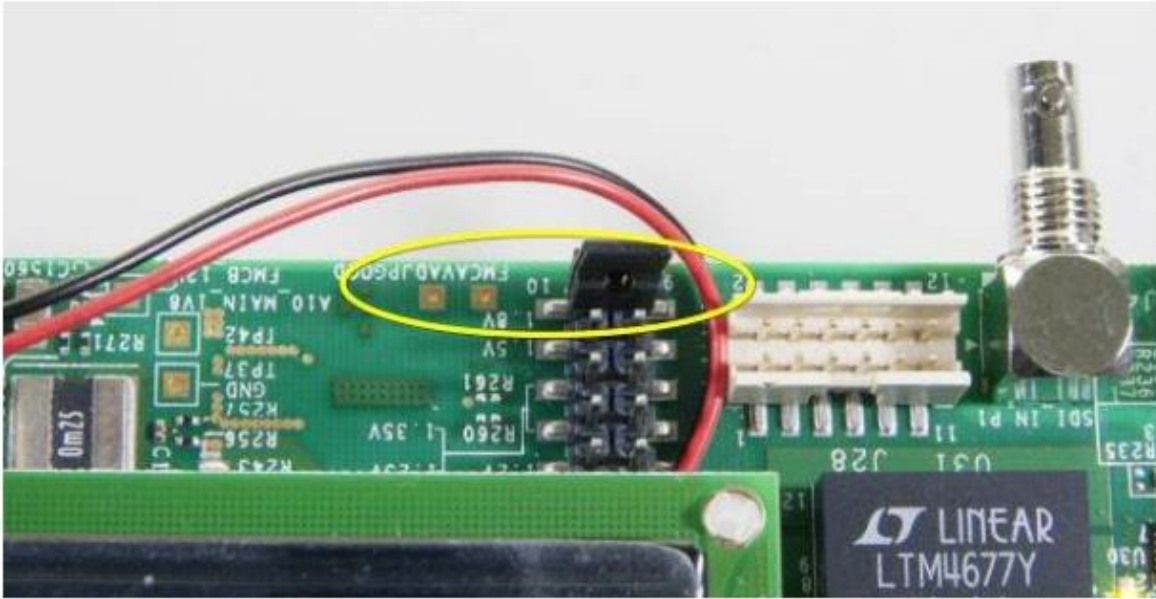
2. Insert the Terasic SDI-FMC Daughter Card into the Development Kit Board FMC-A connector (J29), as illustrated in Figure 1-2.

Figure 1-2. Inserting Terasic SDI-FMC Daughter Card into Development Kit Board FMC-A connector (J29).



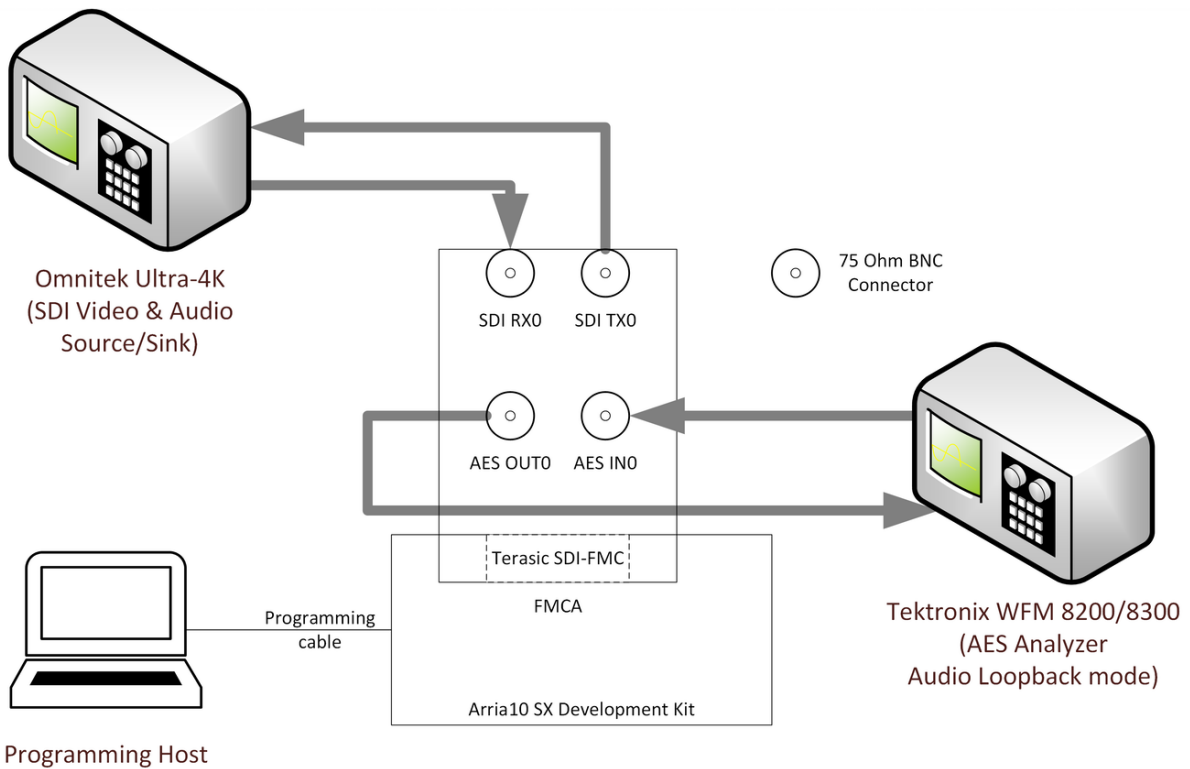
3. Make sure the FMC_A VADJ is set to 1.8V by shorting J42.9 and J42.10, as illustrated in Figure 1-3.

Figure 1-3. Short J42.9 and J42.10



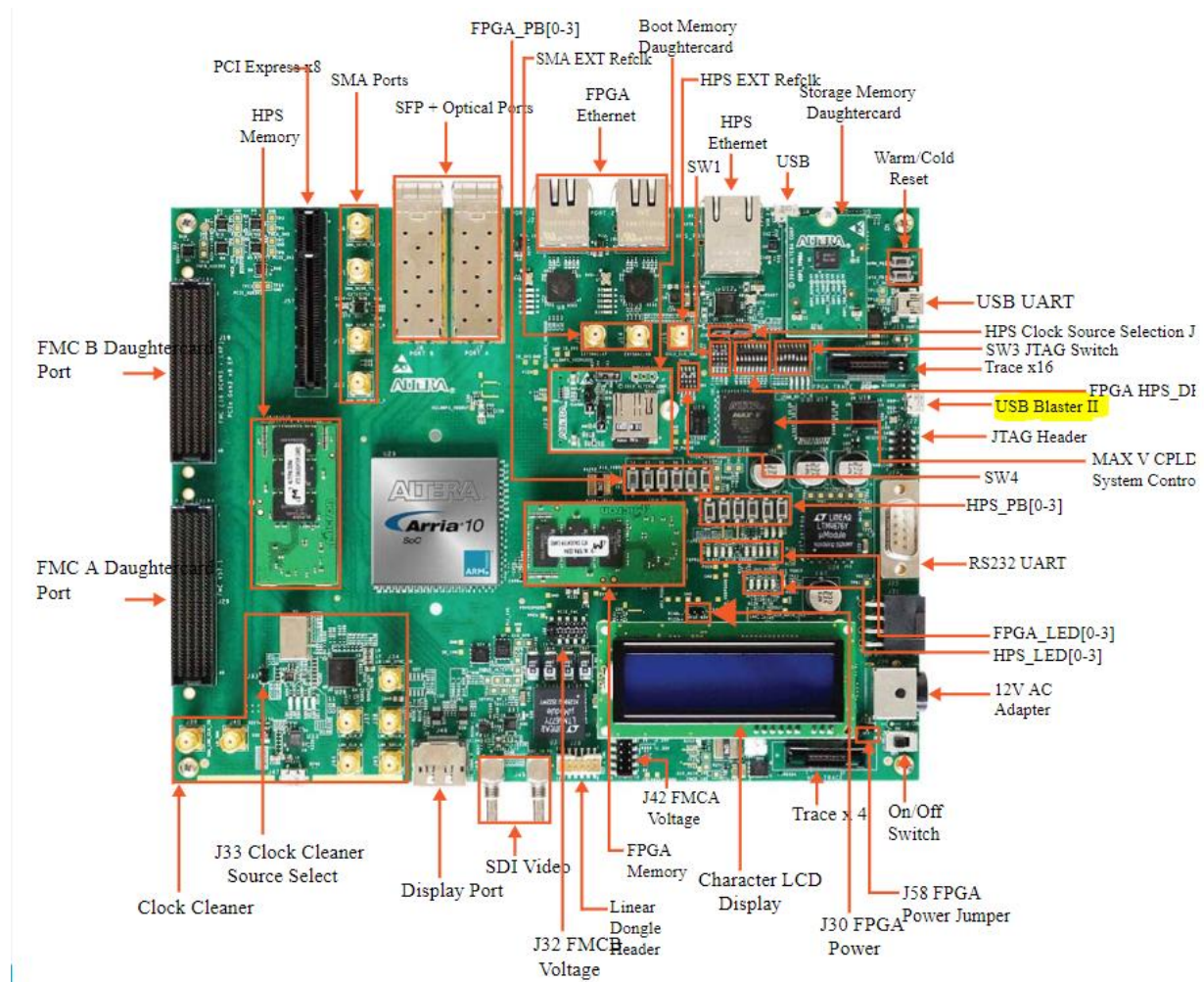
4. Connect two BNC cables between the Terasic SDI-FMC Daughter Card and Omnitek Ultra-4K lab equipment input and output interface, as illustrated in Figure 1-4.
5. Connect the other two BNC cables between the Terasic SDI-FMC Daughter Card and the Tektronix WFM 8200/8300 lab equipment, as illustrated in Figure 1-4.
6. Connect the USB cable between computer and the Development Kit Board USB-Blaster II MICRO_USB connector, as illustrated in Figure 1-4.

Figure 1-4. Hardware Setup.



7. Power on the Arria 10 SX SoC Development Kit.
8. Make sure Quartus Prime 20.1 has been installed in the host computer.
9. Connect the USB cable between computer and the Development Kit Board USB-Blaster II MICRO_USB connector(J22), as illustrated in Figure 1-5.

Figure 1-5. Connecting USB cable to Development Kit Board USB-Blaster II MICRO_USB connector (J22).



10. Connect the power supply cable to the Development Kit Board DC_INPUT connector(J36), and power on the Development Kit Board through the Power ON switch(SW5), as illustrated in Figure 1-6

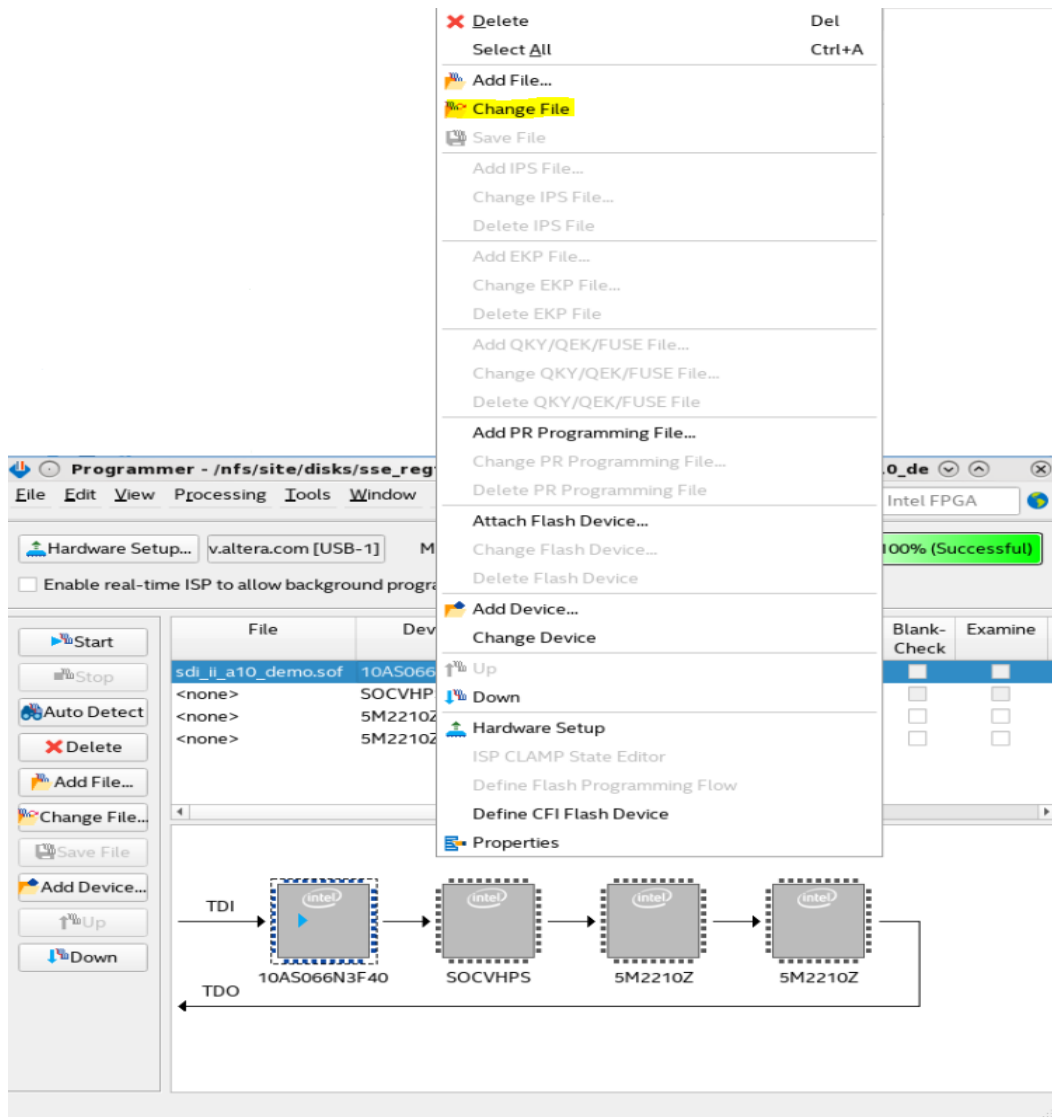
Figure 1-6. Connecting power supply to Development Kit Board DC_INPUT connector (J36) and powering on through the Power ON switch (SW5).



1.3 How to Reconstruct and Run the Reference Design

1. Download the reference design at <https://fpgacloud.intel.com/devstore/platform/20.1.0/Pro/12g-sdi-audio-reference-design/>
2. Follow the instruction in the Design Store to prepare the design template and load the design into Intel Quartus Prime Pro Edition version 20.1 software
3. Perform full compilation with the design
4. Run the Quartus Prime 20.1 Programmer on computer, select the correspondent USB Blaster interface, and click on *Auto Detect* button. Make sure the Arria 10 SoC is correctly identified, as illustrated in Figure 1-7

Figure 1-7. Devices detected in the Development Kit Board JTAG chain.



NOTE: If you find problems in identifying the right chain, it is recommended to configure JTAG clock frequency to 16 MHz by issuing “jtagconfig --setparam 1 JtagClock 16M” on the computer OS command prompt. (See Quartus documentation for more details.)

5. Set the image file to Arria 10, and program the device
6. Open Quartus Prime 20.1, then run System Console by clicking on “Tools > System Debugging Tools > System Console”
7. Change to the folder that contains the Reference Design TCL scripts.

```
% cd {C:\a10sx_sdi_audio_12g\quartus\lab_scripts}
```

8. Load the *syscon_top.tcl* file. This file loads all the needed TCL files, defines some general procedures, prints basic instructions, and finally lists all JTAG Master devices available.

```
% source syscon_top.tcl
=====
12G-SDI Audio Embedder & Extractor Reference Design

This design provides audio embedding and extraction of from a 12G-SDI signal.

Each audio pair is looped back from Extractor to Embedder. One Extractor audio
pair can be forwarded to an AES3 Tx output interface. An Embedder audio pair can
be selected to receive audio data from an AES3 Rx input interface.

Selection of Extractor and Embedder audio pairs are independent from each other.

* Available commands:

register_test - provide a basic register read/write test on some registers
config_design - basic configuration (embedder, extractor, enable VPG)
config_audio - enable/disable set of audio pairs
enable_aes_rx - select Embedder SDI/Pair to receive AES3 Rx
enable_aes_tx - select Extractor SDI/Pair to be forwarded to AES3 Tx
-----

JTAG master selection:

[0] /devices/10AT115S1@1#USB-1/(link)/JTAG/(110:132 v1 #0)/phy_0/master
[1] /devices/5M(1270ZF324|2210Z)|EPM2210@2#USB-1/(link)/JTAG/(110:130 v3 #0)/jtagmem_0

Find the index of the right JTAG device (0-n), and type

    set_jtag_master <index>

%
```

9. Open JTAG Master for the Arria 10 device

```
% set_jtag_master 0
```

10. Run the procedure "*config_design*". This procedure configures all the audio pairs on the SDI Audio Extractor and SDI Audio Embedder, sets the SDI TX video standard, and enable the Video Pattern Generator (VPG)

```
% config_design
-----
Initialize Embedders:
-----
...
-----
Initialize Extractors:
-----
...
-----
Set Video Standard
-----
...
-----
Enable VPG
-----
...
-----
Chip Id:
-----
Chip name:      io_embed_extract
Version:        0-3-0-5
Scratch value:  0x00000000
Build number:   34
Time:           01/27/2017,16:05:23
Seed:           1
Hash:           0x09a38405

%
```

11. Enable the SDI Audio Embedder SDI 0 Audio Pair 0 by issuing the following command.

```
% embed_config_pair 0 0 1
```

12. The expected result is the 12G-SDI lab equipment will detect a video signal with audio coming from the SDI TX

Chapter 2: Functional Description

This chapter describes the functional blocks of the Reference Design.

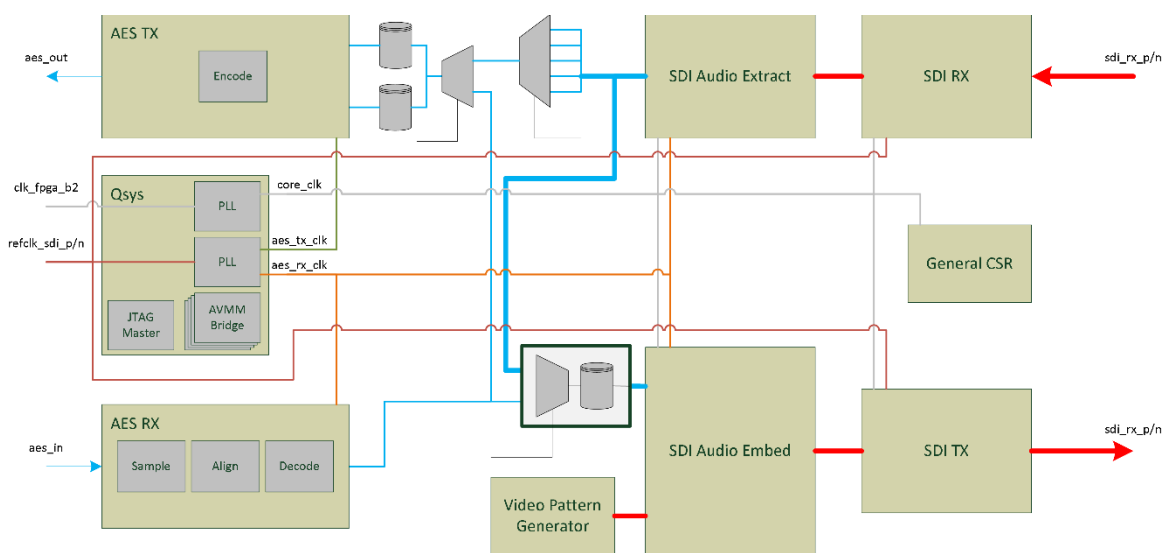
2.1 Overview

SDI Audio Reference Design demonstrates the audio extract from SDI stream and audio embed into another SDI stream. The reference design is built on top of Arria 10 12G SDI II design example. The SDI generator generates SDI stream with embedded audio to the SDI audio reference design. The design extracts the audio from the SDI stream. The audio is then embedded into another SDI stream from the test pattern generator.

2.2 Block Diagram

Figure 2-1 shows the block level overview of the FPGA design.

Figure 2-1: 12G-SDI Audio Reference Design Block Diagram



Related Information

[SDI II Intel Arria 10 FPGA IP Design Example User Guide](#)

2.3 Key Modules

The following section describes the key modules in the reference design.

2.3.1 SDI II Intel FPGA IP

The SDI II Intel FPGA IP core is configured in 12G SDI module running at 11.88-Gbps or 11.868-Gbps 12G-SDI, as defined by SMPTE ST 2082

Related Information

[SDI II Intel FPGA IP User Guide](#)

2.3.2 SDI Audio Embed/Extract IP cores

These IPs perform the audio extraction from SDI stream and audio embedding into SDI stream. The SDI Audio Embedder consists of 4 instances of the SDI Audio Embed IP core, and a Paged Register System that provides access to all Avalon MM register interface within the same address space. The SDI Audio Extractor consists of 32 instances of the SDI Audio Extract IP core, and a Paged Register System that provides access to all Avalon MM register interface within the same address space.

Related Information

[SDI Audio Intel FPGA IP User Guide](#)

2.3.3 Video Pattern Generator

The Video Pattern Generator (VPG) generates a color bar or pathological pattern. The color bar is preferable for image generation while the pathological pattern can stress the PLL and cable equalizer of the attached video equipment. You can configure the VPG to generate various video formats.

2.3.3 AES Processing Blocks

The AES3 Transmitter and Receiver blocks converts the original parallel interface into the AES Format parallel interface compatible with SDI Audio IP cores

2.3.4 Qsys

The Qsys subsystem contains the PLLs which provided clocking to the modules in the reference design. The JTAG master in the Qsys subsystem provides access to the reference design register space through System Console.

3.3.5 General Config/Status Registers

The General Configuration and Status Registers (CSR) block provides the control and status of the modules in the reference design including SDI II IP, Audio embed/extract blocks and AES blocks.

Chapter 3: Register Descriptions

3.1 Register map

Refer to the table in the following pages.

Names	Default Value	Address
chip_id_0		0x00040 - 0x0007F
chip_name	0x00000000	0x00040 - 0x0004C
version		0x00060 - 0x00067
nano_pico_version	0x00000000	0x00060
major_minor_version	0x00000000	0x00064
scratch	0x00000000	0x00068
build_info		0x00070 - 0x0007F
build_number	0x00000000	0x00070
date_time	0x00000000	0x00074
seed	0x00000000	0x00078
hash	0x00000000	0x0007C
general_csr_mm		0x00800 - 0x0087F
vid_ctrl	0x0000000E	0x00800
embed_aes_rx_sel	0x00000000	0x00804
extract_aes_tx_sel	0x00000000	0x00808
mux_sel	0x00000000	0x0080C
sw_reset	0x00000000	0x00810
sdi_rx_status	0x00000000	0x00820
aes_fifo_interrupts		0x00850 - 0x0085B
pending_intr	0x00000000	0x00850
enable_intr	0x00000000	0x00854
status_intr	0x00000000	0x00858
pll_interrupts		0x00860 - 0x0086B
pending_intr	0x00000000	0x00860
enable_intr	0x00000000	0x00864
status_intr	0x00000000	0x00868
sdi_interrupt_status		0x00870 - 0x0087B
sdi_interrupts		0x00870 - 0x0087B
pending_intr	0x00000000	0x00870
enable_intr	0x00000000	0x00874
status_intr	0x00000000	0x00878
paged_audio_extract_mm		0x10000 - 0x100FF
audio_control	0x00000080	0x10000
audio_presence	0x00000000	0x10004
audio_status	0x00000000	0x10008
sd_edp_presence	0x00000000	0x1000C
error_status	0x00000000	0x10010
fifo_status	0x00000000	0x10018
clock_status	0x00000000	0x1001C
ch_status_ram_start	0x00000000	0x10040
ch_status_ram_end	0x00000000	0x100FC
audio_extract_page_sel_reg	0x00000000	0x10200
paged_audio_embed_mm		0x20000 - 0x200FF
control	0x00000000	0x20000
ext_ctrl	0x00000040	0x20004
video_status	0x00000000	0x20008

sd_edp_ctrl	0x00000000	0x2000C
ch_stat_ctrla	0x00000000	0x20010
ch_stat_ctrlb	0x00000000	0x20014
strip_ctrl	0x00000000	0x20018
strip_stat	0x00000000	0x2001C
sine_freq1	0x00000004	0x20020
sine_freq2	0x00000005	0x20024
sine_freq3	0x00000006	0x20028
sine_freq4	0x00000007	0x2002C
audio_status	0x00000000	0x20030
csram_start	0x00000000	0x20040
csram_end	0x00000000	0x200FC
audio_embed_page_sel_reg	0x00000000	0x20200
pattgen_controls	0x00000000	0x30000

chip_id_0

Name	Address
chip_name_group	0x00040
version	0x00060
scratch	0x00068
build_info	0x00070

chip_name

Register	0	1	2	3	Description
Address	0x00040	0x00044	0x00048	0x0004C	Chip Name as a ASCII/UTF-8 String

Bits	Field name	sw	hw	default	Description
31:0	chip_name_field	ro	wo	0x0	Up to 16-byte UTF-8 NULL terminated string

Version

Name	Address
nano_pico_version	0x00060
major_minor_version	0x00064

nano_pico_version

0x00060

Bits	Field name	sw	hw	default	Description
15:0	pico	ro	wo	0x0	Versions are encoded as Major_Minor_Nano[_Pico], where pico is optional
31:16	nano	ro	wo	0x0	Versions are encoded as Major_Minor_Nano[_Pico], where pico is optional

major_minor_version

0x00064

Bits	Field name	sw	hw	default	Description
15:0	minor	ro	wo	0x0	Versions are encoded as Major_Minor_Nano[_Pico], where pico is optional
31:16	major	ro	wo	0x0	Versions are encoded as Major_Minor_Nano[_Pico], where pico is optional

scratch

0x00068

Bits	Field name	sw	hw	default	Description
31:0	value	rw	na	0x0	Read and Write scratch register

build_info

Name	Address
build_number	0x00070
date_time	0x00074
seed	0x00078
hash	0x0007C

build_number

0x00070

Bits	Field name	sw	hw	default	Description
31:0	build_number	ro	wo	0x0	A unique sequential, restarts every time source revision changes

date_time

0x00074

Bits	Field name	sw	hw	default	Description
31:0	date_time	ro	wo	0x0	Date/Time is encoded as follow: 32-bit seconds counts since epoch [Jan 1, 1970 00:00:00]

seed

0x00078

Bits	Field name	sw	hw	default	Description
31:0	seed	ro	wo	0x0	Seed used for Qsys

hash

0x0007C

Bits	Field name	sw	hw	default	Description
31:0	hash	ro	wo	0x0	Hash

general_csr_mm

Name	Address
vid_ctrl	0x00800
embed_aes_rx_sel	0x00804
extract_aes_tx_sel	0x00808
mux_sel	0x0080C
sw_reset	0x00810
sdi_rx_status	0x00820
aes_interrupt_status	0x00850
pll_interrupt_status	0x00860
sdi_interrupt_status	0x00870

vid_ctrl

0x00800

Bits	Field name	sw	hw	default	Description
3:1	vid_std	rw	ro	0x7	Transmitter video standard. [000] 10-bit SD-SDI [001] 20-bit HD-SDI [010] 3G-SDI Level B [011] 3G-SDI Level A [100] 6G-SDI 8 streams interleaved [101] 6G-SDI 4 streams interleaved [110] 12G-SDI 16 streams interleaved [111] 12G-SDI 8 streams interleaved
0:0	vid_std_rate	rw	ro	0x0	Video frame rate. [0] 1 [1] 1/1.001

embed_aes_rx_sel

0x00804

Bits	Field name	sw	hw	default	Description
4:3	sdi_sel	rw	ro	0x0	Select SDI interface of the Embed audio pair to get AES Rx data.
2:0	audp_sel	rw	ro	0x0	Select Embed audio pair to get AES Rx data.

extract_aes_tx_sel

0x00808

Bits	Field name	sw	hw	default	Description
4:3	sdi_sel	rw	ro	0x0	Select SDI interface of the Extract audio pair to be forwarded to AES Tx interface.
2:0	audp_sel	rw	ro	0x0	Select Extract audio pair to be forwarded to AES Tx interface.

mux_sel

0x0080C

Bits	Field name	sw	hw	default	Description
3:3	ser_loopback_mode	rw	ro	0x0	Enable AES RX-to-TX serial loopback. [0] disable [1] enable
2:2	par_loopback_mode	rw	ro	0x0	Enable AES RX-to-TX parallel loopback. [0] disable [1] enable
1:1	aes_loopback_mode	rw	ro	0x0	Enable AES RX-to-TX AES format loopback. [0] disable [1] enable
0:0	sdi_tx_sel	rw	ro	0x0	Select source of SDI TX. [0] from Embedder [1] from VPG

sw_reset

0x00810

Bits	Field name	sw	hw	default	Description
3:3	sdi_rx_reset	rw	ro	0x0	Reset SDI RX block.
2:2	sdi_tx_reset	rw	ro	0x0	Reset SDI TX block.
1:1	aes_rx_reset	rw	ro	0x0	Reset AES3 RX block.
0:0	aes_tx_reset	rw	ro	0x0	Reset AES3 TX block.

sdi_rx_status

0x00820

Bits	Field name	sw	hw	default	Description
2:0	sdi_rx_std	ro	wo	0x0	Received video standard. [000] 10-bit SD-SDI [001] 20-bit HD-SDI [010] 3G-SDI Level B [011] 3G-SDI Level A [100] 6G-SDI 8 streams interleaved [101] 6G-SDI 4 streams interleaved [110] 12G-SDI 16 streams interleaved [111] 12G-SDI 8 streams interleaved

aes_fifo_interrupts

Name	Address
pending_intr	0x00850
enable_intr	0x00854
status_intr	0x00858

pending_intr

0x00850

Bits	Field name	sw	hw	default	Description
0:0	aes_tx_fifo_full_pending	r/w1c	wo	0x0	AES Tx FIFO overflow
1:1	aes_tx_fifo_empty_pending	r/w1c	wo	0x0	AES Tx FIFO underflow
2:2	aes_rx_fifo_full_pending	r/w1c	wo	0x0	AES Rx FIFO overflow
3:3	aes_rx_ready_pending	r/w1c	wo	0x0	AES Rx Ready

enable_intr

0x00854

Bits	Field name	sw	hw	default	Description
0:0	aes_tx_fifo_full_enable	rw	na	0x0	AES Tx FIFO overflow
1:1	aes_tx_fifo_empty_enable	rw	na	0x0	AES Tx FIFO underflow
2:2	aes_rx_fifo_full_enable	rw	na	0x0	AES Rx FIFO overflow
3:3	aes_rx_ready_enable	rw	na	0x0	AES Rx Ready

status_intr

0x00858

Bits	Field name	sw	hw	default	Description
0:0	aes_tx_fifo_full_status	ro	wo	0x0	AES Tx FIFO overflow
1:1	aes_tx_fifo_empty_status	ro	wo	0x0	AES Tx FIFO underflow
2:2	aes_rx_fifo_full_status	ro	wo	0x0	AES Rx FIFO overflow
3:3	aes_rx_ready_status	ro	wo	0x0	AES Rx Ready

pll_interrupts

Name	Address
pending_intr	0x00860
enable_intr	0x00864
status_intr	0x00868

pending_intr

0x00860

Bits	Field name	sw	hw	default	Description
0:0	core_pll_locked_pending	r/w1c	wo	0x0	Set to 1 when Core PLL is locked.
1:1	audio_pll_locked_pending	r/w1c	wo	0x0	Set to 1 when Audio PLL is locked.
2:2	sdi_tx_pll_locked_pending	r/w1c	wo	0x0	Set to 1 when SDI TX PLL is locked.

enable_intr

0x00864

Bits	Field name	sw	hw	default	Description
0:0	core_pll_locked_enable	rw	na	0x0	Set to 1 when Core PLL is locked.
1:1	audio_pll_locked_enable	rw	na	0x0	Set to 1 when Audio PLL is locked.
2:2	sdi_tx_pll_locked_enable	rw	na	0x0	Set to 1 when SDI TX PLL is locked.

status_intr

0x00868

Bits	Field name	sw	hw	default	Description
0:0	core_pll_locked_status	ro	wo	0x0	Set to 1 when Core PLL is locked.
1:1	audio_pll_locked_status	ro	wo	0x0	Set to 1 when Audio PLL is locked.
2:2	sdi_tx_pll_locked_status	ro	wo	0x0	Set to 1 when SDI TX PLL is locked.

sdi_interrupts

Name	Address
pending_intr	0x00870
enable_intr	0x00874
status_intr	0x00878

pending_intr

0x00870

Bits	Field name	sw	hw	default	Description
0:0	sdi_rx_crc_error_pending	r/w1c	wo	0x0	Set to 1 when SDI RX CRC error occurs.
1:1	sdi_rx_frame_locked_pending	r/w1c	wo	0x0	Set to 1 when SDI RX frame is locked.
2:2	sdi_rx_align_locked_pending	r/w1c	wo	0x0	Set to 1 when SDI RX is aligned.
3:3	sdi_rx_trs_locked_pending	r/w1c	wo	0x0	Set to 1 when SDI RX TRSs are locked.

enable_intr

0x00874

Bits	Field name	sw	hw	default	Description
0:0	sdi_rx_crc_error_enable	rw	na	0x0	Set to 1 when SDI RX CRC error occurs.
1:1	sdi_rx_frame_locked_enable	rw	na	0x0	Set to 1 when SDI RX frame is locked.
2:2	sdi_rx_align_locked_enable	rw	na	0x0	Set to 1 when SDI RX is aligned.
3:3	sdi_rx_trs_locked_enable	rw	na	0x0	Set to 1 when SDI RX TRSs are locked.

status_intr

0x00878

Bits	Field name	sw	hw	default	Description
0:0	sdi_rx_crc_error_status	ro	wo	0x0	Set to 1 when SDI RX CRC error occurs.
1:1	sdi_rx_frame_locked_status	ro	wo	0x0	Set to 1 when SDI RX frame is locked.
2:2	sdi_rx_align_locked_status	ro	wo	0x0	Set to 1 when SDI RX is aligned.
3:3	sdi_rx_trs_locked_status	ro	wo	0x0	Set to 1 when SDI RX TRSs are locked.

paged_audio_extract_mm

Name	Address
audio_control	0x10000
audio_presence	0x10004
audio_status	0x10008
sd_edp_presence	0x1000C
error_status	0x10010
fifo_status	0x10018
clock_status	0x1001C
ch_status_ram_start	0x10040
ch_status_ram_end	0x100FC

audio_control

0x10000

Bits	Field name	sw	hw	default	Description
7:7	clk_mode	rw	ro	0x1	Select 3.072-MHz/48-kHz clock generation mode. 0 - generated by recovered audio clock 1 - generated by recovered video clock.
6:6	unused6	rw	ro	0x0	Unused
5:5	mute	rw	ro	0x0	Write 1 to mute the audio output, 0 to unmute.
4:4	extract_pair_msb	rw	ro	0x0	For 3G-SDI Level A standard, this field extends the extract pair field to allow for future implementations with 32 embedded audio channels. For 3G-SDI Level B standard, this field selects the active video half of the 3G multiplex.
3:1	extract_pair	rw	ro	0x0	Defines the audio pair that the component extracts.
0:0	enable_audio_extract	rw	ro	0x0	Enables the audio extraction component and internal AES output.

audio_presence

0x10004

Bits	Field name	sw	hw	default	Description
7:4	ctrl_pkt_present	ro	wo	0x0	Reports which audio control packets are detected in the SDI stream. The following bits correspond to the number of audio groups detected: - Bit [4] = Audio group 1 - Bit [5] = Audio group 2 - Bit [6] = Audio group 3 - Bit [7] = Audio group 4
3:0	data_pkt_present	ro	wo	0x0	Reports which audio data groups are detected in the SDI stream. The following bits correspond to the number of audio groups detected: - Bit [0] = Audio group 1 - Bit [1] = Audio group 2 - Bit [2] = Audio group 3 - Bit [3] = Audio group 4

audio_status

0x10008

Bits	Field name	sw	hw	default	Description
7:7	status_valid	ro	wo	0x0	Set to 1 when the audio control packet is present in the video stream.
6:5	sample_rate	ro	wo	0x0	Reports the X1 and X0 bits of the sample rate code from the RATE (Sampling Rate) field of the audio control packet. X1,X0 = 0,0: 48.0 kHz; X1,X0 = 0,1: 44.1 kHz; X1,X0 = 1,0: 32.0 kHz; X1,X0 = 1,1: reserved / free running.
4:4	async_bit	ro	wo	0x0	Reflects the asx bit (synchronous mode bit) of the RATE (Sampling Rate) field of the audio control packet. 0 = channel pairs in a given audio group are isochronous; 1 = channel pairs in a given audio group are asynchronous.
3:0	active_ch	ro	wo	0x0	Reflects the lower four bits of the ACT field of the audio control packet. - Bit [0]: a1 bit (1 = CH1 active; 0 = CH1 inactive); - Bit [1]: a2 bit (1 = CH2 active; 0 = CH2 inactive); - Bit [2]: a3 bit (1 = CH3 active; 0 = CH3 inactive); - Bit [3]: a4 bit (1 = CH4 active; 0 = CH4 inactive).

sd_edp_presence

0x1000C

Bits	Field name	sw	hw	default	Description
3:0	edp_present	ro	wo	0x0	Reports which audio extended data groups are detected in the SD-SDI stream.

error_status

0x10010

Bits	Field name	sw	hw	default	Description
7:7	audio_pkt_ecrc_fail	r/w1c	wo	0x0	Indicates that an error has been detected in the ECRC that forms part of the HD audio data packet. This bit stays set until cleared by writing 1 to it.
6:6	ch_status_crc_fail	r/w1c	wo	0x0	Indicates that an error has been detected in the channel status CRC. This bit stays set until cleared by writing 1 to it.
5:5	anc_parity_fail	r/w1c	wo	0x0	Indicates that an error has been detected in at least one of the parity fields: ancillary packet parity bit, audio sample parity bit (SD-SDI), AES sample parity bit (HD-SDI). This bit stays set until cleared by writing 1 to it.
4:4	anc_cs_fail	r/w1c	wo	0x0	Indicates that an error has been detected in the ancillary packet checksum. This bit stays set until cleared by writing 1 to it.
3:0	error_counter	r/w1c	wo	0x0	Counts up to 15 errors since last reset. Write 1 to any bit of this field to reset counter to 0.

fifo_status

0x10018

Bits	Field name	sw	hw	default	Description
7:7	overflow_underflow	r/w1c	wo	0x0	This register bit goes high if one of the following occurs (based on the output mode used): - underflow or overflow of the audio output FIFO; - overflow of the Avalon-ST audio FIFO. This bit stays set until cleared by writing 1 to it. This register always goes high at the beginning, so you must clear the audio FIFO first for the register to indicate underflow or overflow.
6:0	fifo_fill_level	r/w1c	wo	0x0	Reports the amount of data in either the audio output FIFO or the Avalon-ST audio FIFO when the optional Avalon-ST Audio interface is used.

clock_status

0x1001C

Bits	Field name	sw	hw	default	Description
7:7	video_clk_rate	ro	wo	0x0	74.17 MHz video clock indication. 0 = 1/1 video clock rate detected. 1 = 1/1.001 video clock rate detected.
4:0	offset	ro	wo	0x0	Defines the frequency of the generated audio.

ch_status_ram_start

0x10040

Bits	Field name	sw	hw	default	Description
7:0	data	ro	wo	0x0	Read accesses to the Channel Status RAM. Fields ch_status_ram_start to ch_status_ram_end return the 24 bytes of Channel Status for the first channel, followed by the 24 bytes of Channel Status for the second channel.

ch_status_ram_end

0x100FC

Bits	Field name	sw	hw	default	Description
7:0	data	ro	wo	0x0	Read accesses to the Channel Status RAM. Fields ch_status_ram_start to ch_status_ram_end return the 24 bytes of Channel Status for the first channel, followed by the 24 bytes of Channel Status for the second channel.

audio_extract_page_sel_reg

0x10200

Bits	Field name	sw	hw	default	Description
31:16	channel_sel	rw	ro	0x0	Sets the channel portion of the register area page
15:0	port_sel	rw	ro	0x0	Sets the port portion of the register area page

paged_audio_embed_mm

Name	Address
control	0x20000
ext_ctrl	0x20004
video_status	0x20008
sd_edp_ctrl	0x2000C
ch_stat_ctrla	0x20010
ch_stat_ctrlb	0x20014
strip_ctrl	0x20018
strip_stat	0x2001C
sine_freq1	0x20020
sine_freq2	0x20024
sine_freq3	0x20028
sine_freq4	0x2002C
audio_status	0x20030
csram_start	0x20040
csram_end	0x200FC

control

0x20000

Bits	Field name	sw	hw	default	Description
7:0	ag_enable	rw	ro	0x0	<p>Enables the embedding of each audio group. When working with HD-SDI or 3G-SDI video, this register also enables the embedding of the audio control packets when one or more audio groups are enabled.</p> <p>The following bits correspond to the number of audio groups you specify:</p> <ul style="list-style-type: none"> - Bit [1:0] = Audio group 1 - Bit [3:2] = Audio group 2 - Bit [5:4] = Audio group 3 - Bit [7:6] = Audio group 4

Bits	Field name	sw	hw	default	Description
2:0	ch_ram_sel	rw	ro	0x0	Channel Status RAM Select. When Channel Status RAM parameter is 2, this field selects the channel pair for the RAM written to by registers csram_start to csram_end. * If Channel Status RAM parameter is 0 or 1, this value is ignored.
4:4	sine_en	rw	ro	0x0	Test sine generator enable. When set to 1, this bit ignores the audio inputs and uses the output of the sine generator as the data for each audio group.
6:5	lnk_ab	rw	ro	0x2	Link AB Control. * This register applies only for 3G-SDI Level B standard. Controls which link the ancillary data is embedded in. 00b = No data is embedded. 01b = Data is embedded only in Link B. 10b = Data is embedded only in Link A (default value). 11b = Data is embedded in Link A and Link B at the same time.

video_status

0x20008

Bits	Field name	sw	hw	default	Description
7:0	val	ro	wo	0x0	<p>Reports the detected video input standard.</p> <p>Bits[7:5] = Picture structure code. Defined values for picture structure code are:</p> <ul style="list-style-type: none"> - 001b = 486 or 576 line SD-SDI - 100b = 720 line HD-SDI - 101b = 1080 line HD-SDI - 010b = 1080 line 3G-SDI - 011b = 1080 line 3GA-SDI - 110b = 720 line 3GA-SDI - 111b = 720 line 3GB-SDI <p>Bit[4] = 0b: Interlace or segmented frame, 1b: Progressive.</p> <p>Bits[3:0] = Frame rate code. Defined values for frame rate code (in Hz) are:</p> <ul style="list-style-type: none"> - 0010b = 23.97 - 0011b = 24 - 0101b = 25 - 0110b = 29.97 - 0111b = 30 - 1001b = 50 - 1010b = 59.94 - 1011b = 60

sd_edp_ctrl

0x2000C

Bits	Field name	sw	hw	default	Description
3:0	en_sd_edp	rw	ro	0x0	Enables the embedding of SD-SDI Extended Data Packets (EDP) for each audio group.
7:4	en_sd_acp	rw	ro	0x0	Enables the embedding of SD-SDI Audio Control Packets (ACP) for each audio group.

ch_stat_ctrla

0x20010

Bits	Field name	sw	hw	default	Description
7:0	val	rw	ro	0x0	<p>Channel Status Control Registers (3:0).</p> <p>When set to 00b, the core keeps the existing channel status data.</p> <p>When set to 01b, the core replaces the channel status data with these default values:</p> <ul style="list-style-type: none"> - Channel status byte 0: 0x8 - Channel status byte 1: 0x02 - Channel status byte 2–22: 0x00 - Channel status byte 23: 0xDD <p>When set to 10b, the core replaces the data with the contents of the appropriate channel status RAM.</p> <p>The following bits correspond to the number of audio groups you specify:</p> <ul style="list-style-type: none"> - Bit [1:0] = Audio group 1 - Bit [3:2] = Audio group 2 - Bit [5:4] = Audio group 3 - Bit [7:6] = Audio group 4

ch_stat_ctrlb

0x20014

Bits	Field name	sw	hw	default	Description
7:0	val	rw	ro	0x0	<p>Channel Status Control Registers (7:4).</p> <p>When set to 00b, the core keeps the existing channel status data.</p> <p>When set to 01b, the core replaces the channel status data with these default values:</p> <ul style="list-style-type: none"> - Channel status byte 0: 0x8 - Channel status byte 1: 0x02 - Channel status byte 2–22: 0x00 - Channel status byte 23: 0xDD <p>When set to 10b, the core replaces the data with the contents of the appropriate channel status RAM.</p> <p>The following bits correspond to the number of audio groups you specify:</p> <ul style="list-style-type: none"> - Bit [1:0] = Audio group 1 - Bit [3:2] = Audio group 2 - Bit [5:4] = Audio group 3 - Bit [7:6] = Audio group 4

strip_ctrl

0x20018

Bits	Field name	sw	hw	default	Description
3:0	val	rw	ro	0x0	Enables the removal of both ACP and ADP (and any SD-SDI EDP) for each of the four audio groups.

strip_stat

0x2001C

Bits	Field name	sw	hw	default	Description
3:0	data_pkt_pres	ro	wo	0x0	Reports which audio data groups are detected in the SDI stream.
7:4	ctrl_pkt_pres	ro	wo	0x0	Reports which audio control groups are detected in the SDI stream.

sine_freq1

0x20020

Bits	Field name	sw	hw	default	Description
7:0	val	wo	ro	0x4	Defines the frequency of the generated audio for CH1 of all audio groups.

sine_freq2

0x20024

Bits	Field name	sw	hw	default	Description
7:0	val	wo	ro	0x5	Defines the frequency of the generated audio for CH2 of all audio groups.

sine_freq3

0x20028

Bits	Field name	sw	hw	default	Description
7:0	val	wo	ro	0x6	Defines the frequency of the generated audio for CH3 of all audio groups.

sine_freq4

0x2002C

Bits	Field name	sw	hw	default	Description
7:0	val	wo	ro	0x7	Defines the frequency of the generated audio for CH4 of all audio groups.

audio_status

0x20030

Bits	Field name	sw	hw	default	Description
3:0	ag_present	ro	wo	0x0	Reports which audio groups are detected in the SDI stream.
4:4	val	ro	wo	0x0	Reports whether the video frame with the embedded audio is locked.

csram_start

0x20040

Bits	Field name	sw	hw	default	Description
7:0	data	wo	ro	0x0	Write accesses to the Channel Status RAM. Fields csram_start to csram_end represent the 24 bytes of Channel Status for the first channel, followed by the 24 bytes of Channel Status for the second channel.

csram_end

0x200FC

Bits	Field name	sw	hw	default	Description
7:0	data	wo	ro	0x0	Write accesses to the Channel Status RAM. Fields csram_start to csram_end represent the 24 bytes of Channel Status for the first channel, followed by the 24 bytes of Channel Status for the second channel.

audio_embed_page_sel_reg

0x20200

Bits	Field name	sw	hw	default	Description
15:0	port_sel	rw	ro	0x0	Sets the port portion of the register area page

Bits	Field name	sw	hw	default	Description
0:0	bar_100_75n	rw	ro	0x0	Set to '1' for 100% color bars, '0' for 75%.
1:1	patho	rw	ro	0x0	Set to '1' to generate the pathological test pattern.
2:2	count_mode	rw	ro	0x0	Set to '1' to output a simple count.
3:3	count_error	rw	ro	0x0	Singlepulse to inject an error into the counter data.
4:4	blank	rw	ro	0x0	Set to '1' to generate a black screen pattern.
5:5	no_color	rw	ro	0x0	Set to '1' to generate greyscale bars.
6:6	sgmt_frame	rw	ro	0x0	Set to '1' to generate segmented frame picture for tx_format: 0001: 1080sF30 and 0101: 1080sF25 (SMPTE274M).
7:7	enable_gen	rw	ro	0x0	Set to '1' to enable the generation of a test pattern.
8:8	dl_mapping	rw	ro	0x0	Set to '1' for HD dual link and 3GB only.
9:9	ntsc_paln	rw	ro	0x0	Set to '0' for PAL (eg 1080p30), set to '1' for NTSC (eg 1080p29.97).
10:10	sd_20_bits	rw	ro	0x0	Set to '0' for an SD bit width of 10, '1' for SD at 20 bits.
12:11	tx_std	rw	ro	0x0	Transmit video standard: '00' = SD, '01' = HD, '10' = 3GB, '11' = 3GA.
16:13	tx_format	rw	ro	0x0	Transmit video format: '0111' = 720p60, '1100' = 1080p30 or 1080p60 depending on tx_std.

Revision History

Date	Version	Changes
March 19, 2020	1.0	Initial Release