

Intel® Iris® Xe and UHD Graphics Open Source

Programmer's Reference Manual

**For the 2020-2021 11th Generation Intel Xeon®, Core™, Celeron®,
Pentium® Gold Processors based on the "Tiger Lake" Platform**

Volume 2c: Command Reference: Registers

Part 2 – Registers M through Z

December 2021, Revision 1.0



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MAILBOX0

MAILBOX0 - MAILBOX0								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	120800h							
This register contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.								
DWord	Bit	Description						
0	31:0	DATA <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This field contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.</p>	Default Value:	00000000h	Access:	R/W	_Custom_GTIRreset:	BUS
Default Value:	00000000h							
Access:	R/W							
_Custom_GTIRreset:	BUS							



MAILBOX1

MAILBOX1 - MAILBOX1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	120804h	
This register contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		_Custom_GTIReset: BUS
This field contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.		

MAILBOX2

MAILBOX2 - MAILBOX2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	120808h	
This register contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		_Custom_GTIRreset: BUS
This field contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.		



MAILBOX3

MAILBOX3 - MAILBOX3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	12080Ch	
This register contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		_Custom_GTIReset: BUS
This field contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.		

Maximum Latency

MAXLAT_0_2_0_PCI - Maximum Latency								
Register Space:	PCI: 0/2/0							
Size (in bits):	8							
Address:	0003Fh							
The Integrated Graphics Device has no requirement for the settings of Latency Timers.								
DWord	Bit	Description						
0	7:0	Maximum Latency Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.</p>	Default Value:	00000000b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	00000000b							
Access:	RO							
_Custom_GTIReset:	BUS							



MBC Control Register

MBCTL - MBC Control Register			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	0907Ch		
MBC Control Register			
DWord	Bit	Description	
0	31:18	ECORSVD	
		Access:	R/W
		_Custom_GTIReset:	BUS
		ECO purposes Reserved	
17		U2C Global PMON Enable Override	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIReset:	BUS
U2C Performance Monitor Global Enable Override 0 - U2C Global PMON needs to be enabled for performance monitors to be enabled (default) 1 - Override U2C Global PMON Enable is ignored in baled performance monitor counters			
16		VCR Fuse Writes as Posted	
		Access:	R/W
		_Custom_GTIReset:	BUS
Non-posted fuse fetching is NOT supported. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted.			
15:8		Reserved	
		Access:	RO
Format:		MBZ	
7		Disable Wait for SQempty in MAE	
		Access:	R/W
		_Custom_GTIReset:	BUS
0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.			
6		Reserved	

MBCTL - MBC Control Register			
	5:4	Reserved	
		Access: RO	
		Format: MBZ	
	3	Context Fetch Needed	
		Access: R/W	
		_Custom_GTIReset: BUS	
		Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).	
	2:0	Reserved	
		Access: RO	
		Format: MBZ	



MBUS_ABOX_CTL

MBUS_ABOX_CTL			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	45038h-4503Bh		
Name:	MBox ABox Control		
ShortName:	MBUS_ABOX_CTL		
Reset:	soft		
Address:	45048h-4504Bh		
Name:	MBox ABox 1 Control		
ShortName:	MBUS_ABOX1_CTL		
Reset:	soft		
Address:	4504Ch-4504Fh		
Name:	MBox ABox 2 Control		
ShortName:	MBUS_ABOX2_CTL		
Reset:	soft		
DWord	Bit	Description	
0	31	Status	
		Access:	RO
		This field indicates if the box is enabled.	
		Value	Name
	0b	Disabled	
	1b	Enabled	
	30:27	Ring Stop Address	
		Access:	RO
	This field indicates the address of the box in the ring.		
	26:22	B2B Transactions Max	
This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.			
Value		Name	
10		[Default]	
[1-31]			
21:20	BW Credits		
	Default Value:	1h	
BW credits are used by the Arbiter to initiate write cycles when performing VRH read-modified-writes to the display buffer.			

MBUS_ABOX_CTL							
19:16	<p>B Credits</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">1h</td> </tr> </table> <p>B credits are used by the Arbiter to initiate read cycles when performing VRH read-modified-writes to the display buffer.</p>	Default Value:	1h				
Default Value:	1h						
15:14	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
13	<p>Regulate B2B Transactions</p> <p>This field controls the regulation of back to back transactions from this ring stop.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable [Default]
Value	Name						
0b	Disable						
1b	Enable [Default]						
12:8	<p>BT Credits Pool2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">10h</td> </tr> </table> <p>BT credits are used by the Arbiter to request trackers from the Display Buffer.</p>	Default Value:	10h				
Default Value:	10h						
7:5	<p>B2B Transactions Delay</p> <p>This field indicates the number of wait cycles after the maximum back to back transactions is sent.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0-7]</td> <td></td> </tr> <tr> <td>2</td> <td>[Default]</td> </tr> </tbody> </table>	Value	Name	[0-7]		2	[Default]
Value	Name						
[0-7]							
2	[Default]						
4:0	<p>BT Credits Pool1</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">10h</td> </tr> </table> <p>BT credits are used by the Arbiter to request trackers from the Display Buffer.</p>	Default Value:	10h				
Default Value:	10h						

MBUS_BBOX_CTL

MBUS_BBOX_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	45040h-45043h							
Name:	MBus BBox 1 Control							
ShortName:	MBUS_BBOX_CTL_S1							
Reset:	soft							
Address:	45044h-45047h							
Name:	MBus BBox 2 Control							
ShortName:	MBUS_BBOX_CTL_S2							
Reset:	soft							
DWord	Bit	Description						
0	31	Status						
		Access: RO						
		This field indicates if the box is enabled.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
		Value	Name					
0b	Disabled							
1b	Enabled							
	30:27	Ring Stop Address						
		Access: RO						
		This field indicates the address of the box in the ring.						
	26:25	Reserved						
		Access: RO						
		Format: MBZ						
	24:20	B2B Transactions Max						
		This field indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>16</td> <td>[Default]</td> </tr> <tr> <td>[1-31]</td> <td></td> </tr> </tbody> </table>	Value	Name	16	[Default]	[1-31]	
Value	Name							
16	[Default]							
[1-31]								
	19:17	B2B Transactions Delay						
		This field indicates the number of wait cycles after the maximum back to back transactions is sent.						

MBUS_BBOX_CTL								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>[0-7]</td> <td></td> </tr> <tr> <td>1</td> <td>[Default]</td> </tr> </tbody> </table>	Value	Name	[0-7]		1	[Default]
Value	Name							
[0-7]								
1	[Default]							
16	Regulate B2B Transactions This field controls the regulation of back to back transactions from this ring stop.							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable [Default]
Value	Name							
0b	Disable							
1b	Enable [Default]							
15:0	Reserved							
	Access:	RO						
	Format:	MBZ						

MBUS_DBOX_CTL

MBUS_DBOX_CTL			
Register Space:	MMIO: 0/2/0		
Access:	Double Buffered		
Size (in bits):	32		
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled			
Address:	7003Ch-7003Fh		
Name:	Pipe MBus DBox Control		
ShortName:	PIPE_MBUS_DBOX_CTL_A		
Reset:	soft		
Address:	7103Ch-7103Fh		
Name:	Pipe MBus DBox Control		
ShortName:	PIPE_MBUS_DBOX_CTL_B		
Reset:	soft		
Address:	7203Ch-7203Fh		
Name:	Pipe MBus DBox Control		
ShortName:	PIPE_MBUS_DBOX_CTL_C		
Reset:	soft		
Address:	7303Ch-7303Fh		
Name:	Pipe MBus DBox Control		
ShortName:	PIPE_MBUS_DBOX_CTL_D		
Reset:	soft		
DWord	Bit	Description	
0	31	Status	
		Access: RO	
		This field indicates if the box is enabled.	
		Value	Name
		0b	Disabled
		1b	Enabled
	30:27	Ring Stop Address	
		Access: RO This field indicates the address of the box in the ring.	
	26:25	Reserved	
		Access: RO	
Format: MBZ			

MBUS_DBOX_CTL

24:20	<p>B2B Transactions Max This field indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">16</td> <td style="text-align: center;">[Default]</td> </tr> <tr> <td style="text-align: center;">[1-31]</td> <td></td> </tr> </tbody> </table>	Value	Name	16	[Default]	[1-31]	
Value	Name						
16	[Default]						
[1-31]							
19:17	<p>B2B Transactions Delay This field indicates the number of wait cycles after the maximum back to back transactions is sent.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0-7]</td> <td></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">[Default]</td> </tr> </tbody> </table>	Value	Name	[0-7]		1	[Default]
Value	Name						
[0-7]							
1	[Default]						
16	<p>Regulate B2B Transactions This field controls the regulation of back to back transactions from this ring stop.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable [Default]
Value	Name						
0b	Disable						
1b	Enable [Default]						
15:14	<p>BW Credits BW credits are used by the display pipe to write color clear data to DBUF.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">[Default]</td> </tr> </tbody> </table>	Value	Name	1h	[Default]		
Value	Name						
1h	[Default]						
13	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
12:8	<p>B Credits B credits are used by the display pipe to request data from display buffer.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">06h</td> <td style="text-align: center;">[Default]</td> </tr> </tbody> </table>	Value	Name	06h	[Default]		
Value	Name						
06h	[Default]						
7:5	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
4	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
3:0	<p>A Credits A credits are used by the display pipe to make data/TLB/VTd/MCS requests to Arbiter.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">2h</td> <td style="text-align: center;">2 credits [Default]</td> </tr> </tbody> </table>	Value	Name	2h	2 credits [Default]		
Value	Name						
2h	2 credits [Default]						

MBUS_UBOX_CTL

MBUS_UBOX_CTL			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	4503Ch-4503Fh		
Name:	Mbus UBox Control		
ShortName:	MBUS_UBOX_CTL		
Reset:	soft		
DWord	Bit	Description	
0	31	Status	
		Access:	RO
		This field indicates if the box is enabled.	
		Value	Name
		0b	Disabled
		1b	Enabled
	30:27	Ring Stop Address	
		Access:	RO
	This field indicates the address of the box in the ring.		
	26:25	Reserved	
Access:		RO	
Format:		MBZ	
24:20	B2B Transactions Max		
	This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.		
	Value	Name	
	16	[Default]	
	[1-31]		
19:17	B2B Transactions Delay		
	This field indicates the number of wait cycles after the maximum back to back transactions is sent.		
	Value	Name	
	[0-7]		
	1	[Default]	
16	Regulate B2B Transactions		
This field controls the regulation of back to back transactions from this ring stop.			

MBUS_UBOX_CTL			
		Value	Name
		0b	Disable
		1b	Enable [Default]
15:7	Reserved		
	Access:		RO
	Format:		MBZ
6:4	KVM Sprite A Credits		
	Default Value:		1
	A Credits used by KVM to make data requests to Arbiter.		
3	Reserved		
	Access:		RO
	Format:		MBZ
2:0	VGA B Credits		
	Default Value:		4
	B credits used by VGA to request data from Display Buffer.		



MCPG1 Hysteresis Time Free

OAG_MCPG1_HYSTERESIS_TIME_FREE - MCPG1 Hysteresis Time Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBB4h			
This register counts the time that MCPG hysteresis time is accumulating for media slice 1. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

MCR Packet Control

MCRPKT_CTRL - MCR Packet Control								
Register Space:		MMIO: 0/2/0						
Size (in bits):		32						
_Custom_GTIReset:		BUS						
Address:		00FDCh-00FDFh						
DWord	Bit	Description						
0	31	MULTICAST Access: R/W Value determines the multicast value driven to MCR. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Multicast [Default]</td> </tr> <tr> <td>0b</td> <td>Unicast</td> </tr> </tbody> </table>	Value	Name	1b	Multicast [Default]	0b	Unicast
		Value	Name					
1b	Multicast [Default]							
0b	Unicast							
Programming Notes								
		SLICEID and DUAL_SUBSLICEID are used in Unicast but ignored for Multicast.						
30:27		SLICEID Access: R/W Value determines the slice ID driven to MCR.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>[Default]</td> </tr> <tr> <td>[0001b,1111b]</td> <td></td> </tr> </tbody> </table>	Value	Name	0000b	[Default]	[0001b,1111b]	
		Value	Name					
0000b	[Default]							
[0001b,1111b]								
Programming Notes								
		Values must be in range of slices and subslices in the configuration.						
26:24		DUAL_SUBSLICEID Access: R/W Value determines the dual-subslice ID (or I3_bank) driven to MCR.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>[Default]</td> </tr> <tr> <td>[001b,111b]</td> <td></td> </tr> </tbody> </table>	Value	Name	000b	[Default]	[001b,111b]	
		Value	Name					
000b	[Default]							
[001b,111b]								
Programming Notes								
		Values must be in range of slices and subslices in the configuration.						

MCRPKT_CTRL - MCR Packet Control			
	23:0	Reserved	
		Access:	RO
		Format:	MBZ

MCR Packet Control 0

MCRPKT_CTRL_MCFG - MCR Packet Control 0		
Register Space: MMIO: 0/2/0		
Size (in bits): 32		
_Custom_GTIReset: BUS		
Address: 00FD0h-00FD3h		
DWord	Bit	Description
0	31	MULTICAST MCFG
		Default Value: 1b
		Access: R/W
		Value determines the multicast value driven to MCR for accesses to MCFG. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
30:27		SLICEID MCFG
		Default Value: 0000b
		Access: R/W Value driven on packet field Slice ID targeting MCFG.
26:24		DUAL_SUBSLICEID MCFG
		Default Value: 000b
		Access: R/W Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting MCFG.
23:0		Reserved
		Access: RO
		Format: MBZ



MCRPacketControl1

MCRPKT_CTRL_MDRB - MCRPacketControl1						
Register Space:		MMIO: 0/2/0				
Size (in bits):		32				
_Custom_GTIReset:		BUS				
Address:		00FD4h-00FD7h				
DWord	Bit	Description				
0	31	<p>MULTICAST MDRB</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">1b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Value determines the multicast value driven to MCR for accesses to MDRB. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.</p>	Default Value:	1b	Access:	R/W
	Default Value:	1b				
	Access:	R/W				
	30:27	<p>SLICEID MDRB</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Value driven on packet field Slice ID targeting MDRB.</p>	Default Value:	0000b	Access:	R/W
Default Value:	0000b					
Access:	R/W					
26:24	<p>DUAL_SUBSLICEID MDRB</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting MDRB.</p>	Default Value:	000b	Access:	R/W	
Default Value:	000b					
Access:	R/W					
23:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					

MCR Packet Control 2

MCRPKT_CTRL_SF - MCR Packet Control 2			
Register Space:		MMIO: 0/2/0	
Size (in bits):		32	
_Custom_GTIReset:		BUS	
Address:		00FD8h-00FDBh	
DWord	Bit	Description	
0	31	MULTICAST SF	
		Default Value:	1b
		Access:	R/W
		Value determines the multicast value driven to MCR for accesses to SF. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.	
30:27		SLICEID SF	
		Default Value:	0000b
		Access:	R/W
Value driven on packet field Slice ID targeting SF.			
26:24		DUAL_SUBSLICEID SF	
		Default Value:	000b
		Access:	R/W
Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting SF.			
23:0		Reserved	
		Access:	RO
		Format:	MBZ



MDRB Context Base 1

MDRB_CTXBASE1 - MDRB Context Base 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00DC8h	
RC6 Save Location NOTE: This register is not used since MDRB unit no longer exists. This will be removed in a future project		
DWord	Bit	Description
0	31:6	MDRB Memory Base Low
		Access: R/W Lock
		_Custom_GTIReset: BUS
This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1		
0	5:1	Reserved
		Access: RO
		Format: MBZ
This field is reserved and must be set to 0.		
0	0	Ctx Base is Enabled
		Access: R/W Lock
		_Custom_GTIReset: BUS
1'b0 : The MDRB base has not been enabled, so don't do the MDRB context save (This is default value and BIOS has to program it to enable context save) 1'b1 : The MDRB base has been enabled, so go ahead with the context save		

MDRB Context Base 2

MDRB_CTXBASE2 - MDRB Context Base 2						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	00DCCh					
RC6 Base Location NOTE: This register is not used since MDRB unit is no more there.						
DWord	Bit	Description				
0	31:0	MDRB Memory Base High <table border="1"> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1</p>	Access:	R/W Lock	_Custom_GTIRreset:	BUS
Access:	R/W Lock					
_Custom_GTIRreset:	BUS					



MED0HCP0PowerGoodDelay

MED0HCP0_PG_DLY - MED0HCP0PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay Default Value: 00C8h RAMP_DLY Value

MED0MFX0PowerGoodDelay

MED0MFX0_PG_DLY - MED0MFX0PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay Default Value: 00C8h RAMP_DLY Value



MED0PowerGoodDelay

MED0_PG_DLY - MED0PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay Default Value: 00C8h RAMP_DLY Value

MED1HCP0PowerGoodDelay

MED1HCP0_PG_DLY - MED1HCP0PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay Default Value: 00C8h RAMP_DLY Value



MED1MFX0PowerGoodDelay

MED1MFX0_PG_DLY - MED1MFX0PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay Default Value: 00C8h RAMP_DLY Value

MED1PowerGoodDelay

MED1_PG_DLY - MED1PowerGoodDelay		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	Bit	Description
0	31:16	Power Good Delay
		Default Value: 00C8h PWRGOOD_DLY Value
	15:0	RAMP Delay
		Default Value: 00C8h RAMP_DLY Value

Media Die Recovery

MED_DIE_RECOVERY - Media Die Recovery		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	12298h	
Name:	VCS Media Die Recovery	
ShortName:	VCS_MED_DIE_RECOVERY	
This register is stored in the VCS but is used in the HWM unit. This register programs the die recovery override and engine ID's.		
DWord	Bit	Description
0	31:12	Reserved
		Access: RO
		Format: MBZ
	11:9	Forced Next Engine ID
		Access: R/W This field is the next engine ID.
	8	Force Next Engine ID
		Access: R/W The bit forces the next engine ID.
7:4	Reserved	
	Access: RO	
	Format: MBZ	
3:1	Forced Previous Engine ID	
	Access: R/W This field is the previous engine ID.	
0	Force Previous Engine ID	
	Access: R/W The bit forces the previous engine ID.	

Media FIFO Messaging Register for Shadow Register Unit

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	080E4h		
Name:	Media FIFO Messaging Register for Shadow Register Unit		
ShortName:	MSG_FIFO_MGSR_MEDIA		
<p>Register that has the ACK information, back from MGSR as to whether a specific VD/VE Box has been blocked/unblocked</p> <p>0 -- Box has been blocked</p> <p>1 -- Box has been unblocked</p> <p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].</p> <p>To set bit0, for example, the data would be 0x0001_0001.</p> <p>To clear bit0, for example, the data would be 0x0001_0000.</p> <p>Note that mask bit is the data bit offset + 16.</p> <p>Message registers are protected from non-GT writes via the Message Channel.</p>			
DWord	Bit	Description	
0	31:12	Reserved	
		Access:	RO
		Format:	MBZ
11		Acknowledge that Media FIFO has been Blocked for VEBOX3	
		Access:	R/W
		_Custom_GTIReset:	BUS
<p>Acknowledge that MEDIA FIFO has been Blocked for VEBOX3</p> <p>1'b0 : Media FIFO Block Ack for VEBOX3(default)</p> <p>1'b1 : Media FIFO Unblock Ack VEBOX3</p> <p>Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>			
10		Acknowledge that Media FIFO has been Blocked for VEBOX2	
		Access:	R/W
		_Custom_GTIReset:	BUS
<p>Acknowledge that MEDIA FIFO has been Blocked for VEBOX2</p> <p>1'b0 : Media FIFO Block Ack for VEBOX2(default)</p> <p>1'b1 : Media FIFO Unblock Ack VEBOX2</p> <p>Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>			

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

	9	Acknowledge that Media FIFO has been Blocked for VEBOX1	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>Acknowledge that MEDIA FIFO has been Blocked for VEBOX1 1'b0 : Media FIFO Block Ack for VEBOX1(default) 1'b1 : Media FIFO Unblock Ack VEBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>		
	8	Acknowledge that Media FIFO has been Blocked for VEBOX0	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>Acknowledge that MEDIA FIFO has been Blocked for VEBOX0 1'b0 : Media FIFO Block Ack for VEBOX0(default) 1'b1 : Media FIFO Unblock Ack VEBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>		
	7	Acknowledge that Media FIFO has been Blocked for VDBOX7	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>Acknowledge that MEDIA FIFO has been Blocked for VDBOX7 1'b0 : Media FIFO Block Ack for VDBOX7(default) 1'b1 : Media FIFO Unblock Ack VDBOX7 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>		
	6	Acknowledge that Media FIFO has been Blocked for VDBOX6	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>Acknowledge that MEDIA FIFO has been Blocked for VDBOX6 1'b0 : Media FIFO Block Ack for VDBOX6(default) 1'b1 : Media FIFO Unblock Ack VDBOX6 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.</p>		
	5	Acknowledge that Media FIFO has been Blocked for VDBOX5	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>Acknowledge that MEDIA FIFO has been Blocked for VDBOX5 1'b0 : Media FIFO Block Ack for VDBOX5(default)</p>		

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

		1'b1 : Media FIFO Unblock Ack VDBOX5 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.			
	4	Acknowledge that Media FIFO has been Blocked for VDBOX4			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:
	Access:	R/W			
	_Custom_GTIReset:	BUS			
		Acknowledge that MEDIA FIFO has been Blocked for VDBOX4 1'b0 : Media FIFO Block Ack for VDBOX4(default) 1'b1 : Media FIFO Unblock Ack VDBOX4 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.			
3	Acknowledge that Media FIFO has been Blocked for VDBOX3				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
		Acknowledge that MEDIA FIFO has been Blocked for VDBOX3 1'b0 : Media FIFO Block Ack for VDBOX3(default) 1'b1 : Media FIFO Unblock Ack VDBOX3 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.			
2	Acknowledge that Media FIFO has been Blocked for VDBOX2				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
		Acknowledge that MEDIA FIFO has been Blocked for VDBOX2 1'b0 : Media FIFO Block Ack for VDBOX2(default) 1'b1 : Media FIFO Unblock Ack VDBOX2 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.			
1	Acknowledge that Media FIFO has been Blocked for VDBOX1				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
		Acknowledge that MEDIA FIFO has been Blocked for VDBOX1 1'b0 : Media FIFO Block Ack for VDBOX1(default) 1'b1 : Media FIFO Unblock Ack VDBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.			

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

	0	Acknowledge that Media FIFO has been Blocked for VDBOX0	
		Access:	R/W
		_Custom_GTIReset:	BUS
		Acknowledge that MEDIA FIFO has been Blocked for VDBOX0 1'b0 : Media FIFO Block Ack for VDBOX0(default) 1'b1 : Media FIFO Unblock Ack VDBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.	

Media unit Level Clock Gating override during rstflow 94B0

MEDMISCCP94B0 - Media unit Level Clock Gating override during rstflow 94B0				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	094B0h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	miscpc Clock Gating Disable during rstflow		
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>miscpc Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) w/a for A-step would be to make BIOS to write value 1 to this bit for power-on. Default value = 1</p>	Access:	R/W
Access:	R/W			
_Custom_GTIReset:	BUS			



MEMRR_BASE_LSB

MEMRR_BASE_LSB - MEMRR_BASE_LSB			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	108340h		
<p>The EMRR range is used to protect Xocode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.</p>			
DWord	Bit	Description	
0	31:12	RANGE_BASE	
		Default Value:	0000000h
		Access:	RO
		_Custom_GTIReset:	BUS
	This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.		
	11:4	Reserved	
		Access:	RO
		Format:	MBZ
	3	CONFIGURED	
		Default Value:	0h
		Access:	RO
		_Custom_GTIReset:	BUS
This bitfield is required to enable the PRMRR range			
2:0	Reserved		
	Access:	RO	
	Format:	MBZ	

MEMRR_BASE_MSB

MEMRR_BASE_MSB - MEMRR_BASE_MSB								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	108344h							
<p>The EMRR range is used to protect Xocode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.</p>								
DWord	Bit	Description						
0	31:0	<p>RANGE_BASE</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This field corresponds to bits 63:12 of the base address memory range which is allocated to EMRR memory.</p>	Default Value:	000h	Access:	RO	_Custom_GTIRreset:	BUS
Default Value:	000h							
Access:	RO							
_Custom_GTIRreset:	BUS							



MEMRR_MASK_LSB

MEMRR_MASK_LSB - MEMRR_MASK_LSB			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	108380h		
This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.			
DWord	Bit	Description	
0	31:12	RANGE_BASE	
		Default Value:	0000000h
		Access:	RO
		_Custom_GTIRreset:	BUS
		This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.	
11	11	RANGE_EN	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
		Indicates whether the EMRR range is enabled and valid.	
10	10	LOCK	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
		Setting this bit locks all writeable settings in this register, including itself.	
9:0	9:0	Reserved	
		Access:	RO
		Format:	MBZ

MEMRR_MASK_MSB

MEMRR_MASK_MSB - MEMRR_MASK_MSB								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	108384h							
This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.								
DWord	Bit	Description						
0	31:0	<p>RANGE_MASK</p> <table border="1"> <tr> <td>Default Value:</td> <td>000h</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.</p>	Default Value:	000h	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	000h							
Access:	RO							
_Custom_GTIReset:	BUS							



Message Address

MA_0_2_0_PCI - Message Address								
Register Space:	PCI: 0/2/0							
Size (in bits):	32							
Address:	000B0h							
This register contains the Message Address for MSIs sent by the device.								
DWord	Bit	Description						
0	31:2	<p>Message Address Field</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Default Value:</td> <td>0000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.</p>	Default Value:	0000000000000000000000000000000b	Access:	R/W	_Custom_GTIReset:	BUS
	Default Value:	0000000000000000000000000000000b						
Access:	R/W							
_Custom_GTIReset:	BUS							
1:0	<p>Force Dword Align</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Default Value:</td> <td>00b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.</p>	Default Value:	00b	Access:	RO	_Custom_GTIReset:	BUS	
Default Value:	00b							
Access:	RO							
_Custom_GTIReset:	BUS							

Message Control

MC_0_2_0_PCI - Message Control					
Register Space:	PCI: 0/2/0				
Size (in bits):	16				
Address:	000AEh				
<p>Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.</p>					
DWord	Bit	Description			
0	15:9	Reserved			
		Access:	RO		
		Format:	MBZ		
	8	Per Vector Mask Capable			
		Default Value:	1b		
		Access:	RO		
		_Custom_GTIRreset:	BUS		
	SR-IOV requires this capability.				
	7	64 Bit Capable			
		Access:	RO		
		_Custom_GTIRreset:	BUS		
		Description			
Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.					
<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">[Default]</td> </tr> </tbody> </table>		Value	Name	0b	[Default]
Value	Name				
0b	[Default]				
6:4	Multiple Message Enable				
	Default Value:	000b			
	Access:	R/W			
	_Custom_GTIRreset:	BUS			
	System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests 000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved 111: Reserved				
3:1	Multiple Message Capable				
	Default Value:	000b			
	Access:	RO			

MC_0_2_0_PCI - Message Control											
	<table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> <tr> <td colspan="2">System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.</td> </tr> </table>	_Custom_GTIReset:	BUS	System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.							
_Custom_GTIReset:	BUS										
System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.											
0	<table border="1"> <tr> <td colspan="2">MSI Enable</td> </tr> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> <tr> <td colspan="2">Controls the ability of this device to generate MSIs.</td> </tr> </table>	MSI Enable		Default Value:	0b	Access:	R/W	_Custom_GTIReset:	BUS	Controls the ability of this device to generate MSIs.	
MSI Enable											
Default Value:	0b										
Access:	R/W										
_Custom_GTIReset:	BUS										
Controls the ability of this device to generate MSIs.											

Message Data

MD_0_2_0_PCI - Message Data								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	000B4h							
This register contains the Message Data for MSIs sent by the device.								
DWord	Bit	Description						
0	15:0	<p>MESSDATA</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.</p>	Default Value:	0000000000000000b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	0000000000000000b							
Access:	R/W							
_Custom_GTIReset:	BUS							



Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	000ACh							
When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.								
DWord	Bit	Description						
0	15:8	Pointer to Next Capability <table border="1"><tr><td>Default Value:</td><td>11010000b</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIRreset:</td><td>BUS</td></tr></table> <p>This is a hardwired pointer to the next item in the capabilities list.</p>	Default Value:	11010000b	Access:	RO	_Custom_GTIRreset:	BUS
	Default Value:	11010000b						
Access:	RO							
_Custom_GTIRreset:	BUS							
7:0	Capability ID <table border="1"><tr><td>Default Value:</td><td>00000101b</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIRreset:</td><td>BUS</td></tr></table> <p>This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.</p>	Default Value:	00000101b	Access:	RO	_Custom_GTIRreset:	BUS	
Default Value:	00000101b							
Access:	RO							
_Custom_GTIRreset:	BUS							

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128ACh	
This register stores the count in bytes of CABAC_ZERO_WORD insertion. It is primarily provided for statistical data gathering .		
DWord	Bit	Description
0	31:0	MFC AVC Cabac Insertion Count Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.



MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	12804h					
DWord	Bit	Description				
0 avd_error_flagsR[31:0]	31:0	Reserved <table border="1"><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control						
Register Space:	MMIO: 0/2/0					
Access:	RO					
Size (in bits):	32					
Address:	128B8h					
This register stores the suggested data for next frame in multi-pass.						
DWord	Bit	Description				
0	31:24	Cumulative slice delta QP				
	23:16	QP Value suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve				
	15	QP-Polarity Change Cumulative slice delta QP polarity change.				
	14:13	Num-Pass Polarity Change Number of passes after cumulative slice delta QP polarity changes.				
	12	VDENC Slice Overflow Error Occurred Format: <table border="1"><tr><td></td><td>U1</td></tr></table> True when slice size exceeds slice max size on final pass when VDENC is using attempting to use slice overflow prevention.		U1		
		U1				
	11:8	Total Num-Pass				
	7:4	Reserved Access: <table border="1"><tr><td></td><td>RO</td></tr></table> Format: <table border="1"><tr><td></td><td>MBZ</td></tr></table>		RO		MBZ
		RO				
		MBZ				
3	Missing Huffman Code Jpeg HW encoder reports if Huffman table entry is missing.					
2	Panic Panic triggered to avoid too big packed file.					
1	Frame Bit Count Frame Bit count over-run/under-run flag					
0	Max Conformance Flag Max Macroblock conformance flag or Frame Bit count over-run/under-run					



MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128B4h	
This register stores the image status(flags).		
DWord	Bit	Description
0	31:0	Control Mask Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	128BCh			
This register stores the suggested QP COUNTS in multi-pass.				
DWord	Bit	Description		
0	31:24	Cumulative QP Adjust <table border="1"> <tr> <td>Format:</td> <td>U8</td> </tr> </table> <p>Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).</p>	Format:	U8
	Format:	U8		
23:0	Cumulative QP <table border="1"> <tr> <td>Format:</td> <td>U24</td> </tr> </table> <p>Cumulative QP for all MB of a Frame (Can be used for computing average QP).</p>	Format:	U24	
Format:	U24			



MFD Error Status

MFD_ERROR_STATUS - MFD Error Status		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1C0800h	
ShortName:	MFD_ERROR_STATUS_VCS0	
Description:	For VDBox0	
Address:	1C4800h	
ShortName:	MFD_ERROR_STATUS_VCS1	
Description:	For VDBox1	
Address:	1D0800h	
ShortName:	MFD_ERROR_STATUS_VCS2	
Description:	For VDBox2	
Address:	1D4800h	
ShortName:	MFD_ERROR_STATUS_VCS3	
Description:	For VDBox3	
Address:	1E0800h	
ShortName:	MFD_ERROR_STATUS_VCS4	
Description:	For VDBox4	
Address:	1E4800h	
ShortName:	MFD_ERROR_STATUS_VCS5	
Description:	For VDBox5	
Address:	1F0800h	
ShortName:	MFD_ERROR_STATUS_VCS6	
Description:	For VDBox6	
Address:	1F4800h	
ShortName:	MFD_ERROR_STATUS_VCS7	
Description:	For VDBox7	
<p>This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.</p>		
DWord	Bit	Description
0	31:20	Reserved
		Access: RO
		Format: MBZ

MFD_ERROR_STATUS - MFD Error Status			
19:16	<p>AVC Short Format Error Flags</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Exists If:</td> <td>// AVC Short Format == True</td> </tr> </table> <p>Bit-stream error detected by VLD short format bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <p>[19] Slice Type SE Error Flag Invalid Slice Type SE</p> <p>[18] MMCO SE Error Flag Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit</p> <p>[17] Reordering IDC Error Flag Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value</p> <p>[16] Premature bitstream end is hit before finishing slice header decode</p>	Exists If:	// AVC Short Format == True
Exists If:	// AVC Short Format == True		
15:0	<p>Bit-stream Error flags</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Exists If:</td> <td>// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True</td> </tr> </table> <p>Bitstream error detected by the VLD bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame.</p> <p>AVC CAVLC: Please refer to AVC CAVLC table for each bit field</p> <p>AVC CABAC: Please refer to AVC CABAC table for each bit field</p> <p>VC1: Please refer to VC1 table for each bit field</p> <p>MPEG2: Please refer to MPEG2 table for each bit field</p>	Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True
Exists If:	// AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True		



MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	1C0820h	
ShortName:	MFD_PICTURE_PARAM_VCS0	
Description:	For VDbbox0	
Address:	1C4820h	
ShortName:	MFD_PICTURE_PARAM_VCS1	
Description:	For VDbbox1	
Address:	1D0820h	
ShortName:	MFD_PICTURE_PARAM_VCS2	
Description:	For VDbbox2	
Address:	1D4820h	
ShortName:	MFD_PICTURE_PARAM_VCS3	
Description:	For VDbbox3	
Address:	1E0820h	
ShortName:	MFD_PICTURE_PARAM_VCS4	
Description:	For VDbbox4	
Address:	1E4820h	
ShortName:	MFD_PICTURE_PARAM_VCS5	
Description:	For VDbbox5	
Address:	1F0820h	
ShortName:	MFD_PICTURE_PARAM_VCS6	
Description:	For VDbbox6	
Address:	1F4820h	
ShortName:	MFD_PICTURE_PARAM_VCS7	
Description:	For VDbbox7	
DWord	Bit	Description
0	31:0	Reserved
		Access: RO
		Format: MBZ

MFX Frame BitStream SE/BIN Count

MFX_SE_BIN_CT - MFX Frame BitStream SE/BIN Count		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1C086Ch	
ShortName:	MFX_SE_BIN_CT_VCS0	
Description:	For VDBox0	
Address:	1C486Ch	
ShortName:	MFX_SE_BIN_CT_VCS1	
Description:	For VDBox1	
Address:	1D086Ch	
ShortName:	MFX_SE_BIN_CT_VCS2	
Description:	For VDBox2	
Address:	1D486Ch	
ShortName:	MFX_SE_BIN_CT_VCS3	
Description:	For VDBox3	
Address:	1E086Ch	
ShortName:	MFX_SE_BIN_CT_VCS4	
Description:	For VDBox4	
Address:	1E486Ch	
ShortName:	MFX_SE_BIN_CT_VCS5	
Description:	For VDBox5	
Address:	1F086Ch	
ShortName:	MFX_SE_BIN_CT_VCS6	
Description:	For VDBox6	
Address:	1F486Ch	
ShortName:	MFX_SE_BIN_CT_VCS7	
Description:	For VDBox7	
<p>This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFX Frame Bit-stream SE/BIN Count</p> <p>Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clock or SE/clock.</p>



MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count						
Register Space:	MMIO: 0/2/0					
Access:	RO					
Size (in bits):	32					
Address:	1C0868h					
ShortName:	MFX_MB_COUNT_VCS0					
Description:	For VDBox0					
Address:	1C4868h					
ShortName:	MFX_MB_COUNT_VCS1					
Description:	For VDBox1					
Address:	1D0868h					
ShortName:	MFX_MB_COUNT_VCS2					
Description:	For VDBox2					
Address:	1D4868h					
ShortName:	MFX_MB_COUNT_VCS3					
Description:	For VDBox3					
Address:	1E0868h					
ShortName:	MFX_MB_COUNT_VCS4					
Description:	For VDBox4					
Address:	1E4868h					
ShortName:	MFX_MB_COUNT_VCS5					
Description:	For VDBox5					
Address:	1F0868h					
ShortName:	MFX_MB_COUNT_VCS6					
Description:	For VDBox6					
Address:	1F4868h					
ShortName:	MFX_MB_COUNT_VCS7					
Description:	For VDBox7					
<p>This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.</p>						
DWord	Bit	Description				
0	31:20	<p>MBZ</p> <table border="1" style="width: 100%;"> <tr> <td>Exists If:</td> <td>// JPEG == True</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table> <p>This field is currently reserved</p>	Exists If:	// JPEG == True	Format:	MBZ
Exists If:	// JPEG == True					
Format:	MBZ					

MFx_MB_COUNT - MFx Frame Macroblock Count	
31:16	Intra MB Count
	Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True
	Format: U16
19:0	JPEG Block Count
	Exists If: // JPEG == True
	Format: U20
This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.	
15:0	Number of MB Concealment
	Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True
This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.	



MFX Frame Row-Stored/BitStream Read Count

MFX_ROW_PER_BS_COUNT - MFX Frame Row-Stored/BitStream Read Count		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12880h	
This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
	Format: MBZ	
15:0	MFX row-stored/bit-stream read request Count Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.	

MFX PAK MPEG TS STATUS

MFX_PAK_MPEG_TS_STATUS - MFX PAK MPEG TS STATUS					
Register Space:	MMIO: 0/2/0				
Access:	RO				
Size (in bits):	32				
Address:	12950h				
This register stores MPEGTS packet status information					
DWord	Bit	Description			
0	31:28	Next Continuity Center <table border="1"> <tr> <td>Format:</td> <td>U4</td> </tr> </table> <p>HW will update the continuity counter the next MPEGTS packet stream for this stream ID needs to place in the bitstream.</p>	Format:	U4	
	Format:	U4			
	27:16	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:	RO				
Format:	MBZ				
15:0	MPEGTS Packet Count <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> </table> <p>This field counts the total number of written MPEGTS video packets by PAK HW. The PES header (which contains the PCR and PTS value) is included in this count as well.</p>	Format:	U16		
Format:	U16				



MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1C0838h	
ShortName:	MFX_STATUS_FLAGS_VCS0	
Description:	For VDBox0	
Address:	1C4838h	
ShortName:	MFX_STATUS_FLAGS_VCS1	
Description:	For VDBox1	
Address:	1D0838h	
ShortName:	MFX_STATUS_FLAGS_VCS2	
Description:	For VDBox2	
Address:	1D4838h	
ShortName:	MFX_STATUS_FLAGS_VCS3	
Description:	For VDBox3	
Address:	1E0838h	
ShortName:	MFX_STATUS_FLAGS_VCS4	
Description:	For VDBox4	
Address:	1E4838h	
ShortName:	MFX_STATUS_FLAGS_VCS5	
Description:	For VDBox5	
Address:	1F0838h	
ShortName:	MFX_STATUS_FLAGS_VCS6	
Description:	For VDBox6	
Address:	1F4838h	
ShortName:	MFX_STATUS_FLAGS_VCS7	
Description:	For VDBox7	
This register stores the various pipeline status flags. This register is not part of hardware context save and restore.		
DWord	Bit	Description
0	31:17	Reserved
		Access: RO
		Format: MBZ

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

16	MFX Active Frame decoding/encoding is in progress. Set on frame_start; clear on frame_end.		
15:10	Reserved		
	Access:	RO	
	Format:	MBZ	
9	Streamout Enable		
8	Reserved		
7	Post Deblocking Mode Enable		
6	Pre Deblocking Mode Enable		
5	Decoder Mode Select		
	Value	Name	
	0	Configure the MFD Engine for VLD Mode	
	1	Configure the MFD Engine for IT Mode	
4	Codec Select		
	Value	Name	
	0	Decode	
	1	Encode	
3:2	Video Mode		
	Value	Name	
	00b	MPEG2	
	01b	VC1	
	10b	AVC	
	11b	JPEG	
1	Decoder Short Format Mode		
	Value	Name	Description
	0		AVC/VC1 Short Format Mode is in use
	1		AVC/VC1 Long Format Mode is in use
0	Stitch Mode		
	Value	Name	Description
	0b		Not in Stitch Mode
	1b		In the Special Stitch Mode



MFX SFC LOCK Request

MFX_SFC_LOCK_REQUEST - MFX SFC LOCK Request				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	1C088Ch			
ShortName:	MFX_SFC_LOCK_REQUEST_VCS0			
Description:	For VDBox0			
Address:	1D088Ch			
ShortName:	MFX_SFC_LOCK_REQUEST_VCS2			
Description:	For VDBox2			
Address:	1E088Ch			
ShortName:	MFX_SFC_LOCK_REQUEST_VCS4			
Description:	For VDBox4			
Address:	1F088Ch			
ShortName:	MFX_SFC_LOCK_REQUEST_VCS6			
Description:	For VDBox6			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	MFX_SFC_Forced_Lock		
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells MFX that a software reset is going to happen. MFX then issues a forced lock to SFC. If SFC is currently locked to MFX, SFC should not unlock itself from MFX. If SFC is NOT currently locked to MFX, SFC should not accept the lock request from MFX. Driver needs to clear this bit after the software reset sequence is complete.</p>	Format:	U1
Format:	U1			

MFX SFC LOCK Status

MFX_SFC_LOCK_STATUS - MFX SFC LOCK Status		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1C0890h	
ShortName:	MFX_SFC_LOCK_STATUS_VCS0	
Description:	For VDbbox0	
Address:	1D0890h	
ShortName:	MFX_SFC_LOCK_STATUS_VCS2	
Description:	For VDBox2	
Address:	1E0890h	
ShortName:	MFX_SFC_LOCK_STATUS_VCS4	
Description:	For VDBox4	
Address:	1F0890h	
ShortName:	MFX_SFC_LOCK_STATUS_VCS6	
Description:	For VDBox6	
DWord	Bit	Description
0	31:2	Reserved
		Access: RO
		Format: MBZ
1		MFX_SFC_Forced_Act
		Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that MFX has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert MFX_SFC_Forced_Lock as well.
0		MFX_SFC_Usage
		Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to MFX. This bit should be set after SFC accepts the lock request from MFX. This bit should be clear once SFC finishes the workload and unlocked from MFX. In case a reset happens on MFX, this bit must be reset once a new workload is received

MGCMD

MGCMD - MGCMD					
Register Space:	MMIO: 0/2/0				
Size (in bits):	32				
SOC_Consumer:	BIOS				
Address:	108300h				
Mirror GT hardware uses for Vtd state.					
DWord	Bit	Description			
0	31	TE			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>0: Disable Vtd DMA remapping 1: Enable Vtd DMA remapping</p>	Access:	RO	_Custom_GTIReset:
	Access:	RO			
	_Custom_GTIReset:	BUS			
30:26	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
25	25	IRE			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>No HW usage model. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware</p>	Access:	RO	_Custom_GTIReset:
	Access:	RO			
	_Custom_GTIReset:	BUS			
24:0	Reserved				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				

MGSR GTI PD Control

GTIPD_CTRL - MGSR GTI PD Control		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
CrashLogSaved:	true	
CrashLogVisibility:	cspec	
Address:	00E04h-00E07h	
DWord	Bit	Description
0	31:16	Mask Bits
		Access: RO
	Mask bits apply to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.	
	15:6	Reserved
		Access: RO
		Format: MBZ
	5:4	Reserved
		Access: RO
		Format: MBZ
	3	Reserved
		Access: RO
		Format: MBZ
2	Render Unblock	
	Default Value: 0b Block	
	Access: R/WC	
Render unblock (1) or block (0)		
1	GT Block Mode	
	Default Value: 1b Standby mode	
	Access: R/WC	
Set GT C6 Standby mode (1) or CPD (0)		
0	GT Unblock	
	Default Value: 0b Block	
	Access: R/WC	
GT unblock (1) or block (0)		



MGSR Media PD Control

MEDIAPD_CTRL - MGSR Media PD Control		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
CrashLogSaved:	true	
CrashLogVisibility:	cspec	
Address:	00E00h-00E03h	
DWord	Bit	Description
0	31:16	Mask Bits
		Access: RO
	Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.	
	15:12	Reserved
Access: RO Format: MBZ		
11:8	VEBOX Unblock	
	Default Value: 0b Access: R/WC	
VEBOX unblock indications for VEBOX[3:0] (1) or block (0)		
7:0	VDBOX Unblock	
	Default Value: 0b Access: R/WC	
VDBOX unblock indications for VDBOX[7:0] (1) or block (0) VDBOX[1:0] reside in Media slice0, VDBOX[3:2] in slice1, VDBOX[5:4] in slice2, VDBOX[7:6] in slice3		

MGSR Programmable Shadow 0

PROGSHADOW_0 - MGSR Programmable Shadow 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	00EE0h-00EE3h	
DWord	Bit	Description
0	31:26	Reserved
		Access: RO
		Format: MBZ
	25:0	Shadow Address
		Default Value: 00000h
		Access: R/W
Programmable shadow register address.		



MGSR Programmable Shadow 1

PROGSHADOW_1 - MGSR Programmable Shadow 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	00EE4h-00EE7h	
DWord	Bit	Description
0	31:26	Reserved
		Access: RO
		Format: MBZ
	25:0	Shadow Address
		Default Value: 00000h
		Access: R/W
Programmable shadow register address.		

Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant								
Register Space:	PCI: 0/2/0							
Size (in bits):	8							
Address:	0003Eh							
The Integrated Graphics Device has no requirement for the settings of Latency Timers.								
DWord	Bit	Description						
0	7:0	Minimum Grant Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table>	Default Value:	00000000b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	00000000b							
Access:	RO							
_Custom_GTIReset:	BUS							



Minute IA Force Fence

MIA_FORCE_FENCE - Minute IA Force Fence		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Programming Notes		
Write by MinIAto issue a fence. Written value is not stored.		
Write to this register by the core will trigger GUC Hardware to do following sequencing Stall the core interface. Check for all prior writes generated by the core are completed and to global observable point. Un-Stall the core interface.		
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
	Format: MBZ	
	0	Reserved
Access: RO		
Format: MBZ		

Minute IA Force TLB Invalidate

MIA_INV_TLB - Minute IA Force TLB Invalidate		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Programming Notes		
Write to issue a TLB invalidate or Fence write. Written value is not stored.		
Write to this register by the core will trigger GUC Hardware to do following sequencing Stall the core interface. Check for all prior writes generated by the core are completed and to global observable point. TLB invalidation generation and completion to memory interface. Un-Stall the core interface.		
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
	Format: MBZ	
	0	Reserved
Access: RO		
Format: MBZ		



Mirror FUSE A

MIRROR_FUSE_A - Mirror FUSE A		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Mirror Register for Fuses in INF domain.		
DWord	Bit	Description
0	31:1	Reserved Reserved
	0	Reserved
		Access:
Format:	MBZ	

Mirror GT C6 entry Count

MIRROR_GT_C6_ENTRY_COUNT - Mirror GT C6 entry Count						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	00DACH					
Name:	Mirror GT C6 entry Count					
ShortName:	MIRROR_GT_C6_ENTRY_COUNT					
This register holds the mirrored value, from OA, of the number of GT C6 entries that have happened						
DWord	Bit	Description				
0	31:0	Count for number of C6 entries <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> Mirror the number of times that GT has entered C6	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					



Mirror of Base Data of Stolen Memory

BDSM_0_2_0_PCI - Mirror of Base Data of Stolen Memory			
Register Space:	PCI: 0/2/0		
Size (in bits):	64		
Address:	000C0h		
Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.			
DWord	Bit	Description	
0..1	63:32	Graphics Base of Stolen Memory MSB	
		Default Value:	000000000000b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.			
31:20		Graphics Base of Stolen Memory LSB	
		Default Value:	000000000000b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.			
19:1		Reserved	
		Access:	RO
		Format:	MBZ
0		Spare	
		Default Value:	0b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
This was a lock bit prior.			

Mirror of Device Enable

DEVEN0_0_2_0_PCI - Mirror of Device Enable			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00054h		
Mirror of DEVEN_0_0_0_PCI.			
DWord	Bit	Description	
0	15	Reserved	
		Access:	RO
		Format:	MBZ
	14	Chap Enable	
		Default Value:	0b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
	13	Device 6 Enable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
	12:11	Reserved	
		Access:	RO
		Format:	MBZ
	10	Device 5 Enable	
Default Value:		0b	
Access:		RO	
	_Custom_GTIReset:	BUS	
9:8	Reserved		
	Access:	RO	
	Format:	MBZ	
7	Device 4 Enable		
	Default Value:	1b	
	Access:	RO Variant	
	_Custom_GTIReset:	BUS	
6	Reserved		
	Access:	RO	
	Format:	MBZ	

DEVEN0_0_2_0_PCI - Mirror of Device Enable

5	Device 3 enable for Display HD Audio		
	Default Value:	1b	
	Access:	RO Variant	
	_Custom_GTIRreset:	BUS	
	4	Internal Graphics Engine	
		Default Value:	1b
		Access:	RO Variant
		_Custom_GTIRreset:	BUS
	0: Bus 0 Device 2 is disabled and hidden1: Bus 0 Device 2 is enabled and visibleThis bit will be set to 0b and remain 0b if Device 2 capability is disabled.		
	3	PEG10 Enable	
		Default Value:	1b
		Access:	RO Variant
		_Custom_GTIRreset:	BUS
	2	PEG11 Enable	
		Default Value:	1b
		Access:	RO Variant
		_Custom_GTIRreset:	BUS
	1	PEG12 Enable	
Default Value:		1b	
Access:		RO Variant	
_Custom_GTIRreset:		BUS	
0	Host Bridge		
	Default Value:	1b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	

Mirror of DPRB LSB

DPRB_LSB - Mirror of DPRB LSB					
Register Space:	MMIO: 0/2/0				
Size (in bits):	32				
Address:	090E8h				
DWord	Bit	Description			
0	31:20	DPRBASE			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table>	Access:	RO	_Custom_GTIRreset:
	Access:	RO			
	_Custom_GTIRreset:	BUS			
1MB aligned base of DMA Range					
19:0	Spares				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table>	Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO				
_Custom_GTIRreset:	BUS				



Mirror of DPRB MSB

DPRB_MSB - Mirror of DPRB MSB						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	090ECh					
DWord	Bit	Description				
0	31:0	DPRBASE <table border="1"><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIReset:</td><td>BUS</td></tr></table> <p>1MB aligned base of DMA Range. Bits 63:32 of the DPRbase.</p>	Access:	RO	_Custom_GTIReset:	BUS
Access:	RO					
_Custom_GTIReset:	BUS					

Mirror of DSMBASE LSB

DSMB_LSB - Mirror of DSMBASE LSB			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	090D0h		
DSM Base			
DWord	Bit	Description	
0	31:20	DSM Base Register LSB	
		Access:	RO
		_Custom_GTIRreset:	BUS
	This register contains the base address of stolen DRAM memory.		
	19:0	Spares	
		Access:	RO
		_Custom_GTIRreset:	BUS



Mirror of DSMBASE MSB

DSMB_MSB - Mirror of DSMBASE MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	090D4h	
DSM Base		
DWord	Bit	Description
0	31:0	DSM Base Register
		Access: RO
		_Custom_GTIRreset: BUS
		This register contains the base address of stolen DRAM memory.

Mirror of EMRR Base LSB

EMRRBASE_LSB - Mirror of EMRR Base LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09200h	
Mirror of EMRR Base		
DWord	Bit	Description
0	31:12	EMRR Base LSB
		Access: RO
		_Custom_GTIReset: BUS
	EMRR Base Value.	
11:0	Spares	
	Access: RO	
	_Custom_GTIReset: BUS	



Mirror of EMRR Base MSB

EMRRBASE_MSB - Mirror of EMRR Base MSB						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	09204h					
Mirror of EMRR Base						
DWord	Bit	Description				
0	31:0	EMRR Base MSB <table border="1"><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIRreset:</td><td>BUS</td></tr></table> EMRR Base Value.	Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO					
_Custom_GTIRreset:	BUS					

Mirror of EU Disable Fuses - Register0

MIRROR_EU_DISABLE0 - Mirror of EU Disable Fuses - Register0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09134h		
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7:0	EU Disable Fuses	
		Access:	RO Variant
		_Custom_GTIReset:	BUS
		One Bit per EU In a sub-slice. Enable/Disable the same EU# in all the Sub-Slices.	
		Programming Notes	
	Bit values of 0 indicate enabled; Bit values of 1 indicate disabled.		



Mirror of FUSE1 Control DW

FUSE1 - Mirror of FUSE1 Control DW		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0911Ch	
DWord	Bit	Description
0	31:27	Spares
		Access: RO
		_Custom_GTIReset: BUS
	26	VA DISABLE
		Access: RO
		_Custom_GTIReset: BUS
	25:24	Reserved
		Access: RO
		Format: MBZ
	23	Reserved
	22	Reserved
	21	Reserved
	20	HUC AUTH BYPASS
		Access: RO
		_Custom_GTIReset: BUS
19	HUC DISABLE	
	Access: RO	
	_Custom_GTIReset: BUS	
		This fuse works for both Micro Controllers present in Media pipeline.
18	Reserved	
17:16	Spares1	
	Access: RO	
	_Custom_GTIReset: BUS	
15	Authentication Bypass	
	Access: RO	
	_Custom_GTIReset: BUS	
14	Reserved	

FUSE1 - Mirror of FUSE1 Control DW

	13	Spares2	Access:	RO
			_Custom_GTIRreset:	BUS
	12	Reserved		
	11	Render Disable	Access:	RO
			_Custom_GTIRreset:	BUS
	10:9	Spares3	Access:	RO
			_Custom_GTIRreset:	BUS
	8	VME IME Enable	Access:	RO
			_Custom_GTIRreset:	BUS
	7	VME CRE Enable	Access:	RO
			_Custom_GTIRreset:	BUS
	6:5	Media Decode	Access:	RO
			_Custom_GTIRreset:	BUS
		Applicable to Media - Fuse to disable VIN from processing media_obj or turn off the entire crclk tree trunk.		
4	Disable GT3 Slice Shutdown	Access:	RO	
		_Custom_GTIRreset:	BUS	
		N/A -- Not used by GT hardware: This fuse is actually enforced by the PCU;it is reflected here for driver information only.		
3	Reserved			
2	Spares4	Access:	RO	
		_Custom_GTIRreset:	BUS	
1:0	Media Encode	Access:	RO	
		_Custom_GTIRreset:	BUS	
		Applicable to Media - One fuse to disable VIN from processing Pak_obj. Second fuse to disable VME.		



Mirror of Fuse 3 control DW

FUSE3 - Mirror of Fuse 3 control DW			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09118h		
FUSE MIRROR 3			
DWord	Bit	Description	
0	31:29	Reserved	
		Access:	RO
		Format:	MBZ
	28	GT L3 HASH MODE FUSE	
		Access:	RO
		_Custom_GTIReset:	BUS
	L3 Bank Hash Mode (used in certain dynamic slice configurations) 0b = Use safe mode, hashing to fewer banks in specific cases 1b = Use all banks when possible		
	27:26	Reserved	
		Access:	RO
		Format:	MBZ
25:24	GT WGBBox Configuration Fuse		
	Access:	RO	
	_Custom_GTIReset:	BUS	
WGBBox configuration 00b = Both WGBBOXes enabled 01b = WGBBOX1 enabled 10b = WGBBOX0 enabled			
23:16	Reserved		
	Access:	RO	
	Format:	MBZ	
15:8	Reserved		
	Access:	RO	
	Format:	MBZ	
7:0	GT L3 MODE FUSE		
	Access:	RO	
	_Custom_GTIReset:	BUS	
L3 Bank Disable Select (only used in certain dynamic slice configurations and sub-single slice			

FUSE3 - Mirror of Fuse 3 control DW

	<p>SKUs) 1 - Disabled; 0 - Enabled Bit0 - Bank0 Bit1 - Bank1 Likewise, Bit7 - Bank7</p>
--	---

Mirror of Global Command Register

GCMD - Mirror of Global Command Register						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	090CCh					
DWord	Bit	Description				
0	31	<p>Translation Enable</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware.</p> <p>Hardware reports the status of the translation enable operation through the TES field in the Global Status register.</p> <p>Before enabling (or re-enabling) DMA-remapping hardware through this field, software must:</p> <ul style="list-style-type: none"> • Setup the DMA-remapping structures in memory. • Flush the write buffers (through WBF field), if write buffer flushing is reported as required. • Set the root-entry table pointer in hardware (through SRTP field). • Perform global invalidation of the context-cache and global invalidation of IOTLB • If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). <p>Refer to Section 9 for detailed software requirements.</p> <p>There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all.</p> <p>Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG. Value returned on read of this field is undefined.</p>	Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO					
_Custom_GTIRreset:	BUS					
30	30	<p>Set Root Table Pointer</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register.</p> <p>Hardware reports the status of the "root table pointer set" operation through the RTPS field in the Global Status register.</p> <p>The root table pointer set operation must be performed before enabling or re-enabling(after disabling) DMA remapping through the TE field.</p> <p>After a "root table pointer set" operation, software must globally invalidate the context cache and then globally invalidate the IOTLB. This is required to ensure hardware uses only there mapping structures referenced by the new root table pointer, and not any stale cached entries.</p> <p>While DMA remapping is active, software may update the root table pointer through this field.</p>	Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO					
_Custom_GTIRreset:	BUS					

GCMD - Mirror of Global Command Register

However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.

29 Set Fault Log

Access:	RO
_Custom_GTIRreset:	BUS

This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the fault log set operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFI field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

28 Enable Fault Logging

Access:	RO
_Custom_GTIRreset:	BUS

This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging. 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through SFI field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. Value returned on read of this field is undefined.

27 Write Buffer Flush

Access:	RO
_Custom_GTIRreset:	BUS

This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Refer to Section 11.1 for details on write-buffer flushing requirements. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. Value returned on read of this field is undefined.

GCMD - Mirror of Global Command Register

26	Queued Invalidation Enable		
		Access:	RO
		_Custom_GTIRreset:	BUS
		<p>This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations.</p> <p>0: Disable queued invalidations. 1: Enable use of queued invalidations.</p> <p>Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register.</p> <p>Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations. The value returned on a read of this field is undefined.</p>	
25	Interrupt Remapping Enable		
		Access:	RO
		_Custom_GTIRreset:	BUS
		<p>This field is valid only for implementations supporting interrupt remapping.</p> <p>0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware</p> <p>Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register.</p> <p>There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all.</p> <p>Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register.</p> <p>The value returned on a read of this field is undefined.</p>	
24	Set Interrupt Remap Table Pointer		
		Access:	RO
		_Custom_GTIRreset:	BUS
		<p>This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register.</p> <p>Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register.</p> <p>The interrupt remap table pointer set operation must be performed before enabling or re-enabling(after disabling) interrupt-remapping hardware through the IRE field.</p> <p>After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries.</p> <p>While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by</p>	

GCMD - Mirror of Global Command Register

	<p>the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.</p>					
23	<p>Compatibility Format Interrupt</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active.</p> <p>0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. Refer to Section 5.4.1 for details on Compatibility Format interrupt requests. The value returned on a read of this field is undefined. This field is not implemented on Itanium(TM) implementations.</p>		Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO					
_Custom_GTIRreset:	BUS					
22:0	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table>		Access:	RO	_Custom_GTIRreset:	BUS
Access:	RO					
_Custom_GTIRreset:	BUS					

Mirror of GMCH Graphics Control Register

MGGC - Mirror of GMCH Graphics Control Register			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09094h		
Mirror of GMCH Graphics Control Register.			
DWord	Bit	Description	
0	31:16	Spares	
		Access:	RO
		_Custom_GTIRreset:	BUS
	15:8	Graphics Mode Select	
		Default Value:	3h
		Access:	RO
		_Custom_GTIRreset:	BUS
	<p>This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.</p> <p>1h-4h: Reserved.</p> <p>5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table.</p> <p>Eh-Fh: Reserved.</p> <p>NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable.</p> <p>Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.</p> <p>BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p>		
	7:6	GTT Graphics Memory Size	
		Access:	RO
_Custom_GTIRreset:		BUS	
<p>This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register.</p> <p>0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed.</p> <p>1h: 2 MB of memory pre-allocated for GTT.</p> <p>2h: 4 MB of memory pre-allocated for GTT.</p>			

MGGC - Mirror of GMCH Graphics Control Register

		<p>3h: 8 MB of memory pre-allocated for GTT. Hardware functionality in case of programming this value to Reserved is not guaranteed. This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.</p>	
5:3	Spares2	Access:	RO
		_Custom_GTIRreset:	BUS
2	Versatile Acceleration Mode Enable	Access:	RO
		_Custom_GTIRreset:	BUS
		<p>Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.</p>	
1	IGD VGA Disable	Access:	RO
		_Custom_GTIRreset:	BUS
		<p>0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register)pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override(CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.</p>	
0	Spares3	Access:	RO
		_Custom_GTIRreset:	BUS



Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09124h		
<p>This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.</p> <p>For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.</p> <p>The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter. The allocation is for 4MB and the base address is defined by bits [38:22].</p>			
DWord	Bit	Description	
0	31:22	Memory Base Address (LSB - 31:22 of 38:22)	
		Access: RO	
		_Custom_GTIRreset: BUS	
		Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).	
21:4	Spares	Access: RO	
		_Custom_GTIRreset: BUS	
		Prefetchable Memory	
		Access: RO	
3	Prefetchable Memory	_Custom_GTIRreset: BUS	
		Hardwired to 0 to prevent prefetching.	
		Memory Type	
		Access: RO	
2:1	Memory Type	_Custom_GTIRreset: BUS	
		00b: To indicate 32 bit base address.	
		01b: Reserved.	
		10b: To indicate 64 bit base address.	
		11b: Reserved.	

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

	0	Memory I/O Space	
		Access:	RO
		_Custom_GTIReset:	BUS
		Hardwired to 0 to indicate memory space.	



Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

GTTMMADR_MSB - Mirror of Graphics Translation Table and Memory Mapped Range Address UDW		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09128h	
<p>This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.</p> <p>For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.</p> <p>The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter. The allocation is for 4MB and the base address is defined by bits [38:22].</p>		
DWord	Bit	Description
0	31:7	Spares
		Access: RO
	_Custom_GTIRreset: BUS	
	6:0	Memory Base Address (MSB - 38:32 of 38:22)
Access: RO		
_Custom_GTIRreset: BUS		
<p>Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).</p>		

Mirror of GSMBASE LSB

GSMB_LSB - Mirror of GSMBASE LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	090D8h	
This register contains the base address of stolen DRAM memory for the GTT.		
DWord	Bit	Description
0	31:20	GSM Base
		Access: RO
	_Custom_GTIRreset: BUS	
	This register contains the base address of stolen DRAM memory for the GTT.	
19:0	Spares	
	Access: RO	
	_Custom_GTIRreset: BUS	



Mirror of GSMBASE MSB

GSMB - Mirror of GSMBASE MSB						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	090DCh					
This register contains the base address of stolen DRAM memory for the GTT.						
DWord	Bit	Description				
0	31:0	GSMB Base <table border="1"><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIReset:</td><td>BUS</td></tr></table> <p>This register contains the base address of stolen DRAM memory for the GTT.</p>	Access:	RO	_Custom_GTIReset:	BUS
Access:	RO					
_Custom_GTIReset:	BUS					

Mirror of GT DSS Enable Fuses

MIRROR_GT_DSS_ENABLE - Mirror of GT DSS Enable Fuses								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
Address:	0913Ch							
DWord	Bit	Description						
0	31:0	<p>GT DSS Enable Fuses</p> <table border="1"> <tr> <td>Default Value:</td> <td>0000003fh Default Value</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p style="text-align: center;">Description</p> <p>DSS Enable Fuses Encoding:- 32'h0000 = All Sub-Slices Disabled Note: Encoding starts with bit 0 mapped to DSS0 of slice0 and goes on up to bit 31 as per the Project's Number of DSS per Slice. See below for elaborated mapping note for example where there are 6 DSS per Slice- bit0 - DSS 0 of Slice 0 bit1 - DSS 1 of Slice 0 Likewise - bit5- DSS 5of Slice 0 bit 6- DSS0 of Slice 1</p> <p style="text-align: center;">Programming Notes</p> <p>Bit values of 1 indicate DSS Enabled. Bit values of 0 indicate DSS Disabled.</p>	Default Value:	0000003fh Default Value	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	0000003fh Default Value							
Access:	RO							
_Custom_GTIReset:	BUS							



Mirror of GT Slice Enable Fuses

MIRROR_GT_SLICE_EN - Mirror of GT Slice Enable Fuses								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
Address:	09138h							
DWord	Bit	Description						
0	31:8	Reserved						
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
	7:0	GT slice Enable Fuses						
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Slice Enable Fuses Bit0 - Slice 0 Enabled Bit1 - Slice;1 Enabled Likewise; Bit7 - Slice;7 Enabled</p> <table border="1"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">Bit values of;1 indicate enabled. Bit values of;0 indicate disabled.</td> </tr> </tbody> </table>	Access:	RO	_Custom_GTIReset:	BUS	Programming Notes	
Access:	RO							
_Custom_GTIReset:	BUS							
Programming Notes								
Bit values of;1 indicate enabled. Bit values of;0 indicate disabled.								

Mirror of GT VEBOX and VDBOX Disable

MIRROR_GT_VEBOX_VDBOX_DISABLE - Mirror of GT VEBOX and VDBOX Disable		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09140h	
Mirror of GT VEBOX and VDBOX Disable		
DWord	Bit	Description
0	31:20	Reserved
		Access: RO
	Format: MBZ	
	19:16	GT VEBOX DISABLE _Custom_GTIRreset: BUS VEBOX config fuses encoding:- bit 0 = VEBOX 0 disabled bit 1 = VEBOX 1 disabled bit 2 = VEBOX 2 disabled bit 3 = VEBOX 3 disabled <div style="text-align: center;">Programming Notes</div> Bit values of 0 indicate enabled. Bit values of 1 indicate disabled.
15:8	Reserved	
	Access: RO	
Format: MBZ		
7:0	7:0	GT VDBOX DISABLE
		Access: RO
	_Custom_GTIRreset: BUS	
	VDBOX config fuses encoding:- bit 0 = VDBOX 0 disabled bit 1 = VDBOX 1 disabled Likewise, bit 7 = VDBOX 7 disabled <div style="text-align: center;">Programming Notes</div> Bit values of 0 indicate enabled. Bit values of 1 indicate disabled.	

Mirror of MBC IDIMSG Reg

GAM_MBC_MIRROR - Mirror of MBC IDIMSG Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
MBC IDI Message Register Mirror in GAM			
DWord	Bit	Description	
0	31:16	Mask Bits	
		Access:	RO
		_Custom_GTIReset:	BUS
		Reserved.	
	15:9	Reserved	
		Access:	RO
		Format:	MBZ
	8	Reserved	
	7:0	Reserved	
		Access:	RO
		Format:	MBZ

Mirror of PCICMD MAE/BME

PCICMD - Mirror of PCICMD MAE/BME					
Register Space:	MMIO: 0/2/0				
Size (in bits):	32				
Address:	0912Ch				
DWord	Bit	Description			
0	31:11	Spare			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:
	Access:	R/W			
	_Custom_GTIReset:	BUS			
	10	Interrupt Disable			
<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of an MSI interrupt and blocks the sending of a Line interrupt.(The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of an MSI interrupt or Line interrupt.</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
9	Fast Back to Back				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Not Implemented. Hardwired to 0.</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
8	SERR Enable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Not Implemented. Hardwired to 0.</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
7	Address/Data Stepping Enable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Not Implemented. Hardwired to 0.</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
6	Parity Error Enable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

PCICMD - Mirror of PCICMD MAE/BME

	5	Video Palette Snooping	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	This bit is hardwired to 0 to disable snooping.		
	4	Memory Write and Invalidate Enable	
		Access:	R/W
	_Custom_GTIRreset:	BUS	
Hardwired to 0. The IGD does not support memory write and invalidate commands.			
3	Special Cycle Enable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
This bit is hardwired to 0. The IGD ignores Special cycles.			
2	Bus Primary Enable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
0: Disable IGD bus priming. 1: Enable the IGD to function as a PCI compliant primary. GSA Implementation: When 0, blocks the sending of MSI interrupts. When 1, permits the sending of above. (Note: See descriptions of the INTDIS, MSE, and INTSTS bits.)			
1	Memory Access Enable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.			
0	I/O Access Enable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.			

Mirror of PMR HIGH LIMIT (31-0)

PMRHLIMIT_LSB - Mirror of PMR HIGH LIMIT (31-0)						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	090C0h					
<p>Register to set up the limit address of DMA-protected high-memory region. When the LT CMD.LOCK.PMRC command is invoked, this register is locked (treated as RO). When the LT CMD.UNLOCK.PMRC command is invoked, this register is unlocked (treated as RW). This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as 0 in the Capability register).</p> <p>The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1's to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all 1s.</p> <p>The protected high-memory base & limit registers function as follows. Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size $2^{(N+1)}$ bytes. Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region.</p>						
DWord	Bit	Description				
0	31:20	<p>PMR HIGH LIMIT (LSB - 31:20 of 38:20)</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This register specifies the last host physical address of the DMA-protected high-memory region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.0</p>	Access:	RO	_Custom_GTIReset:	BUS
	Access:	RO				
_Custom_GTIReset:	BUS					
19:0	<p>Spares</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	RO	_Custom_GTIReset:	BUS	
Access:	RO					
_Custom_GTIReset:	BUS					



Mirror of PMR HIGH LIMIT 63-32

PMRHLIMIT_MSB - Mirror of PMR HIGH LIMIT 63-32			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	090C4h		
<p>Register to set up the limit address of DMA-protected high-memory region. When the LT CMD.LOCK.PMRC command is invoked, this register is locked (treated as RO). When the LT CMD.UNLOCK.PMRC command is invoked, this register is unlocked (treated as RW). Refer to Chapter 12 for security considerations.</p> <p>This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as 0 in the Capability register).</p> <p>The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all 1s.</p> <p>The protected high-memory base & limit registers function as follows. Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size $2^{(N+1)}$ bytes. Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region.</p>			
DWord	Bit	Description	
0	31:7	Spares	
		Access:	RO
		_Custom_GTIRreset:	BUS
	6:0	PMR HIGH LIMIT (MSB - 38:32 of 38:20)	
		Access:	RO
		_Custom_GTIRreset:	BUS
		<p>This register specifies the last host physical address of the DMA-protected high-memory region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.</p>	

Mirror of RC0 Hysterisis free

MIRROR_RC0_HYSTERISIS_FREE - Mirror of RC0 Hysterisis free		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00D94h	
Name:	Mirror of RC0 Hysterisis free	
ShortName:	MIRROR_RC0_HYSTERISIS_FREE	
Mirror of RC0 Hysterisis free from OA register DB84h		
DWord	Bit	Description
0	31:0	Count RC0 Hysterisis free
		Access: R/W
		_Custom_GTIRreset: BUS



Mirror RC0 Any Engine Busy Free

MIRROR_RC0_ANY_ENGINE_BUSY_FREE - Mirror RC0 Any Engine Busy Free						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	00D90h					
Name:	Mirror RC0 Any Engine Busy Free					
ShortName:	MIRROR_RC0_ANY_ENGINE_BUSY_FREE					
This register mirrors the count from OA register DB80h						
DWord	Bit	Description				
0	31:0	Count for RC0 Any Engine Busy Free <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
Mirror RC0 Any Engine Busy Free by OA						

Mirror RC0 wake count free

MIRROR_RC0_WAKE_COUNT_FREE - Mirror RC0 wake count free		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00D98h	
Name:	Mirror RC0 wake count free	
ShortName:	MIRROR_RC0_WAKE_COUNT_FREE	
Access:	R/W	
This mirrors the OA register DB88h		
DWord	Bit	Description
0	31:0	Count for RC0 wake count free
		Access: R/W
		_Custom_GTIRreset: BUS



Mirror Rc6 post hysteresis overhead free

MIRROR_RC6_POST_HYSTERISIS_OVERHEAD_FREE - Mirror Rc6 post hysteresis overhead free		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00DA0h	
Name:	Mirror Rc6 post hysteresis overhead free	
ShortName:	MIRROR_RC6_POST_HYSTERISIS_OVERHEAD_FREE	
This is the mirror from OA for register DB90h		
DWord	Bit	Description
0	31:0	Count for Mirror Rc6 post hysteresis overhead free
		Access: R/W
		_Custom_GTIReset: BUS

Mirror rc6 pre Engine wake overhead free

MIRROR_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE - Mirror rc6 pre Engine wake overhead free		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00D9Ch	
Name:	Mirror rc6 pre Engine wake overhead free	
ShortName:	MIRROR_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE	
Mirrors the OA register DB8Ch		
DWord	Bit	Description
0	31:0	Count for rc6 pre Engine wake overhead free
		Access: R/W
		_Custom_GTIReset: BUS

Misc Clocking Reset Control Registers

MISCCPCTL - Misc Clocking Reset Control Registers									
Register Space:	MMIO: 0/2/0								
Size (in bits):	32								
Address:	09424h								
Miscellaneous Clocking / Reset Control Registers									
DWord	Bit	Description							
0	31	clock gate control Lock							
		Access:	R/W Lock						
		_Custom_GTIReset:	BUS						
		0 = Bits of MISCCPCTL register are R/W 1 = All bits of MISCCPCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.							
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>Bits of MISCCPCTL register are R/W</td> </tr> <tr> <td>1</td> <td></td> <td>All bits of MISCCPCTL register are RO (including this lock bit)</td> </tr> </tbody> </table>	Value	Name	Description	0		Bits of MISCCPCTL register are R/W	1
Value	Name	Description							
0		Bits of MISCCPCTL register are R/W							
1		All bits of MISCCPCTL register are RO (including this lock bit)							
30:24		Bonus ECO bits							
		Access:	R/W						
		_Custom_GTIReset:	BUS						
		Bonus ECO bits							
23:20		DOP clock gating enable for VEbox clks							
		Access:	R/W						
		_Custom_GTIReset:	BUS						
		Controls the Enabling of the DOP-level Vebox (cv0clk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled							
19:16		DOP clock gating enable for SFC media clks							
		Access:	R/W						
		_Custom_GTIReset:	BUS						
		Controls the Enabling of the DOP-level SFC (csfclk) Clock Gating in media1 via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled							
15:8		DOP clock gate enable for Media Clocks							
		Access:	R/W						
		_Custom_GTIReset:	BUS						
		Controls the Enabling of the DOP-level Render (cmclk) Clock Gating via PM event messages							

MISCCPCTL - Misc Clocking Reset Control Registers

		<p>1 - Clock gating is enabled 0 - Clock gating is disabled</p>					
	7	<p>DOP clock gating enable for posh clks</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level posh (cposclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						
	6	<p>DOP clock gating enable for Media ampler clks</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level Media sampler (scmsclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						
	5	<p>WIDI1 DOP clock gating enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level Media sampler (cw1clk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						
	4	<p>DOP Clock gating Enable for Widi 0 clks</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						
	3	<p>DOP Clcok gating enable for GUC clks</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level Render (cpclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						
	2	<p>DOP clock gating Enable for Fix clks (cfclk)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W						
_Custom_GTIReset:	BUS						

MISCCPCTL - Misc Clocking Reset Control Registers

1	DOP Clock Gating Enable for Render Clocks	
	Access:	R/W
	_Custom_GTIReset:	BUS
<p>Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages</p> <p>1 - Clock gating is enabled 0 - Clock gating is disabled</p>		
0	Reserved	
	Access:	RO
	Format:	MBZ

MISC CTX control register

MISCCTXCTL - MISC CTX control register				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	0942Ch			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	Context Restore ACk indication from Csunit		
		<table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Context Restore ACk indication from Csunit 1'b1 : Csunit has completed restoring CPunits adress space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits adress space</p>	Access:	R/W Set
Access:	R/W Set			
_Custom_GTIReset:	BUS			



Miscellaneous Message Register 0 for GTI Doorbell Unit

DRBMISC0 - Miscellaneous Message Register 0 for GTI Doorbell Unit			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	01980h		
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>			
DWord	Bit	Description	
0	31:16	Context Save Mask	
		Default Value:	001bh
		Access:	WO
		_Custom_GTIReset:	BUS
	When context save (a read) is in progress, mask is forced to particular value to save off messages that need to be retained across an RC6 event.		
15:7	Reserved		
	Access:	RO	
6	U2CDATPERR		
	Default Value:	0	
	Access:	RO	
	_Custom_GTIReset:	BUS	
A one indicates that Data Parity Error was detected.			
5	U2CADDPERR		
	Default Value:	0	
	Access:	RO	
	_Custom_GTIReset:	BUS	
A one indicates that Address Parity Error was detected.			
4	CV History Bit		
	Access:	R/W Hardware Clear	
	_Custom_GTIReset:	BUS	

DRBMISC0 - Miscellaneous Message Register 0 for GTI Doorbell Unit

		<p>CV History Bit</p> <p>Indicates that doorbell unit should mark all active doorbells as RFO required. Basically it means there may have been some snoops that were missed. RPM writes bit every time CV changes.</p>	
	3	Reserved	
	2	Reserved	
		Access:	RO
		Format:	MBZ
	1	RFO Enable indication from RPM	
		Access:	R/W Hardware Clear
		_Custom_GTIReset:	BUS
		RFO Enable bit from RPM	
		Requires MDRB to handshake with ack	
		Value	Name
		1	Allow RFOs (RPM Enable)
		0	Block RFOs (RPM Disable) [Default]
	0	RFO Enable indication from U2C	
		Access:	R/W Hardware Clear
		_Custom_GTIReset:	BUS
		RFO Enable bit from U2C	
		Requires MDRB to handshake with ack	
		Value	Name
		1	Allow RFOs (Enable)
		0	Block RFOs (Disable) [Default]

Misc Reset Control Register

RSTCTL - Misc Reset Control Register			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09420h		
Miscellaneous reset control registers.			
DWord	Bit	Description	
0	31:4	Reserved	
		Access:	RO
		Format:	MBZ
	3:2	Reset Staggering Period Control	
		Access:	R/W
		_Custom_GTIReset:	BUS
		Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclock staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks	
	1:0	Reset Residency Control	
		Access:	R/W
		_Custom_GTIReset:	BUS
Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks			

MMIO_INDEX

MMIO_INDEX - MMIO_INDEX								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	00000h							
<p>Contains address and target. Punit cannot access IO space from message channel. A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.</p>								
DWord	Bit	Description						
0	31:2	<p>Register_offset</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: right;">00000000h</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: right;">BUS</td> </tr> </table> <p>This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.</p>	Default Value:	00000000h	Access:	R/W	_Custom_GTIRreset:	BUS
	Default Value:	00000000h						
Access:	R/W							
_Custom_GTIRreset:	BUS							
1:0	<p>Target</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: right;">00b</td> </tr> <tr> <td>Access:</td> <td style="text-align: right;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: right;">BUS</td> </tr> </table> <p>00 = MMIO Registers, 01 = GTT, 1X = Reserved</p>	Default Value:	00b	Access:	R/W	_Custom_GTIRreset:	BUS	
Default Value:	00b							
Access:	R/W							
_Custom_GTIRreset:	BUS							

Mode Register for GAB

GAB_MODE - Mode Register for GAB			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIRreset:	DEV		
The GAB_MODE register contains information that controls configurations in the GAB.			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		Format:	Mask
		_Custom_GTIRreset:	DEV
	15:10	Reserved	
		Access:	RO
	9	Reserved	
		Format:	PBC
	8:7	Reserved	
		Format:	PBC
6	6	Disable Hashing on BCS	
		_Custom_GTIRreset:	DEV
	Two command ports (P0 and P1) from BLT to GAM are address hashed. BLB to GAB has two ports and address hashing is done internal to BLB. BCS to GAB is a single command port, and GAB address hashes the BCS requests into P0 and P1.		
	Value	Name	Description
	0b	[Default]	BCS traffic is hashed onto P0 and P1
	1b		BCS traffic is sent only on P0 (no hashing)
	Programming Notes		
	When PendQ hashing control is disabled in GAM BLT Module, BCS hashing in GAB must also be disabled by setting this bit to '1. If this is not followed, there can be memory ordering violations on BCS transactions.		
	5:3	BLB Arbitration Priority	
		Format:	U3
_Custom_GTIRreset:		DEV	
2:0	BCS Arbitration Priority		
	Format:	U3	
	_Custom_GTIRreset:	DEV	

Mode Register for GAC

GAC_MODE - Mode Register for GAC			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	1C00A0h-1C00A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE0		
Address:	1C40A0h-1C40A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE1		
Address:	1D00A0h-1D00A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE2		
Address:	1D40A0h-1D40A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE3		
Address:	1E00A0h-1E00A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE4		
Address:	1E40A0h-1E40A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE5		
Address:	1F00A0h-1F00A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE6		
Address:	1F40A0h-1F40A3h		
Name:	Mode Register for GAC		
ShortName:	GAC_MODE_VCSUNIT_BE7		
The GAC_MODE register contains information that controls configurations in the GAC.			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		Format:	Mask
		_Custom_GTIRreset:	BUS

GAC_MODE - Mode Register for GAC				
15:1	Reserved			
	Access:	RO		
	Format:	MBZ		
	0	GACunit VCS Fence Performance fix Override		
		Format:	Disable	
		_Custom_GTIReset:	BUS	
		Value	Name	Description
		0	[Default]	Performance fix enabled to block client credits until VCS fence advances.
	1		Performance fix to block credits until VCS fence advances, disabled . Fence will not block input traffic from clients and will advance only after ingress FIFOs are empty (Legacy behavior.)	

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
_Custom_GTIReset:	DEV				
Address:	0212Ch				
DWord	Bit	Description			
0	31:16	Mask Bits			
		<table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table> <p>Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.</p>	Access:	WO	Format:
	Access:	WO			
	Format:	Mask			
	15:13	Reserved			
Format: PBC					
12:11	CLR0 clients ROB low priority threshold Control				
	This bit field is used to control the threshold at which CLR0 clients will move to the low priority group in the GAFS ROB arbiter.				
	Value	Name Description			
	00b	[Default] Low priority threshold value = 'd12			
	01b	Low priority threshold value = 'd24			
10b	Low priority threshold value = 'd36				
11b	Low priority threshold value = 'd48				
10	Reserved				
	Format: PBC				
9	Min Alloc Configuration				
	<p>This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [2] of this register.</p> <p>{Bit[9], Bit[2]} = 2'b00 : Original values {Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 : Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values</p> <table border="1"> <thead> <tr> <th colspan="2">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">This bit must be programmed to 1 for achieving performance targets.</td> </tr> </tbody> </table>	Programming Notes		This bit must be programmed to 1 for achieving performance targets.	
Programming Notes					
This bit must be programmed to 1 for achieving performance targets.					
8:3	Reserved				
	Format: PBC				

GAFS_MODE - Mode Register for GAFS					
2	<p>Min Alloc Configuration control0</p> <p>This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [9] of this register.</p> <p>{Bit[9], Bit[2]} = 2'b00 : Original values {Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 :Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2" style="text-align: center; background-color: #e6f2ff;">Programming Notes</th> </tr> <tr> <td colspan="2">This bit must be programmed to 0 for achieving performance targets.</td> </tr> </table>	Programming Notes		This bit must be programmed to 0 for achieving performance targets.	
Programming Notes					
This bit must be programmed to 0 for achieving performance targets.					
1:0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">PBC</td> </tr> </table>	Format:	PBC		
Format:	PBC				

Mode Register for Software Interface

MI_MODE - Mode Register for Software Interface	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0209Ch-0209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_RCSUNIT
Address:	1809Ch-1809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_POCSUNIT
Address:	2209Ch-2209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_BCSUNIT
Address:	1C009Ch-1C009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT0
Address:	1C409Ch-1C409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT1
Address:	1C809Ch-1C809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT0
Address:	1D009Ch-1D009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT2
Address:	1D409Ch-1D409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT3
Address:	1D809Ch-1D809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT1
Address:	1E009Ch-1E009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT4

MI_MODE - Mode Register for Software Interface

Address: 1E409Ch-1E409Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_VCSUNIT5

Address: 1E809Ch-1E809Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_VECSUNIT2

Address: 1F009Ch-1F009Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_VCSUNIT6

Address: 1F409Ch-1F409Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_VCSUNIT7

Address: 1F809Ch-1F809Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_VECSUNIT3

Address: 1A09Ch-1A09Fh
 Name: Mode Register for Software Interface
 ShortName: MI_MODE_CCSUNIT0

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description											
0	31:16	Mask <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table> <p>A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0</p>	Access:	WO	Format:	Mask							
		Access:	WO										
Format:	Mask												
15		Suspend Flush <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>U1</td> </tr> </table> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>No Delay [Default]</td> <td>HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>Delay Flush</td> <td>Suspend flush is active</td> </tr> </tbody> </table>	Format:	U1	Value	Name	Description	0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well	1h	Delay Flush	Suspend flush is active
		Format:	U1										
		Value	Name	Description									
		0h	No Delay [Default]	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well									
		1h	Delay Flush	Suspend flush is active									
Programming Notes													
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO													

MI_MODE - Mode Register for Software Interface

14	RCS POSH LRCA Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Exists If:</td> <td>//RCS</td> </tr> </table> <p>This bit controls the context save of the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the RCS context image. This primary purpose of this bit is for backward compatibility for the render context image.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td></td> <td>RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA in context image as NOOPs.</td> </tr> <tr> <td style="text-align: center;">0</td> <td>[Default]</td> <td>RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the context image.</td> </tr> </tbody> </table>	Source:	RenderCS	Exists If:	//RCS	Value	Name	Description	1		RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA in context image as NOOPs.	0	[Default]	RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the context image.
Source:	RenderCS														
Exists If:	//RCS														
Value	Name	Description													
1		RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA in context image as NOOPs.													
0	[Default]	RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the context image.													
13	Disable MI_SET_CONTEXT for Execution List	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>U1</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 10%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>Allow [Default]</td> <td>Allow MI_SET_CONTEXT in Execlist mode</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>Disable</td> <td>Disable MI_SET_CONTEXT in Execlist Mode</td> </tr> </tbody> </table>	Format:	U1	Value	Name	Description	0h	Allow [Default]	Allow MI_SET_CONTEXT in Execlist mode	1h	Disable	Disable MI_SET_CONTEXT in Execlist Mode		
Format:	U1														
Value	Name	Description													
0h	Allow [Default]	Allow MI_SET_CONTEXT in Execlist mode													
1h	Disable	Disable MI_SET_CONTEXT in Execlist Mode													
12	Nested Batch Buffer Enable	<p>This bit is used to enable or disable third level batch buffer and associated functionality.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>[Default]</td> <td>HW will only support first level, second level, chained first level and chained second level batch buffer. Nested Level Batch Buffer field must be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer as a chained second level batch buffer.</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>HW will support first level, second level, third level, chained first level, chained second level and chained third level batch buffer. Nested Level Batch Buffer field must not be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer a chained second level batch buffer and similarly for chained third level batch buffer.</td> </tr> </tbody> </table> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p style="text-align: center; color: #0070c0; font-weight: bold;">Programming Notes</p> <p>This bit must be only programmed from a ring buffer and must not be programmed from a batch buffer.</p> <p>This bit must be static for a given context and remain same through out the life time of a given context.</p> </div>	Value	Name	Description	0	[Default]	HW will only support first level, second level, chained first level and chained second level batch buffer. Nested Level Batch Buffer field must be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer as a chained second level batch buffer.	1		HW will support first level, second level, third level, chained first level, chained second level and chained third level batch buffer. Nested Level Batch Buffer field must not be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer a chained second level batch buffer and similarly for chained third level batch buffer.				
Value	Name	Description													
0	[Default]	HW will only support first level, second level, chained first level and chained second level batch buffer. Nested Level Batch Buffer field must be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer as a chained second level batch buffer.													
1		HW will support first level, second level, third level, chained first level, chained second level and chained third level batch buffer. Nested Level Batch Buffer field must not be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer a chained second level batch buffer and similarly for chained third level batch buffer.													
11	Invalidate UHPTR enable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%;">Source:</td> <td>RenderCS, VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> <tr> <td>Exists If:</td> <td>//RCS, VCS, VECS, BCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.</p>	Source:	RenderCS, VideoCS, VideoCS2, VideoEnhancementCS	Exists If:	//RCS, VCS, VECS, BCS	Format:	Enable							
Source:	RenderCS, VideoCS, VideoCS2, VideoEnhancementCS														
Exists If:	//RCS, VCS, VECS, BCS														
Format:	Enable														

MI_MODE - Mode Register for Software Interface

10	Atomic Read Return for MI_COPY_MEM_MEM	
Format:		U1
Value	Name	Description
0h	Disable [Default]	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.
9	Rings Idle	
Format:		U1
Read Only Status bit		
Value	Name	Description
0h	Not Idle [Default]	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.
Programming Notes		
Writes to this bit are not allowed.		
8	Stop Rings	
Format:		U1
Value	Name	Description
0h	[Default]	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.
Programming Notes		
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.		
Software must clear this bit for Rings to resume normal operation.		
7:5	Reserved	
Format:		PBC
4:2	Reserved	
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	
Format:	PBC	
4:1	Predicate Enable	
Source:	RenderCS, PositionCS	
This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.		

MI_MODE - Mode Register for Software Interface

Value	Name	Description
0h	Predicate Disable	Predication is Disabled and RCS will process commands as usual.
1h	Predicate on Result2 clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
2h	Predicate on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
3h	Predicate on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
4h	Predicate on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
5h	Predicate when two or more slices enabled	Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
6h	Predicate when one or three slices enabled	Following Commands will be Executed by RCS only when two slices are enabled, NOOPED when one or three slices are enabled.
7h	Predicate when one or two slices enabled	Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
Bh	NOOP in RenderCS	When RenderCS parses MI_SET_PREDICATE command with Predicate Enable set to NOOP in RenderCS, RenderCS NOOPs all the subsequent commands parsed unconditionally until the predication is disabled/modified using MI_SET_PREDICATE command. Other command streamers (non RenderCS) on parsing MI_SET_PREDICATE command with Predicate Enable set to NOOP in RenderCS dont take any action and is equivalent to parsing MI_NOOP command.
Ch	NOOP in PositionCS	When PositionCS parses MI_SET_PREDICATE command with Predicate Enable set to NOOP in PositionCS, PositionCS NOOPs all the subsequent commands parsed unconditionally until the predication is disabled/modified using MI_SET_PREDICATE command. Other command streamers (non PositionCS) on parsing MI_SET_PREDICATE command with Predicate Enable set to NOOP in PositionCS dont take any action and is equivalent to parsing MI_NOOP command.
8h, 9h, Ah	Reserved	
Dh, Eh	Reserved	
Fh	Predicate Always	Following Commands will be NOOPED by RCS unconditionally.

MI_MODE - Mode Register for Software Interface

Programming Notes				
SW must use MI_SET_PREDICATE instead of MMIO access.				
1	Reserved			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Source:</td> <td>VideoCS, VideoCS2, VideoEnhancementCS</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Source:	VideoCS, VideoCS2, VideoEnhancementCS	Format:
Source:	VideoCS, VideoCS2, VideoEnhancementCS			
Format:	PBC			
1	Reserved			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Source:</td> <td>BlitterCS</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Source:	BlitterCS	Format:
Source:	BlitterCS			
Format:	PBC			
0	Reserved			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Source:</td> <td>CommandStreamer</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Source:	CommandStreamer	Format:
Source:	CommandStreamer			
Format:	PBC			

MSI Mask Bits

MSI_MASK_0_2_0_PCI - MSI Mask Bits				
Register Space:	PCI: 0/2/0			
Size (in bits):	32			
Address:	000B8h			
This register contains the MSI Mask Bits				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	Mask Bit for Vector 0		
		Default Value:	0b	
		Access:	R/W	
		_Custom_GTIReset:	BUS	
For each Mask bit that is set, the function is prohibited from sending the associated message.				



MSI Pending Bits

MSI_PEND_0_2_0_PCI - MSI Pending Bits								
Register Space:	PCI: 0/2/0							
Size (in bits):	32							
Address:	000BCh							
This register contains the MSI Pending Bits								
DWord	Bit	Description						
0	31:1	Reserved						
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
0	0	Pending Bit for Vector 0						
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>RO Variant</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table>	Default Value:	0b	Access:	RO Variant	_Custom_GTIRreset:	BUS
		Default Value:	0b					
		Access:	RO Variant					
_Custom_GTIRreset:	BUS							
<p>For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.</p>								

Multi Context Control Register

MLTICTXCTL - Multi Context Control Register			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	0B170h		
Masked register for Multi Context			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		Format:	Mask
			Mask bits for each corresponding bit in [15:0]
	15	AID for RCS AID0: The AID value for QID = 0	
	14	AID for CCS AID1: The AID value for QID = 1	
	13:4	Reserved	
Access:		RO	
	Format:	MBZ	
	3	Reserved	
Access:		RO	
	Format:	MBZ	
	2	3D on Render 3D_ON_RENDER: When set, the L3 will use Render config values, else compute config values.	
1:0	Multi Context Enable This Mode enables dual queues to execute on the machine: 1 RCS + 1 CCS If set, then L3 will carve out 4KB of URB per bank for CCS usage. Reserved: 10b, 11b		
	Value	Name	
	0	RCS only enabled [Default]	
	1	RCS and CCS enabled	



Multi Size Aperture Control

MSAC_0_2_0_PCI - Multi Size Aperture Control				
Register Space:	PCI: 0/2/0			
Size (in bits):	32			
Address:	00060h			
Description				
<p>This register contains MSAC register which determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register.</p> <p>Bits [20:16] 00000b: 128MB, GMADR[26:4] is hardwired to all 0 Bits [20:16] 00001b: 256MB, GMADR[27:4] overridden to all 0 Bits [20:16] 00010b: illegal (hardware will treat this as 00011b) Bits [20:16] 00011b: 512MB, GMADR[28:27] overridden to all 0 Bits [20:16] 00100-00110b: illegal (hardware will treat this as 00111b) Bits [20:16] 00111b: 1024MB, GMADR[29:27] overridden to all 0 Bits [20:16] 01000-01110b: illegal (hardware will treat this as 01111b) Bits [20:16] 01111b: 2048MB, GMADR[30:27] overridden to all 0 Bits [20:16] 10000-11110b: illegal (hardware will treat this as 11111b) Bits [20:16] 11111b: 4096MB, GMADR[31:27] overridden to all 0</p>				
DWord	Bit	Description		
0	31:21	Reserved R/W		
		Default Value:	000h	
		Access:	R/W	
		_Custom_GTIReset:	BUS	
	Scratch Bits			
	20	Untrusted Aperture Size Bit 4		
		Default Value:	0b	
		Access:	R/W Key	
	19	Untrusted Aperture Size Bit 3		
		Default Value:	0b	
		Access:	R/W Key	
	18	Untrusted Aperture Size Bit 2		
		Default Value:	0b	
		Access:	R/W Key	
			_Custom_GTIReset:	BUS

MSAC_0_2_0_PCI - Multi Size Aperture Control				
	17	Untrusted Aperture Size Bit 1		
		Default Value: 0b		
		Access: R/W Key		
			_Custom_GTIRreset: BUS	
	16	Untrusted Aperture Size Bit 0		
		Access: R/W Key		
		_Custom_GTIRreset: BUS		
		Value	Name	Description
		0b	[Default]	
	15:0	Reserved		
Access: RO				
Format: MBZ				



NDE_RSTWRN_OPT

NDE_RSTWRN_OPT			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	46408h-4640Bh		
Name:	North Display Reset Warn Options		
ShortName:	NDE_RSTWRN_OPT		
Reset:	global		
This register is used to control the display behavior on receiving a Reset Warning or FLR.			
DWord	Bit	Description	
0	31:7	Reserved	
		Access:	RO
		Format:	MBZ
	6	Reserved	
		Access:	RO
		Format:	MBZ
	5	Reserved	
	4	RST PCH Handshake En	
		This field enables the handshake with south display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset.	
		Value	Name
		0b	Disable
		1b	Enable
Programming Notes			
This must be programmed as part of the display initialization sequence.			
3:0	Reserved		
	Access:	RO	
	Format:	MBZ	

NONPIPE_ISOCREQ

NONPIPE_ISOCREQ										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	64									
Address:	45230h-45237h									
Name:	Non Pipe Isoch Request									
ShortName:	NONPIPE_ISOCREQ									
Reset:	soft									
<p>This register is used to trigger an IsocReq that is not associated with a pipe. When enabled, the write to DWord 1 (higher address DWord) of this register triggers an IsocReq to be sent with the last written values from both DWords.</p>										
DWord	Bit	Description								
0	31:16	LTR <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field specifies the latency tolerance (LTR) in microseconds.</p>	Access:	R/W						
	Access:	R/W								
15:0	Bandwidth <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field specifies the bandwidth requirement in multiples of 100 MB/s.</p>	Access:	R/W							
Access:	R/W									
1	31	Enable <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field enables IsocReq to be sent when DWord 1 of this register is written.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Enable</td> </tr> <tr> <td>0b</td> <td>Disable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	1b	Enable	0b	Disable
		Access:	R/W							
		Value	Name							
	1b	Enable								
0b	Disable									
30:8	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
Access:	RO									
Format:	MBZ									
7:0	Delay <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field specifies the downwards transition delay in milliseconds.</p>	Access:	R/W							
Access:	R/W									



NOP Identification Register

NOPID - NOP Identification Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02094h-02097h
Name:	NOP Identification Register
ShortName:	NOPID_RCSUNIT
Address:	18094h-18097h
Name:	NOP Identification Register
ShortName:	NOPID_POCSUNIT
Address:	22094h-22097h
Name:	NOP Identification Register
ShortName:	NOPID_BCSUNIT
Address:	1C0094h-1C0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT0
Address:	1C4094h-1C4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT1
Address:	1C8094h-1C8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT0
Address:	1D0094h-1D0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT2
Address:	1D4094h-1D4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT3
Address:	1D8094h-1D8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT1
Address:	1E0094h-1E0097h
Name:	NOP Identification Register

NOPID - NOP Identification Register

ShortName:	NOPID_VCSUNIT4
Address:	1E4094h-1E4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT5
Address:	1E8094h-1E8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT2
Address:	1F0094h-1F0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT6
Address:	1F4094h-1F4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT7
Address:	1F8094h-1F8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT3
Address:	1A094h-1A097h
Name:	NOP Identification Register
ShortName:	NOPID_CCSUNIT0

The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.

DWord	Bit	Description				
0	31:22	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
	21:0	Reserved				



Number Of VFs

SRIOV_NUMOFVFS_0_2_0_PCI - Number Of VFs			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00330h		
Number of VFs enabled by the VMM.			
DWord	Bit	Description	
0	31:24	Reserved	
		Access:	RO
		Format:	MBZ
	23:16	Function Dependency Link	
		Default Value:	00000000b
		Access:	RO
		_Custom_GTIReset:	BUS
		Same value as the Physical function number indicating no Dependency	
	15:0	Number of Virtual Functions	
		Default Value:	0000000000000000b
		Access:	R/W
		_Custom_GTIReset:	BUS
System SW shall set this field to control the number of VFs that are visible. This field must be programmed before setting VF Enable. Changing this field when VF Enable is set will produced undefined behavior as per the SR-IOV specification. HW will ignore the new value programmed.			

OAC Aggregate Perf Counter A0

OAC_OAPERF_A0 - OAC Aggregate Perf Counter A0										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
This register reflects the count value of the OA Performance counter A0.										
DWord	Bit	Description								
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0x00000000</td> <td>[Default]</td> </tr> <tr> <td>[0x00000001-0xFFFFFFFF]</td> <td></td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	0x00000000	[Default]	[0x00000001-0xFFFFFFFF]	
_Custom_GTIRreset:	DEV									
Value	Name									
0x00000000	[Default]									
[0x00000001-0xFFFFFFFF]										



OAC Aggregate Perf Counter A0 Upper DWord

OAC_OAPERF_A0_UPPER - OAC Aggregate Perf Counter A0 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A4

OAC_OAPERF_A4 - OAC Aggregate Perf Counter A4				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A4 Upper DWord

OAC_OAPERF_A4_UPPER - OAC Aggregate Perf Counter A4 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A4 to be read. .Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32of the live performance counter value when read..Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A7

OAC_OAPERF_A7 - OAC Aggregate Perf Counter A7				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A7 Upper DWord

OAC_OAPERF_A7_UPPER - OAC Aggregate Perf Counter A7 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A8

OAC_OAPERF_A8 - OAC Aggregate Perf Counter A8				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A8 Upper DWord

OAC_OAPERF_A8_UPPER - OAC Aggregate Perf Counter A8 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A9

OAC_OAPERF_A9 - OAC Aggregate Perf Counter A9				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAC Aggregate Perf Counter A9 Upper DWord

OAC_OAPERF_A9_UPPER - OAC Aggregate Perf Counter A9 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A10

OAC_OAPERF_A10 - OAC Aggregate Perf Counter A10				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A10 Upper DWord

OAC_OAPERF_A10_UPPER - OAC Aggregate Perf Counter A10 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A11

OAC_OAPERF_A11 - OAC Aggregate Perf Counter A11				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A11 Upper DWord

OAC_OAPERF_A11_UPPER - OAC Aggregate Perf Counter A11 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A12

OAC_OAPERF_A12 - OAC Aggregate Perf Counter A12				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A12 Upper DWord

OAC_OAPERF_A12_UPPER - OAC Aggregate Perf Counter A12 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A13

OAC_OAPERF_A13 - OAC Aggregate Perf Counter A13				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A13 Upper DWord

OAC_OAPERF_A13_UPPER - OAC Aggregate Perf Counter A13 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A14

OAC_OAPERF_A14 - OAC Aggregate Perf Counter A14				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A14 Upper DWord

OAC_OAPERF_A14_UPPER - OAC Aggregate Perf Counter A14 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>__Custom_GTIReset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	__Custom_GTIReset:	DEV
Format:	U32					
__Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A15

OAC_OAPERF_A15 - OAC Aggregate Perf Counter A15				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A15 Upper DWord

OAC_OAPERF_A15_UPPER - OAC Aggregate Perf Counter A15 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A16

OAC_OAPERF_A16 - OAC Aggregate Perf Counter A16				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A16 Upper DWord

OAC_OAPERF_A16_UPPER - OAC Aggregate Perf Counter A16 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A17

OAC_OAPERF_A17 - OAC Aggregate Perf Counter A17				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A17 Upper DWord

OAC_OAPERF_A17_UPPER - OAC Aggregate Perf Counter A17 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A18

OAC_OAPERF_A18 - OAC Aggregate Perf Counter A18				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A18 Upper DWord

OAC_OAPERF_A18_UPPER - OAC Aggregate Perf Counter A18 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A19

OAC_OAPERF_A19 - OAC Aggregate Perf Counter A19				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A19 Upper DWord

OAC_OAPERF_A19_UPPER - OAC Aggregate Perf Counter A19 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A20

OAC_OAPERF_A20 - OAC Aggregate Perf Counter A20				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A20 Upper DWord

OAC_OAPERF_A20_UPPER - OAC Aggregate Perf Counter A20 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A28

OAC_OAPERF_A28 - OAC Aggregate Perf Counter A28				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A28 Upper DWord

OAC_OAPERF_A28_UPPER - OAC Aggregate Perf Counter A28 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A29

OAC_OAPERF_A29 - OAC Aggregate Perf Counter A29				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A29 Upper DWord

OAC_OAPERF_A29_UPPER - OAC Aggregate Perf Counter A29 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A30

OAC_OAPERF_A30 - OAC Aggregate Perf Counter A30				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAC Aggregate Perf Counter A30 Upper DWord

OAC_OAPERF_A30_UPPER - OAC Aggregate Perf Counter A30 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A31

OAC_OAPERF_A31 - OAC Aggregate Perf Counter A31						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register reflects the count value of the OA Performance counter A31						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC Aggregate Perf Counter A31 Upper DWord

OAC_OAPERF_A31_UPPER - OAC Aggregate Perf Counter A31 Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>__Custom_GTIReset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	__Custom_GTIReset:	DEV
Format:	U32					
__Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A32

OAC_OAPERF_A32 - OAC Aggregate Perf Counter A32						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register reflects the count value of the OA Performance counter A32						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OACAggregatePerfCounterA32UpperDWord

OAC_OAPERF_A32_UPPER - OACAggregatePerfCounterA32UpperDWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A32 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Aggregate Perf Counter A33

OAC_OAPERF_A33 - OAC Aggregate Perf Counter A33						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register reflects the count value of the OA Performance counter A33						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					



OACAggregatePerfCounterA33UpperDWord

OAC_OAPERF_A33_UPPER - OACAggregatePerfCounterA33UpperDWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A33 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A34

OAC_OAPERF_A34 - OAC Aggregate Perf Counter A34						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register reflects the count value of the OA Performance counter A34						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OACAggregatePerfCounterA34UpperDWord

OAC_OAPERF_A34_UPPER - OACAggregatePerfCounterA34UpperDWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register enables the current live value of performance counter A34 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAC Aggregate Perf Counter A35

OAC_OAPERF_A35 - OAC Aggregate Perf Counter A35						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
This register reflects the count value of the OA Performance counter A35						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OACAggregatePerfCounterA35UpperDWord

OAC_OAPERF_A35_UPPER - OACAggregatePerfCounterA35UpperDWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter A35 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Boolean_Counter_B0

OAC_OAPERF_B0 - OAC Boolean_Counter_B0						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC Boolean_Counter_B1

OAC_OAPERF_B1 - OAC Boolean_Counter_B1						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Boolean_Counter_B2

OAC_OAPERF_B2 - OAC Boolean_Counter_B2						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC Boolean_Counter_B3

OAC_OAPERF_B3 - OAC Boolean_Counter_B3						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Boolean_Counter_B4

OAC_OAPERF_B4 - OAC Boolean_Counter_B4						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC Boolean_Counter_B5

OAC_OAPERF_B5 - OAC Boolean_Counter_B5						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC Boolean_Counter_B6

OAC_OAPERF_B6 - OAC Boolean_Counter_B6						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC Boolean_Counter_B7

OAC_OAPERF_B7 - OAC Boolean_Counter_B7						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAC GPU Ticks Counter

OAC_GPU_TICKS - OAC GPU Ticks Counter						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAC GPU Ticks Counter Upper DWord

OAC_GPU_TICKS_UPPER - OAC GPU Ticks Counter Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.		
DWord	Bit	Description
0	31:0	Upper Value
		Format: U32
		_Custom_GTIReset: DEV
This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.		

OAC Observation Architecture Control

OAC_OACONTROL - OAC Observation Architecture Control			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
This register controls OAC functionality, report format, and context filtering. If OAC is enabled then it should be enabled in CS as well			
DWord	Bit	Description	
0	31:4	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	3:1	Counter Select	
		_Custom_GTIRreset:	DEV
	This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.		
	0	Performance Counter Enable	
		Format:	Enable
		_Custom_GTIRreset:	DEV
		Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.	
Programming Notes			
"OAC Context Enable" mode bit in RenderEngne CTX_SR_CTL register must be set when "Programmer Counter Enable" is set.			



OAC Observation Architecture Status Register

OAC_OASTATUS - OAC Observation Architecture Status Register									
Register Space:	MMIO: 0/2/0								
Access:	R/W								
Size (in bits):	32								
<p>This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)</p>									
DWord	Bit	Description							
0	31:22	Reserved							
		Format:	PBC						
		_Custom_GTIReset:	DEV						
	21		Start Trigger Flag 1						
			_Custom_GTIReset:	DEV					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1	
		Value	Name						
		0	[Default]						
		1							
	<p style="text-align: center;">Programming Notes</p> <p>This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.</p>								
	20		Start Trigger Flag 2						
			_Custom_GTIReset:	DEV					
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1			
Value		Name							
0		[Default]							
1									
<p style="text-align: center;">Programming Notes</p> <p>This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.</p>									
19		Report Trigger Flag 1							
		_Custom_GTIReset:	DEV						
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1		
	Value	Name							
0	[Default]								
1									

OAC_OASTATUS - OAC Observation Architecture Status Register

Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.		
18	Report Trigger Flag 2	
	_Custom_GTIRreset:	DEV
	Value	Name
	0	[Default]
1		
Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.		
17:6	Reserved	
	Format:	PBC
	_Custom_GTIRreset:	DEV
5:2	Reserved	
	Format:	PBC
	_Custom_GTIRreset:	DEV
1	Accumulator Overflow	
	_Custom_GTIRreset:	DEV
	This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.	
	Value	Name
0	[Default]	No overflow has occurred.
1		Overflow has occurred.
0	Counter Overflow	
	_Custom_GTIRreset:	DEV
	This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 1 to it.	
	Value	Name
0	[Default]	Counter Overflow not occurred
1		Counter Overflow occurred



OAG Aggregate Perf Counter A0

OAG_OAPERF_A0 - OAG Aggregate Perf Counter A0										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	0D980h									
This register reflects the count value of the OA Performance counter A0.										
DWord	Bit	Description								
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0x00000000</td> <td>[Default]</td> </tr> <tr> <td>[0x00000001-0xFFFFFFFF]</td> <td></td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	0x00000000	[Default]	[0x00000001-0xFFFFFFFF]	
_Custom_GTIRreset:	DEV									
Value	Name									
0x00000000	[Default]									
[0x00000001-0xFFFFFFFF]										

OAG Aggregate Perf Counter A0 Upper DWord

OAG_OAPERF_A0_UPPER - OAG Aggregate Perf Counter A0 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D984h		
<p>This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A1

OAG_OAPERF_A1 - OAG Aggregate Perf Counter A1				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D988h			
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A1 Upper DWord

OAG_OAPERF_A1_UPPER - OAG Aggregate Perf Counter A1 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D98Ch	
<p>This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAG Aggregate Perf Counter A2

OAG_OAPERF_A2 - OAG Aggregate Perf Counter A2				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D990h			
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A2 Upper DWord

OAG_OAPERF_A2_UPPER - OAG Aggregate Perf Counter A2 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D994h		
<p>This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A3

OAG_OAPERF_A3 - OAG Aggregate Perf Counter A3				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D998h			
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A3 Upper DWord

OAG_OAPERF_A3_UPPER - OAG Aggregate Perf Counter A3 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D99Ch		
<p>This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A4

OAG_OAPERF_A4 - OAG Aggregate Perf Counter A4				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9A0h			
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A4 Lower DWord Free

OAG_OAPERF_A4_LOWER_FREE - OAG Aggregate Perf Counter A4 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DAD4h			
<p>This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Aggregate Perf Counter A4 Upper DWord

OAG_OAPERF_A4_UPPER - OAG Aggregate Perf Counter A4 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9A4h		
<p>This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			

OAG Aggregate Perf Counter A4 Upper DWord Free

OAG_OAPERF_A4_UPPER_FREE - OAG Aggregate Perf Counter A4 Upper DWord Free		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DAD8h	
<p>This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
		_Custom_GTIRreset: DEV
	7:0	Upper Value
Format: U8		
_Custom_GTIRreset: DEV		
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAG Aggregate Perf Counter A5

OAG_OAPERF_A5 - OAG Aggregate Perf Counter A5				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9A8h			
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A5 Upper DWord

OAG_OAPERF_A5_UPPER - OAG Aggregate Perf Counter A5 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9ACh	
<p>This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAG Aggregate Perf Counter A6

OAG_OAPERF_A6 - OAG Aggregate Perf Counter A6				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9B0h			
This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A6 Lower DWord Free

OAG_OAPERF_A6_LOWER_FREE - OAG Aggregate Perf Counter A6 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DADCh			
<p>This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Aggregate Perf Counter A6 Upper DWord

OAG_OAPERF_A6_UPPER - OAG Aggregate Perf Counter A6 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9B4h		
<p>This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			

OAG Aggregate Perf Counter A6 Upper DWord Free

OAG_OAPERF_A6_UPPER_FREE - OAG Aggregate Perf Counter A6 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DAE0h		
<p>This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A7

OAG_OAPERF_A7 - OAG Aggregate Perf Counter A7				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9B8h			
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A7 Upper DWord

OAG_OAPERF_A7_UPPER - OAG Aggregate Perf Counter A7 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9BCh		
<p>This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A8

OAG_OAPERF_A8 - OAG Aggregate Perf Counter A8				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9C0h			
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A8 Upper DWord

OAG_OAPERF_A8_UPPER - OAG Aggregate Perf Counter A8 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9C4h		
<p>This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A9

OAG_OAPERF_A9 - OAG Aggregate Perf Counter A9				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9C8h			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A9 Upper DWord

OAG_OAPERF_A9_UPPER - OAG Aggregate Perf Counter A9 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9CCh		
<p>This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A10

OAG_OAPERF_A10 - OAG Aggregate Perf Counter A10				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9D0h			
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A10 Upper DWord

OAG_OAPERF_A10_UPPER - OAG Aggregate Perf Counter A10 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9D4h		
<p>This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A11

OAG_OAPERF_A11 - OAG Aggregate Perf Counter A11				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9D8h			
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A11 Upper DWord

OAG_OAPERF_A11_UPPER - OAG Aggregate Perf Counter A11 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D9DCh				
<p>This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAG Aggregate Perf Counter A12

OAG_OAPERF_A12 - OAG Aggregate Perf Counter A12				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9E0h			
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A12 Upper DWord

OAG_OAPERF_A12_UPPER - OAG Aggregate Perf Counter A12 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9E4h		
<p>This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A13

OAG_OAPERF_A13 - OAG Aggregate Perf Counter A13				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9E8h			
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A13 Upper DWord

OAG_OAPERF_A13_UPPER - OAG Aggregate Perf Counter A13 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D9ECh		
<p>This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A14

OAG_OAPERF_A14 - OAG Aggregate Perf Counter A14				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9F0h			
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A14 Upper DWord

OAG_OAPERF_A14_UPPER - OAG Aggregate Perf Counter A14 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D9F4h				
<p>This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAG Aggregate Perf Counter A15

OAG_OAPERF_A15 - OAG Aggregate Perf Counter A15				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D9F8h			
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A15 Upper DWord

OAG_OAPERF_A15_UPPER - OAG Aggregate Perf Counter A15 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9FCh	
<p>This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAG Aggregate Perf Counter A16

OAG_OAPERF_A16 - OAG Aggregate Perf Counter A16				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA00h			
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A16 Upper DWord

OAG_OAPERF_A16_UPPER - OAG Aggregate Perf Counter A16 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA04h		
<p>This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIReset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIReset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A17

OAG_OAPERF_A17 - OAG Aggregate Perf Counter A17				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA08h			
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A17 Upper DWord

OAG_OAPERF_A17_UPPER - OAG Aggregate Perf Counter A17 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA0Ch		
<p>This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A18

OAG_OAPERF_A18 - OAG Aggregate Perf Counter A18				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA10h			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A18 Upper DWord

OAG_OAPERF_A18_UPPER - OAG Aggregate Perf Counter A18 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA14h		
<p>This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A19

OAG_OAPERF_A19 - OAG Aggregate Perf Counter A19				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA18h			
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A19 Lower DWord Free

OAG_OAPERF_A19_LOWER_FREE - OAG Aggregate Perf Counter A19 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DAE4h			
<p>This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG Aggregate Perf Counter A19 Upper DWord

OAG_OAPERF_A19_UPPER - OAG Aggregate Perf Counter A19 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA1Ch		
<p>This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			

OAG Aggregate Perf Counter A19 Upper DWord Free

OAG_OAPERF_A19_UPPER_FREE - OAG Aggregate Perf Counter A19 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DAE8h		
<p>This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A20

OAG_OAPERF_A20 - OAG Aggregate Perf Counter A20				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA20h			
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A20 Lower DWord Free

OAG_OAPERF_A20_LOWER_FREE - OAG Aggregate Perf Counter A20 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DAECh			
<p>This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Aggregate Perf Counter A20 Upper DWord

OAG_OAPERF_A20_UPPER - OAG Aggregate Perf Counter A20 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA24h		
<p>This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			

OAG Aggregate Perf Counter A20 Upper DWord Free

OAG_OAPERF_A20_UPPER_FREE - OAG Aggregate Perf Counter A20 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DAF0h		
<p>This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A21

OAG_OAPERF_A21 - OAG Aggregate Perf Counter A21				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA28h			
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A21 Upper DWord

OAG_OAPERF_A21_UPPER - OAG Aggregate Perf Counter A21 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DA2Ch				
<p>This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAG Aggregate Perf Counter A22

OAG_OAPERF_A22 - OAG Aggregate Perf Counter A22				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA30h			
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter A22 Upper DWord

OAG_OAPERF_A22_UPPER - OAG Aggregate Perf Counter A22 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA34h		
<p>This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A23

OAG_OAPERF_A23 - OAG Aggregate Perf Counter A23				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA38h			
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A23 Upper DWord

OAG_OAPERF_A23_UPPER - OAG Aggregate Perf Counter A23 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA3Ch	
<p>This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAG Aggregate Perf Counter A24

OAG_OAPERF_A24 - OAG Aggregate Perf Counter A24				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA40h			
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A24 Upper DWord

OAG_OAPERF_A24_UPPER - OAG Aggregate Perf Counter A24 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA44h		
<p>This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A25

OAG_OAPERF_A25 - OAG Aggregate Perf Counter A25				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA48h			
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A25 Upper DWord

OAG_OAPERF_A25_UPPER - OAG Aggregate Perf Counter A25 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA4Ch		
<p>This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A26

OAG_OAPERF_A26 - OAG Aggregate Perf Counter A26				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA50h			
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A26 Upper DWord

OAG_OAPERF_A26_UPPER - OAG Aggregate Perf Counter A26 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DA54h				
<p>This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAG Aggregate Perf Counter A27

OAG_OAPERF_A27 - OAG Aggregate Perf Counter A27				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA58h			
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A27 Upper DWord

OAG_OAPERF_A27_UPPER - OAG Aggregate Perf Counter A27 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA5Ch		
<p>This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A28

OAG_OAPERF_A28 - OAG Aggregate Perf Counter A28				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA60h			
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A28 Upper DWord

OAG_OAPERF_A28_UPPER - OAG Aggregate Perf Counter A28 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA64h		
<p>This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A29

OAG_OAPERF_A29 - OAG Aggregate Perf Counter A29				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA68h			
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A29 Upper DWord

OAG_OAPERF_A29_UPPER - OAG Aggregate Perf Counter A29 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DA6Ch				
<p>This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAG Aggregate Perf Counter A30

OAG_OAPERF_A30 - OAG Aggregate Perf Counter A30				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DA70h			
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter A30 Upper DWord

OAG_OAPERF_A30_UPPER - OAG Aggregate Perf Counter A30 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA74h		
<p>This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A31

OAG_OAPERF_A31 - OAG Aggregate Perf Counter A31						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA78h					
This register reflects the count value of the OA Performance counter A31						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Aggregate Perf Counter A31 Upper DWord

OAG_OAPERF_A31_UPPER - OAG Aggregate Perf Counter A31 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DA7Ch		
<p>This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter A32

OAG_OAPERF_A32 - OAG Aggregate Perf Counter A32						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA80h					
This register reflects the count value of the OA Performance counter A32						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Aggregate Perf Counter A33

OAG_OAPERF_A33 - OAG Aggregate Perf Counter A33						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA84h					
This register reflects the count value of the OA Performance counter A33						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Aggregate Perf Counter A34

OAG_OAPERF_A34 - OAG Aggregate Perf Counter A34						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA88h					
This register reflects the count value of the OA Performance counter A34						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Aggregate Perf Counter A35

OAG_OAPERF_A35 - OAG Aggregate Perf Counter A35						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA8Ch					
This register reflects the count value of the OA Performance counter A35						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Aggregate Perf Counter SPM0 Lower DWord Free

OAG_OAPERF_SPM0_LOWER_FREE - OAG Aggregate Perf Counter SPM0 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB30h			
<p>This register counts the same event as counter SPM0 however is not affected by context ID or other conditions that prevent SPM0 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter SPM0 Upper DWord Free

OAG_OAPERF_SPM0_UPPER_FREE - OAG Aggregate Perf Counter SPM0 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB34h		
<p>This register counts the same event as counter SPM0 however is not affected by context ID or other conditions that prevent SPM0 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
_Custom_GTIRreset:		DEV	
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter SPM1 Lower DWord Free

OAG_OAPERF_SPM1_LOWER_FREE - OAG Aggregate Perf Counter SPM1 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB38h			
This register counts the same event as counter SPM1 however is not affected by context ID or other conditions that prevent SPM1 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter SPM1 Upper DWord Free

OAG_OAPERF_SPM1_UPPER_FREE - OAG Aggregate Perf Counter SPM1 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB3Ch		
<p>This register counts the same event as counter SPM1 however is not affected by context ID or other conditions that prevent SPM1 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter SPM2 Lower DWord Free

OAG_OAPERF_SPM2_LOWER_FREE - OAG Aggregate Perf Counter SPM2 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB40h			
This register counts the same event as counter SPM2 however is not affected by context ID or other conditions that prevent SPM2 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter SPM2 Upper DWord Free

OAG_OAPERF_SPM2_UPPER_FREE - OAG Aggregate Perf Counter SPM2 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB44h		
<p>This register counts the same event as counter SPM2 however is not affected by context ID or other conditions that prevent SPM2 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter SPM3 Lower DWord Free

OAG_OAPERF_SPM3_LOWER_FREE - OAG Aggregate Perf Counter SPM3 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB48h			
<p>This register counts the same event as counter SPM3 however is not affected by context ID or other conditions that prevent SPM3 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter SPM3 Upper DWord Free

OAG_OAPERF_SPM3_UPPER_FREE - OAG Aggregate Perf Counter SPM3 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB4Ch		
<p>This register counts the same event as counter SPM3 however is not affected by context ID or other conditions that prevent SPM3 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
_Custom_GTIRreset:		DEV	
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter SPM4 Lower DWord Free

OAG_OAPERF_SPM4_LOWER_FREE - OAG Aggregate Perf Counter SPM4 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB50h			
<p>This register counts the same event as counter SPM4 however is not affected by context ID or other conditions that prevent SPM4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Aggregate Perf Counter SPM4 Upper DWord Free

OAG_OAPERF_SPM4_UPPER_FREE - OAG Aggregate Perf Counter SPM4 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB54h		
<p>This register counts the same event as counter SPM4 however is not affected by context ID or other conditions that prevent SPM4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAG Aggregate Perf Counter SPM5 Lower DWord Free

OAG_OAPERF_SPM5_LOWER_FREE - OAG Aggregate Perf Counter SPM5 Lower DWord Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB58h			
Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register. This counter is free running, always enabled and counts irrespective of OA enable configuration.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Aggregate Perf Counter SPM5 Upper DWord Free

OAG_OAPERF_SPM5_UPPER_FREE - OAG Aggregate Perf Counter SPM5 Upper DWord Free			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB5Ch		
Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register. This counter is free running, always enabled and counts irrespective of OA enable configuration.			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.			



OAG Any Media Fixed Function 0 Wake Count Free

OAG_ANY_MEDIA_FF0_WAKE_COUNT_FREE - OAG Any Media Fixed Function 0 Wake Count Free

Register Space: MMIO: 0/2/0

Access: R/W

Size (in bits): 32

Address: 0DBA8h

This register counts the number of media fixed function wake events for Media FF0. This counter is free running, always enabled and counts irrespective of OA being enabled or disabled.

DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Any Media Fixed Function 1 Wake Count Free

OAG_ANY_MEDIA_FF1_WAKE_COUNT_FREE - OAG Any Media Fixed Function 1 Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBB8h			
This register counts the number of media fixed function wake events. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Any Media Fixed Function Busy Free

OAG_ANY_MEDIA_FF_BUSY_FREE - OAG Any Media Fixed Function Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBA0h			
This register counts the time that any media fixed function is busy. This counter is free running, always enabled and counts irrespective of OA being enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG BLT Busy Free

OAG_BLT_BUSY_FREE - OAG BLT Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBBCh			
This register counts the time that BLT engine is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG BLT Wake Count Free

OAG_BLT_WAKE_COUNT_FREE - OAG BLT Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBC0h			
This register counts the number of times that BLT wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Boolean Counter B0

OAG_OAPERF_B0 - OAG Boolean Counter B0						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA94h					
<p>This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Boolean Counter B1

OAG_OAPERF_B1 - OAG Boolean Counter B1						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA98h					
This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAG Boolean Counter B2

OAG_OAPERF_B2 - OAG Boolean Counter B2						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA9Ch					
<p>This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Boolean Counter B3

OAG_OAPERF_B3 - OAG Boolean Counter B3						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DAA0h					
This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Boolean Counter B4

OAG_OAPERF_B4 - OAG Boolean Counter B4						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DAA4h					
<p>This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Boolean Counter B5

OAG_OAPERF_B5 - OAG Boolean Counter B5						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DAA8h					
This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Boolean Counter B6

OAG_OAPERF_B6 - OAG Boolean Counter B6						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DAACH					
<p>This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG Boolean Counter B7

OAG_OAPERF_B7 - OAG Boolean Counter B7						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DAB0h					
This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG Context Control

OAG_OAGLBCTXCTRL - OAG Context Control			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	02B28h		
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	PBC
		_Custom_GTIReset:	DEV
	7:2	Timer Period	
		Default Value:	00b
		Access:	R/W
		Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 (TimerPeriod + 1) The exponent is defined by this field.	
		Programming Notes	
		Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.	
1	Timer Enable		
	Access:	R/W	
	This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.		
	Value	Name	
	Description		
0	Disable [Default]	Counter does not get written out on regular interval	
1	Enable	Counter gets written out on regular intervals, defined by the Timer Period	
Programming Notes			
When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context.			

OAG_OAGLBCTXCTRL - OAG Context Control		
		When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.
	0	Counter Stop-Resume Mechanism
		Access: R/W
		Counter stop-resume mechanism
Value	Name	Description
1	Resume	Resume counting for all counters

OAG Customizable Event Creation 0-0

OAG_CEC00 - OAG Customizable Event Creation 0-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D940h				
Description					
This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	
01b	Prev Event			Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC00 - OAG Customizable Event Creation 0-0

2:0	Compare Function		
	Format:	U3	
	_Custom_GTIRreset:	DEV	
	This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	Description
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

OAG Customizable Event Creation 1-0

OAG_CEC10 - OAG Customizable Event Creation 1-0				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D948h			
Description				
This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.				
This register can be used to customize counters for events from both unslice and slice units.				
DWord	Bit	Description		
0	31:21	Negate		
		Format:	U11	
		_Custom_GTIRreset:	DEV	
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.		
		Value	Name	Description
		0b	Pass-through	Input bit is passed through to comparator as is
	1b	Negated	Input bit is negated before passing to comparator	
	20:19	Source Select		
		Format:	U2	
		_Custom_GTIRreset:	DEV	
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).		
		Value	Name	Description
01b		Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved			
18:3	Compare Value			
	Format:	U16		
	_Custom_GTIRreset:	DEV		
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC10 - OAG Customizable Event Creation 1-0

2:0	Compare Function	
	Format:	U3
	_Custom_GTIRreset:	DEV
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).	
	Value	Name Description
	000b	Any Are Equal Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than Compare and assert output if greater than
	010b	Equal Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal Compare and assert output if greater than or equal
	100b	Less Than Compare and assert output if less than
101b	Not Equal Compare and assert output if not equal	
110b	Less Than or Equal Compare and assert output if less than or equal	
111b	Reserved	

OAG Customizable Event Creation 1-1

OAG_CEC11 - OAG Customizable Event Creation 1-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0D94Ch												
Description													
This register configures the input conditioning portion of CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.													
This register can be used to customize counters for events from both unslice and slice units.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	<p>Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Customizable Event Creation 2-0

OAG_CEC20 - OAG Customizable Event Creation 2-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D950h				
Description					
This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC20 - OAG Customizable Event Creation 2-0

2:0	Compare Function		
	Format:	U3	
	_Custom_GTIRreset:	DEV	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	Description
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

OAG Customizable Event Creation 2-1

OAG_CEC21 - OAG Customizable Event Creation 2-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0D954h												
Description													
This register configures the input conditioning portion of CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.													
This register can be used to customize counters for events from both unslice and slice units.													
DWord	Bit	Description											
0	31:16	Considerations <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	Mask	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Customizable Event Creation 3-0

OAG_CEC30 - OAG Customizable Event Creation 3-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D958h				
Description					
This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC30 - OAG Customizable Event Creation 3-0

2:0	Compare Function		
	Format:	U3	
	_Custom_GTIRreset:	DEV	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
		Description	
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than	
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

OAG Customizable Event Creation 3-1

OAG_CEC31 - OAG Customizable Event Creation 3-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0D95Ch												
Description													
This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
This register can be used to customize counters for events from both unslice and slice units.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	<p>Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Customizable Event Creation 4-0

OAG_CEC40 - OAG Customizable Event Creation 4-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D960h				
Description					
This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	
01b	Prev Event			Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC40 - OAG Customizable Event Creation 4-0

2:0

Compare Function

Format:	U3
_Custom_GTIRreset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 5-0

OAG_CEC50 - OAG Customizable Event Creation 5-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D968h				
Description					
This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC50 - OAG Customizable Event Creation 5-0

2:0	Compare Function		
	Format:	U3	
	_Custom_GTIRreset:	DEV	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	Description
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
	100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

OAG Customizable Event Creation 5-1

OAG_CEC51 - OAG Customizable Event Creation 5-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0D96Ch												
Description													
<p>This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p> <p>This register can be used to customize counters for events from both unslice and slice units.</p>													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	<p>Mask</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Customizable Event Creation 6-0

OAG_CEC60 - OAG Customizable Event Creation 6-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D970h				
Description					
This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	Programming Notes
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).					
Value	Name			Description	Programming Notes
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC60 - OAG Customizable Event Creation 6-0

2:0	Compare Function		
	Format:	U3	
	_Custom_GTIRreset:	DEV	
	This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).		
	Value	Name	
		Description	
	000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
	001b	Greater Than	Compare and assert output if greater than
	010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
	011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than	
101b	Not Equal	Compare and assert output if not equal	
110b	Less Than or Equal	Compare and assert output if less than or equal	
111b	Reserved		

OAG Customizable Event Creation 6-1

OAG_CEC61 - OAG Customizable Event Creation 6-1														
Register Space:	MMIO: 0/2/0													
Access:	R/W													
Size (in bits):	32													
Address:	0D974h													
Description														
This register configures the input conditioning portion of CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.														
This register can be used to customize counters for events from both unslice and slice units.														
DWord	Bit	Description												
0	31:16	<p>Considerations</p> <table border="1"> <tr> <td colspan="2">_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:		DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:		DEV											
Value	Name	Description												
0b	Live	Input bit is not delayed by 1 clock before event calculation												
1b	Delayed	Input bit is delayed by 1 clock before event calculation												
15:0	<p>Mask</p> <table border="1"> <tr> <td colspan="2">_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:		DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:		DEV												
Value	Name	Description												
0b	Unmasked	Input bit is considered in event calculation												
1b	Masked	Input bit is ignored in event calculation												

OAG Customizable Event Creation 7-0

OAG_CEC70 - OAG Customizable Event Creation 7-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0D978h				
Description					
This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
This register can be used to customize counters for events from both unslice and slice units.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
				Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).	
				Value	Name
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3		Compare Value			
		Format:	U16		
		_Custom_GTIRreset:	DEV		
		The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.			

OAG_CEC70 - OAG Customizable Event Creation 7-0

2:0

Compare Function

Format:	U3
_Custom_GTIRreset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 7-1

OAG_CEC71 - OAG Customizable Event Creation 7-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0D97Ch												
Description													
<p>This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.</p> <p>This register can be used to customize counters for events from both unslice and slice units.</p>													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	Mask	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG GPU Ticks Counter

OAG_GPU_TICKS - OAG GPU Ticks Counter						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0DA90h					
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAG GPU Ticks Counter Upper DWord

OAG_GPU_TICKS_UPPER - OAG GPU Ticks Counter Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.						
DWord	Bit	Description				
0	31:0	Upper Value <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAG GTI Busy Free

OAG_GTI_BUSY_FREE - OAG GTI Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBCCh			
This register counts the time that any engine residing in GTI (currently WG, BLT, or GuC) is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG GTI Wake Count Free

OAG_GTI_WAKE_COUNT_FREE - OAG GTI Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBD0h			
This register counts the number of times that GTI wakes up due to one of the engines resident in GTI (currently WG, BLT, and GuC) becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG GuC Busy Free

OAG_GUC_BUSY_FREE - OAG GuC Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBC4h			
This register counts the time that GuC is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG GuC Wake Count Free

OAG_GUC_WAKE_COUNT_FREE - OAG GuC Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBC8h			
This register counts the number of times that GuC wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Interrupt Mask Register

OAG_OA_IMR - OAG Interrupt Mask Register				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB14h			
The OAIMR register is used by software to control whether OA generates an interrupt or not.				
DWord	Bit	Description		
0	31:29	Reserved		
		Default Value:	7h	
		Format:	PBC	
		_Custom_GTIRreset:	DEV	
	28	Mask Bit		
		_Custom_GTIRreset:	DEV	
		Value	Name	Description
		0h	Not Masked	May generate an interrupt
		1h	Masked [Default]	Will not generate an interrupt
	27:0	Reserved		
		Default Value:	FFFFFFh	
		Format:	PBC	
_Custom_GTIRreset:		DEV		



OAG MCPG0 Hysteresis Time Free

OAG_MCPG0_HYSTERESIS_TIME_FREE - OAG MCPG0 Hysteresis Time Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBA4h			
This register counts the time that MCPG hysteresis time is accumulating for media slice 0. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Media Sampler Really Busy Free

OAG_MEDIA_SAMPLER_REALLY_BUSY_FREE - OAG Media Sampler Really Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBACh			
This register counts the time that media sampler is really busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Media Sampler Wake Count Free

OAG_MEDIA_SAMPLER_WAKE_COUNT_FREE - OAG Media Sampler Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBB0h			
This register counts the number of times that media sampler wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Observation Architecture Buffer

OAG_OABUFFER - OAG Observation Architecture Buffer																															
Register Space:	MMIO: 0/2/0																														
Access:	R/W																														
Size (in bits):	32																														
Address:	0DB08h																														
This register is used to program the OA unit.																															
Programming Notes																															
This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.																															
DWord	Bit	Description																													
0	31:6	Report Buffer Offset																													
		<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This field specifies 64B aligned GFX MEM address where the chap counter values are reported.</p>	_Custom_GTIRreset:	DEV																											
	_Custom_GTIRreset:	DEV																													
	5:3	5:3	Inter Trigger Report Buffer Size																												
			<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This field indicates the size of report buffer for time/event-based report trigger mechanisms.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>128 KB or 1MB [Default]</td> <td>All context considered.</td> </tr> <tr> <td>1h</td> <td>256 KB or 2MB</td> <td></td> </tr> <tr> <td>2h</td> <td>512 KB or 4MB</td> <td></td> </tr> <tr> <td>3h</td> <td>1 MB or 8MB</td> <td></td> </tr> <tr> <td>4h</td> <td>2 MB or 16MB</td> <td></td> </tr> <tr> <td>5h</td> <td>4 MB or 32MB</td> <td></td> </tr> <tr> <td>6h</td> <td>8 MB or 64MB</td> <td></td> </tr> <tr> <td>7h</td> <td>16 MB or 128MB</td> <td></td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0h	128 KB or 1MB [Default]	All context considered.	1h	256 KB or 2MB		2h	512 KB or 4MB		3h	1 MB or 8MB		4h	2 MB or 16MB		5h	4 MB or 32MB		6h	8 MB or 64MB		7h	16 MB or 128MB
		_Custom_GTIRreset:	DEV																												
		Value	Name	Description																											
		0h	128 KB or 1MB [Default]	All context considered.																											
		1h	256 KB or 2MB																												
		2h	512 KB or 4MB																												
3h		1 MB or 8MB																													
4h		2 MB or 16MB																													
5h		4 MB or 32MB																													
6h	8 MB or 64MB																														
7h	16 MB or 128MB																														
2	2	OA Report Trigger Select																													
		<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>Level Report trigger</td> </tr> <tr> <td>1</td> <td></td> <td>Edge Report trigger</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0		Level Report trigger	1		Edge Report trigger																		
	_Custom_GTIRreset:	DEV																													
	Value	Name	Description																												
0		Level Report trigger																													
1		Edge Report trigger																													
1	1	Disable Overrun Mode																													
		<table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when</p>	Format:	Enable	_Custom_GTIRreset:	DEV																									
Format:	Enable																														
_Custom_GTIRreset:	DEV																														

OAG_OABUFFER - OAG Observation Architecture Buffer											
	<p>HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>Disable [Default]</td> <td>Counter gets written out on regular intervals, defined by the Timer Period</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>Enable</td> <td>Counter does not get written out on regular interval</td> </tr> </tbody> </table>		Value	Name	Description	0h	Disable [Default]	Counter gets written out on regular intervals, defined by the Timer Period	1h	Enable	Counter does not get written out on regular interval
Value	Name	Description									
0h	Disable [Default]	Counter gets written out on regular intervals, defined by the Timer Period									
1h	Enable	Counter does not get written out on regular interval									
0	<p>Memory Select PPGTT/GGTT Access</p> <table border="1"> <tr> <td style="width: 70%;">_Custom_GTIReset:</td> <td style="width: 30%;">DEV</td> </tr> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>PPGTT</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>GGTT [Default]</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>When each context has its own Per Process GTT, this field should be always set to GGTT.</p>		_Custom_GTIReset:	DEV	Value	Name	0h	PPGTT	1h	GGTT [Default]	
_Custom_GTIReset:	DEV										
Value	Name										
0h	PPGTT										
1h	GGTT [Default]										

OAG Observation Architecture Control

OAG_OACONTROL - OAG Observation Architecture Control									
Register Space:	MMIO: 0/2/0								
Access:	R/W								
Size (in bits):	32								
Address:	0DAF4h								
This register controls global OA functionality, report format, interrupt steering and context filtering.									
DWord	Bit	Description							
0	31:18	Reserved							
		Format:	PBC						
		_Custom_GTIReset:	DEV						
	17:7	Reserved							
		Access:	RO						
		Format:	MBZ						
	6	OA Context control select							
		_Custom_GTIReset:	DEV						
		Description							
		This field is obsolete Bit field to indicate which context control inputs are to be chosen in the OACS							
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>OAG RCS Select [Default]</td> <td>Select the OA context control from RCS (Default)</td> </tr> <tr> <td>1</td> <td>Global</td> <td>Select the Global OA context control</td> </tr> </tbody> </table>		Value	Name	Description	0	OAG RCS Select [Default]	Select the OA context control from RCS (Default)	1	Global
Value	Name	Description							
0	OAG RCS Select [Default]	Select the OA context control from RCS (Default)							
1	Global	Select the Global OA context control							
5	Interrupt Steering Bit								
	_Custom_GTIReset:	DEV							
When set, OACS unit sends interrupt messages to the SHIM of the GUC through message channel. When reset, OACS unit sends the interrupt message to Display Engine as config writes on GAM interface.									
4:2	Counter Select								
	_Custom_GTIReset:	DEV							
This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.									
1	Reserved								
	Access:	RO							
	Format:	MBZ							

OAG_OACONTROL - OAG Observation Architecture Control						
0	<p>Performance Counter Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Programming Notes</td> </tr> </table> <p>When this bit is set, OABUFFER, OAHEADPTR and OATAILPTR must be programmed correctly to ensure report triggers due to Context Switch and GO transition happen correctly.</p>	Format:	Enable	_Custom_GTIReset:	DEV	Programming Notes
Format:	Enable					
_Custom_GTIReset:	DEV					
Programming Notes						

OAG Observation Architecture Report Trigger 2

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

Register Space: MMIO: 0/2/0

Access: R/W

Size (in bits): 32

Address: 0D924h

This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	Report Trigger Enable
		Format: Enable
		_Custom_GTIReset: DEV
<p>Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.</p> <p>When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.</p>		
30:24	Reserved	Format: PBC
		_Custom_GTIReset: DEV
23	Threshold Enable	Format: Enable
		_Custom_GTIReset: DEV
		Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

22	Invert D Enable 0		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
	Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).		
	21	Invert C Enable 1	
		Format:	Enable
		_Custom_GTIReset:	DEV
	Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).		
20	Invert C Enable 0		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
19	Invert B Enable 3		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
18	Invert B Enable 2		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
17	Invert B Enable 1		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
16	Invert B Enable 0		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
15	Invert A Enable 15		
	Format:	Enable	
	_Custom_GTIReset:	DEV	

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
14	Invert A Enable 14	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
13	Invert A Enable 13	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
12	Invert A Enable 12	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
11	Invert A Enable 11	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
10	Invert A Enable 10	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
9	Invert A Enable 9	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
8	Invert A Enable 8	
	Format:	Enable
	_Custom_GTIRreset:	DEV
		Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

7	Invert A Enable 7		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
	Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).		
	6	Invert A Enable 6	
		Format:	Enable
		_Custom_GTIRreset:	DEV
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
5	Invert A Enable 5		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
4	Invert A Enable 4		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
3	Invert A Enable 3		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
2	Invert A Enable 2		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			
1	Invert A Enable 1		
	Format:	Enable	
	_Custom_GTIRreset:	DEV	
Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).			

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	0	Invert A Enable 0	
		Format:	Enable
		_Custom_GTIReset:	DEV
<p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).</p>			



OAG Observation Architecture Report Trigger 6

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0D934h			
<p>This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.</p> <p>Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.</p>				
DWord	Bit	Description		
0	31	Report Trigger Enable		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.</p> <p>When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.</p>	_Custom_GTIReset:	DEV
	_Custom_GTIReset:	DEV		
	30:24	Reserved		
23	Threshold Enable			
0	22	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
		_Custom_GTIReset:	DEV	
<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table>	_Custom_GTIReset:	DEV		
_Custom_GTIReset:	DEV			

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

		Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).		
21	Invert C Enable 1	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
20	Invert C Enable 0	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
19	Invert B Enable 3	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
18	Invert B Enable 2	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
17	Invert B Enable 1	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
16	Invert B Enable 0	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
15	Invert A Enable 15	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
14	Invert A Enable 14	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			
13	Invert A Enable 13	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIRreset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

12	Invert A Enable 12 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
11	Invert A Enable 11 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
10	Invert A Enable 10 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
9	Invert A Enable 9 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
8	Invert A Enable 8 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
7	Invert A Enable 7 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
6	Invert A Enable 6 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
5	Invert A Enable 5 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
4	Invert A Enable 4 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		
3	Invert A Enable 3 <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV		

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

		block diagram in the Performance Counter Reporting section).	
	2	Invert A Enable 2	
		<input type="checkbox"/> _Custom_GTIReset:	DEV
	Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).		
	1	Invert A Enable 1	
		<input type="checkbox"/> _Custom_GTIReset:	DEV
	Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).		
	0	Invert A Enable 0	
		<input type="checkbox"/> _Custom_GTIReset:	DEV
	Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).		



OAG Observation Architecture Report Trigger Counter

OAG_OARPTTRIG_COUNTER - OAG Observation Architecture Report Trigger Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB10h		
<p>This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.</p>			
DWord	Bit	Description	
0	31:16	Report Trig Threshold Count 1 Status	
		<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table>	_Custom_GTIReset:
	_Custom_GTIReset:	DEV	
	Programming Notes		
<p>This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.</p>			
0	15:0	Report Trig Threshold count 2 status	
		<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table>	_Custom_GTIReset:
	_Custom_GTIReset:	DEV	
	Programming Notes		
<p>This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.</p>			

OAG Observation Architecture Start Trigger 5

OAG_OASTARTTRIG5 - OAG Observation Architecture Start Trigger 5			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0D910h		
<p>This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.</p>			
DWord	Bit	Description	
0	31:16	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	15:0	Threshold Value	
		Format:	U16
		_Custom_GTIRreset:	DEV
		Programming Notes	
		Threshold value for the compare logic within the start trigger logic for B7-B4 counters.	



OAG Observation Architecture Start Trigger Counter

OAG_OASTARTTRIG_COUNTER - OAG Observation Architecture Start Trigger Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DB0Ch		
This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.			
DWord	Bit	Description	
0	31:16	Start Trig Threshold Count 1 Status	
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%; text-align: center;">DEV</td> </tr> </table>	_Custom_GTIReset:
	_Custom_GTIReset:	DEV	
	Programming Notes		
This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.			
0	15:0	Start Trig Threshold count 2 status	
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%; text-align: center;">DEV</td> </tr> </table>	_Custom_GTIReset:
	_Custom_GTIReset:	DEV	
	Programming Notes		
: This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.			

OAG Observation Architecture Status Register

OAG_OASTATUS - OAG Observation Architecture Status Register									
Register Space:	MMIO: 0/2/0								
Access:	R/W								
Size (in bits):	32								
Address:	0DAFCh								
<p>This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)</p>									
DWord	Bit	Description							
0	31:22	Reserved							
		Format:	PBC						
		_Custom_GTIReset:	DEV						
	21		Start Trigger Flag 1						
			_Custom_GTIReset:	DEV					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1	
		Value	Name						
		0	[Default]						
		1							
		<p style="text-align: center;">Programming Notes</p> <p>This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.</p>							
		20		Start Trigger Flag 2					
				_Custom_GTIReset:	DEV				
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>			Value	Name	0	[Default]	1		
Value	Name								
0	[Default]								
1									
<p style="text-align: center;">Programming Notes</p> <p>This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.</p>									
19		Report Trigger Flag 1							
		_Custom_GTIReset:	DEV						
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> </tbody> </table>		Value	Name	0	[Default]			
Value	Name								
0	[Default]								

OAG_OASTATUS - OAG Observation Architecture Status Register

	1	
Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.		
18	Report Trigger Flag 2	
	_Custom_GTIRreset:	DEV
	Value	Name
	0	[Default]
	1	
Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.		
17	Tail Pointer Wrap Flag	
	Format:	U1
	_Custom_GTIRreset:	DEV
	Value	Name
	0	
	1	[Default]
Programming Notes		
This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.		
16	Head Pointer Wrap Flag	
	Format:	U1
	_Custom_GTIRreset:	DEV
	Value	Name
	0	
	1	[Default]
Programming Notes		
This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.		

OAG_OASTATUS - OAG Observation Architecture Status Register

	15:7	Reserved		
		Format:	PBC	
		_Custom_GTIRreset:	DEV	
	6	Reserved		
		Access:	RO	
		Format:	MBZ	
	5	Reserved		
		Format:	PBC	
		_Custom_GTIRreset:	DEV	
	4	Accumulator Overflow		
		_Custom_GTIRreset:	DEV	
		This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.		
		Value	Name	Description
		0	[Default]	No overflow has occurred.
	1		Overflow has occurred.	
3	Overrun Status			
	_Custom_GTIRreset:	DEV		
	This bit is read only and writing to this bit will have no effect. This bit will reflect the status of overrun irrespective of Overrun Mode enabled or disabled.			
	Value	Name	Description	
	0	[Default]	No overrun has occurred	
1		Overrun has occurred		
2	Counter Overflow			
	_Custom_GTIRreset:	DEV		
	This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 0 to it.			
	Value	Name	Description	
	0	[Default]	Counter Overflow Not Occurred	
1		Counter Overflow Occurred		
1	Buffer Overflow			
	_Custom_GTIRreset:	DEV		
	This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size			
	Value	Name	Description	
	0h	[Default]	Buffer Overflow Not Occurred	
1		Buffer Overflow Occurred		

OAG_OASTATUS - OAG Observation Architecture Status Register

0	Report Lost Error		
	Format:	Enable	
	_Custom_GTIReset:	DEV	
	<p>This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" or "MMIO Trigger" to write out the counter values is dropped, while there is an ongoing report in progress. The report request is ignored and the counter continue to count. This bit will be set along with this MMIO Trigger Queue Full, in case of dropped request for MMIO trigger.</p>		
	Value	Name	Description
	0	[Default]	Report Lost Error Not Occurred
1		Report Lost Error Occurred	
Programming Notes			
This bit can be reset by SW by either soft reset or writing a 0 to it.			

OAG Observation Architecture Tail Pointer

OAG_OATAILPTR - OAG Observation Architecture Tail Pointer				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB04h			
This register allows software to program tail pointer and also indicates current tail pointer value.				
DWord	Bit	Description		
0	31:6	Tail Pointer		
		<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes.</p>	_Custom_GTIRreset:	DEV
		_Custom_GTIRreset:	DEV	
		Programming Notes		
Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.				
5:0		Reserved		
		<table border="1"> <tr> <td>Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
		Format:	PBC	
<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	_Custom_GTIRreset:	DEV		
_Custom_GTIRreset:	DEV			



OAG RC0 Any Engine Busy Free

OAG_RC0_ANY_ENGINE_BUSY_FREE - OAG RC0 Any Engine Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB80h			
This register counts the time that any engine is truly busy (not simply powered up). This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads. Unit in GPMusec. Refer to Timestamp Bases for details.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG RC0 Clocks Free

OAG_RC0_CLOCKS_FREE - OAG RC0 Clocks Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB90h			
This register counts the clocks that GFX has been in RC0 in increments of 64 GFX clocks. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG RC0 Hysteresis Free

OAG_RC0_HYSTERISIS_FREE - OAG RC0 Hysteresis Free				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	0DB84h			
This register counts the time that any engine is truly busy (not simply powered up). This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG RC0 Wake Count Free

OAG_RC0_WAKE_COUNT_FREE - OAG RC0 Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	0DB88h			
This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG RC6 Entry Count Free

OAG_RC6_ENTRY_COUNT_FREE - OAG RC6 Entry Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB9Ch			
This register counts number rc6 entries. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. This is an RPM mirrored register.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG RC6 Pre Engine Wake Overhead Free

OAG_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE - OAG RC6 Pre Engine Wake Overhead Free				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	0DB8Ch			
This register counts the time between boot complete and Go=1. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG RCPG Hysteresis Time Free

OAG_RCPG_HYSTERESIS_TIME_FREE - OAG RCPG Hysteresis Time Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBE0h			
This register counts the time RCPG hysteresis count is accumulating. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAG Render Busy Free

OAG_RENDER_BUSY_FREE - OAG Render Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBDCh			
This register counts the time that any render engine is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG Render Wake Count Free

OAG_RENDER_WAKE_COUNT_FREE - OAG Render Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBE4h			
This register counts the number of render wakes that have occurred. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Slice Customizable Event Creation 0-0

OAG_SCEC0_0 - OAG Slice Customizable Event Creation 0-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DC00h				
This register is used to define the slice custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19		Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
				Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).	
				Value	Name
01b	Prev Event			Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	
11b	Reserved				
18:3				Compare Value	
				Format:	U16
				_Custom_GTIRreset:	DEV
				The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.	
				2:0	
		Format:	U3		
		_Custom_GTIRreset:	DEV		
		This field selects the function used by the CEC0 comparator when comparing the compare value			

OAG_SCECO_0 - OAG Slice Customizable Event Creation 0-0

to the value active on the CECO conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 1-0

OAG_SCEC1_0 - OAG Slice Customizable Event Creation 1-0												
Register Space:	MMIO: 0/2/0											
Access:	R/W											
Size (in bits):	32											
Address:	0DC08h											
This register is used to define slice custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.												
DWord	Bit	Description										
0	31:21	Negate										
		Format:	U11									
		_Custom_GTIRreset:	DEV									
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>			Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
	Value	Name	Description									
	0b	Pass-through	Input bit is passed through to comparator as is									
	1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select										
		Format:	U2									
		_Custom_GTIRreset:	DEV									
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).										
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>			Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved		
Value	Name	Description										
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block										
11b	Reserved											
18:3	Compare Value											
	Format:	U16										
	_Custom_GTIRreset:	DEV										
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.											
2:0	Compare Function											
	Format:	U3										
	_Custom_GTIRreset:	DEV										
This field selects the function used by the CEC comparator when comparing the compare value												

OAG_SCEC1_0 - OAG Slice Customizable Event Creation 1-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 1-1

OAG_SCEC1_1 - OAG Slice Customizable Event Creation 1-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC0Ch												
This register configures the input conditioning portion of slice CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	<p>Mask</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Slice Customizable Event Creation 2-0

OAG_SCEC2_0 - OAG Slice Customizable Event Creation 2-0												
Register Space:	MMIO: 0/2/0											
Access:	R/W											
Size (in bits):	32											
Address:	0DC10h											
This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.												
DWord	Bit	Description										
0	31:21	Negate										
		Format:	U11									
		_Custom_GTIRreset:	DEV									
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>			Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
	Value	Name	Description									
	0b	Pass-through	Input bit is passed through to comparator as is									
	1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select										
		Format:	U2									
		_Custom_GTIRreset:	DEV									
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).										
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>			Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved		
Value	Name	Description										
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block										
11b	Reserved											
18:3	Compare Value											
	Format:	U16										
	_Custom_GTIRreset:	DEV										
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.											
2:0	Compare Function											
	Format:	U3										
	_Custom_GTIRreset:	DEV										
This field selects the function used by the CEC comparator when comparing the compare value												

OAG_SCEC2_0 - OAG Slice Customizable Event Creation 2-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 2-1

OAG_SCEC2_1 - OAG Slice Customizable Event Creation 2-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC14h												
This register configures the input conditioning portion of slice CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	<p>Mask</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation	
_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Slice Customizable Event Creation 3-0

OAG_SCEC3_0 - OAG Slice Customizable Event Creation 3-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DC18h				
This register is used to define slice custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19	20:19	Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
				Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).	
				Value	Name
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3	18:3			Compare Value	
				Format:	U16
				_Custom_GTIRreset:	DEV
				The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.	
				2:0	2:0
		Format:	U3		
		_Custom_GTIRreset:	DEV		
		This field selects the function used by the CEC comparator when comparing the compare value			

OAG_SCEC3_0 - OAG Slice Customizable Event Creation 3-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 3-1

OAG_SCEC3_1 - OAG Slice Customizable Event Creation 3-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC1Ch												
This register configures the input conditioning portion of Slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
DWord	Bit	Description											
0	31:16	Considerations <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
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15:0	Mask	<table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Slice Customizable Event Creation 4-0

OAG_SCEC4_0 - OAG Slice Customizable Event Creation 4-0															
Register Space:	MMIO: 0/2/0														
Access:	R/W														
Size (in bits):	32														
Address:	0DC20h														
This register is used to define slice custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.															
DWord	Bit	Description													
0	31:21	Negate <table border="1"> <tr> <td>Format:</td> <td>U11</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Pass-through</td> <td>Input bit is passed through to comparator as is</td> </tr> <tr> <td>1b</td> <td>Negated</td> <td>Input bit is negated before passing to comparator</td> </tr> </tbody> </table>	Format:	U11	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Pass-through	Input bit is passed through to comparator as is	1b	Negated	Input bit is negated before passing to comparator
		Format:	U11												
		_Custom_GTIRreset:	DEV												
		Value	Name	Description											
0b	Pass-through	Input bit is passed through to comparator as is													
1b	Negated	Input bit is negated before passing to comparator													
20:19		Source Select <table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Format:	U2	_Custom_GTIRreset:	DEV	Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block	11b	Reserved	
		Format:	U2												
		_Custom_GTIRreset:	DEV												
		Value	Name	Description											
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block													
11b	Reserved														
18:3		Compare Value <table border="1"> <tr> <td>Format:</td> <td>U16</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.</p>	Format:	U16	_Custom_GTIRreset:	DEV									
		Format:	U16												
		_Custom_GTIRreset:	DEV												
		2:0		Compare Function <table border="1"> <tr> <td>Format:</td> <td>U3</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This field selects the function used by the CEC comparator when comparing the compare value</p>	Format:	U3	_Custom_GTIRreset:	DEV							
Format:	U3														
_Custom_GTIRreset:	DEV														

OAG_SCEC4_0 - OAG Slice Customizable Event Creation 4-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 5-0

OAG_SCEC5_0 - OAG Slice Customizable Event Creation 5-0					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	0DC28h				
This register is used to define slice custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.					
DWord	Bit	Description			
0	31:21	Negate			
		Format:	U11		
		_Custom_GTIRreset:	DEV		
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.			
		Value	Name	Description	
		0b	Pass-through	Input bit is passed through to comparator as is	
		1b	Negated	Input bit is negated before passing to comparator	
		20:19	20:19	Source Select	
				Format:	U2
				_Custom_GTIRreset:	DEV
				Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).	
				Value	Name
01b	Prev Event			Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	
11b	Reserved				
18:3	18:3			Compare Value	
				Format:	U16
				_Custom_GTIRreset:	DEV
				The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.	
				2:0	2:0
		Format:	U3		
		_Custom_GTIRreset:	DEV		
		This field selects the function used by the CEC comparator when comparing the compare value			

OAG_SCEC5_0 - OAG Slice Customizable Event Creation 5-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 5-1

OAG_SCEC5_1 - OAG Slice Customizable Event Creation 5-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC2Ch												
This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
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_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Slice Customizable Event Creation 6-0

OAG_SCEC6_0 - OAG Slice Customizable Event Creation 6-0												
Register Space:	MMIO: 0/2/0											
Access:	R/W											
Size (in bits):	32											
Address:	0DC30h											
This register is used to define slice custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.												
DWord	Bit	Description										
0	31:21	Negate										
		Format:	U11									
		_Custom_GTIRreset:	DEV									
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.										
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	Value	Name	Description									
	0b	Pass-through	Input bit is passed through to comparator as is									
	1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select										
		Format:	U2									
		_Custom_GTIRreset:	DEV									
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).										
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Value	Name	Description										
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block										
11b	Reserved											
18:3	Compare Value											
	Format:	U16										
	_Custom_GTIRreset:	DEV										
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.											
2:0	Compare Function											
	Format:	U3										
	_Custom_GTIRreset:	DEV										
This field selects the function used by the CEC comparator when comparing the compare value												

OAG_SCEC6_0 - OAG Slice Customizable Event Creation 6-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 6-1

OAG_SCEC6_1 - OAG Slice Customizable Event Creation 6-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC34h												
This register configures the input conditioning portion of slice CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
DWord	Bit	Description											
0	31:16	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
	_Custom_GTIRreset:	DEV											
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
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_Custom_GTIRreset:	DEV												
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG Slice Customizable Event Creation 7-0

OAG_SCEC7_0 - OAG Slice Customizable Event Creation 7-0												
Register Space:	MMIO: 0/2/0											
Access:	R/W											
Size (in bits):	32											
Address:	0DC38h											
This register is used to define slice custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.												
DWord	Bit	Description										
0	31:21	Negate										
		Format:	U11									
		_Custom_GTIRreset:	DEV									
		The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B !C)). Note that LSB of this field affects bit 0 of the selected input bus.										
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	Value	Name	Description									
	0b	Pass-through	Input bit is passed through to comparator as is									
	1b	Negated	Input bit is negated before passing to comparator									
	20:19	Source Select										
		Format:	U2									
		_Custom_GTIRreset:	DEV									
		Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).										
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>01b</td> <td>Prev Event</td> <td>Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>			Value	Name	Description	01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block	11b	Reserved		
Value	Name	Description										
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block										
11b	Reserved											
18:3	Compare Value											
	Format:	U16										
	_Custom_GTIRreset:	DEV										
	The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.											
2:0	Compare Function											
	Format:	U3										
	_Custom_GTIRreset:	DEV										
This field selects the function used by the CEC comparator when comparing the compare value												

OAG_SCEC7_0 - OAG Slice Customizable Event Creation 7-0

to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 7-1

OAG_SCEC7_1 - OAG Slice Customizable Event Creation 7-1													
Register Space:	MMIO: 0/2/0												
Access:	R/W												
Size (in bits):	32												
Address:	0DC3Ch												
This register configures the input conditioning portion of slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.													
DWord	Bit	Description											
0	31:16	Considerations <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Live</td> <td>Input bit is not delayed by 1 clock before event calculation</td> </tr> <tr> <td>1b</td> <td>Delayed</td> <td>Input bit is delayed by 1 clock before event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Live	Input bit is not delayed by 1 clock before event calculation	1b	Delayed	Input bit is delayed by 1 clock before event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Live	Input bit is not delayed by 1 clock before event calculation											
1b	Delayed	Input bit is delayed by 1 clock before event calculation											
15:0	15:0	Mask <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Unmasked</td> <td>Input bit is considered in event calculation</td> </tr> <tr> <td>1b</td> <td>Masked</td> <td>Input bit is ignored in event calculation</td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	Description	0b	Unmasked	Input bit is considered in event calculation	1b	Masked	Input bit is ignored in event calculation
		_Custom_GTIRreset:	DEV										
Value	Name	Description											
0b	Unmasked	Input bit is considered in event calculation											
1b	Masked	Input bit is ignored in event calculation											

OAG SQ Full Occupancy count Free

OAG_SQ_FULL_OCCUPANCY_COUNT_FREE - OAG SQ Full Occupancy count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB98h			
This register counts the number of GFX clocks that SQ was full. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">_Custom_GTIReset:</td> <td style="width: 20%;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			



OAG SQ Memory Bound Stall count Free

OAG_SQ_MBSTALL_COUNT_FREE - OAG SQ Memory Bound Stall count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB94h			
This register counts the number of GFX clocks that SQ read has been stalled. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAG Unslice Busy Free

OAG_UNSLICE_BUSY_FREE - OAG Unslice Busy Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBD4h			
This register counts the number of times that unslice wakes up due to any unslice engine (currently WG, BLT, GuC, and media fixed functions) becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			



OAG Unslice Wake Count Free

OAG_UNSLICE_WAKE_COUNT_FREE - OAG Unslice Wake Count Free				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DBD8h			
<p>This register counts the number of times that unslice wakes up due to any unslice engine (currently WG, BLT, GuC, and media fixed functions) becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.</p>				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">_Custom_GTIReset:</td> <td style="width: 20%; padding: 2px;">DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAM GPU Ticks Counter

OAM_GPU_TICKS - OAM GPU Ticks Counter						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					



OAM GPU Ticks Counter Upper DWord

OAM_GPU_TICKS_UPPER - OAM GPU Ticks Counter Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.		
DWord	Bit	Description
0	31:0	Upper Value
		Format: U32
		_Custom_GTIReset: DEV
This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.		

OA Programmable Event Source Select Register

OAG_OA_PESS - OA Programmable Event Source Select Register			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02B2Ch		
The OA_PESS register is used by software to control programmable event P15 to P0 source selection generated from 'unslice' or 'aggregated P events generated from slice'. Bit[0] indicates selection for P0, bit[1] for P1 and so on.			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000h
		Format:	PBC
		_Custom_GTIRreset:	DEV
	15:0	P event source select	
		_Custom_GTIRreset:	DEV
		Value	Name
0h	P event generated from unslice [Default]	Bit wise select for P[15:0] events generated from boolean logic present in unslice	
1h	P event generated from slice	Bit wise select for P[15:0] events generated from boolean logic present in slice in an aggregated manner	



OAR Aggregate Perf Counter A0

OAR_OAPERF_A0 - OAR Aggregate Perf Counter A0										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	02800h									
This register reflects the count value of the OA Performance counter A0.										
DWord	Bit	Description								
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0x00000000</td> <td>[Default]</td> </tr> <tr> <td>[0x00000001-0xFFFFFFFF]</td> <td></td> </tr> </tbody> </table>	_Custom_GTIRreset:	DEV	Value	Name	0x00000000	[Default]	[0x00000001-0xFFFFFFFF]	
_Custom_GTIRreset:	DEV									
Value	Name									
0x00000000	[Default]									
[0x00000001-0xFFFFFFFF]										

OAR Aggregate Perf Counter A0 Upper DWord

OAR_OAPERF_A0_UPPER - OAR Aggregate Perf Counter A0 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02804h	
<p>This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A1

OAR_OAPERF_A1 - OAR Aggregate Perf Counter A1				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02808h			
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A1 Upper DWord

OAR_OAPERF_A1_UPPER - OAR Aggregate Perf Counter A1 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0280Ch	
<p>This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A2

OAR_OAPERF_A2 - OAR Aggregate Perf Counter A2				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02810h			
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A2 Upper DWord

OAR_OAPERF_A2_UPPER - OAR Aggregate Perf Counter A2 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02814h		
<p>This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A3

OAR_OAPERF_A3 - OAR Aggregate Perf Counter A3				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02818h			
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A3 Upper DWord

OAR_OAPERF_A3_UPPER - OAR Aggregate Perf Counter A3 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0281Ch		
<p>This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A4

OAR_OAPERF_A4 - OAR Aggregate Perf Counter A4				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02820h			
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A4 Upper DWord

OAR_OAPERF_A4_UPPER - OAR Aggregate Perf Counter A4 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02824h	
<p>This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIReset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIReset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A5

OAR_OAPERF_A5 - OAR Aggregate Perf Counter A5				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02828h			
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A5 Upper DWord

OAR_OAPERF_A5_UPPER - OAR Aggregate Perf Counter A5 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0282Ch	
<p>This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A6

OAR_OAPERF_A6 - OAR Aggregate Perf Counter A6				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02830h			
This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A6 Upper DWord

OAR_OAPERF_A6_UPPER - OAR Aggregate Perf Counter A6 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02834h		
<p>This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A7

OAR_OAPERF_A7 - OAR Aggregate Perf Counter A7				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02838h			
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A7 Upper DWord

OAR_OAPERF_A7_UPPER - OAR Aggregate Perf Counter A7 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0283Ch		
<p>This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A8

OAR_OAPERF_A8 - OAR Aggregate Perf Counter A8				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02840h			
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A8 Upper DWord

OAR_OAPERF_A8_UPPER - OAR Aggregate Perf Counter A8 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02844h	
<p>This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A9

OAR_OAPERF_A9 - OAR Aggregate Perf Counter A9				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02848h			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A9 Upper DWord

OAR_OAPERF_A9_UPPER - OAR Aggregate Perf Counter A9 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0284Ch	
<p>This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A10

OAR_OAPERF_A10 - OAR Aggregate Perf Counter A10				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02850h			
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A10 Upper DWord

OAR_OAPERF_A10_UPPER - OAR Aggregate Perf Counter A10 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02854h		
<p>This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A11

OAR_OAPERF_A11 - OAR Aggregate Perf Counter A11				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02858h			
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A11 Upper DWord

OAR_OAPERF_A11_UPPER - OAR Aggregate Perf Counter A11 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0285Ch		
<p>This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A12

OAR_OAPERF_A12 - OAR Aggregate Perf Counter A12				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02860h			
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A12 Upper DWord

OAR_OAPERF_A12_UPPER - OAR Aggregate Perf Counter A12 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02864h		
<p>This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A13

OAR_OAPERF_A13 - OAR Aggregate Perf Counter A13				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02868h			
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A13 Upper DWord

OAR_OAPERF_A13_UPPER - OAR Aggregate Perf Counter A13 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0286Ch		
<p>This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A14

OAR_OAPERF_A14 - OAR Aggregate Perf Counter A14				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02870h			
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A14 Upper DWord

OAR_OAPERF_A14_UPPER - OAR Aggregate Perf Counter A14 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02874h		
<p>This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A15

OAR_OAPERF_A15 - OAR Aggregate Perf Counter A15				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02878h			
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A15 Upper DWord

OAR_OAPERF_A15_UPPER - OAR Aggregate Perf Counter A15 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0287Ch		
<p>This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A16

OAR_OAPERF_A16 - OAR Aggregate Perf Counter A16				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02880h			
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A16 Upper DWord

OAR_OAPERF_A16_UPPER - OAR Aggregate Perf Counter A16 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02884h		
<p>This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A17

OAR_OAPERF_A17 - OAR Aggregate Perf Counter A17				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02888h			
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A17 Upper DWord

OAR_OAPERF_A17_UPPER - OAR Aggregate Perf Counter A17 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0288Ch		
<p>This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A18

OAR_OAPERF_A18 - OAR Aggregate Perf Counter A18				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02890h			
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A18 Upper DWord

OAR_OAPERF_A18_UPPER - OAR Aggregate Perf Counter A18 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02894h		
<p>This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A19

OAR_OAPERF_A19 - OAR Aggregate Perf Counter A19				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02898h			
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A19 Upper DWord

OAR_OAPERF_A19_UPPER - OAR Aggregate Perf Counter A19 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0289Ch		
<p>This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A20

OAR_OAPERF_A20 - OAR Aggregate Perf Counter A20				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028A0h			
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A20 Upper DWord

OAR_OAPERF_A20_UPPER - OAR Aggregate Perf Counter A20 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028A4h		
<p>This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A21

OAR_OAPERF_A21 - OAR Aggregate Perf Counter A21				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028A8h			
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A21 Upper DWord

OAR_OAPERF_A21_UPPER - OAR Aggregate Perf Counter A21 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028ACh	
<p>This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A22

OAR_OAPERF_A22 - OAR Aggregate Perf Counter A22				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028B0h			
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A22 Upper DWord

OAR_OAPERF_A22_UPPER - OAR Aggregate Perf Counter A22 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028B4h		
<p>This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A23

OAR_OAPERF_A23 - OAR Aggregate Perf Counter A23				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028B8h			
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A23 Upper DWord

OAR_OAPERF_A23_UPPER - OAR Aggregate Perf Counter A23 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028BCh		
<p>This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A24

OAR_OAPERF_A24 - OAR Aggregate Perf Counter A24				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028C0h			
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A24 Upper DWord

OAR_OAPERF_A24_UPPER - OAR Aggregate Perf Counter A24 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028C4h		
<p>This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A25

OAR_OAPERF_A25 - OAR Aggregate Perf Counter A25				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028C8h			
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A25 Upper DWord

OAR_OAPERF_A25_UPPER - OAR Aggregate Perf Counter A25 Upper DWord					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	32				
Address:	028CCh				
<p>This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>					
DWord	Bit	Description			
0	31:8	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">PBC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	PBC	_Custom_GTIRreset:
	Format:	PBC			
	_Custom_GTIRreset:	DEV			
	7:0	Upper Value			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U8</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table>	Format:	U8	_Custom_GTIRreset:
Format:		U8			
_Custom_GTIRreset:		DEV			
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>					



OAR Aggregate Perf Counter A26

OAR_OAPERF_A26 - OAR Aggregate Perf Counter A26				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028D0h			
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A26 Upper DWord

OAR_OAPERF_A26_UPPER - OAR Aggregate Perf Counter A26 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028D4h		
<p>This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A27

OAR_OAPERF_A27 - OAR Aggregate Perf Counter A27				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028D8h			
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A27 Upper DWord

OAR_OAPERF_A27_UPPER - OAR Aggregate Perf Counter A27 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028DCh		
<p>This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A28

OAR_OAPERF_A28 - OAR Aggregate Perf Counter A28				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028E0h			
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A28 Upper DWord

OAR_OAPERF_A28_UPPER - OAR Aggregate Perf Counter A28 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028E4h		
<p>This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A29

OAR_OAPERF_A29 - OAR Aggregate Perf Counter A29				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028E8h			
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OAR Aggregate Perf Counter A29 Upper DWord

OAR_OAPERF_A29_UPPER - OAR Aggregate Perf Counter A29 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028ECh		
<p>This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A30

OAR_OAPERF_A30 - OAR Aggregate Perf Counter A30				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	028F0h			
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"				
DWord	Bit	Description		
0	31:0	Considerations <table border="1"><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

OAR Aggregate Perf Counter A30 Upper DWord

OAR_OAPERF_A30_UPPER - OAR Aggregate Perf Counter A30 Upper DWord			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	028F4h		
<p>This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>			
DWord	Bit	Description	
0	31:8	Reserved	
		Format:	PBC
		_Custom_GTIRreset:	DEV
	7:0	Upper Value	
		Format:	U8
		_Custom_GTIRreset:	DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>			



OAR Aggregate Perf Counter A31

OAR_OAPERF_A31 - OAR Aggregate Perf Counter A31						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	028F8h					
This register reflects the count value of the OA Performance counter A31						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAR Aggregate Perf Counter A31 Upper DWord

OAR_OAPERF_A31_UPPER - OAR Aggregate Perf Counter A31 Upper DWord		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028FCh	
<p>This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.</p>		
DWord	Bit	Description
0	31:8	Reserved
		Format: PBC
	_Custom_GTIRreset: DEV	
	7:0	Upper Value
		Format: U8
		_Custom_GTIRreset: DEV
<p>This 8-bit field returns bits 39:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>		



OAR Aggregate Perf Counter A32

OAR_OAPERF_A32 - OAR Aggregate Perf Counter A32						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02900h					
This register reflects the count value of the OA Performance counter A32						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAR Aggregate Perf Counter A33

OAR_OAPERF_A33 - OAR Aggregate Perf Counter A33						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02904h					
This register reflects the count value of the OA Performance counter A33						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAR Aggregate Perf Counter A34

OAR_OAPERF_A34 - OAR Aggregate Perf Counter A34						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02908h					
This register reflects the count value of the OA Performance Aggregating counter A34						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAR Aggregate Perf Counter A35

OAR_OAPERF_A35 - OAR Aggregate Perf Counter A35						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0290Ch					
This register reflects the count value of the OA Performance counter A35						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAR Boolean_Counter_B0

OAR_OAPERF_B0 - OAR Boolean_Counter_B0						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02920h					
This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAR Boolean_Counter_B1

OAR_OAPERF_B1 - OAR Boolean_Counter_B1						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02924h					
<p>This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					



OAR Boolean_Counter_B2

OAR_OAPERF_B2 - OAR Boolean_Counter_B2						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02928h					
This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAR Boolean_Counter_B3

OAR_OAPERF_B3 - OAR Boolean_Counter_B3						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0292Ch					
<p>This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAR Boolean_Counter_B4

OAR_OAPERF_B4 - OAR Boolean_Counter_B4						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02930h					
This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					

OAR Boolean_Counter_B5

OAR_OAPERF_B5 - OAR Boolean_Counter_B5						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02934h					
<p>This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					



OAR Boolean_Counter_B6

OAR_OAPERF_B6 - OAR Boolean_Counter_B6						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02938h					
<p>This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAR Boolean_Counter_B7

OAR_OAPERF_B7 - OAR Boolean_Counter_B7						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	0293Ch					
<p>This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.</p>						
DWord	Bit	Description				
0	31:0	<p>Considerations</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					



OAR GPU Ticks Counter

OAR_GPU_TICKS - OAR GPU Ticks Counter						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	02910h					
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.						
DWord	Bit	Description				
0	31:0	Considerations <table border="1"><tr><td>Format:</td><td>U32</td></tr><tr><td>_Custom_GTIRreset:</td><td>DEV</td></tr></table> <p>This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIRreset:	DEV
Format:	U32					
_Custom_GTIRreset:	DEV					

OAR GPU Ticks Counter Upper DWord

OAR_GPU_TICKS_UPPER - OAR GPU Ticks Counter Upper DWord						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
<p>Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.</p>						
DWord	Bit	Description				
0	31:0	<p>Upper Value</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.</p>	Format:	U32	_Custom_GTIReset:	DEV
Format:	U32					
_Custom_GTIReset:	DEV					



OAR Observation Architecture Control

OAR_OACONTROL - OAR Observation Architecture Control			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02960h		
Name:	OAR Observation Architecture Control		
ShortName:	OAR_OACONTROL		
This register controls OAR functionality, report format, and context filtering. If OAR is enabled then it should be enabled in CS as well			
DWord	Bit	Description	
0	31:4	Reserved	
		Format:	PBC
		_Custom_GTIReset:	DEV
	3:1	Counter Select	
		_Custom_GTIReset:	DEV
	This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.		
	0	Performance Counter Enable	
		Format:	Enable
		_Custom_GTIReset:	DEV
		Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.	
Programming Notes			
"OAR Context Enable" mode bit in RenderEngine CTX_SR_CTL register must be set when "Programmer Counter Enable" is set.			
OAC and OAR concurrent enabling is not supported (OAG is recommended instead).			

OAR Observation Architecture Status Register

OAR_OASTATUS - OAR Observation Architecture Status Register									
Register Space:	MMIO: 0/2/0								
Access:	R/W								
Size (in bits):	32								
Address:	02968h								
Name:	OAR Observation Architecture Status Register								
ShortName:	OAR_OASTATUS								
<p>This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)</p>									
DWord	Bit	Description							
0	31:22	Reserved							
		Format:	PBC						
		_Custom_GTIReset:	DEV						
	21		Start Trigger Flag 1						
			_Custom_GTIReset:	DEV					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1	
		Value	Name						
		0	[Default]						
		1							
	<p style="text-align: center;">Programming Notes</p>								
	<p>This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.</p>								
	20		Start Trigger Flag 2						
_Custom_GTIReset:			DEV						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> </tr> <tr> <td>1</td> <td></td> </tr> </tbody> </table>		Value	Name	0	[Default]	1			
Value		Name							
0		[Default]							
1									
<p style="text-align: center;">Programming Notes</p>									
<p>This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.</p>									
19		Report Trigger Flag 1							
		_Custom_GTIReset:	DEV						
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> </tr> </tbody> </table>		Value	Name					
Value	Name								

OAR_OASTATUS - OAR Observation Architecture Status Register

	0	[Default]
	1	
Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.		
18	Report Trigger Flag 2	
	_Custom_GTIRreset:	DEV
	Value	Name
	0	[Default]
	1	
Programming Notes		
This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.		
17:6	Reserved	
	Format:	PBC
	_Custom_GTIRreset:	DEV
5:2	Reserved	
	Format:	PBC
	_Custom_GTIRreset:	DEV
1	Accumulator Overflow	
	_Custom_GTIRreset:	DEV
This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.		
	Value	Name
	0	[Default]
	1	
		Description
	0	No overflow has occurred.
	1	Overflow has occurred.
0	Counter Overflow	
	_Custom_GTIRreset:	DEV
This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 1 to it.		
	Value	Name
	0	[Default]
	1	
		Description
	0	Counter Overflow not occurred
	1	Counter Overflow occurred

Observation Architecture Control Context ID

OACTXID - Observation Architecture Control Context ID				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	02364h			
Name:	Observation Architecture Control Context ID			
ShortName:	OACTXID			
<p>This register has the context details when Specific context Enable is set. This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.</p>				
DWord	Bit	Description		
0	31:0	<p>Select Context ID</p> <table border="1"> <tr> <td>_Custom_GTIRreset:</td> <td>DEV</td> </tr> </table> <p>Specifies the context ID of the one context that affects the performance counters when "Specific Context Enable" bit is set. All other contexts are ignored. Ring Buffer Mode of Scheduling: Bits[31:12] represent the CCID and bits [11:0] must be zero. Exclist mode of scheduling: Bits[31:0] represent the context id.</p>	_Custom_GTIRreset:	DEV
_Custom_GTIRreset:	DEV			

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	02360h		
Name:	Observation Architecture Control per Context		
ShortName:	OACTXCONTROL		
This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.			
DWord	Bit	Description	
0	31	Reserved	
		Format:	PBC
		_Custom_GTIReset:	DEV
	30:8	Reserved	
		Format:	PBC
		_Custom_GTIReset:	DEV
	7:2	Timer Period	
		_Custom_GTIReset:	DEV
		<p>Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: $\text{StrobePeriod} = \text{MinimumTimeStampPeriod} * 2^{(\text{TimerPeriod} + 1)}$ The exponent is defined by this field.</p> <p>Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.</p>	
	1	Timer Enable	
_Custom_GTIReset:		DEV	
<p>This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.</p> <p>When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all</p>			

OACTXCONTROL - Observation Architecture Control per Context		
	contexts.	
	Value	Name
		Description
	0h	Disable [Default]
		Counter does not get written out on regular interval
	1h	Enable
		Counter gets written out on regular intervals, defined by the Timer Period
0	Counter Stop-Resume Mechanism	
	_Custom_GTIReset:	DEV
	Value	Name
		Description
	1h	
		resume counting for all counters



Observation Architecture Head Pointer

OAG_OAHEADPTR - Observation Architecture Head Pointer				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0DB00h			
This register allows SW to program head pointer.				
DWord	Bit	Description		
0	31:6	Head Pointer		
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">_Custom_GTIReset:</td> <td style="width: 20%; padding: 2px;">DEV</td> </tr> </table>	_Custom_GTIReset:	DEV
		_Custom_GTIReset:	DEV	
		Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering.		
	Programming Notes			
SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.				
5:0	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">Format:</td> <td style="width: 20%; padding: 2px;">PBC</td> </tr> </table>	Format:	PBC
		Format:	PBC	
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%; padding: 2px;">_Custom_GTIReset:</td> <td style="width: 20%; padding: 2px;">DEV</td> </tr> </table>	_Custom_GTIReset:	DEV
_Custom_GTIReset:	DEV			

OUTPUT_CSC_COEFF

OUTPUT_CSC_COEFF		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	192	
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE	
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed	
Address:	49050h-49067h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_A	
Reset:	soft	
Address:	49150h-49167h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_B	
Reset:	soft	
Address:	49250h-49267h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_C	
Reset:	soft	
Address:	49350h-49367h	
Name:	Pipe Output CSC Coefficients	
ShortName:	OUTPUT_CSC_COEFF_D	
Reset:	soft	
DWord	Bit	Description
0	31:16	RY Format: CSC COEFFICIENT FORMAT
	15:0	GY Format: CSC COEFFICIENT FORMAT
1	31:16	BY Format: CSC COEFFICIENT FORMAT
	15:0	Reserved Access: RO Format: MBZ
2	31:16	RU Format: CSC COEFFICIENT FORMAT

OUTPUT_CSC_COEFF		
	15:0	GU Format: CSC COEFFICIENT FORMAT
3	31:16	BU Format: CSC COEFFICIENT FORMAT
	15:0	Reserved Access: RO Format: MBZ
4	31:16	RV Format: CSC COEFFICIENT FORMAT
	15:0	GV Format: CSC COEFFICIENT FORMAT
5	31:16	BV Format: CSC COEFFICIENT FORMAT
	15:0	Reserved Access: RO Format: MBZ

OUTPUT_CSC_POSTOFF

OUTPUT_CSC_POSTOFF		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	96	
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE	
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed	
Address:	49074h-4907Fh	
Name:	Pipe Output CSC Post-Offsets	
ShortName:	OUTPUT_CSC_POSTOFF_A	
Reset:	soft	
Address:	49174h-4917Fh	
Name:	Pipe Output CSC Post-Offsets	
ShortName:	OUTPUT_CSC_POSTOFF_B	
Reset:	soft	
Address:	49274h-4927Fh	
Name:	Pipe Output CSC Post-Offsets	
ShortName:	OUTPUT_CSC_POSTOFF_C	
Reset:	soft	
Address:	49374h-4937Fh	
Name:	Pipe Output CSC Post-Offsets	
ShortName:	OUTPUT_CSC_POSTOFF_D	
Reset:	soft	
<p>The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe output color space conversion (CSC).</p>		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
	12:0	PostCSC High Offset This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	Reserved
		Access: RO
		Format: MBZ

OUTPUT_CSC_POSTOFF					
	12:0	<p>PostCSC Medium Offset</p> <p>This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>			
2	31:13	<p>Reserved</p>			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
Format:	MBZ				
12:0	<p>PostCSC Low Offset</p> <p>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>				

OUTPUT_CSC_PREOFF

OUTPUT_CSC_PREOFF				
Register Space:	MMIO: 0/2/0			
Access:	Double Buffered			
Size (in bits):	96			
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE			
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed			
Address:	49068h-49073h			
Name:	Pipe Output CSC Pre-Offsets			
ShortName:	OUTPUT_CSC_PREOFF_A			
Reset:	soft			
Address:	49168h-49173h			
Name:	Pipe Output CSC Pre-Offsets			
ShortName:	OUTPUT_CSC_PREOFF_B			
Reset:	soft			
Address:	49268h-49273h			
Name:	Pipe Output CSC Pre-Offsets			
ShortName:	OUTPUT_CSC_PREOFF_C			
Reset:	soft			
Address:	49368h-49373h			
Name:	Pipe Output CSC Pre-Offsets			
ShortName:	OUTPUT_CSC_PREOFF_D			
Reset:	soft			
<p>The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe output color space conversion (CSC).</p>				
DWord	Bit	Description		
0	31:13	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
	12:0	<p>PreCSC High Offset</p> <p>This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>		
1	31:13	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			

OUTPUT_CSC_PREOFF					
	12:0	<p>PreCSC Medium Offset</p> <p>This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>			
2	31:13	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
Format:	MBZ				
12:0	<p>PreCSC Low Offset</p> <p>This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>				

Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation								
Register Space:	PCI: 0/2/0							
Size (in bits):	32							
Address:	0030Ch							
DWord	Bit	Description						
0	31:0	<p>Outstanding Page Request Allocation</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.</p>	Default Value:	00000000000000000000000000000000b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	00000000000000000000000000000000b							
Access:	R/W							
_Custom_GTIReset:	BUS							



Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	00308h	
DWord	Bit	Description
0	31:0	Outstanding Page Request Capacity
		Default Value: 00000000000000001000000000000000b
		Access: RO
		_Custom_GTIReset: BUS
		This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	0E454h			
Name:	PAGE_FAULT_MODE			
ShortName:	PAGE_FAULT_MODE			
This register is written as part of Context Submission to TDL. The data written is the lower 32 bits of the Context Descriptor Format structure.				
DWord	Bit	Description		
0	31:8	Reserved		
		Access:	RO	
		Format:	MBZ	
	7:6	FAULT_MODE		
		Access:	WO	
		Fault Model: Applicable only in advanced context		
		Value	Name	Description
		00b	Fault and Hang [Default]	In Legacy Context mode, this is the only valid encoding.
		01b	Fault and Halt	Restriction : Only valid in Advanced Context mode.
		010b	Fault and Stream	Restriction : Only valid in Advanced Context mode.
	Others	Reserved		
	5:0	Reserved		
Access:		RO		
Format:		MBZ		



Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT
Address:	18270h-18277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_POCSUNIT
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT
Address:	1C0270h-1C0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0
Address:	1C4270h-1C4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1
Address:	1C8270h-1C8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT0
Address:	1D0270h-1D0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT2
Address:	1D4270h-1D4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT3
Address:	1D8270h-1D8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT1
Address:	1E0270h-1E0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT4

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Address: 1E4270h-1E4277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_VCSUNIT5

Address: 1E8270h-1E8277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_VECSUNIT2

Address: 1F0270h-1F0277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_VCSUNIT6

Address: 1F4270h-1F4277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_VCSUNIT7

Address: 1F8270h-1F8277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_VECSUNIT3

Address: 1A270h-1A277h
 Name: Page Directory Pointer Descriptor - PDP0/PML4/PASID
 ShortName: PDP0_CCSUNIT0

PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition.
PASID[19:0]: Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling.
PML4[38:12]: Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected.
PDP0[38:12]: Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.
Note: This is a guest physical address.

Programming Notes

Execlist Based Scheduling: SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.

Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPTOR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP*_DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0_DESCRIPTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptors are context save restored in VCS, BCS and VECS engines and must be programmed following setup of CCID register, in case of PDP descriptors programmed without CCID set will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

DWord	Bit	Description		
0	63	PD Load Busy <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%; text-align: center;">RO</td> </tr> </table> <p>This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.</p>	Access:	RO
Access:	RO			
	62:0	PDP0 Descriptor		

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02278h-0227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_RCSUNIT
Address:	18278h-1827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_POCSUNIT
Address:	22278h-2227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_BCSUNIT
Address:	1C0278h-1C027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT0
Address:	1C4278h-1C427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT1
Address:	1C8278h-1C827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT0
Address:	1D0278h-1D027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT2
Address:	1D4278h-1D427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT3
Address:	1D8278h-1D827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT1
Address:	1E0278h-1E027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT4

PDP1 - Page Directory Pointer Descriptor - PDP1

Address:	1E4278h-1E427Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT5	
Address:	1E8278h-1E827Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VECSUNIT2	
Address:	1F0278h-1F027Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT6	
Address:	1F4278h-1F427Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VCSUNIT7	
Address:	1F8278h-1F827Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_VECSUNIT3	
Address:	1A278h-1A27Fh	
Name:	Page Directory Pointer Descriptor - PDP1	
ShortName:	PDP1_CCSUNIT0	
<p>PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. <i>Note: This is a guest physical address.</i></p>		
DWord	Bit	Description
0	63:0	PDP1 Descriptor

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02280h-02287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_RCSUNIT
Address:	18280h-18287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_POCSUNIT
Address:	22280h-22287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_BCSUNIT
Address:	1C0280h-1C0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT0
Address:	1C4280h-1C4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT1
Address:	1C8280h-1C8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT0
Address:	1D0280h-1D0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT2
Address:	1D4280h-1D4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT3
Address:	1D8280h-1D8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT1
Address:	1E0280h-1E0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT4

PDP2 - Page Directory Pointer Descriptor - PDP2

Address:	1E4280h-1E4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT5
Address:	1E8280h-1E8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT2
Address:	1F0280h-1F0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT6
Address:	1F4280h-1F4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT7
Address:	1F8280h-1F8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT3
Address:	1A280h-1A287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_CCSUNIT0

PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.
Note: This is a guest physical address.

DWord	Bit	Description
0	63:0	PDP2 Descriptor

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02288h-0228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_RCSUNIT
Address:	18288h-1828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_POCSUNIT
Address:	22288h-2228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_BCSUNIT
Address:	1C0288h-1C028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT0
Address:	1C4288h-1C428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT1
Address:	1C8288h-1C828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT0
Address:	1D0288h-1D028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT2
Address:	1D4288h-1D428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT3
Address:	1D8288h-1D828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT1
Address:	1E0288h-1E028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT4

PDP3 - Page Directory Pointer Descriptor - PDP3

Address:	1E4288h-1E428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT5
Address:	1E8288h-1E828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT2
Address:	1F0288h-1F028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT6
Address:	1F4288h-1F428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT7
Address:	1F8288h-1F828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT3
Address:	1A288h-1A28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_CCSUNIT0

PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.
Note: This is a guest physical address.

DWord	Bit	Description
0	63:0	PDP3 Descriptor

Page Req Queue Tail Shadow Register DW0

PRQTP_DW0 - Page Req Queue Tail Shadow Register DW0				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
_Custom_GTIReset:	BUS			
Address:	00EC4h-00EC7h			
DWord	Bit	Description		
0	31:0	TailPtr <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Shadow register for Page Req Queue Tail register DW0. Usage: GAM will provide the data which is readable via address F0C8.	Access:	R/W
Access:	R/W			



Page Req Queue Tail Shadow Register DW1

PRQTP_DW1 - Page Req Queue Tail Shadow Register DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	00EC8h-00ECBh	
DWord	Bit	Description
0	31:0	TailPtr Access: R/W Shadow register for Page Req Queue Tail register DW1. Usage: GAM will provide the data which is readable via address F0CC.

Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00304h		
DWord	Bit	Description	
0	15:2	Reserved	
		Access:	RO
		Format:	MBZ
	1	Reset	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
	<p>When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).</p>		
	0	Page-Request Enable	
		Default Value:	0b
Access:		R/W	
_Custom_GTIReset:		BUS	
<p>When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.</p>			



Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00300h		
Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification			
DWord	Bit	Description	
0	31:20	Next Capability Offset	
		Default Value:	000000000000b
		Access:	RO Variant
		_Custom_GTIReset:	BUS
			This is a hardwired pointer to the next item in the capabilities list. Value 000h (Default) indicates that this is the end of the PCI-Express Extended capability Linked List. When Graphics Virtualization is enabled, this field is hardwired to point to the next PCI Capability structure, the SRIOV Extended Capability Header at 320h. When Graphics Virtualization is disabled, this field will be hardwired to 000h to indicate the end of PCI-Express Extended capability Linked List.
	19:16	Version	
		Default Value:	0001b
		Access:	RO
		_Custom_GTIReset:	BUS
			Hardwired to capability version 1.
15:0	Capability ID		
	Default Value:	000000000010011b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
		Hardwired to the Page Request Extended Capability ID	

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIReset:	BUS		
Address:	0F0D0h		
Register to configure the base address and size of the page request queue.			
DWord	Bit	Description	
0	31:12	Page Request Queue Base Register	
		Default Value:	00000h
		Access:	R/W
		This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.	
	11:3	Reserved	
		Access:	RO
		Format:	MBZ
	2:0	Queue Size	
		Default Value:	000b
		Access:	R/W
This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).			



Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	0F0D4h	
Register to configure the base address and size of the page request queue.		
DWord	Bit	Description
0	31:0	Page Request Queue Base Register
		Default Value: 00000000h
		Access: R/W
		This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIReset:	BUS		
Address:	0F0C0h		
Register indicating the page request queue head.			
DWord	Bit	Description	
0	31:19	Reserved	
		Access:	RO
		Format:	MBZ
	18:4	Queue Head	
		Default Value:	000000000000000b
		Access:	R/W
			Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.
3:0	Reserved		
	Access:	RO	
	Format:	MBZ	



Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	0F0C4h	
Register indicating the page request queue head.		
DWord	Bit	Description
0	31:0	Page Request Queue Head Register 1 Reserved
		Default Value: 00000000h
		Access: RO
		Bit[63:32]: Reserved.

Page Request Queue Tail Register 0

PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIRreset:	BUS		
Address:	0F0C8h		
Register indicating the page request queue tail.			
DWord	Bit	Description	
0	31:1	Queue Tail	
		Default Value:	00000000000000000000000000000000b
		Access:	R/W
		Bit[31:19]: Reserved. Bit[18:4]: Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware. GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit. Bit[3:1]: Reserved.	
0	0	Valid Bit	
		Default Value:	0b
		Access:	R/W
This bit can only be cleared by SW, which also clears the other fields.			



Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request Queue Tail Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	BUS	
Address:	0F0CCh	
Register indicating the page request queue tail.		
DWord	Bit	Description
0	31:0	Page Request Queue Tail Register 1 Reserved
		Default Value: 00000000h
		Access: RO
		Bit[63:32]: Reserved.

Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00306h		
DWord	Bit	Description	
0	15	PRG Response PASID Required	
		Default Value:	1b
		Access:	RO
		_Custom_GTIRreset:	BUS
		<p>If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.</p>	
14:9	Reserved	Access:	RO
		Format:	MBZ
8	Stopped	Access:	RO
		_Custom_GTIRreset:	BUS
		<p>When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.</p>	
		Value	Name
		1b	[Default]
7:2	Reserved	Access:	RO
		Format:	MBZ
1	Unexpected Page Request Group Index	Default Value:	0b
		Access:	R/W One Clear
		_Custom_GTIRreset:	BUS
		<p>When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.</p>	

PR_STATUS_0_2_0_PCI - Page Request Status

0	<p>Response Failure</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W One Clear</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.</p>	Default Value:	0b	Access:	R/W One Clear	_Custom_GTIReset:	BUS
Default Value:	0b						
Access:	R/W One Clear						
_Custom_GTIReset:	BUS						

PAK_NUM_OF_SLICES

PAK_NUM_OF_SLICES - PAK_NUM_OF_SLICES		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12954h	
ShortName:	PAK_NUM_OF_SLICES1	
Address:	1C954h	
ShortName:	PAK_NUM_OF_SLICES2	
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
	Format: MBZ	
	15:0	Number of slices in a frame. This field indicates number of slices in the current frame. This register is updated at the end of each slice.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	128E8h		
DWord	Bit	Description	
0	31:22	Reserved	
		Access:	RO
		Format:	MBZ
	21	Incorrect IntraMBFlag in I-slice(AVCf)	
	20	Out of Range Symbol Code(AVC/mpeg2)	
	19	Incorrect MBType(AVC/mpeg2)	
	18	Motion Vectors are not inside the frame boundary(mpeg2)	
	17	Scale code is zero(mpeg2)	
	16	Incorrect DCTtype for given motionType(mpeg2)	
	15:8	MB Y-position This field indicates Macro Block(MB) Y- position where an error occurred while encoding.	
7:0	MB X-position This field indicates Macro Block(MB) X- position where an error occurred while encoding.		

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128E4h	
DWord	Bit	Description
0	31:22	Reserved
		Access: RO
		Format: MBZ
	21	Skip Run Greater Than 8192 (AVC)
	20	Incorrect SkipMB (AVC and mpeg2)
	19	Incorrect MV difference for dual-prime MB (mpeg2)
	18	End of Slice signal missing on last MB of a Row(mpeg2)
	17	Incorrect DCT type for field picture
	16	MVs are not within defined range by fcode
15:8	MB Y-position	
7:0	MB X-position	



PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	128ECh		
DWord	Bit	Description	
0	31:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	PAK Status	
		Value	Name
0			PAK engine is IDLE
1		PAK engine is currently generating bit stream.	

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX					
Register Space:	MMIO: 0/2/0				
Access:	R/W				
Size (in bits):	96				
Address:	4A420h-4A42Bh				
Name:	Pipe Extended Gamma Correction Max				
ShortName:	PAL_EXT_GC_MAX_A				
Reset:	soft				
Address:	4AC20h-4AC2Bh				
Name:	Pipe Extended Gamma Correction Max				
ShortName:	PAL_EXT_GC_MAX_B				
Reset:	soft				
Address:	4B420h-4B42Bh				
Name:	Pipe Extended Gamma Correction Max				
ShortName:	PAL_EXT_GC_MAX_C				
Reset:	soft				
Address:	4BC20h-4BC2Bh				
Name:	Pipe Extended Gamma Correction Max				
ShortName:	PAL_EXT_GC_MAX_D				
Reset:	soft				
DWord	Bit	Description			
0	31:19	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
18:0	Red Ext Max GC Point				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Default Value:</td> <td>11111111111111111111b</td> </tr> <tr> <td>Format:</td> <td>U3.16</td> </tr> </table> <p>The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.</p>	Default Value:	11111111111111111111b	Format:	U3.16
	Default Value:	11111111111111111111b			
Format:	U3.16				
1	31:19	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
18:0	Green Ext Max GC Point				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Default Value:</td> <td>11111111111111111111b</td> </tr> <tr> <td>Format:</td> <td>U3.16</td> </tr> </table> <p>The extended point for green color channel gamma correction. This value is represented in a</p>	Default Value:	11111111111111111111b	Format:	U3.16
	Default Value:	11111111111111111111b			
Format:	U3.16				

PAL_EXT_GC_MAX						
		3.16 format with 3 integer and 16 fractional bits.				
2	31:19	Reserved				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
	18:0	Blue Ext Max GC Point				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 45%;">Default Value:</td> <td>111111111111111111b</td> </tr> <tr> <td>Format:</td> <td>U3.16</td> </tr> </table>	Default Value:	111111111111111111b	Format:	U3.16
		Default Value:	111111111111111111b			
Format:	U3.16					
The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.						

PAL_EXT2_GC_MAX

PAL_EXT2_GC_MAX		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	96	
Address:	4A430h-4A43Bh	
Name:	Pipe Extended Second Gamma Correction Max	
ShortName:	PAL_EXT2_GC_MAX_A	
Reset:	soft	
Address:	4AC30h-4AC3Bh	
Name:	Pipe Extended Second Gamma Correction Max	
ShortName:	PAL_EXT2_GC_MAX_B	
Reset:	soft	
Address:	4B430h-4B43Bh	
Name:	Pipe Extended Second Gamma Correction Max	
ShortName:	PAL_EXT2_GC_MAX_C	
Reset:	soft	
Address:	4BC30h-4BC3Bh	
Name:	Pipe Extended Second Gamma Correction Max	
ShortName:	PAL_EXT2_GC_MAX_D	
Reset:	soft	
DWord	Bit	Description
0	31:19	Reserved
		Access: RO
	Format: MBZ	
	18:0	Red Ext Max GC Point
Default Value: 111111111111111111b		
Format: U3.16		
		The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	Reserved
		Access: RO
	Format: MBZ	
	18:0	Green Ext Max GC Point
Default Value: 111111111111111111b		
Format: U3.16		
		The extended point for green color channel gamma correction. This value is represented in a

PAL_EXT2_GC_MAX		
		3.16 format with 3 integer and 16 fractional bits.
2	31:19	Reserved
		Access: RO
		Format: MBZ
	18:0	Blue Ext Max GC Point
		Default Value: 111111111111111111b
		Format: U3.16
The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.		

PAL_GC_MAX

PAL_GC_MAX						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	96					
Address:	4A410h-4A41Bh					
Name:	Pipe Gamma Correction Max					
ShortName:	PAL_GC_MAX_A					
Reset:	soft					
Address:	4AC10h-4AC1Bh					
Name:	Pipe Gamma Correction Max					
ShortName:	PAL_GC_MAX_B					
Reset:	soft					
Address:	4B410h-4B41Bh					
Name:	Pipe Gamma Correction Max					
ShortName:	PAL_GC_MAX_C					
Reset:	soft					
Address:	4BC10h-4BC1Bh					
Name:	Pipe Gamma Correction Max					
ShortName:	PAL_GC_MAX_D					
Reset:	soft					
DWord	Bit	Description				
0	31:17	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
16:0		Red Max GC Point				
		<table border="1"> <tr> <td>Default Value:</td> <td>10000000000000000b</td> </tr> <tr> <td>Format:</td> <td>U1.16</td> </tr> </table>	Default Value:	10000000000000000b	Format:	U1.16
		Default Value:	10000000000000000b			
		Format:	U1.16			
The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.						
Restriction						
		The value should always be programmed to be less than or equal to 1.0.				
1	31:17	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					

PAL_GC_MAX						
	16:0	Green Max GC Point				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>100000000000000000b</td> </tr> <tr> <td>Format:</td> <td>U1.16</td> </tr> </table>	Default Value:	100000000000000000b	Format:	U1.16
	Default Value:	100000000000000000b				
	Format:	U1.16				
	Description					
	The 513th entry for the green color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.					
	Restriction					
	The value should always be programmed to be less than or equal to 1.0.					
	2	31:17	Reserved			
			<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:		RO				
Format:		MBZ				
16:0		Blue Max GC Point				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Default Value:</td> <td>100000000000000000b</td> </tr> <tr> <td>Format:</td> <td>U1.16</td> </tr> </table>	Default Value:	100000000000000000b	Format:	U1.16
		Default Value:	100000000000000000b			
		Format:	U1.16			
	Description					
	The 513th entry for the blue color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits.					
Restriction						
The value should always be programmed to be less than or equal to 1.0.						

PAL_LGC

PAL_LGC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A000h-4A003h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_A
Reset:	soft
Address:	4A004h-4A007h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_A
Reset:	soft
Address:	4A008h-4A00Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_A
Reset:	soft
Address:	4A00Ch-4A00Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_A
Reset:	soft
Address:	4A010h-4A013h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_A
Reset:	soft
Address:	4A014h-4A017h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_A
Reset:	soft
Address:	4A018h-4A01Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_A
Reset:	soft
Address:	4A01Ch-4A01Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_A

PAL_LGC	
Reset:	soft
Address:	4A020h-4A023h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_A
Reset:	soft
Address:	4A024h-4A027h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_A
Reset:	soft
Address:	4A028h-4A02Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_A
Reset:	soft
Address:	4A02Ch-4A02Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_A
Reset:	soft
Address:	4A030h-4A033h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_A
Reset:	soft
Address:	4A034h-4A037h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_A
Reset:	soft
Address:	4A038h-4A03Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_A
Reset:	soft
Address:	4A03Ch-4A03Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_A
Reset:	soft
Address:	4A040h-4A043h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_A

PAL_LGC	
Reset:	soft
Address:	4A044h-4A047h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_A
Reset:	soft
Address:	4A048h-4A04Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_A
Reset:	soft
Address:	4A04Ch-4A04Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_A
Reset:	soft
Address:	4A050h-4A053h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_A
Reset:	soft
Address:	4A054h-4A057h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_A
Reset:	soft
Address:	4A058h-4A05Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_A
Reset:	soft
Address:	4A05Ch-4A05Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_A
Reset:	soft
Address:	4A060h-4A063h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_A
Reset:	soft
Address:	4A064h-4A067h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_A

PAL_LGC	
Reset:	soft
Address:	4A068h-4A06Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_A
Reset:	soft
Address:	4A06Ch-4A06Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_A
Reset:	soft
Address:	4A070h-4A073h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_A
Reset:	soft
Address:	4A074h-4A077h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_A
Reset:	soft
Address:	4A078h-4A07Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_A
Reset:	soft
Address:	4A07Ch-4A07Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_A
Reset:	soft
Address:	4A080h-4A083h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_A
Reset:	soft
Address:	4A084h-4A087h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_A
Reset:	soft
Address:	4A088h-4A08Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_A

PAL_LGC	
Reset:	soft
Address:	4A08Ch-4A08Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_A
Reset:	soft
Address:	4A090h-4A093h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_A
Reset:	soft
Address:	4A094h-4A097h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_A
Reset:	soft
Address:	4A098h-4A09Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_A
Reset:	soft
Address:	4A09Ch-4A09Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_A
Reset:	soft
Address:	4A0A0h-4A0A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_A
Reset:	soft
Address:	4A0A4h-4A0A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_A
Reset:	soft
Address:	4A0A8h-4A0ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_A
Reset:	soft
Address:	4A0ACh-4A0AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_A

PAL_LGC	
Reset:	soft
Address:	4A0B0h-4A0B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_A
Reset:	soft
Address:	4A0B4h-4A0B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_A
Reset:	soft
Address:	4A0B8h-4A0BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_A
Reset:	soft
Address:	4A0BCh-4A0BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_A
Reset:	soft
Address:	4A0C0h-4A0C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_A
Reset:	soft
Address:	4A0C4h-4A0C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_A
Reset:	soft
Address:	4A0C8h-4A0CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_A
Reset:	soft
Address:	4A0CCh-4A0CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_A
Reset:	soft
Address:	4A0D0h-4A0D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_A

PAL_LGC	
Reset:	soft
Address:	4A0D4h-4A0D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_A
Reset:	soft
Address:	4A0D8h-4A0DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_A
Reset:	soft
Address:	4A0DCh-4A0DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_A
Reset:	soft
Address:	4A0E0h-4A0E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_A
Reset:	soft
Address:	4A0E4h-4A0E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_A
Reset:	soft
Address:	4A0E8h-4A0EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_A
Reset:	soft
Address:	4A0ECh-4A0EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_A
Reset:	soft
Address:	4A0F0h-4A0F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_A
Reset:	soft
Address:	4A0F4h-4A0F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_A

PAL_LGC	
Reset:	soft
Address:	4A0F8h-4A0FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_A
Reset:	soft
Address:	4A0FCh-4A0FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_A
Reset:	soft
Address:	4A100h-4A103h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_A
Reset:	soft
Address:	4A104h-4A107h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_A
Reset:	soft
Address:	4A108h-4A10Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_A
Reset:	soft
Address:	4A10Ch-4A10Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_A
Reset:	soft
Address:	4A110h-4A113h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_A
Reset:	soft
Address:	4A114h-4A117h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_A
Reset:	soft
Address:	4A118h-4A11Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_A

PAL_LGC	
Reset:	soft
Address:	4A11Ch-4A11Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_A
Reset:	soft
Address:	4A120h-4A123h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_A
Reset:	soft
Address:	4A124h-4A127h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_A
Reset:	soft
Address:	4A128h-4A12Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_A
Reset:	soft
Address:	4A12Ch-4A12Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_A
Reset:	soft
Address:	4A130h-4A133h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_A
Reset:	soft
Address:	4A134h-4A137h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_A
Reset:	soft
Address:	4A138h-4A13Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_A
Reset:	soft
Address:	4A13Ch-4A13Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_A

PAL_LGC	
Reset:	soft
Address:	4A140h-4A143h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_A
Reset:	soft
Address:	4A144h-4A147h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_A
Reset:	soft
Address:	4A148h-4A14Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_A
Reset:	soft
Address:	4A14Ch-4A14Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_A
Reset:	soft
Address:	4A150h-4A153h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_A
Reset:	soft
Address:	4A154h-4A157h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_A
Reset:	soft
Address:	4A158h-4A15Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_A
Reset:	soft
Address:	4A15Ch-4A15Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_A
Reset:	soft
Address:	4A160h-4A163h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_A

PAL_LGC	
Reset:	soft
Address:	4A164h-4A167h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_A
Reset:	soft
Address:	4A168h-4A16Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_A
Reset:	soft
Address:	4A16Ch-4A16Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_A
Reset:	soft
Address:	4A170h-4A173h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_A
Reset:	soft
Address:	4A174h-4A177h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_A
Reset:	soft
Address:	4A178h-4A17Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_A
Reset:	soft
Address:	4A17Ch-4A17Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_A
Reset:	soft
Address:	4A180h-4A183h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_A
Reset:	soft
Address:	4A184h-4A187h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_A

PAL_LGC	
Reset:	soft
Address:	4A188h-4A18Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_A
Reset:	soft
Address:	4A18Ch-4A18Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_A
Reset:	soft
Address:	4A190h-4A193h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_A
Reset:	soft
Address:	4A194h-4A197h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_A
Reset:	soft
Address:	4A198h-4A19Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_A
Reset:	soft
Address:	4A19Ch-4A19Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_A
Reset:	soft
Address:	4A1A0h-4A1A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_A
Reset:	soft
Address:	4A1A4h-4A1A7h
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ShortName:	PAL_LGC_105_A
Reset:	soft
Address:	4A1A8h-4A1ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_A

PAL_LGC	
Reset:	soft
Address:	4A1ACh-4A1AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_A
Reset:	soft
Address:	4A1B0h-4A1B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_A
Reset:	soft
Address:	4A1B4h-4A1B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_A
Reset:	soft
Address:	4A1B8h-4A1BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_A
Reset:	soft
Address:	4A1BCh-4A1BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_A
Reset:	soft
Address:	4A1C0h-4A1C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_A
Reset:	soft
Address:	4A1C4h-4A1C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_A
Reset:	soft
Address:	4A1C8h-4A1CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_A
Reset:	soft
Address:	4A1CCh-4A1CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_A

PAL_LGC	
Reset:	soft
Address:	4A1D0h-4A1D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_A
Reset:	soft
Address:	4A1D4h-4A1D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_A
Reset:	soft
Address:	4A1D8h-4A1DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_A
Reset:	soft
Address:	4A1DCh-4A1DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_A
Reset:	soft
Address:	4A1E0h-4A1E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_A
Reset:	soft
Address:	4A1E4h-4A1E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_A
Reset:	soft
Address:	4A1E8h-4A1EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_A
Reset:	soft
Address:	4A1ECh-4A1EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_A
Reset:	soft
Address:	4A1F0h-4A1F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_A

PAL_LGC	
Reset:	soft
Address:	4A1F4h-4A1F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_A
Reset:	soft
Address:	4A1F8h-4A1FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_A
Reset:	soft
Address:	4A1FCh-4A1FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_A
Reset:	soft
Address:	4A200h-4A203h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_A
Reset:	soft
Address:	4A204h-4A207h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_A
Reset:	soft
Address:	4A208h-4A20Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_A
Reset:	soft
Address:	4A20Ch-4A20Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_A
Reset:	soft
Address:	4A210h-4A213h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_A
Reset:	soft
Address:	4A214h-4A217h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_A

PAL_LGC	
Reset:	soft
Address:	4A218h-4A21Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_A
Reset:	soft
Address:	4A21Ch-4A21Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_A
Reset:	soft
Address:	4A220h-4A223h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_A
Reset:	soft
Address:	4A224h-4A227h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_A
Reset:	soft
Address:	4A228h-4A22Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_A
Reset:	soft
Address:	4A22Ch-4A22Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_A
Reset:	soft
Address:	4A230h-4A233h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_A
Reset:	soft
Address:	4A234h-4A237h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_A
Reset:	soft
Address:	4A238h-4A23Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_A

PAL_LGC	
Reset:	soft
Address:	4A23Ch-4A23Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_A
Reset:	soft
Address:	4A240h-4A243h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_A
Reset:	soft
Address:	4A244h-4A247h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_A
Reset:	soft
Address:	4A248h-4A24Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_A
Reset:	soft
Address:	4A24Ch-4A24Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_A
Reset:	soft
Address:	4A250h-4A253h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_A
Reset:	soft
Address:	4A254h-4A257h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_A
Reset:	soft
Address:	4A258h-4A25Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_A
Reset:	soft
Address:	4A25Ch-4A25Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_A

PAL_LGC	
Reset:	soft
Address:	4A260h-4A263h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_A
Reset:	soft
Address:	4A264h-4A267h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_A
Reset:	soft
Address:	4A268h-4A26Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_A
Reset:	soft
Address:	4A26Ch-4A26Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_A
Reset:	soft
Address:	4A270h-4A273h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_A
Reset:	soft
Address:	4A274h-4A277h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_A
Reset:	soft
Address:	4A278h-4A27Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_A
Reset:	soft
Address:	4A27Ch-4A27Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_A
Reset:	soft
Address:	4A280h-4A283h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_A

PAL_LGC	
Reset:	soft
Address:	4A284h-4A287h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_A
Reset:	soft
Address:	4A288h-4A28Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_A
Reset:	soft
Address:	4A28Ch-4A28Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_A
Reset:	soft
Address:	4A290h-4A293h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_A
Reset:	soft
Address:	4A294h-4A297h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_A
Reset:	soft
Address:	4A298h-4A29Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_A
Reset:	soft
Address:	4A29Ch-4A29Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_A
Reset:	soft
Address:	4A2A0h-4A2A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_A
Reset:	soft
Address:	4A2A4h-4A2A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_A

PAL_LGC	
Reset:	soft
Address:	4A2A8h-4A2ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_A
Reset:	soft
Address:	4A2ACh-4A2AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_A
Reset:	soft
Address:	4A2B0h-4A2B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_A
Reset:	soft
Address:	4A2B4h-4A2B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_A
Reset:	soft
Address:	4A2B8h-4A2BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_A
Reset:	soft
Address:	4A2BCh-4A2BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_A
Reset:	soft
Address:	4A2C0h-4A2C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_A
Reset:	soft
Address:	4A2C4h-4A2C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_A
Reset:	soft
Address:	4A2C8h-4A2CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_A

PAL_LGC	
Reset:	soft
Address:	4A2CCh-4A2CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_A
Reset:	soft
Address:	4A2D0h-4A2D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_A
Reset:	soft
Address:	4A2D4h-4A2D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_A
Reset:	soft
Address:	4A2D8h-4A2DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_A
Reset:	soft
Address:	4A2DCh-4A2DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_A
Reset:	soft
Address:	4A2E0h-4A2E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_A
Reset:	soft
Address:	4A2E4h-4A2E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_A
Reset:	soft
Address:	4A2E8h-4A2EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_A
Reset:	soft
Address:	4A2ECh-4A2EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_A

PAL_LGC	
Reset:	soft
Address:	4A2F0h-4A2F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_A
Reset:	soft
Address:	4A2F4h-4A2F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_A
Reset:	soft
Address:	4A2F8h-4A2FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_A
Reset:	soft
Address:	4A2FCh-4A2FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_A
Reset:	soft
Address:	4A300h-4A303h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_A
Reset:	soft
Address:	4A304h-4A307h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_A
Reset:	soft
Address:	4A308h-4A30Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_A
Reset:	soft
Address:	4A30Ch-4A30Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_A
Reset:	soft
Address:	4A310h-4A313h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_A

PAL_LGC	
Reset:	soft
Address:	4A314h-4A317h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_A
Reset:	soft
Address:	4A318h-4A31Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_A
Reset:	soft
Address:	4A31Ch-4A31Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_A
Reset:	soft
Address:	4A320h-4A323h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_A
Reset:	soft
Address:	4A324h-4A327h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_A
Reset:	soft
Address:	4A328h-4A32Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_A
Reset:	soft
Address:	4A32Ch-4A32Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_A
Reset:	soft
Address:	4A330h-4A333h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_A
Reset:	soft
Address:	4A334h-4A337h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_A

PAL_LGC	
Reset:	soft
Address:	4A338h-4A33Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_A
Reset:	soft
Address:	4A33Ch-4A33Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_A
Reset:	soft
Address:	4A340h-4A343h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_A
Reset:	soft
Address:	4A344h-4A347h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_A
Reset:	soft
Address:	4A348h-4A34Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_A
Reset:	soft
Address:	4A34Ch-4A34Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_A
Reset:	soft
Address:	4A350h-4A353h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_A
Reset:	soft
Address:	4A354h-4A357h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_A
Reset:	soft
Address:	4A358h-4A35Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_A

PAL_LGC	
Reset:	soft
Address:	4A35Ch-4A35Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_A
Reset:	soft
Address:	4A360h-4A363h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_A
Reset:	soft
Address:	4A364h-4A367h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_A
Reset:	soft
Address:	4A368h-4A36Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_A
Reset:	soft
Address:	4A36Ch-4A36Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_A
Reset:	soft
Address:	4A370h-4A373h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_A
Reset:	soft
Address:	4A374h-4A377h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_A
Reset:	soft
Address:	4A378h-4A37Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_A
Reset:	soft
Address:	4A37Ch-4A37Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_A

PAL_LGC	
Reset:	soft
Address:	4A380h-4A383h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_A
Reset:	soft
Address:	4A384h-4A387h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_A
Reset:	soft
Address:	4A388h-4A38Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_A
Reset:	soft
Address:	4A38Ch-4A38Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_A
Reset:	soft
Address:	4A390h-4A393h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_A
Reset:	soft
Address:	4A394h-4A397h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_A
Reset:	soft
Address:	4A398h-4A39Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_A
Reset:	soft
Address:	4A39Ch-4A39Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_A
Reset:	soft
Address:	4A3A0h-4A3A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_A

PAL_LGC	
Reset:	soft
Address:	4A3A4h-4A3A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_A
Reset:	soft
Address:	4A3A8h-4A3ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_A
Reset:	soft
Address:	4A3ACh-4A3AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_A
Reset:	soft
Address:	4A3B0h-4A3B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_A
Reset:	soft
Address:	4A3B4h-4A3B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_A
Reset:	soft
Address:	4A3B8h-4A3BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_A
Reset:	soft
Address:	4A3BCh-4A3BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_A
Reset:	soft
Address:	4A3C0h-4A3C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_A
Reset:	soft
Address:	4A3C4h-4A3C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_A

PAL_LGC	
Reset:	soft
Address:	4A3C8h-4A3CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_A
Reset:	soft
Address:	4A3CCh-4A3CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_A
Reset:	soft
Address:	4A3D0h-4A3D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_A
Reset:	soft
Address:	4A3D4h-4A3D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_A
Reset:	soft
Address:	4A3D8h-4A3DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_A
Reset:	soft
Address:	4A3DCh-4A3DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_A
Reset:	soft
Address:	4A3E0h-4A3E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_A
Reset:	soft
Address:	4A3E4h-4A3E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_A
Reset:	soft
Address:	4A3E8h-4A3EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_A

PAL_LGC	
Reset:	soft
Address:	4A3ECh-4A3EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_A
Reset:	soft
Address:	4A3F0h-4A3F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_A
Reset:	soft
Address:	4A3F4h-4A3F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_A
Reset:	soft
Address:	4A3F8h-4A3FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_A
Reset:	soft
Address:	4A3FCh-4A3FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_A
Reset:	soft
Address:	4A800h-4A803h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_B
Reset:	soft
Address:	4A804h-4A807h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_B
Reset:	soft
Address:	4A808h-4A80Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_B
Reset:	soft
Address:	4A80Ch-4A80Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_B

PAL_LGC	
Reset:	soft
Address:	4A810h-4A813h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_B
Reset:	soft
Address:	4A814h-4A817h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_B
Reset:	soft
Address:	4A818h-4A81Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_B
Reset:	soft
Address:	4A81Ch-4A81Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_B
Reset:	soft
Address:	4A820h-4A823h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_B
Reset:	soft
Address:	4A824h-4A827h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_B
Reset:	soft
Address:	4A828h-4A82Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_B
Reset:	soft
Address:	4A82Ch-4A82Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_B
Reset:	soft
Address:	4A830h-4A833h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_B

PAL_LGC	
Reset:	soft
Address:	4A834h-4A837h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_B
Reset:	soft
Address:	4A838h-4A83Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_B
Reset:	soft
Address:	4A83Ch-4A83Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_B
Reset:	soft
Address:	4A840h-4A843h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_B
Reset:	soft
Address:	4A844h-4A847h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_B
Reset:	soft
Address:	4A848h-4A84Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_B
Reset:	soft
Address:	4A84Ch-4A84Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_B
Reset:	soft
Address:	4A850h-4A853h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_B
Reset:	soft
Address:	4A854h-4A857h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_B

PAL_LGC	
Reset:	soft
Address:	4A858h-4A85Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_B
Reset:	soft
Address:	4A85Ch-4A85Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_B
Reset:	soft
Address:	4A860h-4A863h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_B
Reset:	soft
Address:	4A864h-4A867h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_B
Reset:	soft
Address:	4A868h-4A86Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_B
Reset:	soft
Address:	4A86Ch-4A86Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_B
Reset:	soft
Address:	4A870h-4A873h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_B
Reset:	soft
Address:	4A874h-4A877h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_B
Reset:	soft
Address:	4A878h-4A87Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_B

PAL_LGC	
Reset:	soft
Address:	4A87Ch-4A87Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_B
Reset:	soft
Address:	4A880h-4A883h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_B
Reset:	soft
Address:	4A884h-4A887h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_B
Reset:	soft
Address:	4A888h-4A88Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_B
Reset:	soft
Address:	4A88Ch-4A88Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_B
Reset:	soft
Address:	4A890h-4A893h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_B
Reset:	soft
Address:	4A894h-4A897h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_B
Reset:	soft
Address:	4A898h-4A89Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_B
Reset:	soft
Address:	4A89Ch-4A89Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_B

PAL_LGC	
Reset:	soft
Address:	4A8A0h-4A8A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_B
Reset:	soft
Address:	4A8A4h-4A8A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_B
Reset:	soft
Address:	4A8A8h-4A8ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_B
Reset:	soft
Address:	4A8ACh-4A8AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_B
Reset:	soft
Address:	4A8B0h-4A8B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_B
Reset:	soft
Address:	4A8B4h-4A8B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_B
Reset:	soft
Address:	4A8B8h-4A8BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_B
Reset:	soft
Address:	4A8BCh-4A8BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_B
Reset:	soft
Address:	4A8C0h-4A8C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_B

PAL_LGC	
Reset:	soft
Address:	4A8C4h-4A8C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_B
Reset:	soft
Address:	4A8C8h-4A8CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_B
Reset:	soft
Address:	4A8CCh-4A8CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_B
Reset:	soft
Address:	4A8D0h-4A8D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_B
Reset:	soft
Address:	4A8D4h-4A8D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_B
Reset:	soft
Address:	4A8D8h-4A8DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_B
Reset:	soft
Address:	4A8DCh-4A8DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_B
Reset:	soft
Address:	4A8E0h-4A8E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_B
Reset:	soft
Address:	4A8E4h-4A8E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_B

PAL_LGC	
Reset:	soft
Address:	4A8E8h-4A8EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_B
Reset:	soft
Address:	4A8ECh-4A8EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_B
Reset:	soft
Address:	4A8F0h-4A8F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_B
Reset:	soft
Address:	4A8F4h-4A8F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_B
Reset:	soft
Address:	4A8F8h-4A8FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_B
Reset:	soft
Address:	4A8FCh-4A8FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_B
Reset:	soft
Address:	4A900h-4A903h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_B
Reset:	soft
Address:	4A904h-4A907h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_B
Reset:	soft
Address:	4A908h-4A90Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_B

PAL_LGC	
Reset:	soft
Address:	4A90Ch-4A90Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_B
Reset:	soft
Address:	4A910h-4A913h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_B
Reset:	soft
Address:	4A914h-4A917h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_B
Reset:	soft
Address:	4A918h-4A91Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_B
Reset:	soft
Address:	4A91Ch-4A91Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_B
Reset:	soft
Address:	4A920h-4A923h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_B
Reset:	soft
Address:	4A924h-4A927h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_B
Reset:	soft
Address:	4A928h-4A92Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_B
Reset:	soft
Address:	4A92Ch-4A92Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_B

PAL_LGC	
Reset:	soft
Address:	4A930h-4A933h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_B
Reset:	soft
Address:	4A934h-4A937h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_B
Reset:	soft
Address:	4A938h-4A93Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_B
Reset:	soft
Address:	4A93Ch-4A93Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_B
Reset:	soft
Address:	4A940h-4A943h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_B
Reset:	soft
Address:	4A944h-4A947h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_B
Reset:	soft
Address:	4A948h-4A94Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_B
Reset:	soft
Address:	4A94Ch-4A94Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_B
Reset:	soft
Address:	4A950h-4A953h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_B

PAL_LGC	
Reset:	soft
Address:	4A954h-4A957h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_B
Reset:	soft
Address:	4A958h-4A95Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_B
Reset:	soft
Address:	4A95Ch-4A95Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_B
Reset:	soft
Address:	4A960h-4A963h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_B
Reset:	soft
Address:	4A964h-4A967h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_B
Reset:	soft
Address:	4A968h-4A96Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_B
Reset:	soft
Address:	4A96Ch-4A96Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_B
Reset:	soft
Address:	4A970h-4A973h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_B
Reset:	soft
Address:	4A974h-4A977h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_B

PAL_LGC	
Reset:	soft
Address:	4A978h-4A97Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_B
Reset:	soft
Address:	4A97Ch-4A97Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_B
Reset:	soft
Address:	4A980h-4A983h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_B
Reset:	soft
Address:	4A984h-4A987h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_B
Reset:	soft
Address:	4A988h-4A98Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_B
Reset:	soft
Address:	4A98Ch-4A98Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_B
Reset:	soft
Address:	4A990h-4A993h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_B
Reset:	soft
Address:	4A994h-4A997h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_B
Reset:	soft
Address:	4A998h-4A99Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_B

PAL_LGC	
Reset:	soft
Address:	4A99Ch-4A99Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_B
Reset:	soft
Address:	4A9A0h-4A9A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_B
Reset:	soft
Address:	4A9A4h-4A9A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_B
Reset:	soft
Address:	4A9A8h-4A9ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_B
Reset:	soft
Address:	4A9ACh-4A9AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_B
Reset:	soft
Address:	4A9B0h-4A9B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_B
Reset:	soft
Address:	4A9B4h-4A9B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_B
Reset:	soft
Address:	4A9B8h-4A9BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_B
Reset:	soft
Address:	4A9BCh-4A9BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_B

PAL_LGC	
Reset:	soft
Address:	4A9C0h-4A9C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_B
Reset:	soft
Address:	4A9C4h-4A9C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_B
Reset:	soft
Address:	4A9C8h-4A9CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_B
Reset:	soft
Address:	4A9CCh-4A9CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_B
Reset:	soft
Address:	4A9D0h-4A9D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_B
Reset:	soft
Address:	4A9D4h-4A9D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_B
Reset:	soft
Address:	4A9D8h-4A9DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_B
Reset:	soft
Address:	4A9DCh-4A9DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_B
Reset:	soft
Address:	4A9E0h-4A9E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_B

PAL_LGC	
Reset:	soft
Address:	4A9E4h-4A9E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_B
Reset:	soft
Address:	4A9E8h-4A9EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_B
Reset:	soft
Address:	4A9ECh-4A9EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_B
Reset:	soft
Address:	4A9F0h-4A9F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_B
Reset:	soft
Address:	4A9F4h-4A9F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_B
Reset:	soft
Address:	4A9F8h-4A9FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_B
Reset:	soft
Address:	4A9FCh-4A9FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_B
Reset:	soft
Address:	4AA00h-4AA03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_B
Reset:	soft
Address:	4AA04h-4AA07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_B

PAL_LGC	
Reset:	soft
Address:	4AA08h-4AA0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_B
Reset:	soft
Address:	4AA0Ch-4AA0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_B
Reset:	soft
Address:	4AA10h-4AA13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_B
Reset:	soft
Address:	4AA14h-4AA17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_B
Reset:	soft
Address:	4AA18h-4AA1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_B
Reset:	soft
Address:	4AA1Ch-4AA1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_B
Reset:	soft
Address:	4AA20h-4AA23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_B
Reset:	soft
Address:	4AA24h-4AA27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_B
Reset:	soft
Address:	4AA28h-4AA2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_B

PAL_LGC	
Reset:	soft
Address:	4AA2Ch-4AA2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_B
Reset:	soft
Address:	4AA30h-4AA33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_B
Reset:	soft
Address:	4AA34h-4AA37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_B
Reset:	soft
Address:	4AA38h-4AA3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_B
Reset:	soft
Address:	4AA3Ch-4AA3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_B
Reset:	soft
Address:	4AA40h-4AA43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_B
Reset:	soft
Address:	4AA44h-4AA47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_B
Reset:	soft
Address:	4AA48h-4AA4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_B
Reset:	soft
Address:	4AA4Ch-4AA4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_B

PAL_LGC	
Reset:	soft
Address:	4AA50h-4AA53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_B
Reset:	soft
Address:	4AA54h-4AA57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_B
Reset:	soft
Address:	4AA58h-4AA5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_B
Reset:	soft
Address:	4AA5Ch-4AA5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_B
Reset:	soft
Address:	4AA60h-4AA63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_B
Reset:	soft
Address:	4AA64h-4AA67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_B
Reset:	soft
Address:	4AA68h-4AA6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_B
Reset:	soft
Address:	4AA6Ch-4AA6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_B
Reset:	soft
Address:	4AA70h-4AA73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_B

PAL_LGC	
Reset:	soft
Address:	4AA74h-4AA77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_B
Reset:	soft
Address:	4AA78h-4AA7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_B
Reset:	soft
Address:	4AA7Ch-4AA7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_B
Reset:	soft
Address:	4AA80h-4AA83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_B
Reset:	soft
Address:	4AA84h-4AA87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_B
Reset:	soft
Address:	4AA88h-4AA8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_B
Reset:	soft
Address:	4AA8Ch-4AA8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_B
Reset:	soft
Address:	4AA90h-4AA93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_B
Reset:	soft
Address:	4AA94h-4AA97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_B

PAL_LGC	
Reset:	soft
Address:	4AA98h-4AA9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_B
Reset:	soft
Address:	4AA9Ch-4AA9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_B
Reset:	soft
Address:	4AAA0h-4AAA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_B
Reset:	soft
Address:	4AAA4h-4AAA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_B
Reset:	soft
Address:	4AAA8h-4AAABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_B
Reset:	soft
Address:	4AAACH-4AAAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_B
Reset:	soft
Address:	4AAB0h-4AAB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_B
Reset:	soft
Address:	4AAB4h-4AAB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_B
Reset:	soft
Address:	4AAB8h-4AABBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_B

PAL_LGC	
Reset:	soft
Address:	4AABCh-4AABFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_B
Reset:	soft
Address:	4AAC0h-4AAC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_B
Reset:	soft
Address:	4AAC4h-4AAC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_B
Reset:	soft
Address:	4AAC8h-4AACBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_B
Reset:	soft
Address:	4AACCh-4AACFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_B
Reset:	soft
Address:	4AAD0h-4AAD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_B
Reset:	soft
Address:	4AAD4h-4AAD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_B
Reset:	soft
Address:	4AAD8h-4AADBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_B
Reset:	soft
Address:	4AADCh-4AADFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_B

PAL_LGC	
Reset:	soft
Address:	4AAE0h-4AAE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_B
Reset:	soft
Address:	4AAE4h-4AAE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_B
Reset:	soft
Address:	4AAE8h-4AAEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_B
Reset:	soft
Address:	4AAECh-4AAEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_B
Reset:	soft
Address:	4AAF0h-4AAF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_B
Reset:	soft
Address:	4AAF4h-4AAF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_B
Reset:	soft
Address:	4AAF8h-4AAFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_B
Reset:	soft
Address:	4AAFCh-4AAFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_B
Reset:	soft
Address:	4AB00h-4AB03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_B

PAL_LGC	
Reset:	soft
Address:	4AB04h-4AB07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_B
Reset:	soft
Address:	4AB08h-4AB0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_B
Reset:	soft
Address:	4AB0Ch-4AB0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_B
Reset:	soft
Address:	4AB10h-4AB13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_B
Reset:	soft
Address:	4AB14h-4AB17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_B
Reset:	soft
Address:	4AB18h-4AB1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_B
Reset:	soft
Address:	4AB1Ch-4AB1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_B
Reset:	soft
Address:	4AB20h-4AB23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_B
Reset:	soft
Address:	4AB24h-4AB27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_B

PAL_LGC	
Reset:	soft
Address:	4AB28h-4AB2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_B
Reset:	soft
Address:	4AB2Ch-4AB2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_B
Reset:	soft
Address:	4AB30h-4AB33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_B
Reset:	soft
Address:	4AB34h-4AB37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_B
Reset:	soft
Address:	4AB38h-4AB3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_B
Reset:	soft
Address:	4AB3Ch-4AB3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_B
Reset:	soft
Address:	4AB40h-4AB43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_B
Reset:	soft
Address:	4AB44h-4AB47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_B
Reset:	soft
Address:	4AB48h-4AB4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_B

PAL_LGC	
Reset:	soft
Address:	4AB4Ch-4AB4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_B
Reset:	soft
Address:	4AB50h-4AB53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_B
Reset:	soft
Address:	4AB54h-4AB57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_B
Reset:	soft
Address:	4AB58h-4AB5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_B
Reset:	soft
Address:	4AB5Ch-4AB5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_B
Reset:	soft
Address:	4AB60h-4AB63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_B
Reset:	soft
Address:	4AB64h-4AB67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_B
Reset:	soft
Address:	4AB68h-4AB6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_B
Reset:	soft
Address:	4AB6Ch-4AB6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_B

PAL_LGC	
Reset:	soft
Address:	4AB70h-4AB73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_B
Reset:	soft
Address:	4AB74h-4AB77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_B
Reset:	soft
Address:	4AB78h-4AB7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_B
Reset:	soft
Address:	4AB7Ch-4AB7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_B
Reset:	soft
Address:	4AB80h-4AB83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_B
Reset:	soft
Address:	4AB84h-4AB87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_B
Reset:	soft
Address:	4AB88h-4AB8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_B
Reset:	soft
Address:	4AB8Ch-4AB8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_B
Reset:	soft
Address:	4AB90h-4AB93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_B

PAL_LGC	
Reset:	soft
Address:	4AB94h-4AB97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_B
Reset:	soft
Address:	4AB98h-4AB9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_B
Reset:	soft
Address:	4AB9Ch-4AB9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_B
Reset:	soft
Address:	4ABA0h-4ABA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_B
Reset:	soft
Address:	4ABA4h-4ABA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_B
Reset:	soft
Address:	4ABA8h-4ABABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_B
Reset:	soft
Address:	4ABACH-4ABAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_B
Reset:	soft
Address:	4ABB0h-4ABB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_B
Reset:	soft
Address:	4ABB4h-4ABB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_B

PAL_LGC	
Reset:	soft
Address:	4ABB8h-4ABBBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_B
Reset:	soft
Address:	4ABBCh-4ABBFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_B
Reset:	soft
Address:	4ABC0h-4ABC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_B
Reset:	soft
Address:	4ABC4h-4ABC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_B
Reset:	soft
Address:	4ABC8h-4ACBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_B
Reset:	soft
Address:	4ABCCh-4ABCFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_B
Reset:	soft
Address:	4ABD0h-4ABD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_B
Reset:	soft
Address:	4ABD4h-4ABD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_B
Reset:	soft
Address:	4ABD8h-4ABDBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_B

PAL_LGC	
Reset:	soft
Address:	4ABDCh-4ABDFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_B
Reset:	soft
Address:	4ABE0h-4ABE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_B
Reset:	soft
Address:	4ABE4h-4ABE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_B
Reset:	soft
Address:	4ABE8h-4ABEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_B
Reset:	soft
Address:	4ABECh-4ABEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_B
Reset:	soft
Address:	4ABF0h-4ABF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_B
Reset:	soft
Address:	4ABF4h-4ABF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_B
Reset:	soft
Address:	4ABF8h-4ABFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_B
Reset:	soft
Address:	4ABFCh-4ABFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_B

PAL_LGC	
Reset:	soft
Address:	4B000h-4B003h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_C
Reset:	soft
Address:	4B004h-4B007h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_C
Reset:	soft
Address:	4B008h-4B00Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_C
Reset:	soft
Address:	4B00Ch-4B00Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_C
Reset:	soft
Address:	4B010h-4B013h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_C
Reset:	soft
Address:	4B014h-4B017h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_C
Reset:	soft
Address:	4B018h-4B01Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_C
Reset:	soft
Address:	4B01Ch-4B01Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_C
Reset:	soft
Address:	4B020h-4B023h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_C

PAL_LGC	
Reset:	soft
Address:	4B024h-4B027h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_C
Reset:	soft
Address:	4B028h-4B02Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_C
Reset:	soft
Address:	4B02Ch-4B02Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_C
Reset:	soft
Address:	4B030h-4B033h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_C
Reset:	soft
Address:	4B034h-4B037h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_C
Reset:	soft
Address:	4B038h-4B03Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_C
Reset:	soft
Address:	4B03Ch-4B03Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_C
Reset:	soft
Address:	4B040h-4B043h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_C
Reset:	soft
Address:	4B044h-4B047h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_C

PAL_LGC	
Reset:	soft
Address:	4B048h-4B04Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_C
Reset:	soft
Address:	4B04Ch-4B04Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_C
Reset:	soft
Address:	4B050h-4B053h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_C
Reset:	soft
Address:	4B054h-4B057h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_C
Reset:	soft
Address:	4B058h-4B05Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_C
Reset:	soft
Address:	4B05Ch-4B05Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_C
Reset:	soft
Address:	4B060h-4B063h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_C
Reset:	soft
Address:	4B064h-4B067h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_C
Reset:	soft
Address:	4B068h-4B06Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_C

PAL_LGC	
Reset:	soft
Address:	4B06Ch-4B06Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_C
Reset:	soft
Address:	4B070h-4B073h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_C
Reset:	soft
Address:	4B074h-4B077h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_C
Reset:	soft
Address:	4B078h-4B07Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_C
Reset:	soft
Address:	4B07Ch-4B07Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_C
Reset:	soft
Address:	4B080h-4B083h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_C
Reset:	soft
Address:	4B084h-4B087h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_C
Reset:	soft
Address:	4B088h-4B08Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_C
Reset:	soft
Address:	4B08Ch-4B08Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_C

PAL_LGC	
Reset:	soft
Address:	4B090h-4B093h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_C
Reset:	soft
Address:	4B094h-4B097h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_C
Reset:	soft
Address:	4B098h-4B09Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_C
Reset:	soft
Address:	4B09Ch-4B09Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_C
Reset:	soft
Address:	4B0A0h-4B0A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_C
Reset:	soft
Address:	4B0A4h-4B0A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_C
Reset:	soft
Address:	4B0A8h-4B0ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_C
Reset:	soft
Address:	4B0ACh-4B0AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_C
Reset:	soft
Address:	4B0B0h-4B0B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_C

PAL_LGC	
Reset:	soft
Address:	4B0B4h-4B0B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_C
Reset:	soft
Address:	4B0B8h-4B0BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_C
Reset:	soft
Address:	4B0BCh-4B0BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_C
Reset:	soft
Address:	4B0C0h-4B0C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_C
Reset:	soft
Address:	4B0C4h-4B0C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_C
Reset:	soft
Address:	4B0C8h-4B0CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_C
Reset:	soft
Address:	4B0CCh-4B0CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_C
Reset:	soft
Address:	4B0D0h-4B0D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_C
Reset:	soft
Address:	4B0D4h-4B0D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_C

PAL_LGC	
Reset:	soft
Address:	4B0D8h-4B0DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_C
Reset:	soft
Address:	4B0DCh-4B0DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_C
Reset:	soft
Address:	4B0E0h-4B0E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_C
Reset:	soft
Address:	4B0E4h-4B0E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_C
Reset:	soft
Address:	4B0E8h-4B0EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_C
Reset:	soft
Address:	4B0ECh-4B0EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_C
Reset:	soft
Address:	4B0F0h-4B0F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_C
Reset:	soft
Address:	4B0F4h-4B0F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_C
Reset:	soft
Address:	4B0F8h-4B0FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_C

PAL_LGC	
Reset:	soft
Address:	4B0FCh-4B0FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_C
Reset:	soft
Address:	4B100h-4B103h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_C
Reset:	soft
Address:	4B104h-4B107h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_C
Reset:	soft
Address:	4B108h-4B10Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_C
Reset:	soft
Address:	4B10Ch-4B10Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_C
Reset:	soft
Address:	4B110h-4B113h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_C
Reset:	soft
Address:	4B114h-4B117h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_C
Reset:	soft
Address:	4B118h-4B11Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_C
Reset:	soft
Address:	4B11Ch-4B11Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_C

PAL_LGC	
Reset:	soft
Address:	4B120h-4B123h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_C
Reset:	soft
Address:	4B124h-4B127h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_C
Reset:	soft
Address:	4B128h-4B12Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_C
Reset:	soft
Address:	4B12Ch-4B12Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_C
Reset:	soft
Address:	4B130h-4B133h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_C
Reset:	soft
Address:	4B134h-4B137h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_C
Reset:	soft
Address:	4B138h-4B13Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_C
Reset:	soft
Address:	4B13Ch-4B13Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_C
Reset:	soft
Address:	4B140h-4B143h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_C

PAL_LGC	
Reset:	soft
Address:	4B144h-4B147h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_C
Reset:	soft
Address:	4B148h-4B14Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_C
Reset:	soft
Address:	4B14Ch-4B14Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_C
Reset:	soft
Address:	4B150h-4B153h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_C
Reset:	soft
Address:	4B154h-4B157h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_C
Reset:	soft
Address:	4B158h-4B15Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_C
Reset:	soft
Address:	4B15Ch-4B15Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_C
Reset:	soft
Address:	4B160h-4B163h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_C
Reset:	soft
Address:	4B164h-4B167h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_C

PAL_LGC	
Reset:	soft
Address:	4B168h-4B16Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_C
Reset:	soft
Address:	4B16Ch-4B16Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_C
Reset:	soft
Address:	4B170h-4B173h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_C
Reset:	soft
Address:	4B174h-4B177h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_C
Reset:	soft
Address:	4B178h-4B17Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_C
Reset:	soft
Address:	4B17Ch-4B17Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_C
Reset:	soft
Address:	4B180h-4B183h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_C
Reset:	soft
Address:	4B184h-4B187h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_C
Reset:	soft
Address:	4B188h-4B18Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_C

PAL_LGC	
Reset:	soft
Address:	4B18Ch-4B18Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_C
Reset:	soft
Address:	4B190h-4B193h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_C
Reset:	soft
Address:	4B194h-4B197h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_C
Reset:	soft
Address:	4B198h-4B19Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_C
Reset:	soft
Address:	4B19Ch-4B19Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_C
Reset:	soft
Address:	4B1A0h-4B1A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_C
Reset:	soft
Address:	4B1A4h-4B1A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_C
Reset:	soft
Address:	4B1A8h-4B1ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_C
Reset:	soft
Address:	4B1ACh-4B1AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_C

PAL_LGC	
Reset:	soft
Address:	4B1B0h-4B1B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_C
Reset:	soft
Address:	4B1B4h-4B1B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_C
Reset:	soft
Address:	4B1B8h-4B1BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_C
Reset:	soft
Address:	4B1BCh-4B1BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_C
Reset:	soft
Address:	4B1C0h-4B1C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_C
Reset:	soft
Address:	4B1C4h-4B1C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_C
Reset:	soft
Address:	4B1C8h-4B1CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_C
Reset:	soft
Address:	4B1CCh-4B1CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_C
Reset:	soft
Address:	4B1D0h-4B1D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_C

PAL_LGC	
Reset:	soft
Address:	4B1D4h-4B1D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_C
Reset:	soft
Address:	4B1D8h-4B1DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_C
Reset:	soft
Address:	4B1DCh-4B1DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_C
Reset:	soft
Address:	4B1E0h-4B1E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_C
Reset:	soft
Address:	4B1E4h-4B1E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_C
Reset:	soft
Address:	4B1E8h-4B1EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_C
Reset:	soft
Address:	4B1ECh-4B1EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_C
Reset:	soft
Address:	4B1F0h-4B1F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_C
Reset:	soft
Address:	4B1F4h-4B1F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_C

PAL_LGC	
Reset:	soft
Address:	4B1F8h-4B1FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_C
Reset:	soft
Address:	4B1FCh-4B1FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_C
Reset:	soft
Address:	4B200h-4B203h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_C
Reset:	soft
Address:	4B204h-4B207h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_C
Reset:	soft
Address:	4B208h-4B20Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_C
Reset:	soft
Address:	4B20Ch-4B20Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_C
Reset:	soft
Address:	4B210h-4B213h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_C
Reset:	soft
Address:	4B214h-4B217h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_C
Reset:	soft
Address:	4B218h-4B21Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_C

PAL_LGC	
Reset:	soft
Address:	4B21Ch-4B21Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_C
Reset:	soft
Address:	4B220h-4B223h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_C
Reset:	soft
Address:	4B224h-4B227h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_C
Reset:	soft
Address:	4B228h-4B22Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_C
Reset:	soft
Address:	4B22Ch-4B22Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_C
Reset:	soft
Address:	4B230h-4B233h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_C
Reset:	soft
Address:	4B234h-4B237h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_C
Reset:	soft
Address:	4B238h-4B23Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_C
Reset:	soft
Address:	4B23Ch-4B23Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_C

PAL_LGC	
Reset:	soft
Address:	4B240h-4B243h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_C
Reset:	soft
Address:	4B244h-4B247h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_C
Reset:	soft
Address:	4B248h-4B24Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_C
Reset:	soft
Address:	4B24Ch-4B24Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_C
Reset:	soft
Address:	4B250h-4B253h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_C
Reset:	soft
Address:	4B254h-4B257h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_C
Reset:	soft
Address:	4B258h-4B25Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_C
Reset:	soft
Address:	4B25Ch-4B25Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_C
Reset:	soft
Address:	4B260h-4B263h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_C

PAL_LGC	
Reset:	soft
Address:	4B264h-4B267h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_C
Reset:	soft
Address:	4B268h-4B26Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_C
Reset:	soft
Address:	4B26Ch-4B26Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_C
Reset:	soft
Address:	4B270h-4B273h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_C
Reset:	soft
Address:	4B274h-4B277h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_C
Reset:	soft
Address:	4B278h-4B27Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_C
Reset:	soft
Address:	4B27Ch-4B27Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_C
Reset:	soft
Address:	4B280h-4B283h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_C
Reset:	soft
Address:	4B284h-4B287h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_C

PAL_LGC	
Reset:	soft
Address:	4B288h-4B28Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_C
Reset:	soft
Address:	4B28Ch-4B28Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_C
Reset:	soft
Address:	4B290h-4B293h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_C
Reset:	soft
Address:	4B294h-4B297h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_C
Reset:	soft
Address:	4B298h-4B29Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_C
Reset:	soft
Address:	4B29Ch-4B29Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_C
Reset:	soft
Address:	4B2A0h-4B2A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_C
Reset:	soft
Address:	4B2A4h-4B2A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_C
Reset:	soft
Address:	4B2A8h-4B2ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_C

PAL_LGC	
Reset:	soft
Address:	4B2ACh-4B2AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_C
Reset:	soft
Address:	4B2B0h-4B2B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_C
Reset:	soft
Address:	4B2B4h-4B2B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_C
Reset:	soft
Address:	4B2B8h-4B2BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_C
Reset:	soft
Address:	4B2BCh-4B2BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_C
Reset:	soft
Address:	4B2C0h-4B2C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_C
Reset:	soft
Address:	4B2C4h-4B2C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_C
Reset:	soft
Address:	4B2C8h-4B2CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_C
Reset:	soft
Address:	4B2CCh-4B2CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_C

PAL_LGC	
Reset:	soft
Address:	4B2D0h-4B2D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_C
Reset:	soft
Address:	4B2D4h-4B2D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_C
Reset:	soft
Address:	4B2D8h-4B2DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_C
Reset:	soft
Address:	4B2DCh-4B2DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_C
Reset:	soft
Address:	4B2E0h-4B2E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_C
Reset:	soft
Address:	4B2E4h-4B2E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_C
Reset:	soft
Address:	4B2E8h-4B2EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_C
Reset:	soft
Address:	4B2ECh-4B2EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_C
Reset:	soft
Address:	4B2F0h-4B2F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_C

PAL_LGC	
Reset:	soft
Address:	4B2F4h-4B2F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_C
Reset:	soft
Address:	4B2F8h-4B2FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_C
Reset:	soft
Address:	4B2FCh-4B2FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_C
Reset:	soft
Address:	4B300h-4B303h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_C
Reset:	soft
Address:	4B304h-4B307h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_C
Reset:	soft
Address:	4B308h-4B30Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_C
Reset:	soft
Address:	4B30Ch-4B30Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_C
Reset:	soft
Address:	4B310h-4B313h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_C
Reset:	soft
Address:	4B314h-4B317h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_C

PAL_LGC	
Reset:	soft
Address:	4B318h-4B31Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_C
Reset:	soft
Address:	4B31Ch-4B31Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_C
Reset:	soft
Address:	4B320h-4B323h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_C
Reset:	soft
Address:	4B324h-4B327h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_C
Reset:	soft
Address:	4B328h-4B32Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_C
Reset:	soft
Address:	4B32Ch-4B32Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_C
Reset:	soft
Address:	4B330h-4B333h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_C
Reset:	soft
Address:	4B334h-4B337h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_C
Reset:	soft
Address:	4B338h-4B33Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_C

PAL_LGC	
Reset:	soft
Address:	4B33Ch-4B33Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_C
Reset:	soft
Address:	4B340h-4B343h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_C
Reset:	soft
Address:	4B344h-4B347h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_C
Reset:	soft
Address:	4B348h-4B34Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_C
Reset:	soft
Address:	4B34Ch-4B34Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_C
Reset:	soft
Address:	4B350h-4B353h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_C
Reset:	soft
Address:	4B354h-4B357h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_C
Reset:	soft
Address:	4B358h-4B35Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_C
Reset:	soft
Address:	4B35Ch-4B35Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_C

PAL_LGC	
Reset:	soft
Address:	4B360h-4B363h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_C
Reset:	soft
Address:	4B364h-4B367h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_C
Reset:	soft
Address:	4B368h-4B36Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_C
Reset:	soft
Address:	4B36Ch-4B36Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_C
Reset:	soft
Address:	4B370h-4B373h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_C
Reset:	soft
Address:	4B374h-4B377h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_C
Reset:	soft
Address:	4B378h-4B37Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_C
Reset:	soft
Address:	4B37Ch-4B37Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_C
Reset:	soft
Address:	4B380h-4B383h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_C

PAL_LGC	
Reset:	soft
Address:	4B384h-4B387h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_C
Reset:	soft
Address:	4B388h-4B38Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_C
Reset:	soft
Address:	4B38Ch-4B38Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_C
Reset:	soft
Address:	4B390h-4B393h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_C
Reset:	soft
Address:	4B394h-4B397h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_C
Reset:	soft
Address:	4B398h-4B39Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_C
Reset:	soft
Address:	4B39Ch-4B39Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_C
Reset:	soft
Address:	4B3A0h-4B3A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_C
Reset:	soft
Address:	4B3A4h-4B3A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_C

PAL_LGC	
Reset:	soft
Address:	4B3A8h-4B3ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_C
Reset:	soft
Address:	4B3ACh-4B3AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_C
Reset:	soft
Address:	4B3B0h-4B3B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_C
Reset:	soft
Address:	4B3B4h-4B3B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_C
Reset:	soft
Address:	4B3B8h-4B3BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_C
Reset:	soft
Address:	4B3BCh-4B3BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_C
Reset:	soft
Address:	4B3C0h-4B3C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_C
Reset:	soft
Address:	4B3C4h-4B3C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_C
Reset:	soft
Address:	4B3C8h-4B3CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_C

PAL_LGC	
Reset:	soft
Address:	4B3CCh-4B3CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_C
Reset:	soft
Address:	4B3D0h-4B3D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_C
Reset:	soft
Address:	4B3D4h-4B3D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_C
Reset:	soft
Address:	4B3D8h-4B3DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_C
Reset:	soft
Address:	4B3DCh-4B3DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_C
Reset:	soft
Address:	4B3E0h-4B3E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_C
Reset:	soft
Address:	4B3E4h-4B3E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_C
Reset:	soft
Address:	4B3E8h-4B3EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_C
Reset:	soft
Address:	4B3ECh-4B3EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_C

PAL_LGC	
Reset:	soft
Address:	4B3F0h-4B3F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_C
Reset:	soft
Address:	4B3F4h-4B3F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_C
Reset:	soft
Address:	4B3F8h-4B3FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_C
Reset:	soft
Address:	4B3FCh-4B3FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_C
Reset:	soft
Address:	4B800h-4B803h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_D
Reset:	soft
Address:	4B804h-4B807h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_D
Reset:	soft
Address:	4B808h-4B80Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_D
Reset:	soft
Address:	4B80Ch-4B80Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_D
Reset:	soft
Address:	4B810h-4B813h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_D

PAL_LGC	
Reset:	soft
Address:	4B814h-4B817h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_D
Reset:	soft
Address:	4B818h-4B81Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_D
Reset:	soft
Address:	4B81Ch-4B81Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_D
Reset:	soft
Address:	4B820h-4B823h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_D
Reset:	soft
Address:	4B824h-4B827h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_D
Reset:	soft
Address:	4B828h-4B82Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_D
Reset:	soft
Address:	4B82Ch-4B82Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_D
Reset:	soft
Address:	4B830h-4B833h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_D
Reset:	soft
Address:	4B834h-4B837h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_D

PAL_LGC	
Reset:	soft
Address:	4B838h-4B83Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_D
Reset:	soft
Address:	4B83Ch-4B83Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_D
Reset:	soft
Address:	4B840h-4B843h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_D
Reset:	soft
Address:	4B844h-4B847h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_D
Reset:	soft
Address:	4B848h-4B84Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_D
Reset:	soft
Address:	4B84Ch-4B84Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_D
Reset:	soft
Address:	4B850h-4B853h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_D
Reset:	soft
Address:	4B854h-4B857h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_D
Reset:	soft
Address:	4B858h-4B85Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_D

PAL_LGC	
Reset:	soft
Address:	4B85Ch-4B85Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_D
Reset:	soft
Address:	4B860h-4B863h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_D
Reset:	soft
Address:	4B864h-4B867h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_D
Reset:	soft
Address:	4B868h-4B86Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_D
Reset:	soft
Address:	4B86Ch-4B86Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_D
Reset:	soft
Address:	4B870h-4B873h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_D
Reset:	soft
Address:	4B874h-4B877h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_D
Reset:	soft
Address:	4B878h-4B87Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_D
Reset:	soft
Address:	4B87Ch-4B87Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_D

PAL_LGC	
Reset:	soft
Address:	4B880h-4B883h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_D
Reset:	soft
Address:	4B884h-4B887h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_D
Reset:	soft
Address:	4B888h-4B88Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_D
Reset:	soft
Address:	4B88Ch-4B88Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_D
Reset:	soft
Address:	4B890h-4B893h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_D
Reset:	soft
Address:	4B894h-4B897h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_D
Reset:	soft
Address:	4B898h-4B89Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_D
Reset:	soft
Address:	4B89Ch-4B89Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_D
Reset:	soft
Address:	4B8A0h-4B8A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_D

PAL_LGC	
Reset:	soft
Address:	4B8A4h-4B8A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_D
Reset:	soft
Address:	4B8A8h-4B8ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_D
Reset:	soft
Address:	4B8ACh-4B8AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_D
Reset:	soft
Address:	4B8B0h-4B8B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_D
Reset:	soft
Address:	4B8B4h-4B8B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_D
Reset:	soft
Address:	4B8B8h-4B8BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_D
Reset:	soft
Address:	4B8BCh-4B8BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_D
Reset:	soft
Address:	4B8C0h-4B8C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_D
Reset:	soft
Address:	4B8C4h-4B8C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_D

PAL_LGC	
Reset:	soft
Address:	4B8C8h-4B8CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_D
Reset:	soft
Address:	4B8CCh-4B8CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_D
Reset:	soft
Address:	4B8D0h-4B8D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_D
Reset:	soft
Address:	4B8D4h-4B8D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_D
Reset:	soft
Address:	4B8D8h-4B8DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_D
Reset:	soft
Address:	4B8DCh-4B8DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_D
Reset:	soft
Address:	4B8E0h-4B8E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_D
Reset:	soft
Address:	4B8E4h-4B8E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_D
Reset:	soft
Address:	4B8E8h-4B8EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_D

PAL_LGC	
Reset:	soft
Address:	4B8ECh-4B8EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_D
Reset:	soft
Address:	4B8F0h-4B8F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_D
Reset:	soft
Address:	4B8F4h-4B8F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_D
Reset:	soft
Address:	4B8F8h-4B8FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_D
Reset:	soft
Address:	4B8FCh-4B8FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_D
Reset:	soft
Address:	4B900h-4B903h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_D
Reset:	soft
Address:	4B904h-4B907h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_D
Reset:	soft
Address:	4B908h-4B90Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_D
Reset:	soft
Address:	4B90Ch-4B90Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_D

PAL_LGC	
Reset:	soft
Address:	4B910h-4B913h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_D
Reset:	soft
Address:	4B914h-4B917h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_D
Reset:	soft
Address:	4B918h-4B91Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_D
Reset:	soft
Address:	4B91Ch-4B91Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_D
Reset:	soft
Address:	4B920h-4B923h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_D
Reset:	soft
Address:	4B924h-4B927h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_D
Reset:	soft
Address:	4B928h-4B92Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_D
Reset:	soft
Address:	4B92Ch-4B92Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_D
Reset:	soft
Address:	4B930h-4B933h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_D

PAL_LGC	
Reset:	soft
Address:	4B934h-4B937h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_D
Reset:	soft
Address:	4B938h-4B93Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_D
Reset:	soft
Address:	4B93Ch-4B93Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_D
Reset:	soft
Address:	4B940h-4B943h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_D
Reset:	soft
Address:	4B944h-4B947h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_D
Reset:	soft
Address:	4B948h-4B94Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_D
Reset:	soft
Address:	4B94Ch-4B94Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_D
Reset:	soft
Address:	4B950h-4B953h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_D
Reset:	soft
Address:	4B954h-4B957h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_D

PAL_LGC	
Reset:	soft
Address:	4B958h-4B95Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_D
Reset:	soft
Address:	4B95Ch-4B95Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_D
Reset:	soft
Address:	4B960h-4B963h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_D
Reset:	soft
Address:	4B964h-4B967h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_D
Reset:	soft
Address:	4B968h-4B96Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_D
Reset:	soft
Address:	4B96Ch-4B96Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_D
Reset:	soft
Address:	4B970h-4B973h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_D
Reset:	soft
Address:	4B974h-4B977h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_D
Reset:	soft
Address:	4B978h-4B97Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_D

PAL_LGC	
Reset:	soft
Address:	4B97Ch-4B97Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_D
Reset:	soft
Address:	4B980h-4B983h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_D
Reset:	soft
Address:	4B984h-4B987h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_D
Reset:	soft
Address:	4B988h-4B98Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_D
Reset:	soft
Address:	4B98Ch-4B98Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_D
Reset:	soft
Address:	4B990h-4B993h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_D
Reset:	soft
Address:	4B994h-4B997h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_D
Reset:	soft
Address:	4B998h-4B99Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_D
Reset:	soft
Address:	4B99Ch-4B99Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_D

PAL_LGC	
Reset:	soft
Address:	4B9A0h-4B9A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_D
Reset:	soft
Address:	4B9A4h-4B9A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_D
Reset:	soft
Address:	4B9A8h-4B9ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_D
Reset:	soft
Address:	4B9ACh-4B9AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_D
Reset:	soft
Address:	4B9B0h-4B9B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_D
Reset:	soft
Address:	4B9B4h-4B9B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_D
Reset:	soft
Address:	4B9B8h-4B9BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_D
Reset:	soft
Address:	4B9BCh-4B9BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_D
Reset:	soft
Address:	4B9C0h-4B9C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_D

PAL_LGC	
Reset:	soft
Address:	4B9C4h-4B9C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_D
Reset:	soft
Address:	4B9C8h-4B9CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_D
Reset:	soft
Address:	4B9CCh-4B9CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_D
Reset:	soft
Address:	4B9D0h-4B9D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_D
Reset:	soft
Address:	4B9D4h-4B9D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_D
Reset:	soft
Address:	4B9D8h-4B9DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_D
Reset:	soft
Address:	4B9DCh-4B9DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_D
Reset:	soft
Address:	4B9E0h-4B9E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_D
Reset:	soft
Address:	4B9E4h-4B9E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_D

PAL_LGC	
Reset:	soft
Address:	4B9E8h-4B9EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_D
Reset:	soft
Address:	4B9ECh-4B9EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_D
Reset:	soft
Address:	4B9F0h-4B9F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_D
Reset:	soft
Address:	4B9F4h-4B9F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_D
Reset:	soft
Address:	4B9F8h-4B9FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_D
Reset:	soft
Address:	4B9FCh-4B9FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_D
Reset:	soft
Address:	4BA00h-4BA03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_D
Reset:	soft
Address:	4BA04h-4BA07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_D
Reset:	soft
Address:	4BA08h-4BA0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_D

PAL_LGC	
Reset:	soft
Address:	4BA0Ch-4BA0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_D
Reset:	soft
Address:	4BA10h-4BA13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_D
Reset:	soft
Address:	4BA14h-4BA17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_D
Reset:	soft
Address:	4BA18h-4BA1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_D
Reset:	soft
Address:	4BA1Ch-4BA1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_D
Reset:	soft
Address:	4BA20h-4BA23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_D
Reset:	soft
Address:	4BA24h-4BA27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_D
Reset:	soft
Address:	4BA28h-4BA2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_D
Reset:	soft
Address:	4BA2Ch-4BA2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_D

PAL_LGC	
Reset:	soft
Address:	4BA30h-4BA33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_D
Reset:	soft
Address:	4BA34h-4BA37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_D
Reset:	soft
Address:	4BA38h-4BA3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_D
Reset:	soft
Address:	4BA3Ch-4BA3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_D
Reset:	soft
Address:	4BA40h-4BA43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_D
Reset:	soft
Address:	4BA44h-4BA47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_D
Reset:	soft
Address:	4BA48h-4BA4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_D
Reset:	soft
Address:	4BA4Ch-4BA4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_D
Reset:	soft
Address:	4BA50h-4BA53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_D

PAL_LGC	
Reset:	soft
Address:	4BA54h-4BA57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_D
Reset:	soft
Address:	4BA58h-4BA5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_D
Reset:	soft
Address:	4BA5Ch-4BA5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_D
Reset:	soft
Address:	4BA60h-4BA63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_D
Reset:	soft
Address:	4BA64h-4BA67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_D
Reset:	soft
Address:	4BA68h-4BA6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_D
Reset:	soft
Address:	4BA6Ch-4BA6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_D
Reset:	soft
Address:	4BA70h-4BA73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_D
Reset:	soft
Address:	4BA74h-4BA77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_D

PAL_LGC	
Reset:	soft
Address:	4BA78h-4BA7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_D
Reset:	soft
Address:	4BA7Ch-4BA7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_D
Reset:	soft
Address:	4BA80h-4BA83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_D
Reset:	soft
Address:	4BA84h-4BA87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_D
Reset:	soft
Address:	4BA88h-4BA8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_D
Reset:	soft
Address:	4BA8Ch-4BA8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_D
Reset:	soft
Address:	4BA90h-4BA93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_D
Reset:	soft
Address:	4BA94h-4BA97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_D
Reset:	soft
Address:	4BA98h-4BA9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_D

PAL_LGC	
Reset:	soft
Address:	4BA9Ch-4BA9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_D
Reset:	soft
Address:	4BAA0h-4BAA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_D
Reset:	soft
Address:	4BAA4h-4BAA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_D
Reset:	soft
Address:	4BAA8h-4BAABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_D
Reset:	soft
Address:	4BAACH-4BAAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_D
Reset:	soft
Address:	4BAB0h-4BAB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_D
Reset:	soft
Address:	4BAB4h-4BAB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_D
Reset:	soft
Address:	4BAB8h-4BABBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_D
Reset:	soft
Address:	4BABCh-4BABFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_D

PAL_LGC	
Reset:	soft
Address:	4BAC0h-4BAC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_D
Reset:	soft
Address:	4BAC4h-4BAC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_D
Reset:	soft
Address:	4BAC8h-4BACBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_D
Reset:	soft
Address:	4BACCh-4BACFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_D
Reset:	soft
Address:	4BAD0h-4BAD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_D
Reset:	soft
Address:	4BAD4h-4BAD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_D
Reset:	soft
Address:	4BAD8h-4BADBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_D
Reset:	soft
Address:	4BADCh-4BADFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_D
Reset:	soft
Address:	4BAE0h-4BAE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_D

PAL_LGC	
Reset:	soft
Address:	4BAE4h-4BAE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_D
Reset:	soft
Address:	4BAE8h-4BAEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_D
Reset:	soft
Address:	4BAECh-4BAEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_D
Reset:	soft
Address:	4BAF0h-4BAF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_D
Reset:	soft
Address:	4BAF4h-4BAF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_D
Reset:	soft
Address:	4BAF8h-4BAFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_D
Reset:	soft
Address:	4BAFCh-4BAFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_D
Reset:	soft
Address:	4BB00h-4BB03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_D
Reset:	soft
Address:	4BB04h-4BB07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_D

PAL_LGC	
Reset:	soft
Address:	4BB08h-4BB0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_D
Reset:	soft
Address:	4BB0Ch-4BB0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_D
Reset:	soft
Address:	4BB10h-4BB13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_D
Reset:	soft
Address:	4BB14h-4BB17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_D
Reset:	soft
Address:	4BB18h-4BB1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_D
Reset:	soft
Address:	4BB1Ch-4BB1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_D
Reset:	soft
Address:	4BB20h-4BB23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_D
Reset:	soft
Address:	4BB24h-4BB27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_D
Reset:	soft
Address:	4BB28h-4BB2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_D

PAL_LGC	
Reset:	soft
Address:	4BB2Ch-4BB2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_D
Reset:	soft
Address:	4BB30h-4BB33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_D
Reset:	soft
Address:	4BB34h-4BB37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_D
Reset:	soft
Address:	4BB38h-4BB3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_D
Reset:	soft
Address:	4BB3Ch-4BB3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_D
Reset:	soft
Address:	4BB40h-4BB43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_D
Reset:	soft
Address:	4BB44h-4BB47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_D
Reset:	soft
Address:	4BB48h-4BB4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_D
Reset:	soft
Address:	4BB4Ch-4BB4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_D

PAL_LGC	
Reset:	soft
Address:	4BB50h-4BB53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_D
Reset:	soft
Address:	4BB54h-4BB57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_D
Reset:	soft
Address:	4BB58h-4BB5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_D
Reset:	soft
Address:	4BB5Ch-4BB5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_D
Reset:	soft
Address:	4BB60h-4BB63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_D
Reset:	soft
Address:	4BB64h-4BB67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_D
Reset:	soft
Address:	4BB68h-4BB6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_D
Reset:	soft
Address:	4BB6Ch-4BB6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_D
Reset:	soft
Address:	4BB70h-4BB73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_D

PAL_LGC	
Reset:	soft
Address:	4BB74h-4BB77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_D
Reset:	soft
Address:	4BB78h-4BB7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_D
Reset:	soft
Address:	4BB7Ch-4BB7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_D
Reset:	soft
Address:	4BB80h-4BB83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_D
Reset:	soft
Address:	4BB84h-4BB87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_D
Reset:	soft
Address:	4BB88h-4BB8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_D
Reset:	soft
Address:	4BB8Ch-4BB8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_D
Reset:	soft
Address:	4BB90h-4BB93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_D
Reset:	soft
Address:	4BB94h-4BB97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_D

PAL_LGC	
Reset:	soft
Address:	4BB98h-4BB9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_D
Reset:	soft
Address:	4BB9Ch-4BB9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_D
Reset:	soft
Address:	4BBA0h-4BBA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_D
Reset:	soft
Address:	4BBA4h-4BBA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_D
Reset:	soft
Address:	4BBA8h-4BBABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_D
Reset:	soft
Address:	4BBACH-4BBAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_D
Reset:	soft
Address:	4BBB0h-4BBB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_D
Reset:	soft
Address:	4BBB4h-4BBB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_D
Reset:	soft
Address:	4BBB8h-4BBBBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_D

PAL_LGC	
Reset:	soft
Address:	4BBBCh-4BBBFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_D
Reset:	soft
Address:	4BBC0h-4BBC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_D
Reset:	soft
Address:	4BBC4h-4BBC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_D
Reset:	soft
Address:	4BBC8h-4BBCBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_D
Reset:	soft
Address:	4BBCCh-4BBCFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_D
Reset:	soft
Address:	4BBD0h-4BBD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_D
Reset:	soft
Address:	4BBD4h-4BBD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_D
Reset:	soft
Address:	4BBD8h-4BBD Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_D
Reset:	soft
Address:	4BBDCh-4BBD Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_D

PAL_LGC	
Reset:	soft
Address:	4BBE0h-4BBE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_D
Reset:	soft
Address:	4BBE4h-4BBE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_D
Reset:	soft
Address:	4BBE8h-4BBEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_D
Reset:	soft
Address:	4BBECh-4BBEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_D
Reset:	soft
Address:	4BBF0h-4BBF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_D
Reset:	soft
Address:	4BBF4h-4BBF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_D
Reset:	soft
Address:	4BBF8h-4BBFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_D
Reset:	soft
Address:	4BBFCh-4BBFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_D
Reset:	soft
There are 256 instances of this register format per display pipe.	
Restriction	
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.	

DWord	Bit	Description	
0	31:24	Reserved	
		Access:	RO
		Format:	MBZ
	23:16	Red Legacy Palette Entry	
		Default Value:	UUh
		Red legacy palette entry value.	
	15:8	Green Legacy Palette Entry	
		Default Value:	UUh
		Green legacy palette entry value.	
	7:0	Blue Legacy Palette Entry	
		Default Value:	UUh
		Blue legacy palette entry value.	



PAL_PREC_DATA

PAL_PREC_DATA						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	4A404h-4A407h					
Name:	Pipe Precision Palette Data					
ShortName:	PAL_PREC_DATA_A					
Reset:	soft					
Address:	4AC04h-4AC07h					
Name:	Pipe Precision Palette Data					
ShortName:	PAL_PREC_DATA_B					
Reset:	soft					
Address:	4B404h-4B407h					
Name:	Pipe Precision Palette Data					
ShortName:	PAL_PREC_DATA_C					
Reset:	soft					
Address:	4BC04h-4BC07h					
Name:	Pipe Precision Palette Data					
ShortName:	PAL_PREC_DATA_D					
Reset:	soft					
<p>These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.</p>						
Programming Notes						
<p>For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSBs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs. For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value. For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.</p>						
Restriction						
<p>This register must be written only as a full 32 bit dword. Byte or word writes are not supported.</p>						
DWord	Bit	Description				
0	31:30	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					

PAL_PREC_DATA		
	29:20	Red Precision Palette Entry
		Default Value: UUUUUUUUUUUb
		Red precision palette entry value.
	19:10	Green Precision Palette Entry
		Default Value: UUUUUUUUUUUb
		Green precision palette entry value.
	9:0	Blue Precision Palette Entry
		Default Value: UUUUUUUUUUUb
		Blue precision palette entry value.



PAL_PREC_INDEX

PAL_PREC_INDEX				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	4A400h-4A403h			
Name:	Pipe Precision Palette Index			
ShortName:	PAL_PREC_INDEX_A			
Reset:	soft			
Address:	4AC00h-4AC03h			
Name:	Pipe Precision Palette Index			
ShortName:	PAL_PREC_INDEX_B			
Reset:	soft			
Address:	4B400h-4B403h			
Name:	Pipe Precision Palette Index			
ShortName:	PAL_PREC_INDEX_C			
Reset:	soft			
Address:	4BC00h-4BC03h			
Name:	Pipe Precision Palette Index			
ShortName:	PAL_PREC_INDEX_D			
Reset:	soft			
This index controls access to the array of precision palette data values.				
DWord	Bit	Description		
0	31:16	Reserved		
		Access:	RO	
		Format:	MBZ	
	15	Index Auto Increment		
		This field enables the index auto increment.		
		Value	Name	Description
		0b	No Increment	Do not automatically increment the index value.
		1b	Auto Increment	Increment the index value with each read or write to the data register.
	14:10	Reserved		
		Access:	RO	
Format:		MBZ		

PAL_PREC_INDEX						
	9:0	<p>Index Value</p> <p>This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,1023]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,1023]	
Value	Name					
[0,1023]						



PAL_PREC_MULTI_SEG_DATA

PAL_PREC_MULTI_SEG_DATA		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	4A40Ch-4A40Fh	
Name:	Pipe Precision Multi Segment Palette Data	
ShortName:	PAL_PREC_MULTI_SEG_DATA_A	
Reset:	soft	
Address:	4AC0Ch-4AC0Fh	
Name:	Pipe Precision Multi Segment Palette Data	
ShortName:	PAL_PREC_MULTI_SEG_DATA_B	
Reset:	soft	
Address:	4B40Ch-4B40Fh	
Name:	Pipe Precision Multi Segment Palette Data	
ShortName:	PAL_PREC_MULTI_SEG_DATA_C	
Reset:	soft	
Address:	4BC0Ch-4BC0Fh	
Name:	Pipe Precision Multi Segment Palette Data	
ShortName:	PAL_PREC_MULTI_SEG_DATA_D	
Reset:	soft	
<p>These are the precision palette entries used for the multi segment gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.</p>		
Programming Notes		
<p>For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSBs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.</p>		
Restriction		
<p>This register must be written only as a full 32 bit dword. Byte or word writes are not supported.</p>		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
	Format: MBZ	
	29:20	Red Precision Palette Entry
Default Value: UUUUUUUUUUbb Red precision palette entry value.		

PAL_PREC_MULTI_SEG_DATA			
	19:10	Green Precision Palette Entry	
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>UUUUUUUUUUUb</td> </tr> </table> <p>Green precision palette entry value.</p>	Default Value:
	Default Value:	UUUUUUUUUUU b	
	9:0	Blue Precision Palette Entry	
<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>UUUUUUUUUUUb</td> </tr> </table> <p>Blue precision palette entry value.</p>		Default Value:	UUUUUUUUUUU b
Default Value:	UUUUUUUUUUU b		



PAL_PREC_MULTI_SEG_INDEX

PAL_PREC_MULTI_SEG_INDEX				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	4A408h-4A40Bh			
Name:	Pipe Precision Multi Segment Palette Index			
ShortName:	PAL_PREC_MULTI_SEG_INDEX_A			
Reset:	soft			
Address:	4AC08h-4AC0Bh			
Name:	Pipe Precision Multi Segment Palette Index			
ShortName:	PAL_PREC_MULTI_SEG_INDEX_B			
Reset:	soft			
Address:	4B408h-4B40Bh			
Name:	Pipe Precision Multi Segment Palette Index			
ShortName:	PAL_PREC_MULTI_SEG_INDEX_C			
Reset:	soft			
Address:	4BC08h-4BC0Bh			
Name:	Pipe Precision Multi Segment Palette Index			
ShortName:	PAL_PREC_MULTI_SEG_INDEX_D			
Reset:	soft			
This index controls access to the array of precision palette data values used in the multi-segment gamma mode.				
DWord	Bit	Description		
0	31:16	Reserved		
		Access:	RO	
		Format:	MBZ	
	15	Index Auto Increment		
		This field enables the index auto increment.		
		Value	Name	Description
		0b	No Increment	Do not automatically increment the index value.
	1b	Auto Increment	Increment the index value with each read or write to the data register.	
	14:5	Reserved		
		Access:	RO	
Format:		MBZ		

PAL_PREC_MULTI_SEG_INDEX

	4:0	<p>Index Value</p> <p>This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.</p>				
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0,17]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,17]	
Value	Name					
[0,17]						



PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00104h		
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.			
DWord	Bit	Description	
0	15:13	Reserved	
		Access:	RO
		Format:	MBZ
	12:8	Maximum PASID Width	
		Default Value:	10100b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).		
	7:3	Reserved	
		Access:	RO
Format:		MBZ	
2	Privilege Mode Supported		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.			
1	Execute Permission Supported		
	Access:	RO	
	_Custom_GTIRreset:	BUS	
	Description		
	Hardwired to 0, the Endpoint supports requests-with-PASID that requests execute permission.		
	Value	Name	
0b	[Default]		
0	Reserved		
	Access:	RO	
	Format:	MBZ	

PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00106h		
Process Address Space ID (PASID) control for Device-2.			
DWord	Bit	Description	
0	15:3	Reserved	
		Access:	RO
		Format:	MBZ
	2	Privileged Mode Enable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.		
	1	Execute Permission Enable	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIRreset:	BUS
If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.			
0	PASID Enable		
	Default Value:	0b	
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Privileged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0).Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.			



PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00100h		
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.			
DWord	Bit	Description	
0	31:20	Next Capability Offset	
		Default Value:	001000000000b
		Access:	RO
		_Custom_GTIReset:	BUS
			This is a hardwired pointer to the next item in the capabilities list.
	19:16	Version	
		Default Value:	0001b
		Access:	RO
		_Custom_GTIReset:	BUS
			Hardwired to capability version 1.
	15:0	Capability ID	
		Default Value:	000000000011011b
Access:		RO	
_Custom_GTIReset:		BUS	
		Hardwired to the PASID Extended Capability ID	

PAT Index

PAT_INDEX - PAT Index		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	04800h	
Name:	PAT INDEX 0	
ShortName:	PAT_INDEX_0	
Address:	04804h	
Name:	PAT INDEX 1	
ShortName:	PAT_INDEX_1	
Address:	04808h	
Name:	PAT INDEX 2	
ShortName:	PAT_INDEX_2	
Address:	0480Ch	
Name:	PAT INDEX 3	
ShortName:	PAT_INDEX_3	
Address:	04810h	
Name:	PAT INDEX 4	
ShortName:	PAT_INDEX_4	
Address:	04814h	
Name:	PAT INDEX 5	
ShortName:	PAT_INDEX_5	
Address:	04818h	
Name:	PAT INDEX 6	
ShortName:	PAT_INDEX_6	
Address:	0481Ch	
Name:	PAT INDEX 7	
ShortName:	PAT_INDEX_7	
DWord	Bit	Description
0	31:4	Reserved
		Access: RO
	Format: MBZ	
	3:2	Reserved
Access: RO		
Format: MBZ		

PAT_INDEX - PAT Index		
	1:0	Mem Type
		Default Value: 11b
		Access: R/W
		00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB)

PCI Command

PCICMD_0_2_0_PCI - PCI Command			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00004h		
This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant primary accesses to main memory.			
DWord	Bit	Description	
0	15:11	Reserved	
		Access:	RO
		Format:	MBZ
	10	Interrupt Disable	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.		
	9	Fast Back-to-Back	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Not Implemented. Hardwired to 0.		
	8	SERR Enable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Not Implemented. Hardwired to 0.		
	7	Wait Cycle Control	
		Default Value:	0b
Access:		RO	
_Custom_GTIRreset:		BUS	
Not Implemented. Hardwired to 0.			
6	Parity Error Enable		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does			

PCICMD_0_2_0_PCI - PCI Command

		not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	Video Palette Snooping	
	Default Value:	0b
	Access:	RO
	_Custom_GTIRreset:	BUS
	This bit is hardwired to 0 to disable snooping.	
4	Memory Write and Invalidate Enable	
	Default Value:	0b
	Access:	RO
	_Custom_GTIRreset:	BUS
	Hardwired to 0. The IGD does not support memory write and invalidate commands.	
3	Special Cycle Enable	
	Default Value:	0b
	Access:	RO
	_Custom_GTIRreset:	BUS
	This bit is hardwired to 0. The IGD ignores Special cycles.	
2	Bus Primary Enable	
	Default Value:	0b
	Access:	R/W
	_Custom_GTIRreset:	BUS
	0: Disable IGD bus primaring. 1: Enable the IGD to function as a PCI compliant primary.	
1	Memory Access Enable	
	Default Value:	0b
	Access:	R/W
	_Custom_GTIRreset:	BUS
	This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.	
0	I/O Access Enable	
	Default Value:	0b
	Access:	R/W
	_Custom_GTIRreset:	BUS
	This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b.	

PCI Express Capability

DWord		Bit	Description	
Register Space:		PCI: 0/2/0		
Size (in bits):		16		
Address:		00072h		
PCI Express Capability				
0	15:14	Reserved		
		Access:	RO	
		Format:	MBZ	
	13:9	Interrupt Message Number		
		Default Value:	00000b	
		Access:	RO	
		_Custom_GTIRreset:	BUS	
				This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
	8	Slot Implemented		
		Default Value:	0b	
		Access:	RO	
		_Custom_GTIRreset:	BUS	
				This field is hardwired to 0 for an endpoint device.
	7:4	Device Type		
		Default Value:	1001b	
		Access:	RO	
_Custom_GTIRreset:		BUS		
			This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.	
3:0	Capability Version			
	Default Value:	0010b		
	Access:	RO		
	_Custom_GTIRreset:	BUS		
			This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.	



PCI Express Capability Header

PCIECAPHDR_0_2_0_PCI - PCI Express Capability Header			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00070h		
PCI Express Capability Header			
DWord	Bit	Description	
0	15:8	Next Capability Pointer	
		Default Value:	10101100b
		Access:	RO
		_Custom_GTIReset:	BUS
	This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.		
	7:0	Capability Identifier	
		Default Value:	00010000b
Access:		RO	
_Custom_GTIReset:		BUS	
This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.			

PCI Express Capability Structure

DEVICESTS_0_2_0_PCI - PCI Express Capability Structure			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	0007Ah		
PCI Express Capability Structure			
DWord	Bit	Description	
0	15:6	Reserved	
		Access:	RO
		Format:	MBZ
	5	Transactions Pending	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
			When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
	4	Aux Power Detected	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
			Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
	3	Unsupported Request Detected	
		Default Value:	0b
		Access:	RO
_Custom_GTIRreset:		BUS	
		This bit indicates the Function received an Unsupported Request. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.	
2	Fatal Error Detected		
	Default Value:	0b	
	Access:	R/WC	
	_Custom_GTIRreset:	BUS	
		This bit indicates status of fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.	

DEVICES_0_2_0_PCI - PCI Express Capability Structure

1	<p>Non-Fatal Error Detected</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/WC</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>This bit indicates status of non fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.</p>	Default Value:	0b	Access:	R/WC	_Custom_GTIReset:	BUS
Default Value:	0b						
Access:	R/WC						
_Custom_GTIReset:	BUS						
0	<p>Correctable Error Detected</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/WC</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.</p>	Default Value:	0b	Access:	R/WC	_Custom_GTIReset:	BUS
Default Value:	0b						
Access:	R/WC						
_Custom_GTIReset:	BUS						

PCI Express Device Control

DEVICECTL_0_2_0_PCI - PCI Express Device Control			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00078h		
PCI Express Device Control			
DWord	Bit	Description	
0	15	Initiate Function Level Reset	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
		A write of 1b initiates Function Level Reset to the Function. During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.	
14:12		Max Read Request Size	
		Default Value:	000b
		Access:	RO
		_Custom_GTIReset:	BUS
		Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.	
11		Enable No Snoop	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
		This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.	
10		Aux Power PM Enable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
		Functions that do not implement this capability hardwire this bit to 0b.	
9		Phantom Functions Enable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
		Functions that do not implement this capability hardwire this bit to 0b.	

DEVICECTL_0_2_0_PCI - PCI Express Device Control

8	Extended Tag field Enable	
	Default Value:	0b
	Access:	RO
	_Custom_GTIReset:	BUS
	Functions that do not implement this capability hardwire this bit to 0b.	
7:5	Max Payload Size	
	Default Value:	000b
	Access:	RO
	_Custom_GTIReset:	BUS
Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.		
4	Enable Relaxed Ordering	
	Default Value:	0b
	Access:	RO
	_Custom_GTIReset:	BUS
A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.		
3	Unsupported Request Response Enable	
	Default Value:	0b
	Access:	RO
	_Custom_GTIReset:	BUS
A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.		
2	Fatal Error Enable	
	Default Value:	0b
	Access:	R/W
	_Custom_GTIReset:	BUS
This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (see Section 6.2.5 and Section 6.2.6 for details).		
1	Non-Fatal Error Enable	
	Default Value:	0b
	Access:	R/W
	_Custom_GTIReset:	BUS
This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (see Section 6.2.5 and Section 6.2.6 for details).		

DEVICectl_0_2_0_PCI - PCI Express Device Control

	0	Correctable Error Enable	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
		This bit, in conjunction with other bits, controls sending ERR_COR Messages (see Section 6.2.5 and Section 6.2.6 for details).	



PCI Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	00050h							
Mirror of GGC register from GTTMMADR Space at offset 0x108040.								
DWord	Bit	Description						
0	15:8	<p>GMS</p> <table border="1"> <tr> <td>Default Value:</td> <td>05h</td> </tr> <tr> <td>Access:</td> <td>RO Variant</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.</p> <p>Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.</p> <p>BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.</p> <p>BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions.</p> <p>00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved</p>	Default Value:	05h	Access:	RO Variant	_Custom_GTIReset:	BUS
Default Value:	05h							
Access:	RO Variant							
_Custom_GTIReset:	BUS							

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

F0h: 4MB
 F1h: 8MB
 F2h: 12MB
 F3h: 16MB
 F4h: 20MB
 F5h: 24MB
 F6h: 28MB
 F7h: 32MB
 F8h: 36MB
 F9h: 40MB
 FAh: 44MB
 FBh: 48MB
 FCh: 52MB
 FDh: 56MB
 FEh: 60MB
 FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.

7:6

GGMS

Default Value:	00b
Access:	RO Variant
_Custom_GTIReset:	BUS

This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.
 GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.
 Hardware functionality in case of programming this value to Reserved is not guaranteed.
 0x0:No Preallocated Memory
 0x1:2MB of Preallocated Memory
 0x2:4MB of Preallocated Memory
 0x3:8MB of Preallocated Memory

5:3

Reserved

Access:	RO
Format:	MBZ

2

VAMEN

Default Value:	0b
Access:	RO Variant
_Custom_GTIReset:	BUS

Enables the use of the iGFX engines for Versatile Acceleration.
 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 038000h.

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

1	<p>IVD</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td> <td style="padding: 2px;">0b</td> </tr> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">RO Variant</td> </tr> <tr> <td style="padding: 2px;">_Custom_GTIRreset:</td> <td style="padding: 2px;">BUS</td> </tr> </table> <p>0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory.</p>	Default Value:	0b	Access:	RO Variant	_Custom_GTIRreset:	BUS
Default Value:	0b						
Access:	RO Variant						
_Custom_GTIRreset:	BUS						
0	<p>SPARE</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Default Value:</td> <td style="padding: 2px;">0b</td> </tr> <tr> <td style="padding: 2px;">Access:</td> <td style="padding: 2px;">RO Variant</td> </tr> <tr> <td style="padding: 2px;">_Custom_GTIRreset:</td> <td style="padding: 2px;">BUS</td> </tr> </table> <p>Note: This bit was maintained as a placeholder for compatibility. Prior, it locked the register.</p>	Default Value:	0b	Access:	RO Variant	_Custom_GTIRreset:	BUS
Default Value:	0b						
Access:	RO Variant						
_Custom_GTIRreset:	BUS						

PCI Status

PCISTS2_0_2_0_PCI - PCI Status			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	00006h		
<p>PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant primary abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.</p>			
DWord	Bit	Description	
0	15	Detected Parity Error	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Since the IGD does not detect parity, this bit is always hardwired to 0.		
	14	Signaled System Error	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	The IGD never asserts SERR#, therefore this bit is hardwired to 0.		
	13	Received Primary Abort Status	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	The IGD never gets a Primary Abort, therefore this bit is hardwired to 0.		
	12	Received Target Abort Status	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	The IGD never gets a Target Abort, therefore this bit is hardwired to 0.		
11	Signaled Target Abort Status		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
Hardwired to 0. The IGD does not use target abort semantics.			
10:9	DEVSEL Timing		
	Default Value:	00b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
Hardwired to 00.			

PCISTS2_0_2_0_PCI - PCI Status

8	Primary Data Parity Error Detected		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
	Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.		
	7	Fast Back-to-Back	
		Default Value:	0b
		Access:	RO
_Custom_GTIReset:		BUS	
Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).			
6	User Defined Format		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
Hardwired to 0.			
5	66 MHz PCI Capable		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
Hardwired to 0.			
4	Capability List		
	Default Value:	1b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.			
3	Interrupt Status		
	Default Value:	0b	
	Access:	RO Variant	
	_Custom_GTIReset:	BUS	
This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.			
2:0	Reserved		
	Access:	RO	
	Format:	MBZ	

PCU Interrupt Definition

PCU Interrupt Definition				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
SOC_Consumer:	BIOS			
Address:	444E0h-444EFh			
Name:	PCU Interrupts			
ShortName:	PCU_INTERRUPT			
<p>This table indicates which events are mapped to each bit of the PCU Interrupt registers.</p> <p>0x444E0 = ISR 0x444E4 = IMR 0x444E8 = IIR 0x444EC = IER</p>				
DWord	Bit	Description		
0	31	DDIA DC9 HPD <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> This field indicates DDIA hotplug activity was detected during DC9.	_Custom_GTIRReset:	BUS
	_Custom_GTIRReset:	BUS		
	30	DDIB DC9 HPD <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> This field indicates DDIB hotplug activity was detected during DC9.	_Custom_GTIRReset:	BUS
	_Custom_GTIRReset:	BUS		
	29	DDIC DC9 HPD <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> This field indicates DDIC hotplug activity was detected during DC9.	_Custom_GTIRReset:	BUS
	_Custom_GTIRReset:	BUS		
	28	Spare_28 <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> Spare bit	_Custom_GTIRReset:	BUS
	_Custom_GTIRReset:	BUS		
	27	Spare_27 <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> Spare bit	_Custom_GTIRReset:	BUS
	_Custom_GTIRReset:	BUS		
26	Spare_26 <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> Spare bit	_Custom_GTIRReset:	BUS	
_Custom_GTIRReset:	BUS			
25	PCU_Pcode2driver_Mailbox_Event <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table>	_Custom_GTIRReset:	BUS	
_Custom_GTIRReset:	BUS			
24	PCU_Thermal_Event <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table>	_Custom_GTIRReset:	BUS	
_Custom_GTIRReset:	BUS			
23	Spare_23 <table border="1" style="width: 100%;"> <tr> <td>_Custom_GTIRReset:</td> <td>BUS</td> </tr> </table> Spare bit	_Custom_GTIRReset:	BUS	
_Custom_GTIRReset:	BUS			

PCU Interrupt Definition

	22	Spare_22		
		_Custom_GTIRreset:		BUS
		Spare bit		
	21	Spare_21		
		_Custom_GTIRreset:		BUS
		Spare bit		
	20	Spare_20		
		_Custom_GTIRreset:		BUS
		Spare bit		
	19	Spare_19		
		_Custom_GTIRreset:		BUS
		Spare bit		
	18	Spare_18		
		_Custom_GTIRreset:		BUS
	Spare bit			
17	Spare_17			
	_Custom_GTIRreset:		BUS	
	Spare bit			
16	Spare_16			
	_Custom_GTIRreset:		BUS	
	Spare bit			
15	Spare_15			
	_Custom_GTIRreset:		BUS	
	Spare bit			
14	Spare_14			
	_Custom_GTIRreset:		BUS	
	Spare bit			
13	Spare_13			
	_Custom_GTIRreset:		BUS	
	Spare bit			
12	Spare_12			
	_Custom_GTIRreset:		BUS	
	Spare bit			
11	Spare_11			
	_Custom_GTIRreset:		BUS	
	Spare bit			
10	Spare_10			
	_Custom_GTIRreset:		BUS	
	Spare bit			

PCU Interrupt Definition

9	Spare_9 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
8	Spare_8 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
7	Spare_7 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
6	Spare_6 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
5	Spare_5 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
4	Spare_4 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
3	Spare_3 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
2	Spare_2 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> Spare bit	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
1	Spare_1 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> KVMR Release Display Enable - This field indicates that KVMR is no longer requesting driver to enable a display output.	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		
0	Spare_0 <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">_Custom_GTIRreset:</td> <td style="width: 30%;">BUS</td> </tr> </table> KVMR Request Display Enable -This field indicates that KVMR is requesting driver to enable a display output.	_Custom_GTIRreset:	BUS
_Custom_GTIRreset:	BUS		

PHY_MISC

PHY_MISC		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	64C00h-64C03h	
Name:	PHY_MISC_A	
ShortName:	PHY_MISC_A	
Reset:	global	
Address:	64C04h-64C07h	
Name:	PHY_MISC_B	
ShortName:	PHY_MISC_B	
Reset:	global	
Address:	64C08h-64C0Bh	
Name:	PHY_MISC_C	
ShortName:	PHY_MISC_C	
Reset:	global	
This register is on the ungated clock and the chip reset, not the FLR.		
DWord	Bit	Description
0	31:28	DE to IO Misc Default Value: 0010b
	27:24	IO to DE Misc Access: RO
	23	DE to IO Comp Pwr Down
	22	Spare 22
	21	Spare 21
	20	Spare 20
	19:12	Reserved Access: RO Format: MBZ
	11:4	Reserved Access: RO Format: MBZ
	3:0	Reserved Access: RO Format: MBZ

Pinned Surface Mapping Size Register

PINNED_SURFACE_SIZE - Pinned Surface Mapping Size Register			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Pinned Surface Mapping Size register			
DWord	Bit	Description	
0	31:12	Size	
		Default Value:	00000000000000000000b
		Access:	R/W
		_Custom_GTIReset:	DEV
			Size of the surface(s) in 4KB pages. Must be > 0.
	11:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	Valid	
		Default Value:	0b
Access:		R/W	
_Custom_GTIReset:		DEV	
1'b0: This entry is not valid 1'b1: This entry is valid			



Pinned Surface Per Process Virtual Address Base Register

PINNED_SURFACE_PPBASE_H - Pinned Surface Per Process Virtual Address Base Register			
Register Space: MMIO: 0/2/0			
Size (in bits): 32			
Pinned Surface Per Process Virtual Address Base register			
DWord	Bit	Description	
0	31:0	Per Process Virtual Base_H	
		Default Value:	0000h
		Access:	R/W
		_Custom_GTIReset:	DEV
Per Process Virtual Address Base - PPBASE[47:16] 4KB Page number of the surface(s) in Per-Process Virtual Address Space (ie, index into the PPGTT)			

Pinned Surface Process ID Register

PINNED_SURFACE_PROCESS_ID - Pinned Surface Process ID Register			
Register Space:		MMIO: 0/2/0	
Size (in bits):		32	
Pinned Surface Process ID register			
DWord	Bit	Description	
0	31:0	Process ID	
		Default Value:	0000h
		Access:	R/W
		_Custom_GTIRreset:	DEV
ID of the Process that owns the pinned surfaces represented by this register.			



Pinned Surface Virtual Address Base Register

PINNED_SURFACE_ADDR_BASE - Pinned Surface Virtual Address Base Register			
Register Space: MMIO: 0/2/0			
Size (in bits): 32			
Pinned Surface Virtual Address Base register			
DWord	Bit	Description	
0	31:28	Per Process Virtual Base_L	
		Default Value:	0000b
		Access:	R/W
		_Custom_GTIReset:	DEV
			Per Process Virtual Address Base - PPBASE[15:12] 4KB Page number of the surface(s) in Per-Process Virtual Address Space (ie, index into the PPGTT)
	27:20	Reserved	
		Access:	RO
		Format:	MBZ
	19:0	Global Virtual Address Base	
		Default Value:	00000000000000000000b
Access:		R/W	
_Custom_GTIReset:		DEV	
		4KB Page number of the surface(s) in Global Virtual Address Space (ie, index into the GGTT). The entire range from Base to Base+Size-1 must fall within the Pinned Range of the GGTT.	

PIPE_ARB_CTL

PIPE_ARB_CTL			
Register Space:	MMIO: 0/2/0		
Access:	Double Buffered		
Size (in bits):	32		
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled			
Address:	70028h-7002Bh		
Name:	Pipe Arbiter Control		
ShortName:	PIPE_ARB_CTL_A		
Reset:	soft		
Address:	71028h-7102Bh		
Name:	Pipe Arbiter Control		
ShortName:	PIPE_ARB_CTL_B		
Reset:	soft		
Address:	72028h-7202Bh		
Name:	Pipe Arbiter Control		
ShortName:	PIPE_ARB_CTL_C		
Reset:	soft		
Address:	73028h-7302Bh		
Name:	Pipe Arbiter Control		
ShortName:	PIPE_ARB_CTL_D		
Reset:	soft		
There is one instance of this register per pipe.			
DWord	Bit	Description	
0	31	Reserved	
		Access:	RO
		Format:	MBZ
	30:21	Reserved	
		Access:	RO
		Format:	MBZ
	20	Disable Weighted Arbitration	
		This field disables the weighted pipe slice arbitration.	
		Value	Name
		0b	Enable [Default]
1b	Disable		
19	Reserved		

PIPE_ARB_CTL

	18:16	Additional Slots These additional Slots gets added to each arbitration cycle during which the clients gets serviced in a round robin manner. A programmed value of 1b results in 1 additional slot.																
	15:14	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ											
Access:	RO																	
Format:	MBZ																	
	13	Use Programmed Slots When this field is set, HW uses the Slots programmed in the PLANE_CTL register instead of the HW defaults.																
	12	Disable Block Valid Check The field disables the block valid check done at pipe arbiter. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Enable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Disable</td> </tr> </tbody> </table>		Value	Name	0b	Enable	1b	Disable									
Value	Name																	
0b	Enable																	
1b	Disable																	
	11:10	DSB Arbitration Interval This field defines the DSB requests service interval in the pipe arbitration. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 30%; text-align: center;">Value</th> <th style="width: 70%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">16 clocks</td> </tr> <tr> <td style="text-align: center;">01b</td> <td style="text-align: center;">32 clocks</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">64 clocks [Default]</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">128 clocks</td> </tr> </tbody> </table>		Value	Name	00b	16 clocks	01b	32 clocks	10b	64 clocks [Default]	11b	128 clocks					
Value	Name																	
00b	16 clocks																	
01b	32 clocks																	
10b	64 clocks [Default]																	
11b	128 clocks																	
	9:8	Request Vs Data Arbitration This field selects the arbitration weightage for the Streamer and the DDB requests. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 15%; text-align: center;">Value</th> <th style="width: 15%; text-align: center;">Name</th> <th style="width: 70%; text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td></td> <td style="text-align: center;">Allow 1 Streamer requests every 2 DDB requests.</td> </tr> <tr> <td style="text-align: center;">01b</td> <td></td> <td style="text-align: center;">Allow 1 Streamer requests every 4 DDB requests.</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">[Default]</td> <td style="text-align: center;">Allow 1 Streamer requests every 8 DDB requests.</td> </tr> <tr> <td style="text-align: center;">11b</td> <td></td> <td style="text-align: center;">Allow 1 Streamer requests every 16 DDB requests.</td> </tr> </tbody> </table>		Value	Name	Description	00b		Allow 1 Streamer requests every 2 DDB requests.	01b		Allow 1 Streamer requests every 4 DDB requests.	10b	[Default]	Allow 1 Streamer requests every 8 DDB requests.	11b		Allow 1 Streamer requests every 16 DDB requests.
Value	Name	Description																
00b		Allow 1 Streamer requests every 2 DDB requests.																
01b		Allow 1 Streamer requests every 4 DDB requests.																
10b	[Default]	Allow 1 Streamer requests every 8 DDB requests.																
11b		Allow 1 Streamer requests every 16 DDB requests.																
	7:6	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ											
Access:	RO																	
Format:	MBZ																	
	5:0	Frame Start Drain Delay This field contains the time, in microseconds, the pipe waits before draining the data from the Display Buffer. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[0-31]</td> <td></td> </tr> <tr> <td style="text-align: center;">15</td> <td style="text-align: center;">[Default]</td> </tr> </tbody> </table>		Value	Name	[0-31]		15	[Default]									
Value	Name																	
[0-31]																		
15	[Default]																	

PIPE_BOTTOM_COLOR

PIPE_BOTTOM_COLOR								
Register Space:	MMIO: 0/2/0							
Access:	Double Buffered							
Size (in bits):	32							
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled								
Address:	70034h-70037h							
Name:	Pipe Bottom Color							
ShortName:	PIPE_BOTTOM_COLOR_A							
Reset:	soft							
Address:	71034h-71037h							
Name:	Pipe Bottom Color							
ShortName:	PIPE_BOTTOM_COLOR_B							
Reset:	soft							
Address:	72034h-72037h							
Name:	Pipe Bottom Color							
ShortName:	PIPE_BOTTOM_COLOR_C							
Reset:	soft							
Address:	73034h-73037h							
Name:	Pipe Bottom Color							
ShortName:	PIPE_BOTTOM_COLOR_D							
Reset:	soft							
This register sets the color that appears underneath the bottom most plane in the pipe blender Z-order. The value for each color channel is represented in an unsigned 0.10 format with 0 integer and 10 fractional bits.								
DWord	Bit	Description						
0	31	Pipe Gamma Enable						
		This bit enables pipe gamma correction for the bottom color.						
		This field is deprecated.						
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
	Value	Name						
0b	Disable							
1b	Enable							
30	Pipe CSC Enable	This bit enables pipe color space conversion for the bottom color.						
		This field is deprecated.						

PIPE_BOTTOM_COLOR		
	Value	Name
	0b	Disable
	1b	Enable
	29:20	V R Bottom Color Format: U0.10 This field sets the bottom color for the V or Red channel.
	19:10	Y G Bottom Color Format: U0.10 This field sets the bottom color for the Y or Green channel.
	9:0	U B Bottom Color Format: U0.10 This field sets the bottom color for the U or Blue channel.

PIPE_DMCSKANLINECOMP

PIPE_DMCSKANLINECOMP								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	7000Ch-7000Fh							
Name:	Pipe Scan Line Compare for DMC							
ShortName:	PIPE_DMCSKANLINECOMP_A							
Reset:	soft							
Address:	7100Ch-7100Fh							
Name:	Pipe Scan Line Compare for DMC							
ShortName:	PIPE_DMCSKANLINECOMP_B							
Reset:	soft							
Address:	7200Ch-7200Fh							
Name:	Pipe Scan Line Compare for DMC							
ShortName:	PIPE_DMCSKANLINECOMP_C							
Reset:	soft							
Address:	7300Ch-7300Fh							
Name:	Pipe Scan Line Compare for DMC							
ShortName:	PIPE_DMCSKANLINECOMP_D							
Reset:	soft							
DWord	Bit	Description						
0	31	Enable Compare This field enables the scan line compare for DMC event generation. When this register is written with this bit set to 1b, the display engine will, trigger a scan line event after reaching the programmed scan line number. It will do the same on every frame.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Do nothing</td> </tr> <tr> <td>1b</td> <td>Enable compare</td> </tr> </tbody> </table>	Value	Name	0b	Do nothing	1b	Enable compare
		Value	Name					
		0b	Do nothing					
1b	Enable compare							
<table border="1"> <thead> <tr> <th colspan="2">Restriction</th> </tr> </thead> <tbody> <tr> <td colspan="2">Do not enable this register if the event is not needed in the DMC.</td> </tr> </tbody> </table>	Restriction		Do not enable this register if the event is not needed in the DMC.					
Restriction								
Do not enable this register if the event is not needed in the DMC.								
30:20	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							
19:0	Scan Line Value This field specifies the ending scan line number of the scan line window.							



PIPE_DSS_CTL1

PIPE_DSS_CTL1						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	78000h-78003h					
Name:	PIPE DSS Control 1					
ShortName:	PIPE_DSS_CTL1_PA					
Reset:	soft					
Address:	78200h-78203h					
Name:	PIPE DSS Control 1					
ShortName:	PIPE_DSS_CTL1_PB					
Reset:	soft					
Address:	78400h-78403h					
Name:	PIPE DSS Control 1					
ShortName:	PIPE_DSS_CTL1_PC					
Reset:	soft					
Address:	78600h-78603h					
Name:	PIPE DSS Control 1					
ShortName:	PIPE_DSS_CTL1_PD					
Reset:	soft					
Display stream splitter						
DWord	Bit	Description				
0	31	Splitter Enable				
		<p>This field enables stream splitting.</p> <p>This bit must be set to enable MSO configuration.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p>Restriction</p> <p>Splitter enable is supported for pipe A only.</p>	Value	Name	0b	Disable
Value	Name					
0b	Disable					
1b	Enable					
	30	Joiner Enable				
		<p>This field enables stream joiner after compression.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Disable
Value	Name					
0b	Disable					

PIPE_DSS_CTL1							
	<table border="1"> <tr> <td>1b</td> <td>Enable</td> </tr> </table>	1b	Enable				
1b	Enable						
29	<p>Big Joiner Enable When big_joiner_enable is '1', this dssunit will be working with another dssunit in adjacent pipe either as a primary or as a secondary.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						
28	<p>Primary Big Joiner Enable This bit indicates that this pipe is the primary/secondary when Big_Joiner_Enable bit is set in this register.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Secondary</td> </tr> <tr> <td>1b</td> <td>Primary</td> </tr> </tbody> </table>	Value	Name	0b	Secondary	1b	Primary
Value	Name						
0b	Secondary						
1b	Primary						
27	Reserved						
26:25	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
24	<p>Dual Link Mode This field selects the split pattern. Applicable only if splitter mode is enabled through DSS configuration bits.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Front-Back mode</td> </tr> <tr> <td>1b</td> <td>Interleave mode</td> </tr> </tbody> </table>	Value	Name	0b	Front-Back mode	1b	Interleave mode
Value	Name						
0b	Front-Back mode						
1b	Interleave mode						
23:20	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
19:16	<p>Overlap MIPI use case (mainly dual link mode): This field specifies the number of pixels of overlap. 1 to 15 = valid integer number of overlap pixels. 0 = Sink device requires no overlap pixels. eDP use case: This field specifies the number of overlap pixels the sink device uses in the active data. 1 to 8 = valid integer number of overlap pixels. 0 = Sink device requires no overlap pixels.</p>						
15:12	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						

PIPE_DSS_CTL1	
11:0	<p>Left DL buffer Target Depth</p> <p>This field indicates the number of pixels to hold in the secondary link buffer before enabling the timing generator, so the Primary and Secondary client controllers are in sync.</p> <p>Valid only when operating in front back dual link mode.</p> <p>Value should only be programmed for the Secondary client controller. If bit 31 is set then the target for the Secondary controller must be non-zero.</p> <p>Maximum value is 1440 decimal.</p>

PIPE_DSS_CTL2

PIPE_DSS_CTL2							
Register Space:	MMIO: 0/2/0						
Access:	R/W						
Size (in bits):	32						
Address:	78004h-78007h						
Name:	PIPE DSS Control 2						
ShortName:	PIPE_DSS_CTL2_PA						
Reset:	soft						
Address:	78204h-78207h						
Name:	PIPE DSS Control 2						
ShortName:	PIPE_DSS_CTL2_PB						
Reset:	soft						
Address:	78404h-78407h						
Name:	PIPE DSS Control 2						
ShortName:	PIPE_DSS_CTL2_PC						
Reset:	soft						
Address:	78604h-78607h						
Name:	PIPE DSS Control 2						
ShortName:	PIPE_DSS_CTL2_PD						
Reset:	soft						
Display stream splitter							
DWord	Bit	Description					
0	31	Left Branch VDSC Enable					
		This bit enables Display Stream Compression on left branch. Its double buffered to rising edge of vblank.					
		Restriction : Display stream compression is supported for pipe active sizes up to 4096 pixels.					
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b
	Value	Name					
	0b	Disable					
	1b	Enable					
	30	Reserved					
		Access:	RO				
		Format:	MBZ				
29:27	Reserved						
	Access:	RO					
	Format:	MBZ					

PIPE_DSS_CTL2							
26	Spare 26						
25	Spare 25						
24	Spare 24						
23	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
22:19	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
18:17	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
16	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
15	Right Branch VDSC Enable Display stream compression on right branch enable/disable. It is double buffered on rising edge of vblank. Restriction : Display stream compression is supported for pipe active sizes up to 4096 pixels. <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						
14	Spare 14						
13	Spare 13						
12	Spare 12						
11:0	Right DL Buffer Target Depth This field indicates the number of pixels to hold in the secondary link buffer before enabling the timing generator, so the Primary and Secondary client controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Secondary controller. If bit 31 is set then the target for the Secondary controller must be non-zero. Maximum value is 1440 decimal. Default is 0.						

PIPE_FLIPCNT

PIPE_FLIPCNT		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	70044h-70047h	
Name:	Pipe Flip Count	
ShortName:	PIPE_FLIPCNT_A	
Reset:	soft	
Address:	71044h-71047h	
Name:	Pipe Flip Count	
ShortName:	PIPE_FLIPCNT_B	
Reset:	soft	
Address:	72044h-72047h	
Name:	Pipe Flip Count	
ShortName:	PIPE_FLIPCNT_C	
Reset:	soft	
Address:	73044h-73047h	
Name:	Pipe Flip Count	
ShortName:	PIPE_FLIPCNT_D	
Reset:	soft	
DWord	Bit	Description
0	31:0	<p>Pipe Flip Counter</p> <p>This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the selected plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. It rolls over back to 0 after $(2^{32})-1$ flips.</p> <p>Pipe flipcounter is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.</p>

PIPE_FLIPDONETMSTMP

PIPE_FLIPDONETMSTMP		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	70054h-70057h	
Name:	Pipe Flip Done Time Stamp	
ShortName:	PIPE_FLIPDONETMSTMP_A	
Reset:	soft	
Address:	71054h-71057h	
Name:	Pipe Flip Done Time Stamp	
ShortName:	PIPE_FLIPDONETMSTMP_B	
Reset:	soft	
Address:	72054h-72057h	
Name:	Pipe Flip Done Time Stamp	
ShortName:	PIPE_FLIPDONETMSTMP_C	
Reset:	soft	
Address:	73054h-73057h	
Name:	Pipe Flip Done Time Stamp	
ShortName:	PIPE_FLIPDONETMSTMP_D	
Reset:	soft	
DWord	Bit	Description
0	31:0	<p>Pipe Flip Done Time Stamp</p> <p>This field provides read back of the display pipe flip done time stamp. The time stamp value is sampled when hardware latches on to the new surface and the flip done gets sent. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane. The <code>TIMESTAMP_CTR</code> register has the current time stamp value.</p> <p>Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in <code>PIPE_MISC2->Flip Timestamp Plane Select</code>.</p>

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	7004Ch-7004Fh	
Name:	Pipe Flip Time Stamp	
ShortName:	PIPE_FLIPTMSTMP_A	
Reset:	soft	
Address:	7104Ch-7104Fh	
Name:	Pipe Flip Time Stamp	
ShortName:	PIPE_FLIPTMSTMP_B	
Reset:	soft	
Address:	7204Ch-7204Fh	
Name:	Pipe Flip Time Stamp	
ShortName:	PIPE_FLIPTMSTMP_C	
Reset:	soft	
Address:	7304Ch-7304Fh	
Name:	Pipe Flip Time Stamp	
ShortName:	PIPE_FLIPTMSTMP_D	
Reset:	soft	
DWord	Bit	Description
0	31:0	<p>Pipe Flip Time Stamp</p> <p>This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register will overwrite and update the time stamp value.</p> <p>Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.</p>

PIPE_FRMCNT

PIPE_FRMCNT		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	70040h-70043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_A	
Reset:	soft	
Address:	71040h-71043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_B	
Reset:	soft	
Address:	72040h-72043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_C	
Reset:	soft	
Address:	73040h-73043h	
Name:	Pipe Frame Count	
ShortName:	PIPE_FRMCNT_D	
Reset:	soft	
DWord	Bit	Description
0	31:0	Pipe Frame Counter Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after $(2^{32})-1$ frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	70048h-7004Bh	
Name:	Pipe Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_A	
Reset:	soft	
Address:	71048h-7104Bh	
Name:	Pipe Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_B	
Reset:	soft	
Address:	72048h-7204Bh	
Name:	Pipe Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_C	
Reset:	soft	
Address:	73048h-7304Bh	
Name:	Pipe Frame Time Stamp	
ShortName:	PIPE_FRMTMSTMP_D	
Reset:	soft	
DWord	Bit	Description
0	31:0	<p>Pipe Frame Time Stamp</p> <p>This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value.</p> <p>Writes to this register will overwrite and update the time stamp value.</p>

PIPE_ISOCREQ

PIPE_ISOCREQ - PIPE_ISOCREQ				
Register Space:	MMIO: 0/2/0			
Size (in bits):	64			
Address:	70010h-70017h			
Name:	Pipe Isoch Request			
ShortName:	PIPE_ISOCREQ_A			
Reset:	soft			
Address:	71010h-71017h			
Name:	Pipe Isoch Request			
ShortName:	PIPE_ISOCREQ_B			
Reset:	soft			
Address:	72010h-72017h			
Name:	Pipe Isoch Request			
ShortName:	PIPE_ISOCREQ_C			
Reset:	soft			
Address:	73010h-73017h			
Name:	Pipe Isoch Request			
ShortName:	PIPE_ISOCREQ_D			
Reset:	soft			
When enabled, the write to DWord 1 (higher address DWord) of this register triggers an IsocReq to be sent with the last written values from both DWords.				
DWord	Bit	Description		
0	31:16	LTR <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> This field specifies the latency tolerance (LTR) for this pipe in microseconds.	Access:	R/W
	Access:	R/W		
15:0	Bandwidth <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> This field specifies the bandwidth requirement for this pipe in multiples of 100 MB/s.	Access:	R/W	
Access:	R/W			
1	31	Enable <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> This field enables IsocReq to be sent when DWord 1 of this register is written.	Access:	R/W
		Access:	R/W	
		Value	Name	
		1b	Enable	
0b	Disable			

PIPE_ISOCREQ - PIPE_ISOCREQ		
	30:8	Reserved
		Access: RO
		Format: MBZ
	7:0	Delay
Access: R/W This field specifies the downwards transition delay for this pipe in milliseconds.		

PIPE_ISOCREQ_OFFSET

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET				
Register Space:	MMIO: 0/2/0			
Size (in bits):	64			
Address:	70018h-7001Fh			
Name:	Pipe Isoch Offset addition			
ShortName:	PIPE_ISOCREQ_OFFSET_A			
Reset:	soft			
Address:	71018h-7101Fh			
Name:	Pipe Isoch Offset addition			
ShortName:	PIPE_ISOCREQ_OFFSET_B			
Reset:	soft			
Address:	72018h-7201Fh			
Name:	Pipe Isoch Offset addition			
ShortName:	PIPE_ISOCREQ_OFFSET_C			
Reset:	soft			
Address:	73018h-7301Fh			
Name:	Pipe Isoch Offset addition			
ShortName:	PIPE_ISOCREQ_OFFSET_D			
Reset:	soft			
<p>The values programmed in this register will added as offsets to the LTR, BW and Delay. SW must ensure to clear these registers if no offset is desired to be added.</p> <p>For example, If LTR offset is programmed to 0x0100 in this register, then this value is added to the LTR value programmed in PIPE_ISOCREQ.</p>				
DWord	Bit	Description		
0	31:16	LTR offset Access: <table border="1" style="display: inline-table; width: 100%;"><tr><td> </td></tr></table> R/W This field specifies the latency tolerance (LTR) offset to be added to LTR value in PIPE_ISOCREQ for this pipe in microseconds.		
Bandwidth offset Access: <table border="1" style="display: inline-table; width: 100%;"><tr><td> </td></tr></table> R/W This field specifies the bandwidth requirement offset to be added to BW value in the PIPE_ISOCREQ register				
1	31:8	Reserved Access: <table border="1" style="display: inline-table; width: 100%;"><tr><td> </td></tr></table> RO Format: <table border="1" style="display: inline-table; width: 100%;"><tr><td> </td></tr></table> MBZ		

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET			
7:0	<p>Delay Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>This field specifies the offset to be added to the downwards transition delay programmed in the PIPE_ISOCREQ.</p>	Access:	R/W
Access:	R/W		



PIPE_MISC

PIPE_MISC																	
Register Space:	MMIO: 0/2/0																
Access:	Double Buffered																
Size (in bits):	32																
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled																	
Address:	70030h-70033h																
Name:	Pipe Miscellaneous																
ShortName:	PIPE_MISC_A																
Reset:	soft																
Address:	71030h-71033h																
Name:	Pipe Miscellaneous																
ShortName:	PIPE_MISC_B																
Reset:	soft																
Address:	72030h-72033h																
Name:	Pipe Miscellaneous																
ShortName:	PIPE_MISC_C																
Reset:	soft																
Address:	73030h-73033h																
Name:	Pipe Miscellaneous																
ShortName:	PIPE_MISC_D																
Reset:	soft																
DWord	Bit	Description															
0	31:30	<p>Stereo Mask Pipe Int</p> <p>This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in interrupts during stereo 3D mode.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Mask None</td> <td>No masking. Report both the left and right eye vertical events.</td> </tr> <tr> <td>01b</td> <td>Mask Left</td> <td>Mask the left eye vertical events. Only report right eye events.</td> </tr> <tr> <td>10b</td> <td>Mask Right</td> <td>Mask the right eye vertical events. Only report left eye events.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.</p>	Value	Name	Description	00b	Mask None	No masking. Report both the left and right eye vertical events.	01b	Mask Left	Mask the left eye vertical events. Only report right eye events.	10b	Mask Right	Mask the right eye vertical events. Only report left eye events.	11b	Reserved	Reserved
Value	Name	Description															
00b	Mask None	No masking. Report both the left and right eye vertical events.															
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.															
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.															
11b	Reserved	Reserved															

PIPE_MISC

29:28	Stereo Mask Pipe Render	<p>This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in render responses during stereo 3D mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Mask None</td> <td>No masking. Report both the left and right eye vertical events.</td> </tr> <tr> <td>01b</td> <td>Mask Left</td> <td>Mask the left eye vertical events. Only report right eye events.</td> </tr> <tr> <td>10b</td> <td>Mask Right</td> <td>Mask the right eye vertical events. Only report left eye events.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.</p>	Value	Name	Description	00b	Mask None	No masking. Report both the left and right eye vertical events.	01b	Mask Left	Mask the left eye vertical events. Only report right eye events.	10b	Mask Right	Mask the right eye vertical events. Only report left eye events.	11b	Reserved	Reserved
Value	Name	Description															
00b	Mask None	No masking. Report both the left and right eye vertical events.															
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.															
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.															
11b	Reserved	Reserved															
27	YUV420 Enable	<p>This field enables YUV420 output from this pipe. This is only for use with HDMI and DP.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must be programmed prior to enabling the transcoder attached to this pipe.</p>	Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
26	YUV420 Mode	<p>This field specifies the mode in which YUV420 pixels are generated by this pipe.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Bypass</td> </tr> <tr> <td>1b</td> <td>Full blend</td> </tr> </tbody> </table>	Value	Name	0b	Bypass	1b	Full blend									
Value	Name																
0b	Bypass																
1b	Full blend																
25	Pipe Gamma Input Clamp Disable	<p>This field controls the pipe post csc gamma input clamp operation. When this bit is set to 0b the negative pixel values get clamped to zero at the gamma input.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable [Default]</td> </tr> <tr> <td>1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable [Default]	1b	Disable									
Value	Name																
0b	Enable [Default]																
1b	Disable																
24	Allow Double Buffer Update Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>This field controls whether double buffer updates are allowed to be disabled for the double buffered pipe registers listed below. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for those resources that allow them to be disabled.</p>	Access:	R/W													
Access:	R/W																

PIPE_MISC

		Value	Name
		0b	Not Allowed
		1b	Allowed [Default]
23	HDR Mode	<p>This field enables the HDR mode, allowing for higher precision output from the HDR supporting planes and bypassing the SDR planes in blending.</p> <p>In addition to setting bit 8 of this register (Pixel Rounding), this bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.</p>	
		Value	Name
		0b	Disable
		1b	Enable
22	Change Mask for LDPST	<p>This field controls the change tracking for the LACE. Change tracking can be used by PSR/SRD and WD</p>	
		Value	Name
		0b	Not Masked
		1b	Masked
21	Change Mask for Register Write	<p>This field controls change tracking for the pipe register write. Change tracking can be used by PSR/SRD and WD.</p>	
		Value	Name
		0b	Not Masked
		1b	Masked
20	Change Mask for Vblank Vsync Int	<p>This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD.</p>	
		Value	Name
		0b	Not Masked
		1b	Masked
19	Reserved		
18	Reserved		
17	Reserved		
16	Reserved		
15:14	Rotation Info	<p>This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation. Select the closest value if the rotation is not an exact multiple of 90 degrees. Hardware rotation of the display output is controlled through the plane control registers, not through this field.</p>	

PIPE_MISC																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>None</td> <td>No rotation on this pipe</td> </tr> <tr> <td>01b</td> <td>90</td> <td>90 degree rotation on this pipe</td> </tr> <tr> <td>10b</td> <td>180</td> <td>180 degree rotation on this pipe</td> </tr> <tr> <td>11b</td> <td>270</td> <td>270 degree rotation on this pipe</td> </tr> </tbody> </table>	Value	Name	Description	00b	None	No rotation on this pipe	01b	90	90 degree rotation on this pipe	10b	180	180 degree rotation on this pipe	11b	270	270 degree rotation on this pipe	
Value	Name	Description															
00b	None	No rotation on this pipe															
01b	90	90 degree rotation on this pipe															
10b	180	180 degree rotation on this pipe															
11b	270	270 degree rotation on this pipe															
	<p style="text-align: center;">Restriction</p> <p>This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.</p>																
13	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ											
Access:	RO																
Format:	MBZ																
12	<p>OLED Compensation</p> <p>This field enables the OLED compensation on the pipe. When this bit is set, plane 5 is used as the OLED compensation plane with up to 10 bits per channel precision. OLED compensation must be used only when the pipe is configured to output RGB format.</p> <p>The OLED compensation plane size must be same as the pipe active size.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable									
Value	Name																
0b	Disable																
1b	Enable																
11	<p>Pipe output color space select</p> <p>This field indicates the output color space. This field affects the values of the pipe border and some capture functions. This field does not affect the planes, pipe CSC, or ports.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>RGB</td> </tr> <tr> <td>1b</td> <td>YUV</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.</p>		Value	Name	0b	RGB	1b	YUV									
Value	Name																
0b	RGB																
1b	YUV																
10	<p>xvYCC Color Range Limit</p> <p>This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Full</td> <td>Do not limit the range</td> </tr> <tr> <td>1b</td> <td>Limit</td> <td>Limit range</td> </tr> </tbody> </table>		Value	Name	Description	0b	Full	Do not limit the range	1b	Limit	Limit range						
Value	Name	Description															
0b	Full	Do not limit the range															
1b	Limit	Limit range															

PIPE_MISC

9	Pixel Extension This field controls how the pixel extension is handled in the pipe. In scenarios where the frame buffers bpc is larger or equal to the port output bpc, this bit may be programmed to 'Zero Extend'.		
	Value	Name	
	0b	MSB Extend [Default]	
	1b	Zero Extend	
8	Pixel Rounding This field controls the pixel rounding at the end of the pipe. This bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.		
	Value	Name	
	0b	Round Up [Default]	
	1b	Truncate	
7:5	Dithering BPC This field selects the number of bits per color to be used in dithering.		
	Value	Name	Description
	000b	8 bpc	8 bits per color
	001b	10 bpc	10 bits per color
	010b	6 bpc	6 bits per color
	Others	Reserved	Reserved
	Programming Notes		
	When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.		
4	Dithering enable This field enables dithering.		
	Value	Name	
	0b	Disable	
	1b	Enable	
3:2	Dithering type This field selects the dithering type.		
	Value	Name	Description
	00b	Spatial	Spatial
	01b	ST1	Spatio-Temporal 1
	10b	ST2	Spatio-Temporal 2
	11b	Temporal	Temporal

PIPE_MISC		
	1	Reserved
		Access: RO
	Format: MBZ	
	0	Reserved

PIPE_MISC2

PIPE_MISC2		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	32	
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled		
Address:	7002Ch-7002Fh	
Name:	Pipe Miscellaneous 2	
ShortName:	PIPE_MISC2_A	
Reset:	soft	
Address:	7102Ch-7102Fh	
Name:	Pipe Miscellaneous 2	
ShortName:	PIPE_MISC2_B	
Reset:	soft	
Address:	7202Ch-7202Fh	
Name:	Pipe Miscellaneous 2	
ShortName:	PIPE_MISC2_C	
Reset:	soft	
Address:	7302Ch-7302Fh	
Name:	Pipe Miscellaneous 2	
ShortName:	PIPE_MISC2_D	
Reset:	soft	
There is one instance of this register per pipe.		
DWord	Bit	Description
0	31:24	Reserved
		Access: RO
	Format: MBZ	
	23:20	TLB Throttle
Default Value:		8
This field specifies how often the TLB requests are sent. If the programmed value is x, TLBs requests are sent once in x clocks if there are competing data requests.		
19:16	Reserved	
	Access: RO	
Format: MBZ		
15:12	IPC Demote Req Chunk Size	
	Default Value:	8
This field limits the request burst sizes while in IPC demote. A value of 0 disables the inflight		

PIPE_MISC2		
	limit.	
11	Reserved	
	Access:	RO
	Format:	MBZ
10:9	Reserved	
	Access:	RO
	Format:	MBZ
8	ASFU Flip exception	
	Value	Name
		Description
	1b	mask
0b	No mask	Do not add exception for Flip for global register update event and Pipe register update event.
7	Reserved	
	Access:	RO
	Format:	MBZ
6:4	Scanline Plane Select	
	This field specifies the plane for which scanline compare fetch line is captured. A programmed value of 0b selects plane 1.	
	Value	Name
	[0h-6h]	
3	Reserved	
	Access:	RO
	Format:	MBZ
2:0	Flip Info Plane Select	
	This field specifies the plane for which flip information is captured. A programmed value of 0b selects plane 1.	
	Value	Name
	[0h-6h]	

PIPE_MISC3

PIPE_MISC3		
Register Space:	MMIO: 0/2/0	
Access:	Double Buffered	
Size (in bits):	32	
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled		
There is one instance of this register per pipe.		
DWord	Bit	Description
0	31:16	Reserved
	15:0	Reserved
		Access:
Format:	MBZ	

PIPE_SCANLINE

PIPE_SCANLINE											
Register Space:	MMIO: 0/2/0										
Access:	RO										
Size (in bits):	32										
Address:	70000h-70003h										
Name:	Pipe Scan Line										
ShortName:	PIPE_SCANLINE_A										
Reset:	soft										
Address:	71000h-71003h										
Name:	Pipe Scan Line										
ShortName:	PIPE_SCANLINE_B										
Reset:	soft										
Address:	72000h-72003h										
Name:	Pipe Scan Line										
ShortName:	PIPE_SCANLINE_C										
Reset:	soft										
Address:	73000h-73003h										
Name:	Pipe Scan Line										
ShortName:	PIPE_SCANLINE_D										
Reset:	soft										
<p>This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.</p>											
DWord	Bit	Description									
0	31	Current Field This is an indication of the current display field. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Odd</td> <td>First field (odd field)</td> </tr> <tr> <td>1b</td> <td>Even</td> <td>Second field (even field)</td> </tr> </tbody> </table>	Value	Name	Description	0b	Odd	First field (odd field)	1b	Even	Second field (even field)
		Value	Name	Description							
		0b	Odd	First field (odd field)							
	1b	Even	Second field (even field)								
30:20	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ						
Access:	RO										
Format:	MBZ										
19:0	Line Counter for Display This is an indication of the current display scan line.										

PIPE_SCANLINE

Programming Notes

The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Reset:	soft
Address:	71004h-71007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Reset:	soft
Address:	72004h-72007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Reset:	soft
Address:	73004h-73007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_D
Reset:	soft
<p>This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line \geq start scan line) and the end scan line value (current scan line \leq end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.</p>	
Restriction	
<p>A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all</p>	

PIPE_SCANLINECOMP

the programming rules for LRI targeting the display engine.

DWord	Bit	Description									
0	31	<p>Initiate Compare This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Do nothing</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Initiate compare</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>Do not write this register again until after any previous scan line compare has completed.</p>	Value	Name	0b	Do nothing	1b	Initiate compare			
Value	Name										
0b	Do nothing										
1b	Initiate compare										
	30	<p>Inclusive Exclusive Select This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Exclusive</td> <td>Exclusive mode: trigger scan line event when inside the scan line window</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Inclusive</td> <td>Inclusive mode: trigger scan line event when outside the scan line window</td> </tr> </tbody> </table>	Value	Name	Description	0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window	1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window
Value	Name	Description									
0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window									
1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window									
	29	<p>Counter Select This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Timing generator</td> <td>Use the scanline count from the pipe timing generator</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Plane</td> <td>Use the scanline count from plane selected in PIPE_MISC2.</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.</p>	Value	Name	Description	0b	Timing generator	Use the scanline count from the pipe timing generator	1b	Plane	Use the scanline count from plane selected in PIPE_MISC2.
Value	Name	Description									
0b	Timing generator	Use the scanline count from the pipe timing generator									
1b	Plane	Use the scanline count from plane selected in PIPE_MISC2.									
	28:16	<p>Start Scan Line This field specifies the starting scan line number of the scan line window.</p>									
	15	<p>Render Response Destination This bit indicates what destination to send the scan line event render response to.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>CS</td> <td>Send scan line event response to CS</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>BCS</td> <td>Send scan line event response to BCS</td> </tr> </tbody> </table>	Value	Name	Description	0b	CS	Send scan line event response to CS	1b	BCS	Send scan line event response to BCS
Value	Name	Description									
0b	CS	Send scan line event response to CS									
1b	BCS	Send scan line event response to BCS									

PIPE_SCANLINECOMP		
	14:13	Reserved
		Access: RO
		Format: MBZ
	12:0	End Scan Line This field specifies the ending scan line number of the scan line window.

PIPE_SEAM_EXCESS

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank OR pipe disabled	
Address:	60020h-60023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_A
Reset:	soft
Address:	61020h-61023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_B
Reset:	soft
Address:	62020h-62023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_C
Reset:	soft
Address:	63020h-63023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_D
Reset:	soft
<p>This register defines the number of excess pixels within the Pipe window (on the right or left) that the Scaler will need to remove from the post scaled image.</p> <p>When an image is split across two Pipes, scaled, and then joined at the Port, the Scalers within each Pipe will operate on a split image that contains overlap pixels around where the final seam will be to facilitate a seamless join at the Port. For example, if the left portion of an image is being scaled in Pipe A and the right portion of the image is being scaled in Pipe B, then there will be an excess number of pixels (i.e. overlap pixels) on the right side of the Pipe A image and an excess number of pixels on the left side of the Pipe B image. The overlap pixels of the window within each of the Pipes need to be dropped by the Scaler before they are delivered to the Port.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. Dropping of the overlap/excess pixels is done at the very end of the Pipe within the Scaler regardless of whether a Scaler is bound to the Pipe, or not. 2. The values programmed within this register are one-based (i.e. a programming of 1 equals 1 pixel of excess) 3. The values programmed within this register will be added to the Horizontal Active programming of the TRANS_HTOTAL register of the port bound to this pipe. I.e. the pipe will see a Horizontal size equal to Horizontal Active + Left Excess Amount + Right Excess Amount 	

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS

Restriction :

1. The number of excess pixels cannot exceed the size of the horizontal blank, otherwise there will not be enough time to throw them away before starting the next line and the image will be corrupted
2. Pillarbox borders must be even
3. The source size on each pipe, including pre-scale excess, must be a multiple of 2. When the Pipe output format is YUV 420 with full blend, the source size is required to be a multiple of 4.

DWord	Bit	Description
0	31:29	Reserved
		Access: RO
		Format: MBZ
	28:16	Right Excess Amount This field defines the number of excess pixels to drop, if any, on the right side of the Pipe window
	15:13	Reserved
Access: RO		
Format: MBZ		
12:0	Left Excess Amount This field defines the number of excess pixels to drop, if any, on the left side of the Pipe window	

PIPE_SRC SZ

PIPE_SRC SZ					
Register Space:	MMIO: 0/2/0				
Access:	Double Buffered				
Size (in bits):	32				
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank					
Address:	6001Ch-6001Fh				
Name:	Pipe Source Image Size				
ShortName:	PIPE_SRC SZ_A				
Reset:	soft				
Address:	6101Ch-6101Fh				
Name:	Pipe Source Image Size				
ShortName:	PIPE_SRC SZ_B				
Reset:	soft				
Address:	6201Ch-6201Fh				
Name:	Pipe Source Image Size				
ShortName:	PIPE_SRC SZ_C				
Reset:	soft				
Address:	6301Ch-6301Fh				
Name:	Pipe Source Image Size				
ShortName:	PIPE_SRC SZ_D				
Reset:	soft				
There is one instance of this register for each pipe.					
Programming Notes					
In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.					
DWord	Bit	Description			
0	31:29	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
Format:	MBZ				
28:16	<p>Horizontal Source Size</p> <p>This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> • This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled or DSC pixel replication is enabled. <ul style="list-style-type: none"> • Refer to PS_CTRL for size restrictions when panel fitting is enabled. </td> </tr> </tbody> </table>	Restriction	<ul style="list-style-type: none"> • This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled or DSC pixel replication is enabled. <ul style="list-style-type: none"> • Refer to PS_CTRL for size restrictions when panel fitting is enabled. 		
Restriction					
<ul style="list-style-type: none"> • This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled or DSC pixel replication is enabled. <ul style="list-style-type: none"> • Refer to PS_CTRL for size restrictions when panel fitting is enabled. 					

PIPE_SRC SZ					
	<ul style="list-style-type: none"> Horizontal source size must always be even. The programmed value must be odd. 				
15:13	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
12:0	<p>Vertical Source Size This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one.</p> <p style="text-align: center;">Restriction</p> <p>Vertical source sizes larger than 4320 lines are not supported. This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Refer to PS_CTRL for size restrictions when panel fitting is enabled.</p>				

PIPE_STATUS

PIPE_STATUS		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
CrashLogSaved:	true	
CrashLogPriority:	1	
CrashLogVisibility:	public	
ExternalLongName:	DE Pipe Status	
ExternalDescription:	Display engine pipe status	
Address:	70058h-7005Bh	
Name:	Pipe Status	
ShortName:	PIPE_STATUS_A	
Reset:	soft	
Address:	71058h-7105Bh	
Name:	Pipe Status	
ShortName:	PIPE_STATUS_B	
Reset:	soft	
Address:	72058h-7205Bh	
Name:	Pipe Status	
ShortName:	PIPE_STATUS_C	
Reset:	soft	
Address:	73058h-7305Bh	
Name:	Pipe Status	
ShortName:	PIPE_STATUS_D	
Reset:	soft	
DWord	Bit	Description
0	31	Underrun Access: R/WC This field indicates that there is an underrun on the transcoder attached to this pipe.
	30	Vblank Access: R/WC The field is set at the start of the vertical blank of the transcoder attached to this pipe.
	29	Frame start Access: R/WC The field is set at the frame start of the transcoder attached to this pipe.
	28	Not Used 28

PIPE_STATUS

27	Not Used 27	
26	Not Used 26	
	Access:	R/WC
25	Not Used 25	
	Access:	R/WC
24	Not Used 24	
	Access:	R/WC
23	Not Used 23	
	Access:	R/WC
22	Not Used 22	
	Access:	R/WC
21	Not Used 21	
	Access:	R/WC
20	Not Used 20	
	Access:	R/WC
19	Not Used 19	
	Access:	R/WC
18	Not Used 18	
	Access:	R/WC
17	Not Used 17	
	Access:	R/WC
16	Not Used 16	
	Access:	R/WC
15	Not Used 15	
	Access:	R/WC
14	Not Used 14	
	Access:	R/WC
13	Not Used 13	
	Access:	R/WC
12	Not Used 12	
	Access:	R/WC
11	Not Used 11	
	Access:	R/WC
10	Not Used 10	
	Access:	R/WC

PIPE_STATUS

9	Not Used 9	Access:	R/WC
8	Not Used 8	Access:	R/WC
7	Not Used 7	Access:	R/WC
6	BW Credits Pending At VBlank	Access:	R/WC
	A '1' indicates that the there are some pending MBUS BW-Credits at the start of VBlank. Sticky bit cleared by a write of '1'		
5	B Credits Pending At VBlank	Access:	R/WC
	A '1' indicates that the there are some pending MBUS B-Credits at the start of VBlank. Sticky bit cleared by a write of '1'		
4	A Credits Pending At VBlank	Access:	R/WC
	A '1' indicates that the there are some pending MBUS A-Credits at the start of VBlank. Sticky bit cleared by a write of '1'		
3	Not Used 3	Access:	R/WC
2	Not used 2	Access:	R/WC
1	Valid Block At FrameStart	Access:	R/WC
	A '1' indicates that a valid block is still present in Display Buffer at frame start. Sticky bit cleared by a write of '1'.		
0	Valid Block Overwritten	Access:	R/WC
	A '1' indicates that a valid block in Display Buffer was overwritten. Sticky bit cleared by a write of '1'.		

PIPEDMC_CONTROL

PIPEDMC_CONTROL - PIPEDMC_CONTROL		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	45250h-45253h	
Name:	Pipe DMC Control	
ShortName:	PIPEDMC_CONTROL_A	
Reset:	soft	
Address:	45254h-45257h	
Name:	Pipe DMC Control	
ShortName:	PIPEDMC_CONTROL_B	
Reset:	soft	
Address:	45258h-4525Bh	
Name:	Pipe DMC Control	
ShortName:	PIPEDMC_CONTROL_C	
Reset:	soft	
Address:	4525Ch-4525Fh	
Name:	Pipe DMC Control	
ShortName:	PIPEDMC_CONTROL_D	
Reset:	soft	
This Register is to add pipe DMC enable. To use pipeDMC driver must enable pipeDMC first.		
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
	Format: MBZ	
	0	pipedmc_enable
Access: R/W		
		Setting this bit enables the pipeDMC.



Pixel Shader Scheduling Mode

PSS_MODE - Pixel Shader Scheduling Mode			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	07038h		
Name:	Pixel Shader Scheduling Mode		
ShortName:	PSS_MODE		
Mode registers for Pixel Shader Scheduling.			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		_Custom_GTIReset:	DEV
		Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)	
	15:14	Reserved	
		Access:	R/W
		Format:	PBC
		_Custom_GTIReset:	DEV
	13:10	Maximum Allowed PS Thread Dependencies	
		Default Value:	8h
		Access:	R/W
		Format:	U4
_Custom_GTIReset:		DEV	
Sets the maximum number of dependencies that a pixel shader thread can have. If a thread requires more than this number, thread dispatch will be stalled until enough threads that this thread is dependent on have retired. Since maximum number of dependencies in a Pixel Shader is 8 (for fused-SIMD16, corresponding to 8 2X2 pixel block; fused-SIMD32 corresponding to 8 4x2 pixel blocks), programming a value higher than 0X8 is illegal. If HW chooses to launch lower SIMD thread e.g. fused-SIMD8, it will not have more than 4 dependencies. Hence, programming 0x8 guarantees maximum dependencies for all SIMD width dispatches.			
9	3D Scoreboard Address XOR Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	DEV	
	Value	Name	Description
	0h	Enabled [Default]	3D Scoreboard Address calculation includes XOR of higher bits
	1h	Disabled	3D Scoreboard Address calculation based on lower address bits only

PSS_MODE - Pixel Shader Scheduling Mode

8	Reserved	
	Access:	R/W
	Format:	PBC
	_Custom_GTIReset:	DEV
7	Stalling behavior disable for PS Dispatch for PTBR	
	Access:	R/W
	_Custom_GTIReset:	DEV
	<p>This bit, when enabled, allows PS dispatch function to not stall when no TILE ID is free for incoming new tile access under PTBR. Although this behavior is non stalling, it has a potential to reduce number of color pixel blocks from tile cache in certain cases.</p>	
	Value	Name
	Description	
0	[Default]	This is a default value and default behavior is to have PS dispatch stall when there are no free TILE_IDs available for incoming new access on a new TILE under PTBR.
1		When this bit is set, PS dispatch does not stall for a new incoming tile but simply uses the next TILE_ID without waiting for it to be free. SW should enable this bit if there are perf downsides with stalling behavior and additional discard BW is not significant.
6:5	Thread Scheduler Mode	
	Access:	R/W
	Format:	U2
	_Custom_GTIReset:	DEV
	Selects the PSD selection policy	
	Value	Name
	Description	
0h	8x8 Round-Robin [Default]	Scheduler alternates PSDs to load entire 8x8
1h	8x8 Fixed	Scheduler statically hashes each 8x8 based on xy address
2h	8x8 Dynamic	At the start of each 8x8, scheduler selects a PSD to load entire 8x8 based on EU load
3h	Reserved	
4	Disable 4x4 schedule optimization	
	Access:	R/W
	Format:	Disable
	_Custom_GTIReset:	DEV
	If set, prevent scheduler from attempting to pack 4x4 at SIMD16 alignment.	
	Value	Name
0h	4x4 packed at SIMD16 alignment if possible [Default]	
1h	scheduler does not consider 4x4 when packing threads	

PSS_MODE - Pixel Shader Scheduling Mode			
3	Disable 4x2 schedule optimization		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	DEV	
	If set, prevent scheduler from attempting to pack 4x2 at SIMD8 alignment.		
	Value	Name	
	0h	4x2 packed at SIMD8 alignment if possible [Default]	
	1h	scheduler does not consider 4x2 when packing threads	
	2	Disable fused thread scheduling	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	DEV
		If set, scheduler will only populate the first thread of a fused thread. A fused thread will still be dispatched, but will only contain a single thread.	
		Value	Name
		0h	Fused thread enabled [Default]
1h	Fused thread disabled		
1:0	Limit maximum number of polys per fused-thread		
	Access:	R/W	
	Format:	U2	
	_Custom_GTIReset:	DEV	
	Limit the scheduler to pack no more than the indicated number polys into a single fused-thread.		
	Value	Name	
	0h	Polys per fused-thread is not limited [Default]	
	1h	Maximum polys per fused-thread limited to 1	
2h	Maximum polys per fused-thread limited to 2		
3h	Maximum polys per fused-thread limited to 3		

Pixel Shader Scheduling Mode 2

DWord		Bit	Description																
PSS_MODE2 - Pixel Shader Scheduling Mode 2																			
Register Space:		MMIO: 0/2/0																	
Size (in bits):		32																	
Address:		0703Ch																	
Name:		Pixel Shader Scheduling Mode																	
ShortName:		PSS_MODE2																	
Mode register for Pixel Shader Scheduling.																			
0	31:16	Mask <table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)</p>		Access:	WO	_Custom_GTIReset:	DEV												
Access:	WO																		
_Custom_GTIReset:	DEV																		
	15:9	Reserved <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>PBC</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table>		Access:	R/W	Format:	PBC	_Custom_GTIReset:	DEV										
Access:	R/W																		
Format:	PBC																		
_Custom_GTIReset:	DEV																		
	8	PS Load Bias match size <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>Select the granularity of xy compare for determining if the incoming 8x8 matches history buffer used for 8x8 Match PS Load Bias.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>8x8 [Default]</td> </tr> <tr> <td>1h</td> <td>16x16</td> </tr> </tbody> </table>		Access:	R/W	_Custom_GTIReset:	DEV	Value	Name	0h	8x8 [Default]	1h	16x16						
Access:	R/W																		
_Custom_GTIReset:	DEV																		
Value	Name																		
0h	8x8 [Default]																		
1h	16x16																		
	7:6	8x8 Match PS Load Bias <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>U2</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>When scheduler is in dynamic mode, PSS will be create a load imbalance by the selected number of threads when a new 8x8 matches history buffer or any partially collected threads. This will direct matching 8x8 to the same PSD when load is not extremely skewed.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>2_7 [Default]</td> </tr> <tr> <td>1h</td> <td>4_7</td> </tr> <tr> <td>2h</td> <td>8_7</td> </tr> <tr> <td>3h</td> <td>0_7</td> </tr> </tbody> </table>		Access:	R/W	Format:	U2	_Custom_GTIReset:	DEV	Value	Name	0h	2_7 [Default]	1h	4_7	2h	8_7	3h	0_7
Access:	R/W																		
Format:	U2																		
_Custom_GTIReset:	DEV																		
Value	Name																		
0h	2_7 [Default]																		
1h	4_7																		
2h	8_7																		
3h	0_7																		

PSS_MODE2 - Pixel Shader Scheduling Mode 2

5	Scoreboard Stall Flush Control				
	Access:			R/W	
	_Custom_GTIRreset:			DEV	
	Value	Name	Description		
	0h	Start Thread Group [Default]	pipe_control with Stall at Scoreboard set creates a new thread group instead of stalling at scoreboard. PS threads launched after pipe_control will have sendc dependency to all threads before pipe_control. This is a pipelined flush and will not drain EUs of PS threads.		
	1h	Scoreboard Stall	pipe_control with Stall at Scoreboard set stalls at PSS scoreboard until all previous threads have completed. This will drain EUs of all PS threads.		
	4	Thread Group Dependency Control			
		Access:			R/W
		_Custom_GTIRreset:			DEV
		Value	Name		
		0h	Use 9th dependency to enforce ordering between thread groups. [Default]		
		1h	Perform stall at PSSunit when thread group changes.		
3	Over-subscribe PS thread allocation				
	Access:			R/W	
	Format:			Enable	
	_Custom_GTIRreset:			DEV	
	Value	Name			
	0h	Number of enabled threads does not affect PS thread scheduling [Default]			
1h	Number of PS threads scheduled per-PSD will not exceed number of enabled threads				
2:0	PS Dispatch Time-out Values				
	Access:			R/W	
	_Custom_GTIRreset:			DEV	
	Valid values other than 111, allow SW to program number of clocks PS dispatch function wait to combine fuse thread sequence (aka bundle). Setting 111 disables the time-out mechanism and will wait indefinitely for an event to end the collection of pixels.				
	Value	Name	Description	Programming Notes	
	0h	32_2	PS dispatch function waits for 32 clocks for gathering more pixels in the current bundle.		
1h	64	PS dispatch function waits for 64			

PSS_MODE2 - Pixel Shader Scheduling Mode 2

			clocks for gathering more pixels in the current bundle.	
2h	128		PS dispatch function waits for 128 clocks for gathering more pixels in the current bundle.	
3h	256		PS dispatch function waits for 256 clocks for gathering more pixels in the current bundle.	
4h	512		PS dispatch function waits for 512 clocks for gathering more pixels in the current bundle.	
5h	1024		PS dispatch function waits for 1024 clocks for gathering more pixels in the current bundle.	
6h	2048 [Default]		PS dispatch function waits for 2048 clocks for gathering more pixels in the current bundle.	
7h			PSD waits indefinitely to assemble a bundle before dispatching a PS.	This value may not be programmed if non-promoted depth or stencil is enabled.



PLANE_AUX_DIST

PLANE_AUX_DIST	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704C0h-704C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_A
Reset:	soft
Address:	705C0h-705C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_A
Reset:	soft
Address:	706C0h-706C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_A
Reset:	soft
Address:	707C0h-707C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_A
Reset:	soft
Address:	714C0h-714C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_B
Reset:	soft
Address:	715C0h-715C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_B
Reset:	soft
Address:	716C0h-716C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_B
Reset:	soft
Address:	717C0h-717C3h

PLANE_AUX_DIST	
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_B
Reset:	soft
Address:	724C0h-724C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_C
Reset:	soft
Address:	725C0h-725C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_C
Reset:	soft
Address:	726C0h-726C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_C
Reset:	soft
Address:	727C0h-727C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_C
Reset:	soft
Address:	734C0h-734C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_4_D
Reset:	soft
Address:	735C0h-735C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_5_D
Reset:	soft
Address:	736C0h-736C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_6_D
Reset:	soft
Address:	737C0h-737C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_7_D
Reset:	soft
Address:	701C0h-701C3h

PLANE_AUX_DIST	
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_A
Reset:	soft
Address:	702C0h-702C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_A
Reset:	soft
Address:	703C0h-703C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_A
Reset:	soft
Address:	711C0h-711C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_B
Reset:	soft
Address:	712C0h-712C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_B
Reset:	soft
Address:	713C0h-713C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_B
Reset:	soft
Address:	721C0h-721C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_1_C
Reset:	soft
Address:	722C0h-722C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_2_C
Reset:	soft
Address:	723C0h-723C3h
Name:	Plane Auxiliary Surface Distance
ShortName:	PLANE_AUX_DIST_3_C
Reset:	soft
Address:	731C0h-731C3h

PLANE_AUX_DIST						
Name:	Plane Auxiliary Surface Distance					
ShortName:	PLANE_AUX_DIST_1_D					
Reset:	soft					
Address:	732C0h-732C3h					
Name:	Plane Auxiliary Surface Distance					
ShortName:	PLANE_AUX_DIST_2_D					
Reset:	soft					
Address:	733C0h-733C3h					
Name:	Plane Auxiliary Surface Distance					
ShortName:	PLANE_AUX_DIST_3_D					
Reset:	soft					
<p>This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface. Unlike the surface base address, this register value cannot be updated through flips.</p>						
DWord	Bit	Description				
0	31:12	<p>Auxiliary Surface Distance</p> <p>When using a compressed surface, this field represents the distance of the control surface in 4K pages, where a value of [31:12] = 1 represents one 4K page.</p>				
	11:10	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
Format:	MBZ					
9:0	<p>Auxiliary Surface Stride</p> <table border="1"> <tr> <th style="text-align: center;">Description</th> </tr> <tr> <td>This field is unused. Leave at default value.</td> </tr> </table>	Description	This field is unused. Leave at default value.			
Description						
This field is unused. Leave at default value.						



PLANE_BUF_CFG

PLANE_BUF_CFG	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	7017Ch-7017Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_A
Reset:	soft
Address:	7117Ch-7117Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_B
Reset:	soft
Address:	7217Ch-7217Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_C
Reset:	soft
Address:	7317Ch-7317Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_D
Reset:	soft
Address:	7057Ch-7057Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_A
Reset:	soft
Address:	7067Ch-7067Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_A
Reset:	soft
Address:	7077Ch-7077Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_A
Reset:	soft
Address:	7087Ch-7087Fh

PLANE_BUF_CFG	
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_A
Reset:	soft
Address:	7157Ch-7157Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_B
Reset:	soft
Address:	7167Ch-7167Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_B
Reset:	soft
Address:	7177Ch-7177Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_B
Reset:	soft
Address:	7187Ch-7187Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_B
Reset:	soft
Address:	7257Ch-7257Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_C
Reset:	soft
Address:	7267Ch-7267Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_C
Reset:	soft
Address:	7277Ch-7277Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_C
Reset:	soft
Address:	7287Ch-7287Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_C
Reset:	soft
Address:	7357Ch-7357Fh

PLANE_BUF_CFG	
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_D
Reset:	soft
Address:	7367Ch-7367Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_D
Reset:	soft
Address:	7377Ch-7377Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_6_D
Reset:	soft
Address:	7387Ch-7387Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_7_D
Reset:	soft
Address:	7027Ch-7027Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_A
Reset:	soft
Address:	7037Ch-7037Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_A
Reset:	soft
Address:	7047Ch-7047Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_A
Reset:	soft
Address:	7127Ch-7127Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_B
Reset:	soft
Address:	7137Ch-7137Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_B
Reset:	soft
Address:	7147Ch-7147Fh

PLANE_BUF_CFG			
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_3_B		
Reset:	soft		
Address:	7227Ch-7227Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_1_C		
Reset:	soft		
Address:	7237Ch-7237Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_2_C		
Reset:	soft		
Address:	7247Ch-7247Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_3_C		
Reset:	soft		
Address:	7327Ch-7327Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_1_D		
Reset:	soft		
Address:	7337Ch-7337Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_2_D		
Reset:	soft		
Address:	7347Ch-7347Fh		
Name:	Plane Buffer Config		
ShortName:	PLANE_BUF_CFG_3_D		
Reset:	soft		
DWord	Bit	Description	
0	31:28	Reserved	
		Access:	RO
		Format:	MBZ
	27	Reserved	
		Access:	RO
		Format:	MBZ
	26:16	Buffer End	
		Default Value:	000h

PLANE_BUF_CFG			
		This field contains the buffer end position for this plane.	
	15:12	Reserved	
		Access:	RO
		Format:	MBZ
	11	Reserved	
		Access:	RO
		Format:	MBZ
	10:0	Buffer Start	
		Default Value:	000h
		This field contains the buffer start position for this plane.	

PLANE_CC_VAL

PLANE_CC_VAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	64
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704B4h-704BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_A
Reset:	soft
Address:	705B4h-705BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_A
Reset:	soft
Address:	706B4h-706BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_6_A
Reset:	soft
Address:	707B4h-707BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_7_A
Reset:	soft
Address:	714B4h-714BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_B
Reset:	soft
Address:	715B4h-715BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_B
Reset:	soft
Address:	716B4h-716BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_6_B
Reset:	soft
Address:	717B4h-717BBh

PLANE_CC_VAL	
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_7_B
Reset:	soft
Address:	724B4h-724BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_C
Reset:	soft
Address:	725B4h-725BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_C
Reset:	soft
Address:	726B4h-726BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_6_C
Reset:	soft
Address:	727B4h-727BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_7_C
Reset:	soft
Address:	734B4h-734BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_D
Reset:	soft
Address:	735B4h-735BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_D
Reset:	soft
Address:	736B4h-736BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_6_D
Reset:	soft
Address:	737B4h-737BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_7_D
Reset:	soft
Address:	701B4h-701BBh

PLANE_CC_VAL	
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_A
Reset:	soft
Address:	702B4h-702BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_A
Reset:	soft
Address:	703B4h-703BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_A
Reset:	soft
Address:	711B4h-711BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_B
Reset:	soft
Address:	712B4h-712BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_B
Reset:	soft
Address:	713B4h-713BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_B
Reset:	soft
Address:	721B4h-721BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_C
Reset:	soft
Address:	722B4h-722BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_C
Reset:	soft
Address:	723B4h-723BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_C
Reset:	soft
Address:	731B4h-731BBh

PLANE_CC_VAL		
Name:	Plane Clear Color Value	
ShortName:	PLANE_CC_VAL_1_D	
Reset:	soft	
Address:	732B4h-732BBh	
Name:	Plane Clear Color Value	
ShortName:	PLANE_CC_VAL_2_D	
Reset:	soft	
Address:	733B4h-733BBh	
Name:	Plane Clear Color Value	
ShortName:	PLANE_CC_VAL_3_D	
Reset:	soft	
<p>This register programs the clear color value to be used with render decompression. The value is used only when render decompression and clear color are both enabled in the plane control register.</p> <p>The register value can be updated when flipping to a new surface with new clear color value. It does not need to be updated if the new surface has the same clear color value as the previous surface.</p>		
DWord	Bit	Description
0	31:0	Clear Color Value DW0 This field gives the 32 bit value of the clear color.
1	31:0	Clear Color Value DW1 This field gives the upper 32 bit value of the clear color. This field is used only with 64 bits formats, ignored otherwise.

PLANE_COLOR_CTL

PLANE_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704CCh-704CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_A
Reset:	soft
Address:	705CCh-705CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_A
Reset:	soft
Address:	706CCh-706CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_A
Reset:	soft
Address:	707CCh-707CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_A
Reset:	soft
Address:	714CCh-714CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_B
Reset:	soft
Address:	715CCh-715CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_B
Reset:	soft
Address:	716CCh-716CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_B
Reset:	soft
Address:	717CCh-717CFh

PLANE_COLOR_CTL	
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_B
Reset:	soft
Address:	724CCh-724CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_C
Reset:	soft
Address:	725CCh-725CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_C
Reset:	soft
Address:	726CCh-726CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_C
Reset:	soft
Address:	727CCh-727CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_C
Reset:	soft
Address:	734CCh-734CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_D
Reset:	soft
Address:	735CCh-735CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_D
Reset:	soft
Address:	736CCh-736CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_6_D
Reset:	soft
Address:	737CCh-737CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_7_D
Reset:	soft
Address:	701CCh-701CFh

PLANE_COLOR_CTL	
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_A
Reset:	soft
Address:	702CCh-702CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_A
Reset:	soft
Address:	703CCh-703CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_A
Reset:	soft
Address:	711CCh-711CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_B
Reset:	soft
Address:	712CCh-712CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_B
Reset:	soft
Address:	713CCh-713CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_B
Reset:	soft
Address:	721CCh-721CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_C
Reset:	soft
Address:	722CCh-722CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_C
Reset:	soft
Address:	723CCh-723CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_C
Reset:	soft
Address:	731CCh-731CFh

PLANE_COLOR_CTL											
Name:	Plane Color Control										
ShortName:	PLANE_COLOR_CTL_1_D										
Reset:	soft										
Address:	732CCh-732CFh										
Name:	Plane Color Control										
ShortName:	PLANE_COLOR_CTL_2_D										
Reset:	soft										
Address:	733CCh-733CFh										
Name:	Plane Color Control										
ShortName:	PLANE_COLOR_CTL_3_D										
Reset:	soft										
DWord	Bit	Description									
0	31	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
	Access:	RO									
	Format:	MBZ									
	30	Pipe Gamma Enable This bit enables pipe gamma correction for the plane pixel data. This field is deprecated. Use 'GAMMA_MODE.Post CSC Gamma Enable' for enabling pipe gamma across all pixels from all planes. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 40%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable			
	Value	Name									
	0b	Disable									
	1b	Enable									
	29	Remove YUV Offset This field controls whether the plane removes or preserves the 1/2 offset on U and V components when the source pixel format is YUV and the plane YUV to RGB CSC is disabled. This bit has no effect on RGB source pixel formats <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Remove</td> <td>Remove 1/2 offset on UV components</td> </tr> <tr> <td>1b</td> <td>Preserve</td> <td>Preserve 1/2 offset on UV components</td> </tr> </tbody> </table>	Value	Name	Description	0b	Remove	Remove 1/2 offset on UV components	1b	Preserve	Preserve 1/2 offset on UV components
	Value	Name	Description								
	0b	Remove	Remove 1/2 offset on UV components								
1b	Preserve	Preserve 1/2 offset on UV components									
28	YUV Range Correction Disable Setting this bit disables the YUV range correction logic inside the plane. The range correction logic is used to expand the compressed range YUV to full range YUV. The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range. Extended range values will be preserved after the expansion. This bit has no effect on RGB source pixel formats since they automatically bypass range correction.										

PLANE_COLOR_CTL																				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> </tr> <tr> <td>1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable												
Value	Name																			
0b	Enable																			
1b	Disable																			
27:24	Reserved	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ														
Access:	RO																			
Format:	MBZ																			
23	Pipe CSC Enable	<p>This bit enables pipe color space conversion and the pipe pre color space conversion gamma for the plane pixel data. This is separate from the color conversion logic within the plane.</p> <p>This field is deprecated. Use 'CSC_MODE.Pipe CSC Enable', 'GAMMA_MODE.Pre CSC Gamma Enable' for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Plane CSC must be used for plane specific color space conversion.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable												
Value	Name																			
0b	Disable																			
1b	Enable																			
22	Reserved																			
21	Plane CSC Enable	<p>This field enables the plane color space conversion. This field applies only to planes 1 through 3.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable												
Value	Name																			
0b	Disable																			
1b	Enable																			
20	Plane Input CSC Enable	<p>This field enables the plane input color space conversion. This field applies only to planes 1 through 3.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable												
Value	Name																			
0b	Disable																			
1b	Enable																			
19:17	Plane CSC Mode	<table border="1"> <thead> <tr> <th colspan="3">Description</th> </tr> </thead> <tbody> <tr> <td colspan="3">This field specifies the mode of plane color space conversion operation.</td> </tr> <tr> <td colspan="3">This is used only for planes 4 through 7. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>000b</td> <td>Bypass</td> <td>Pixel data bypasses the plane color space conversion</td> </tr> <tr> <td>001b</td> <td>YUV601 to RGB601</td> <td>YUV BT.601 to RGB BT.601 conversion.</td> </tr> </tbody> </table>	Description			This field specifies the mode of plane color space conversion operation.			This is used only for planes 4 through 7. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.			Value	Name	Description	000b	Bypass	Pixel data bypasses the plane color space conversion	001b	YUV601 to RGB601	YUV BT.601 to RGB BT.601 conversion.
Description																				
This field specifies the mode of plane color space conversion operation.																				
This is used only for planes 4 through 7. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.																				
Value	Name	Description																		
000b	Bypass	Pixel data bypasses the plane color space conversion																		
001b	YUV601 to RGB601	YUV BT.601 to RGB BT.601 conversion.																		

PLANE_COLOR_CTL			
	010b	YUV709 to RGB709	YUV BT.709 to RGB BT.709 conversion.
	011b	YUV2020 to RGB2020	YUV BT.2020 to RGB BT.2020 conversion.
	100b	RGB709 to RGB2020	RGB BT.709 to RGB BT.2020 conversion.
16	Reserved		
	Access:		RO
	Format:		MBZ
15	Plane Post CSC Gamma Multi Segment Enable		
	This bit enables plane post CSC gamma multi segment processing. It is only used for HDR tone Mapping. It is only valid if Plane Gamma (bit[13]) is enabled.		
	Value	Name	
	1b	Enable	
	0b	Disable [Default]	
14	Plane Pre CSC Gamma Enable		
	This bit controls plane internal pre-CSC gamma correction.		
	Value	Name	
	1b	Enable	
	0b	Disable	
13	Plane Gamma Disable		
	This bit controls plane internal post-CSC gamma correction.		
	Value	Name	
	1b	Disable	
	0b	Enable	
12	Plane Gamma Mode		
	This field specifies the plane gamma mode of operation. This field is ignored if plane gamma is disabled.		
	Value	Name	Description
	0b	Direct [Default]	Direct mode is used for regular plane gamma programming. Lookup is based on incoming pixel individual r, g, b values. The output is a computed by lookup of two nearest points and interpolation.
	1b	Multiply	<p>Multiple mode is used when plane gamma is used for HDR tone mapping. Lookup is based on a pseudo luminance of the incoming pixel calculated using $L_{in} = 0.25 * \text{Red input} + 0.625 * \text{Green input} + 0.125 * \text{Blue input}$. An adjustment factor 'F' is computed by lookup of two nearest points and interpolation. Output is computed by multiplying each color channel with the adjustment factor F.</p>
11	Plane Gamma Multiplier Precision		
	This field specifies the plane gamma entry format in the multiplier mode. This field is ignored in the direct lookup mode. The gamma entries can be programmed in either unsigned 0.24 format or unsigned 8.16 format.		

PLANE_COLOR_CTL														
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>U0.24 [Default]</td> </tr> <tr> <td>1b</td> <td>U8.16</td> </tr> </tbody> </table>	Value	Name	0b	U0.24 [Default]	1b	U8.16						
Value	Name													
0b	U0.24 [Default]													
1b	U8.16													
10:6	Reserved	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ								
Access:	RO													
Format:	MBZ													
5:4	Alpha Mode	<p>This field controls how the plane will use per pixel alpha data from frame buffer. Constant plane alpha is defined in PLANE_KEYMSK and PLANE_KEYMAX registers.</p> <p>RGB 64-bit - only alpha in 0-1 range supported with 8 bit granularity. RGB 64-bit UINT - only 8 upper bits of alpha used. RGB 2:10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity. XR_BIAS 10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> <td>Alpha channel ignored.</td> </tr> <tr> <td>10b</td> <td>Enable with SW pre-multiply</td> <td>Alpha channel used. Color channels should be pre-multiplied with alpha by software.</td> </tr> <tr> <td>11b</td> <td>Enable with HW pre-multiply</td> <td>Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>Per pixel alpha is supported only with RGB pixel formats. FBC is not compatible with per pixel alpha.</p>	Value	Name	Description	00b	Disable	Alpha channel ignored.	10b	Enable with SW pre-multiply	Alpha channel used. Color channels should be pre-multiplied with alpha by software.	11b	Enable with HW pre-multiply	Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.
Value	Name	Description												
00b	Disable	Alpha channel ignored.												
10b	Enable with SW pre-multiply	Alpha channel used. Color channels should be pre-multiplied with alpha by software.												
11b	Enable with HW pre-multiply	Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.												
3:0	Reserved	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ								
Access:	RO													
Format:	MBZ													



PLANE_CSC_COEFF

PLANE_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70210h-70227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_A
Reset:	soft
Address:	70310h-70327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_A
Reset:	soft
Address:	70410h-70427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_A
Reset:	soft
Address:	71210h-71227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_B
Reset:	soft
Address:	71310h-71327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_B
Reset:	soft
Address:	71410h-71427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_B
Reset:	soft
Address:	72210h-72227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_C
Reset:	soft
Address:	72310h-72327h

PLANE_CSC_COEFF		
Name:	Plane CSC Coefficients	
ShortName:	PLANE_CSC_COEFF_2_C	
Reset:	soft	
Address:	72410h-72427h	
Name:	Plane CSC Coefficients	
ShortName:	PLANE_CSC_COEFF_3_C	
Reset:	soft	
Address:	73210h-73227h	
Name:	Plane CSC Coefficients	
ShortName:	PLANE_CSC_COEFF_1_D	
Reset:	soft	
Address:	73310h-73327h	
Name:	Plane CSC Coefficients	
ShortName:	PLANE_CSC_COEFF_2_D	
Reset:	soft	
Address:	73410h-73427h	
Name:	Plane CSC Coefficients	
ShortName:	PLANE_CSC_COEFF_3_D	
Reset:	soft	
Programming Notes		
Refer to Color Space Conversion page for programming details and examples.		
DWord	Bit	Description
0	31:16	RY Format: CSC COEFFICIENT FORMAT
	15:0	GY Format: CSC COEFFICIENT FORMAT
1	31:16	BY Format: CSC COEFFICIENT FORMAT
	15:0	Reserved Access: RO Format: MBZ
2	31:16	RU Format: CSC COEFFICIENT FORMAT
	15:0	GU Format: CSC COEFFICIENT FORMAT
3	31:16	BU

PLANE_CSC_COEFF			
		Format:	CSC COEFFICIENT FORMAT
	15:0	Reserved	
		Access:	RO
		Format:	MBZ
4	31:16	RV	
		Format:	CSC COEFFICIENT FORMAT
	15:0	GV	
		Format:	CSC COEFFICIENT FORMAT
5	31:16	BV	
		Format:	CSC COEFFICIENT FORMAT
	15:0	Reserved	
		Access:	RO
		Format:	MBZ

PLANE_CSC_POSTOFF

PLANE_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70234h-7023Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_A
Reset:	soft
Address:	70334h-7033Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_A
Reset:	soft
Address:	70434h-7043Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_A
Reset:	soft
Address:	71234h-7123Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_B
Reset:	soft
Address:	71334h-7133Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_B
Reset:	soft
Address:	71434h-7143Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_B
Reset:	soft
Address:	72234h-7223Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_C
Reset:	soft
Address:	72334h-7233Fh

PLANE_CSC_POSTOFF		
Name:	Plane CSC Post-offset	
ShortName:	PLANE_CSC_POSTOFF_2_C	
Reset:	soft	
Address:	72434h-7243Fh	
Name:	Plane CSC Post-offset	
ShortName:	PLANE_CSC_POSTOFF_3_C	
Reset:	soft	
Address:	73234h-7323Fh	
Name:	Plane CSC Post-offset	
ShortName:	PLANE_CSC_POSTOFF_1_D	
Reset:	soft	
Address:	73334h-7333Fh	
Name:	Plane CSC Post-offset	
ShortName:	PLANE_CSC_POSTOFF_2_D	
Reset:	soft	
Address:	73434h-7343Fh	
Name:	Plane CSC Post-offset	
ShortName:	PLANE_CSC_POSTOFF_3_D	
Reset:	soft	
<p>The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane color space conversion (CSC).</p>		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
	12:0	PostCSC High Offset This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	Reserved
		Access: RO
		Format: MBZ
	12:0	PostCSC Medium Offset This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	Reserved
		Access: RO
		Format: MBZ

PLANE_CSC_POSTOFF

PLANE_CSC_POSTOFF	
12:0	PostCSC Low Offset This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).



PLANE_CSC_PREOFF

PLANE_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70228h-70233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_A
Reset:	soft
Address:	70328h-70333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_A
Reset:	soft
Address:	70428h-70433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_A
Reset:	soft
Address:	71228h-71233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_B
Reset:	soft
Address:	71328h-71333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_B
Reset:	soft
Address:	71428h-71433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_B
Reset:	soft
Address:	72228h-72233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_C
Reset:	soft
Address:	72328h-72333h

PLANE_CSC_PREOFF		
Name:	Plane CSC Pre-offset	
ShortName:	PLANE_CSC_PREOFF_2_C	
Reset:	soft	
Address:	72428h-72433h	
Name:	Plane CSC Pre-offset	
ShortName:	PLANE_CSC_PREOFF_3_C	
Reset:	soft	
Address:	73228h-73233h	
Name:	Plane CSC Pre-offset	
ShortName:	PLANE_CSC_PREOFF_1_D	
Reset:	soft	
Address:	73328h-73333h	
Name:	Plane CSC Pre-offset	
ShortName:	PLANE_CSC_PREOFF_2_D	
Reset:	soft	
Address:	73428h-73433h	
Name:	Plane CSC Pre-offset	
ShortName:	PLANE_CSC_PREOFF_3_D	
Reset:	soft	
<p>The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane color space conversion (CSC). RGB modes: Red is in the High channel, Green in Medium, and Blue in Low. YUV modes: V is in the High channel, Y in Medium, and U in Low.</p>		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PreCSC High Offset This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
1	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PreCSC Medium Offset This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	

PLANE_CSC_PREOFF					
2	31:13	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
Format:	MBZ				
12:0	<p>PreCSC Low Offset</p> <p>This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>				

PLANE_CTL

PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70480h-70483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_A
Reset:	soft
Address:	70580h-70583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_A
Reset:	soft
Address:	70680h-70683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_A
Reset:	soft
Address:	70780h-70783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_A
Reset:	soft
Address:	71480h-71483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_B
Reset:	soft
Address:	71580h-71583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_B
Reset:	soft
Address:	71680h-71683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_B
Reset:	soft
Address:	71780h-71783h

PLANE_CTL	
Name:	Plane Control
ShortName:	PLANE_CTL_7_B
Reset:	soft
Address:	72480h-72483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_C
Reset:	soft
Address:	72580h-72583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_C
Reset:	soft
Address:	72680h-72683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_C
Reset:	soft
Address:	72780h-72783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_C
Reset:	soft
Address:	73480h-73483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_D
Reset:	soft
Address:	73580h-73583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_D
Reset:	soft
Address:	73680h-73683h
Name:	Plane Control
ShortName:	PLANE_CTL_6_D
Reset:	soft
Address:	73780h-73783h
Name:	Plane Control
ShortName:	PLANE_CTL_7_D
Reset:	soft
Address:	70180h-70183h

PLANE_CTL	
Name:	Plane Control
ShortName:	PLANE_CTL_1_A
Reset:	soft
Address:	70280h-70283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_A
Reset:	soft
Address:	70380h-70383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_A
Reset:	soft
Address:	71180h-71183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_B
Reset:	soft
Address:	71280h-71283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_B
Reset:	soft
Address:	71380h-71383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_B
Reset:	soft
Address:	72180h-72183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_C
Reset:	soft
Address:	72280h-72283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_C
Reset:	soft
Address:	72380h-72383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_C
Reset:	soft
Address:	73180h-73183h

PLANE_CTL			
Name:	Plane Control		
ShortName:	PLANE_CTL_1_D		
Reset:	soft		
Address:	73280h-73283h		
Name:	Plane Control		
ShortName:	PLANE_CTL_2_D		
Reset:	soft		
Address:	73380h-73383h		
Name:	Plane Control		
ShortName:	PLANE_CTL_3_D		
Reset:	soft		
The pipe scaler can be attached to a plane to scale the plane output before blending.			
Restriction			
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.			
DWord	Bit	Description	
0	31	Plane Enable When this bit is set, the plane will generate pixels for display. When cleared to zero, plane memory fetches cease and plane output is transparent.	
		Value	Name
		0b	Disable
		1b	Enable
	30:28	Pipe Slice Arbitration Slots This field specifies the number of slots allocated to this plane in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.	
	27:23	Source Pixel Format This field selects the source pixel format for the plane. Before entering the blender, each source format is converted to the pipe pixel format. The 8-bpp indexed format will always use the pipe palette. In planar YUV formats Y samples appear first in memory followed by interleaved UV samples. YUV 4:2:2 byte order is programmed separately. YUV 4:2:0 and YUV 4:4:4 byte order is not programmable. RGB color order is programmed separately for some formats. Refer to Universal Plane, Plane Pixel Formats section for color channel bit mappings. YUV 4:2:0 P010, P012 and P016 formats share the same 16 bpc memory layout but use 10, 12 and 16 bits per channel respectively. The color values are stored in the most significant bits. 64-bit formats supported only on the HDR planes. P01x output is only allowed from HDR planes.	

PLANE_CTL

		Value	Name	Description															
		00000b	YUV 422 Packed 8 bpc	YUV 4:2:2 packed, 8 bpc															
		00010b	YUV 420 Planar 8 bpc	YUV 4:2:0 Planar, 8 bpc - NV12															
		00100b	RGB 2101010	RGB 2:10:10:10, 32 bit.															
		00110b	YUV 420 Planar 10 bpc	YUV 4:2:0 Planar, 10 bpc - P010															
		01000b	RGB 8888	RGB 8:8:8:8, 32 bit															
		01010b	YUV 420 Planar 12 bpc	YUV 4:2:0 Planar 12 bpc - P012															
		01100b	RGB 16161616 Float	RGB 16:16:16:16 Floating Point, 64 bit (FP16)															
		01110b	YUV 420 Planar 16 bpc	YUV 4:2:0 Planar, 16 bpc - P016															
		10000b	YUV 444 Packed 8 bpc	YUV 4:4:4 packed (MSB-X:Y:U:V), 8bpc															
		10100b	RGB 2101010 XR_BIAS	RGB 2:10:10:10 Extended Range Bias (MSB-X:B:G:R), 32 bit															
		11000b	Indexed 8 bit	Indexed 8-bit															
		11100b	RGB 565	RGB 5:6:5 (MSB-R:G:B), 16 bit															
		00001b	YUV 422 Packed 10 bpc	YUV 4:2:2 packed, 10 bpc - Y210															
		00011b	YUV 422 Packed 12 bpc	YUV 4:2:2 packed, 12 bpc - Y212															
		00101b	YUV 422 Packed 16 bpc	YUV 4:2:2 packed, 16 bpc - Y216															
		00111b	YUV 444 Packed 10 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 10 bpc - Y410															
		01001b	YUV 444 Packed 12 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 12 bpc - Y412															
		01011b	YUV 444 Packed 16 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 16 bpc - Y416															
		Restriction																	
		Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS source pixel formats.																	
22:21	Key Enable	<p>This field enables color keying. The key color, range, channel enables, and mask are programmed in PLANE_KEYVAL, PLANE_KEYMSK, and PLANE_KEYMAX.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> <td>Disable keying for this plane.</td> </tr> <tr> <td>01b</td> <td>Source Key Enable</td> <td>This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.</td> </tr> <tr> <td>10b</td> <td>Destination Key Enable</td> <td>This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.</td> </tr> <tr> <td>11b</td> <td>Source Key Window</td> <td>This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as</td> </tr> </tbody> </table>			Value	Name	Description	00b	Disable	Disable keying for this plane.	01b	Source Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.	10b	Destination Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.	11b	Source Key Window	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as
Value	Name	Description																	
00b	Disable	Disable keying for this plane.																	
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11b	Source Key Window	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as																	

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		Enable	transparent only where the plane below is opaque.
Restriction			
<p>Plane color keying is not compatible with the Indexed 8-bit pixel format. Destination key/Source Key Window should be enabled only on one set (a pair) of planes, per pipe, at a time.</p> <p>Source key and Source Key Window must not be enabled on the bottom most active plane. Destination key must not be enabled on the top most active plane.</p>			
20	RGB Color Order This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10 and 16-bit BGRX 5:6:5. For other formats, this field is ignored.		
Value		Name	Description
0b		BGRX	BGRX (MSB-X:R:G:B)
1b		RGBX	RGBX (MSB-X:B:G:R)
19	Planar YUV420 component This field selects the planar YUV420 component for the plane when NV12/P0xx source pixel formats is used. This field must be set to '0b' for other (YUV non-planar/RGB) surface formats.		
Value	Name	Description	
0b	UV	Planes 1 to 5 can be configured as UV plane. Planes 6 and 7 must not be configured as a UV plane.	
1b	Y	Planes 6 and 7 can be configured as Y plane. Planes 1 to 5 must not be configured as a Y plane.	
18	Reserved		
Access:		RO	
Format:		MBZ	
17:16	YUV 422 Byte Order This field is used to select the byte order for YUV 4:2:2 8bpc data formats. For other formats, this field is ignored.		
Value		Name	Description
00b		YUYV	YUYV (MSB-V:Y2:U:Y1)
01b		UYVY	UYVY (MSB-Y2:V:Y1:U)
10b		YVYU	YVYU (MSB-U:Y2:V:Y1)
11b		VYUY	VYUY (MSB-Y2:U:Y1:V)
15	Render Decomp This bit enables the Display decompression of Render compressed surfaces.		
Value		Name	
0b		Disable	
1b		Enable	

PLANE_CTL

Restriction											
Color Clear is supported.											
Only the Left-right cache-line pair decompression is supported. The compressed surface should be Y (Legacy) or Y F Tiled. Decompression is not supported with 90/270 degree rotation.											
Decompression is supported with RGB8888, RGB1010102 and FP16 formats.											
Decompression is supported on all planes and pipes.											
14	Reserved										
Access:		RO									
Format:		MBZ									
13	Clear Color Disable										
Description											
This field disables the render decompression clear color mode. It is ignored when the Render Decomp field is disabled. The color value must be programmed in PLANE_CC_VAL before flipping to the surface that uses clear color value.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Disable</td> </tr> <tr> <td>0b</td> <td>Enable [Default]</td> </tr> </tbody> </table>			Value	Name	1b	Disable	0b	Enable [Default]			
Value	Name										
1b	Disable										
0b	Enable [Default]										
12:10	Tiled Surface										
This field indicates that the surface data is in tiled memory. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Linear memory</td> </tr> <tr> <td>001b</td> <td>Tile X memory</td> </tr> <tr> <td>100b</td> <td>Tile Y (Legacy) memory</td> </tr> </tbody> </table>			Value	Name	000b	Linear memory	001b	Tile X memory	100b	Tile Y (Legacy) memory	
Value	Name										
000b	Linear memory										
001b	Tile X memory										
100b	Tile Y (Legacy) memory										
Restriction											
Interlaced mode is not supported with Y Tiling. Tile Ys is not supported.											
9	Async Address Update Enable										
Access:		R/W									
This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change as soon as possible. This bit is not double buffered and the changes will apply immediately. When performing an asynchronous update, only the plane surface can be updated. Changes to stride, pixel, format, compression, FBC, etc. are not allowed.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Sync</td> <td>Surface Address MMIO writes will update synchronous to start of vertical blank</td> </tr> <tr> <td>1b</td> <td>Async</td> <td>Surface Address MMIO writes will update asynchronous to start of vertical blank</td> </tr> </tbody> </table>			Value	Name	Description	0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank	1b	Async	Surface Address MMIO writes will update asynchronous to start of vertical blank
Value	Name	Description									
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank									
1b	Async	Surface Address MMIO writes will update asynchronous to start of vertical blank									

PLANE_CTL

Restriction		
No command streamer (ring) flips to this plane are allowed when this bit is enabled. Command streamer flips will set a similar bit in the flip message that it sends to display.		
Asynchronous S3D flips are not allowed.		
Each async surface address write must be followed by a wait for flip done indication before writing the surface address register again.		
8	Horizontal Flip This field controls the horizontal flipping of the plane. When horizontal flipping is enabled with rotation, the horizontal flip operation is logically performed first followed by rotation. For further information refer to "Universal Plane" section.	
Value		Name
0b		Disable [Default]
1b		Enable
Restriction		
Horizontal flip is not supported with linear surface formats.		
7:6	Stereo Surface Vblank Mask This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.	
Value	Name	Description
00b	Mask None	Both the left and right eye vertical blanks will be used.
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.
5	Reserved	
4	Media Decomp <div style="text-align: center; background-color: #e1eef6; padding: 2px;">Description</div> This bit enables the Display decompression of Media compressed surfaces. 'Media Decomp' and 'Render Decomp' are mutually exclusive and must not be enabled at the same time for a given plane. Media decompression is supported with NV12, P0xx, YUV422, YUV444, RGB8888, RGB1010102 and FP16 formats.	

PLANE_CTL																
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable									
Value	Name															
0b	Disable															
1b	Enable															
3	<p>Allow Double Buffer Update Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field controls whether double buffer updates are allowed to be disabled for this plane. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled. This field applies only to the plane registers that supports double buffering. Scaler registers used for plane scaling purposes are not included in this.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Allowed</td> </tr> <tr> <td>1b</td> <td>Allowed [Default]</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Not Allowed	1b	Allowed [Default]							
Access:	R/W															
Value	Name															
0b	Not Allowed															
1b	Allowed [Default]															
2	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ											
Access:	RO															
Format:	MBZ															
1:0	<p>Plane Rotation</p> <p>This field controls hardware rotation of the plane.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No rotation</td> </tr> <tr> <td>01b</td> <td>90 degree rotation</td> </tr> <tr> <td>10b</td> <td>180 degree rotation</td> </tr> <tr> <td>11b</td> <td>270 degree rotation</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td>Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td>90/270 degree rotation requires the surface to be Y Tiled. Interlaced mode is not supported with 90/270 degree rotation. Render-Display decompression is not supported with 90/270 degree rotation.</td> </tr> <tr> <td>90/270 rotation is supported with plane width (pre-rotation) up to 4096 pixels.</td> </tr> </tbody> </table>	Value	Name	00b	No rotation	01b	90 degree rotation	10b	180 degree rotation	11b	270 degree rotation	Programming Notes	Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.	Restriction	90/270 degree rotation requires the surface to be Y Tiled. Interlaced mode is not supported with 90/270 degree rotation. Render-Display decompression is not supported with 90/270 degree rotation.	90/270 rotation is supported with plane width (pre-rotation) up to 4096 pixels.
Value	Name															
00b	No rotation															
01b	90 degree rotation															
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Programming Notes																
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90/270 rotation is supported with plane width (pre-rotation) up to 4096 pixels.																



PLANE_CUS_CTL

PLANE_CUS_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	701C8h-701CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_A
Reset:	soft
Address:	702C8h-702CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_A
Reset:	soft
Address:	703C8h-703CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_A
Reset:	soft
Address:	711C8h-711CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_B
Reset:	soft
Address:	712C8h-712CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_B
Reset:	soft
Address:	713C8h-713CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_B
Reset:	soft
Address:	721C8h-721CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_C
Reset:	soft
Address:	722C8h-722CBh

PLANE_CUS_CTL						
Name:	Plane Chroma Upsampler Control					
ShortName:	PLANE_CUS_CTL_2_C					
Reset:	soft					
Address:	723C8h-723CBh					
Name:	Plane Chroma Upsampler Control					
ShortName:	PLANE_CUS_CTL_3_C					
Reset:	soft					
Address:	731C8h-731CBh					
Name:	Plane Chroma Upsampler Control					
ShortName:	PLANE_CUS_CTL_1_D					
Reset:	soft					
Address:	732C8h-732CBh					
Name:	Plane Chroma Upsampler Control					
ShortName:	PLANE_CUS_CTL_2_D					
Reset:	soft					
Address:	733C8h-733CBh					
Name:	Plane Chroma Upsampler Control					
ShortName:	PLANE_CUS_CTL_3_D					
Reset:	soft					
Description						
<p>This register programs the chroma upsampler for processing pixel streams from hybrid planar YUV 420 (NV12, P0xx) surfaces.</p> <p>This dedicated chroma upsampling capability is available only in Planes 1 through 3. Planes 4 and 5 must use plane scaler (PS_CTRL) for chroma upsampling.</p> <p>The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios.</p>						
YUV 420 Chroma Siting	Horz Phase	Vert Phase	Programmed Horz Initial Phase	Programmed Horz Initial Phase Sign	Programmed Vert Initial Phase	Programmed Vert Initial Phase Sign
Top Left	0	0	0	0	0	0
Top	-0.25	0	0.25	1	0	0
Left (MPEG-2)	0	-0.25	0	0	0.25	1
Center (MPEG-1)	-0.25	-0.25	0.25	1	0.25	1
<p>Restriction :</p> <p>When the Chroma upsampler is enabled, then:</p> <ol style="list-style-type: none"> 1. The maximum horizontal plane size allowed is 4096 pixels 2. The minimum horizontal plane size allowed is 8 pixels 						

PLANE_CUS_CTL

3. The minimum vertical plane size allowed is 4 lines
4. The horizontal and vertical plane size should be even

DWord	Bit	Description						
0	31	<p>Chroma Upsampler Enable This field enables the plane chroma upsampler for handling hybrid planar YUV 420 (NV12, P0xx) formats.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	30	<p>Y Binding This field defines the Y plane from where the chroma upsampler will receive the Y pixels stream when processing hybrid planar YUV 420 (NV12, P0xx) formats.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Plane 6</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Plane 7</td> </tr> </tbody> </table>	Value	Name	0b	Plane 6	1b	Plane 7
	Value	Name						
	0b	Plane 6						
	1b	Plane 7						
	29:24	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
	Format:	MBZ						
	23	Reserved						
	22	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
Format:	MBZ							
21:20	Reserved							
19	<p>Horz Initial Phase Sign This field is defines the direction of the horizontal initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels to the right with respect to the Y pixels whereas a negative initial phase will have an effect of shifting left. The sign bit must be zero if the initial phase is zero.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Positive Initial Phase</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Negative Initial Phase</td> </tr> </tbody> </table>	Value	Name	0b	Positive Initial Phase	1b	Negative Initial Phase	
Value	Name							
0b	Positive Initial Phase							
1b	Negative Initial Phase							
18	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							
17:16	<p>Horz Initial Phase This field defines the horizontal initial phase adjustment required on the UV stream during</p>							

PLANE_CUS_CTL

		upsampling. This field should be programmed based on the YUV 420 chroma siting.	
		Value	Name
		00b	0
		01b	0.25
		10b	0.5
		11b	Reserved
15	Vert Initial Phase Sign	<p>This field is defines the direction of the vertical initial phase adjustment on the UV stream during upsampling.</p> <p>A positive initial phase will have an effect of shifting the UV pixels down with respect to the Y pixels whereas a negative initial phase will have an effect of shifting up.</p> <p>The sign bit must be zero if the initial phase is zero.</p>	
		Value	Name
		0b	Positive Initial Phase
		1b	Negative Initial Phase
14	Reserved		
	Access:	RO	
	Format:	MBZ	
13:12	Vert Initial Phase	<p>This field defines the vertical initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting.</p>	
		Value	Name
		00b	0
		01b	0.25
		10b	0.5
		11b	Reserved
11	Reserved		
10:9	Power Up Delay	<p>This field indicates the wait (in CD clocks) between powering up the line buffer arrays.</p>	
8	Reserved		
7:6	Reserved		
	Access:	RO	
	Format:	MBZ	
5	ECC Single Error		
	Access:	R/WC	
	<p>This field indicates that an single bit error encountered at the ECC logic. Hardware will correct the single bit errors. Hardware will set the bit; SW can clear with a write of 1.</p>		

PLANE_CUS_CTL					
	4	ECC Double Error <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>R/WC</td> </tr> </table> <p>This field indicates that a double bit error encountered at the ECC logic. Hardware will not correct the double bit errors. Hardware will set the bit; SW can clear with a write of 1.</p>	Access:	R/WC	
	Access:	R/WC			
	3:1	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:	RO				
Format:	MBZ				
0	Power Up In Progress <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> </table> <p>This field is set when the chroma upsampler line buffers are being powered up. Chroma upsampler cannot handle pixel traffic when this bit is set.</p>	Access:	RO		
Access:	RO				

PLANE_INPUT_CSC_COEFF

PLANE_INPUT_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701E0h-701F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_A
Reset:	soft
Address:	702E0h-702F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_A
Reset:	soft
Address:	703E0h-703F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_A
Reset:	soft
Address:	711E0h-711F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_B
Reset:	soft
Address:	712E0h-712F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_B
Reset:	soft
Address:	713E0h-713F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_B
Reset:	soft
Address:	721E0h-721F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_C
Reset:	soft

PLANE_INPUT_CSC_COEFF		
Address:	722E0h-722F7h	
Name:	Plane Input CSC Coefficients	
ShortName:	PLANE_INPUT_CSC_COEFF_2_C	
Reset:	soft	
Address:	723E0h-723F7h	
Name:	Plane Input CSC Coefficients	
ShortName:	PLANE_INPUT_CSC_COEFF_3_C	
Reset:	soft	
Address:	731E0h-731F7h	
Name:	Plane Input CSC Coefficients	
ShortName:	PLANE_INPUT_CSC_COEFF_1_D	
Reset:	soft	
Address:	732E0h-732F7h	
Name:	Plane Input CSC Coefficients	
ShortName:	PLANE_INPUT_CSC_COEFF_2_D	
Reset:	soft	
Address:	733E0h-733F7h	
Name:	Plane Input CSC Coefficients	
ShortName:	PLANE_INPUT_CSC_COEFF_3_D	
Reset:	soft	
DWord	Bit	Description
0	31:16	RY Format: CSC COEFFICIENT FORMAT
	15:0	GY Format: CSC COEFFICIENT FORMAT
1	31:16	BY Format: CSC COEFFICIENT FORMAT
	15:0	Reserved Access: RO Format: MBZ
2	31:16	RU Format: CSC COEFFICIENT FORMAT
	15:0	GU Format: CSC COEFFICIENT FORMAT
3	31:16	BU Format: CSC COEFFICIENT FORMAT

PLANE_INPUT_CSC_COEFF						
	15:0	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
4	31:16	RV <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>CSC COEFFICIENT FORMAT</td> </tr> </table>	Format:	CSC COEFFICIENT FORMAT		
	Format:	CSC COEFFICIENT FORMAT				
15:0	GV <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>CSC COEFFICIENT FORMAT</td> </tr> </table>	Format:	CSC COEFFICIENT FORMAT			
Format:	CSC COEFFICIENT FORMAT					
5	31:16	BV <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>CSC COEFFICIENT FORMAT</td> </tr> </table>	Format:	CSC COEFFICIENT FORMAT		
	Format:	CSC COEFFICIENT FORMAT				
15:0	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					



PLANE_INPUT_CSC_POSTOFF

PLANE_INPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70204h-7020Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_A
Reset:	soft
Address:	70304h-7030Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_A
Reset:	soft
Address:	70404h-7040Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_A
Reset:	soft
Address:	71204h-7120Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_B
Reset:	soft
Address:	71304h-7130Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_B
Reset:	soft
Address:	71404h-7140Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_B
Reset:	soft
Address:	72204h-7220Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_C
Reset:	soft
Address:	72304h-7230Fh

PLANE_INPUT_CSC_POSTOFF		
Name:	Plane Input CSC Post-offset	
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_C	
Reset:	soft	
Address:	72404h-7240Fh	
Name:	Plane Input CSC Post-offset	
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_C	
Reset:	soft	
Address:	73204h-7320Fh	
Name:	Plane Input CSC Post-offset	
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_D	
Reset:	soft	
Address:	73304h-7330Fh	
Name:	Plane Input CSC Post-offset	
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_D	
Reset:	soft	
Address:	73404h-7340Fh	
Name:	Plane Input CSC Post-offset	
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_D	
Reset:	soft	
<p>The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane input color space conversion (CSC).</p>		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PostCSC High Offset This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
1	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PostCSC Medium Offset This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
2	31:13	Reserved
		Access: RO
		Format: MBZ

PLANE_INPUT_CSC_POSTOFF

	12:0	<p>PostCSC Low Offset</p> <p>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</p>
--	------	---

PLANE_INPUT_CSC_PREOFF

PLANE_INPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701F8h-70203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_A
Reset:	soft
Address:	702F8h-70303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_A
Reset:	soft
Address:	703F8h-70403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_A
Reset:	soft
Address:	711F8h-71203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_B
Reset:	soft
Address:	712F8h-71303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_B
Reset:	soft
Address:	713F8h-71403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_B
Reset:	soft
Address:	721F8h-72203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_C
Reset:	soft
Address:	722F8h-72303h

PLANE_INPUT_CSC_PREOFF		
Name:	Plane Input CSC Pre-offset	
ShortName:	PLANE_INPUT_CSC_PREOFF_2_C	
Reset:	soft	
Address:	723F8h-72403h	
Name:	Plane Input CSC Pre-offset	
ShortName:	PLANE_INPUT_CSC_PREOFF_3_C	
Reset:	soft	
Address:	731F8h-73203h	
Name:	Plane Input CSC Pre-offset	
ShortName:	PLANE_INPUT_CSC_PREOFF_1_D	
Reset:	soft	
Address:	732F8h-73303h	
Name:	Plane Input CSC Pre-offset	
ShortName:	PLANE_INPUT_CSC_PREOFF_2_D	
Reset:	soft	
Address:	733F8h-73403h	
Name:	Plane Input CSC Pre-offset	
ShortName:	PLANE_INPUT_CSC_PREOFF_3_D	
Reset:	soft	
<p>The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane input color space conversion (CSC).</p>		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PreCSC High Offset This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
1	31:13	Reserved
		Access: RO
		Format: MBZ
12:0	PreCSC Medium Offset This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).	
2	31:13	Reserved
		Access: RO
		Format: MBZ

PLANE_INPUT_CSC_PREOFF

PLANE_INPUT_CSC_PREOFF		
	12:0	PreCSC Low Offset This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).



PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A0h-704A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_A
Reset:	soft
Address:	705A0h-705A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_A
Reset:	soft
Address:	706A0h-706A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_A
Reset:	soft
Address:	707A0h-707A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_A
Reset:	soft
Address:	714A0h-714A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_B
Reset:	soft
Address:	715A0h-715A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_B
Reset:	soft
Address:	716A0h-716A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_B
Reset:	soft
Address:	717A0h-717A3h

PLANE_KEYMAX	
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_B
Reset:	soft
Address:	724A0h-724A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_C
Reset:	soft
Address:	725A0h-725A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_C
Reset:	soft
Address:	726A0h-726A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_C
Reset:	soft
Address:	727A0h-727A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_C
Reset:	soft
Address:	734A0h-734A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_D
Reset:	soft
Address:	735A0h-735A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_D
Reset:	soft
Address:	736A0h-736A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_6_D
Reset:	soft
Address:	737A0h-737A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_7_D
Reset:	soft
Address:	701A0h-701A3h



PLANE_KEYMAX

Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_1_A
Reset: soft

Address: 702A0h-702A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_2_A
Reset: soft

Address: 703A0h-703A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_3_A
Reset: soft

Address: 711A0h-711A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_1_B
Reset: soft

Address: 712A0h-712A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_2_B
Reset: soft

Address: 713A0h-713A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_3_B
Reset: soft

Address: 721A0h-721A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_1_C
Reset: soft

Address: 722A0h-722A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_2_C
Reset: soft

Address: 723A0h-723A3h
Name: Plane Key Color Max
ShortName: PLANE_KEYMAX_3_C
Reset: soft

Address: 731A0h-731A3h

PLANE_KEYMAX

Name: Plane Key Color Max
 ShortName: PLANE_KEYMAX_1_D
 Reset: soft

Address: 732A0h-732A3h
 Name: Plane Key Color Max
 ShortName: PLANE_KEYMAX_2_D
 Reset: soft

Address: 733A0h-733A3h
 Name: Plane Key Color Max
 ShortName: PLANE_KEYMAX_3_D
 Reset: soft

When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register is not used.

DWord	Bit	Description
0	31:24	Plane Alpha Value Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	V Key Max Value Specifies the maximum key value for the V channel.
	15:8	Y Key Max Value Specifies the maximum key value for the Y channel.
	7:0	U Key Max Value Specifies the maximum key value for the U channel.



PLANE_KEYMSK

PLANE_KEYMSK	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70498h-7049Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_A
Reset:	soft
Address:	70598h-7059Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_A
Reset:	soft
Address:	70698h-7069Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_A
Reset:	soft
Address:	70798h-7079Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_A
Reset:	soft
Address:	71498h-7149Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_B
Reset:	soft
Address:	71598h-7159Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_B
Reset:	soft
Address:	71698h-7169Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_B
Reset:	soft
Address:	71798h-7179Bh

PLANE_KEYMSK	
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_B
Reset:	soft
Address:	72498h-7249Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_C
Reset:	soft
Address:	72598h-7259Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_C
Reset:	soft
Address:	72698h-7269Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_C
Reset:	soft
Address:	72798h-7279Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_C
Reset:	soft
Address:	73498h-7349Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_D
Reset:	soft
Address:	73598h-7359Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_D
Reset:	soft
Address:	73698h-7369Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_6_D
Reset:	soft
Address:	73798h-7379Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_7_D
Reset:	soft
Address:	70198h-7019Bh

PLANE_KEYMSK	
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_A
Reset:	soft
Address:	70298h-7029Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_A
Reset:	soft
Address:	70398h-7039Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_A
Reset:	soft
Address:	71198h-7119Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_B
Reset:	soft
Address:	71298h-7129Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_B
Reset:	soft
Address:	71398h-7139Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_B
Reset:	soft
Address:	72198h-7219Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_C
Reset:	soft
Address:	72298h-7229Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_C
Reset:	soft
Address:	72398h-7239Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_C
Reset:	soft
Address:	73198h-7319Bh

PLANE_KEYMSK								
Name:	Plane Key Mask							
ShortName:	PLANE_KEYMSK_1_D							
Reset:	soft							
Address:	73298h-7329Bh							
Name:	Plane Key Mask							
ShortName:	PLANE_KEYMSK_2_D							
Reset:	soft							
Address:	73398h-7339Bh							
Name:	Plane Key Mask							
ShortName:	PLANE_KEYMSK_3_D							
Reset:	soft							
DWord	Bit	Description						
0	31	<p>Plane Alpha Enable Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_COLOR_CTL register.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	30:27	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
	Format:	MBZ						
	26	<p>V or R Key Channel Enable Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	25	<p>Y or G Key Channel Enable Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
24	<p>U or B Key Channel Enable Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> </tbody> </table>	Value	Name	0b	Disable			
Value	Name							
0b	Disable							

PLANE_KEYMSK			
	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">1b</td> <td style="width: 50%;">Enable</td> </tr> </table>	1b	Enable
1b	Enable		
23:16	<p>R Key Mask Value Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.</p>		
15:8	<p>G Key Mask Value Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.</p>		
7:0	<p>B Key Mask Value Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.</p>		

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70494h-70497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_A
Reset:	soft
Address:	70594h-70597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_A
Reset:	soft
Address:	70694h-70697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_A
Reset:	soft
Address:	70794h-70797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_A
Reset:	soft
Address:	71494h-71497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_B
Reset:	soft
Address:	71594h-71597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_B
Reset:	soft
Address:	71694h-71697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_B
Reset:	soft
Address:	71794h-71797h

PLANE_KEYVAL	
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_B
Reset:	soft
Address:	72494h-72497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_C
Reset:	soft
Address:	72594h-72597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_C
Reset:	soft
Address:	72694h-72697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_C
Reset:	soft
Address:	72794h-72797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_C
Reset:	soft
Address:	73494h-73497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_D
Reset:	soft
Address:	73594h-73597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_D
Reset:	soft
Address:	73694h-73697h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_6_D
Reset:	soft
Address:	73794h-73797h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_7_D
Reset:	soft
Address:	70194h-70197h

PLANE_KEYVAL	
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_A
Reset:	soft
Address:	70294h-70297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_A
Reset:	soft
Address:	70394h-70397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_A
Reset:	soft
Address:	71194h-71197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_B
Reset:	soft
Address:	71294h-71297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_B
Reset:	soft
Address:	71394h-71397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_B
Reset:	soft
Address:	72194h-72197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_C
Reset:	soft
Address:	72294h-72297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_C
Reset:	soft
Address:	72394h-72397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_C
Reset:	soft
Address:	73194h-73197h

PLANE_KEYVAL		
Name:	Plane Key Color	
ShortName:	PLANE_KEYVAL_1_D	
Reset:	soft	
Address:	73294h-73297h	
Name:	Plane Key Color	
ShortName:	PLANE_KEYVAL_2_D	
Reset:	soft	
Address:	73394h-73397h	
Name:	Plane Key Color	
ShortName:	PLANE_KEYVAL_3_D	
Reset:	soft	
<p>When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.</p>		
<p>Restriction : Keying is not supported in HDR mode.</p>		
DWord	Bit	Description
0	31:24	Reserved
		Access: RO
		Format: MBZ
	23:16	V Min or R Key Value Specifies the minimum key value for the V channel or the compare value for Red channel.
15:8	Y Min or G Key Value Specifies the minimum key value for the Y channel or the compare value for Green channel.	
7:0	U Min or B Key Value Specifies the minimum key value for the U channel or the compare value for Blue channel.	

PLANE_LEFT_SURF

PLANE_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Address:	704B0h-704B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_A
Reset:	soft
Address:	705B0h-705B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_A
Reset:	soft
Address:	706B0h-706B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_A
Reset:	soft
Address:	707B0h-707B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_A
Reset:	soft
Address:	714B0h-714B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_B
Reset:	soft
Address:	715B0h-715B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_B
Reset:	soft
Address:	716B0h-716B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_B
Reset:	soft

PLANE_LEFT_SURF	
Address:	717B0h-717B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_B
Reset:	soft
Address:	724B0h-724B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_C
Reset:	soft
Address:	725B0h-725B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_C
Reset:	soft
Address:	726B0h-726B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_C
Reset:	soft
Address:	727B0h-727B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_C
Reset:	soft
Address:	734B0h-734B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_D
Reset:	soft
Address:	735B0h-735B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_D
Reset:	soft
Address:	736B0h-736B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_6_D
Reset:	soft
Address:	737B0h-737B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_7_D
Reset:	soft

PLANE_LEFT_SURF	
Address:	701B0h-701B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_A
Reset:	soft
Address:	702B0h-702B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_A
Reset:	soft
Address:	703B0h-703B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_A
Reset:	soft
Address:	711B0h-711B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_B
Reset:	soft
Address:	712B0h-712B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_B
Reset:	soft
Address:	713B0h-713B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_B
Reset:	soft
Address:	721B0h-721B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_C
Reset:	soft
Address:	722B0h-722B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_C
Reset:	soft
Address:	723B0h-723B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_C
Reset:	soft

PLANE_LEFT_SURF		
Address:	731B0h-731B3h	
Name:	Plane Left Surface Base Address	
ShortName:	PLANE_LEFT_SURF_1_D	
Reset:	soft	
Address:	732B0h-732B3h	
Name:	Plane Left Surface Base Address	
ShortName:	PLANE_LEFT_SURF_2_D	
Reset:	soft	
Address:	733B0h-733B3h	
Name:	Plane Left Surface Base Address	
ShortName:	PLANE_LEFT_SURF_3_D	
Reset:	soft	
Restriction		
This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.		
DWord	Bit	Description
0	31:12	Left Surface Base Address
		Format: GraphicsAddress[31:12]
		This address specifies the stereo 3D left eye surface base address bits 31:12.
		Restriction
This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.		
11:0		Reserved
		Access: RO
		Format: MBZ

PLANE_OFFSET

PLANE_OFFSET	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A4h-704A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_A
Reset:	soft
Address:	705A4h-705A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_A
Reset:	soft
Address:	706A4h-706A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_A
Reset:	soft
Address:	707A4h-707A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_A
Reset:	soft
Address:	714A4h-714A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_B
Reset:	soft
Address:	715A4h-715A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_B
Reset:	soft
Address:	716A4h-716A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_B
Reset:	soft
Address:	717A4h-717A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_B
Reset:	soft
Address:	724A4h-724A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_C
Reset:	soft
Address:	725A4h-725A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_C
Reset:	soft
Address:	726A4h-726A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_C
Reset:	soft
Address:	727A4h-727A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_C
Reset:	soft
Address:	734A4h-734A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_D
Reset:	soft
Address:	735A4h-735A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_D
Reset:	soft
Address:	736A4h-736A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_6_D
Reset:	soft
Address:	737A4h-737A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_7_D
Reset:	soft
Address:	701A4h-701A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_A
Reset:	soft
Address:	702A4h-702A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_A
Reset:	soft
Address:	703A4h-703A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_A
Reset:	soft
Address:	711A4h-711A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_B
Reset:	soft
Address:	712A4h-712A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_B
Reset:	soft
Address:	713A4h-713A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_B
Reset:	soft
Address:	721A4h-721A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_C
Reset:	soft
Address:	722A4h-722A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_C
Reset:	soft
Address:	723A4h-723A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_C
Reset:	soft
Address:	731A4h-731A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_D
Reset:	soft
Address:	732A4h-732A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_D
Reset:	soft
Address:	733A4h-733A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_D
Reset:	soft
Address:	7089Ch-7089Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_A
Reset:	soft
Address:	708BCh-708BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_A
Reset:	soft
Address:	708DCh-708DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_A
Reset:	soft
Address:	708FCh-708FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_A
Reset:	soft
Address:	7092Ch-7092Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_A
Reset:	soft
Address:	7094Ch-7094Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_6_A
Reset:	soft
Address:	7096Ch-7096Fh

PLANE_OFFSET

Name: Selective Fetch Plane Offset
 ShortName: SEL_FETCH_PLANE_OFFSET_7_A
 Reset: soft

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image.

Restriction

Plane Size + Plane Offset should not exceed the surface <stride/width> (in pixels)
 X and Y offset restrictions are specified in the following table. For formats not specified in the table, both odd and even offsets are supported.

PixelFormat	Rotate	Start X Position	Start Y Position
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even

DWord	Bit	Description
0	31:29	Reserved
		Access: RO
	Format: MBZ	
	28:16	Start Y Position The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface.
15:13	Reserved	
	Access: RO	
Format: MBZ		
12:0	Start X Position The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface.	



PLANE_PIXEL_NORMALIZE

PLANE_PIXEL_NORMALIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701A8h-701ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_A
Reset:	soft
Address:	702A8h-702ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_A
Reset:	soft
Address:	703A8h-703ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_A
Reset:	soft
Address:	711A8h-711ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_B
Reset:	soft
Address:	712A8h-712ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_B
Reset:	soft
Address:	713A8h-713ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_B
Reset:	soft
Address:	721A8h-721ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_C
Reset:	soft
Address:	722A8h-722ABh

PLANE_PIXEL_NORMALIZE				
Name:	Plane Pixel Normalize			
ShortName:	PLANE_PIXEL_NORMALIZE_2_C			
Reset:	soft			
Address:	723A8h-723ABh			
Name:	Plane Pixel Normalize			
ShortName:	PLANE_PIXEL_NORMALIZE_3_C			
Reset:	soft			
Address:	731A8h-731ABh			
Name:	Plane Pixel Normalize			
ShortName:	PLANE_PIXEL_NORMALIZE_1_D			
Reset:	soft			
Address:	732A8h-732ABh			
Name:	Plane Pixel Normalize			
ShortName:	PLANE_PIXEL_NORMALIZE_2_D			
Reset:	soft			
Address:	733A8h-733ABh			
Name:	Plane Pixel Normalize			
ShortName:	PLANE_PIXEL_NORMALIZE_3_D			
Reset:	soft			
DWord	Bit	Description		
0	31	Enable This field enables the normalization of FP16 pixels with the specified normalization factor.		
	30:16	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
15:0	Normalization Factor			
		Description		
		This field specifies the normalization factor in the FP16 format.		
		This programmed value is multiplied with the input pixel value and normalized to range -4.0 to 4.0, exclusive. Out of bound values get clamped to be within the range from -4.0 to 4.0, exclusive. The programmed half float value must be a positive and not de-normalized, zero or NAN.		

PLANE_POS

PLANE_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	7048Ch-7048Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_A
Reset:	soft
Address:	7058Ch-7058Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_A
Reset:	soft
Address:	7068Ch-7068Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_A
Reset:	soft
Address:	7078Ch-7078Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_A
Reset:	soft
Address:	7148Ch-7148Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_B
Reset:	soft
Address:	7158Ch-7158Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_B
Reset:	soft
Address:	7168Ch-7168Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_B
Reset:	soft
Address:	7178Ch-7178Fh

PLANE_POS	
Name:	Plane Position
ShortName:	PLANE_POS_7_B
Reset:	soft
Address:	7248Ch-7248Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_C
Reset:	soft
Address:	7258Ch-7258Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_C
Reset:	soft
Address:	7268Ch-7268Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_C
Reset:	soft
Address:	7278Ch-7278Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_C
Reset:	soft
Address:	7348Ch-7348Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_D
Reset:	soft
Address:	7358Ch-7358Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_D
Reset:	soft
Address:	7368Ch-7368Fh
Name:	Plane Position
ShortName:	PLANE_POS_6_D
Reset:	soft
Address:	7378Ch-7378Fh
Name:	Plane Position
ShortName:	PLANE_POS_7_D
Reset:	soft
Address:	7018Ch-7018Fh

PLANE_POS	
Name:	Plane Position
ShortName:	PLANE_POS_1_A
Reset:	soft
Address:	7028Ch-7028Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_A
Reset:	soft
Address:	7038Ch-7038Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_A
Reset:	soft
Address:	7118Ch-7118Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_B
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_B
Reset:	soft
Address:	7138Ch-7138Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_B
Reset:	soft
Address:	7218Ch-7218Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_C
Reset:	soft
Address:	7228Ch-7228Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_C
Reset:	soft
Address:	7238Ch-7238Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_C
Reset:	soft
Address:	7318Ch-7318Fh

PLANE_POS	
Name:	Plane Position
ShortName:	PLANE_POS_1_D
Reset:	soft
Address:	7328Ch-7328Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_D
Reset:	soft
Address:	7338Ch-7338Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_D
Reset:	soft
Address:	70894h-70897h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_A
Reset:	soft
Address:	708B4h-708B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_A
Reset:	soft
Address:	708D4h-708D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_A
Reset:	soft
Address:	708F4h-708F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_A
Reset:	soft
Address:	70924h-70927h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_A
Reset:	soft
Address:	70944h-70947h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_6_A
Reset:	soft
Address:	70964h-70967h

PLANE_POS

Name: Selective Fetch Plane Position
 ShortName: SEL_FETCH_PLANE_POS_7_A
 Reset: soft

This register specifies the screen position of the plane. The origin of the plane position is always the upper left corner of the display pipe source image area. When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe. When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size \geq plane position + plane size. When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:29	Reserved
		Access: RO
		Format: MBZ
	28:16	Y Position This specifies the vertical position of the plane upper left corner in lines.
	15:13	Reserved
		Access: RO
		Format: MBZ
	12:0	X Position This specifies the horizontal position of the plane upper left corner in pixels.

PLANE_POST_CSC_GAMC_DATA

PLANE_POST_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704DCh-704DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705DCh-705DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	706DCh-706DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_A
Reset:	soft
Address:	707DCh-707DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_A
Reset:	soft
Address:	714DCh-714DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715DCh-715DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	716DCh-716DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_B
Reset:	soft
Address:	717DCh-717DFh

PLANE_POST_CSC_GAMC_DATA	
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_B
Reset:	soft
Address:	724DCh-724DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725DCh-725DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_C
Reset:	soft
Address:	726DCh-726DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_C
Reset:	soft
Address:	727DCh-727DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_C
Reset:	soft
Address:	734DCh-734DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_D
Reset:	soft
Address:	735DCh-735DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_D
Reset:	soft
Address:	736DCh-736DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_6_D
Reset:	soft
Address:	737DCh-737DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_7_D
Reset:	soft
PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values	

PLANE_POST_CSC_GAMC_DATA

that determine the characteristics of the gamma correction for the plane pixel data after plane Color Space Conversion.

The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.

For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.

For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.

For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.

For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.

Plane Post-CSC Gamma correction gets enabled or disabled based on the 'Plane Gamma Disable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing in Direct mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:19	Reserved	
		Access:	RO
	Format:	MBZ	
	18:0	Gamma Value	
Default Value:		00000000000000000000b	
Format:		U3.16	



PLANE_POST_CSC_GAMC_DATA_ENH

PLANE_POST_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701DCh-701DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702DCh-702DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703DCh-703DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711DCh-711DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712DCh-712DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713DCh-713DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721DCh-721DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_C
Reset:	soft
Address:	722DCh-722DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_C

PLANE_POST_CSC_GAMC_DATA_ENH	
Reset:	soft
Address:	723DCh-723DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_C
Reset:	soft
Address:	731DCh-731DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_D
Reset:	soft
Address:	732DCh-732DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_D
Reset:	soft
Address:	733DCh-733DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_D
Reset:	soft
<p>PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed. The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.</p> <p>For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 33rd, 34th and 35th entries are stored as 27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.</p> <p>For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.</p> <p>For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.</p> <p>For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.</p> <p>Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the plane control register. The same set of values is used for gamma correction of the red, blue and green channels. See Pipe Gamma for an example gamma curve diagram.</p> <p>To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the</p>	

PLANE_POST_CSC_GAMC_DATA_ENH

34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

For HDR tone mapping usages, only the first 33 entries get used. The entries are used either in an unsigned 0.24 format or unsigned 8.16 format based on PLANE_COLOR_CTL->Plane Gamma Multiplier Precision programming.

Restriction

The gamma curve must be flat or increasing, never decreasing when used in the direct lookup mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:27	Reserved	
		Access:	RO
	Format:	MBZ	
	26:0	Gamma Value	
Default Value:		0000000000000000000000000000b	
Format:		U3.24	

PLANE_POST_CSC_GAMC_INDEX

PLANE_POST_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D8h-704DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_A
Reset:	soft
Address:	705D8h-705DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_A
Reset:	soft
Address:	706D8h-706DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_6_A
Reset:	soft
Address:	707D8h-707DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_7_A
Reset:	soft
Address:	714D8h-714DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_B
Reset:	soft
Address:	715D8h-715DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_B
Reset:	soft
Address:	716D8h-716DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_6_B
Reset:	soft
Address:	717D8h-717DBh



PLANE_POST_CSC_GAMC_INDEX		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_7_B		
Reset: soft		
Address: 724D8h-724DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_4_C		
Reset: soft		
Address: 725D8h-725DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_5_C		
Reset: soft		
Address: 726D8h-726DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_6_C		
Reset: soft		
Address: 727D8h-727DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_7_C		
Reset: soft		
Address: 734D8h-734DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_4_D		
Reset: soft		
Address: 735D8h-735DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_5_D		
Reset: soft		
Address: 736D8h-736DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_6_D		
Reset: soft		
Address: 737D8h-737DBh		
Name: Plane Post CSC Gamma Index		
ShortName: PLANE_POST_CSC_GAMC_INDEX_7_D		
Reset: soft		
DWord	Bit	Description

PLANE_POST_CSC_GAMC_INDEX			
0	31:11	Reserved	
		Access: RO	
		Format: MBZ	
	10	Index Auto Increment	
		This field enables the index auto increment.	
		Value	Name
		Description	
		0b	No Increment Do not automatically increment the index value.
		1b	Auto Increment Increment the index value with each read or write to the data register. [Default]
	9:6	Reserved	
Access: RO			
Format: MBZ			
5:0	Index Value		
	Access: Write/Read Status		
	This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.		
	When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.		
	While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.		
	Value	Name	
	[0,34]		



PLANE_POST_CSC_GAMC_INDEX_ENH

PLANE_POST_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701D8h-701DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D8h-702DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D8h-703DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D8h-711DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D8h-712DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D8h-713DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D8h-721DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft
Address:	722D8h-722DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_C

PLANE_POST_CSC_GAMC_INDEX_ENH				
Reset:	soft			
Address:	723D8h-723DBh			
Name:	Plane Post CSC Gamma Index			
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_C			
Reset:	soft			
Address:	731D8h-731DBh			
Name:	Plane Post CSC Gamma Index			
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_D			
Reset:	soft			
Address:	732D8h-732DBh			
Name:	Plane Post CSC Gamma Index			
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_D			
Reset:	soft			
Address:	733D8h-733DBh			
Name:	Plane Post CSC Gamma Index			
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_D			
Reset:	soft			
DWord	Bit	Description		
0	31:11	Reserved		
		Access:	RO	
		Format:	MBZ	
	10	Index Auto Increment		
		This field enables the index auto increment.		
		Value	Name	Description
		0b	No Increment	Do not automatically increment the index value.
	1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.	
	9:6	Reserved		
		Access:	RO	
Format:		MBZ		
5:0	Index Value			
	Access:	Write/Read Status		
<p>This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.</p> <p>When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.</p> <p>While in auto increment mode, after performing reads or writes to only part of the range, the</p>				

PLANE_POST_CSC_GAMC_INDEX_ENH	
	auto increment bit must be cleared before resetting the index value.
Value	Name
[0,34]	

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70164h-70167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_A
Reset:	soft
Address:	70264h-70267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_A
Reset:	soft
Address:	70364h-70367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_A
Reset:	soft
Address:	71164h-71167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_B
Reset:	soft
Address:	71264h-71267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_B
Reset:	soft
Address:	71364h-71367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_B
Reset:	soft
Address:	72164h-72167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_C
Reset:	soft
Address:	72264h-72267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_C

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

Reset:	soft
Address:	72364h-72367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_C
Reset:	soft
Address:	73164h-73167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_D
Reset:	soft
Address:	73264h-73267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_D
Reset:	soft
Address:	73364h-73367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_D
Reset:	soft

PLANE_POST_CSC_GAMC_SEG0_INDEX and PLANE_POST_CSC_GAMC_SEG0_DATA registers are used to program the segment 0 values of the HDR tone mapping curve. The entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional.

DWord	Bit	Description			
0	31:24	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
23:0	Gamma Value				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 40%;">Default Value:</td> <td>000000000000000000000000b</td> </tr> <tr> <td>Format:</td> <td>U0.24</td> </tr> </table>	Default Value:	000000000000000000000000b	Format:	U0.24
Default Value:	000000000000000000000000b				
Format:	U0.24				

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70160h-70163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_A
Reset:	soft
Address:	70260h-70263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_A
Reset:	soft
Address:	70360h-70363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_A
Reset:	soft
Address:	71160h-71163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_B
Reset:	soft
Address:	71260h-71263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_B
Reset:	soft
Address:	71360h-71363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_B
Reset:	soft
Address:	72160h-72163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_C
Reset:	soft
Address:	72260h-72263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_C

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH				
Reset:	soft			
Address:	72360h-72363h			
Name:	Plane Post CSC Gamma Segment0 Index			
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_C			
Reset:	soft			
Address:	73160h-73163h			
Name:	Plane Post CSC Gamma Segment0 Index			
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_D			
Reset:	soft			
Address:	73260h-73263h			
Name:	Plane Post CSC Gamma Segment0 Index			
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_D			
Reset:	soft			
Address:	73360h-73363h			
Name:	Plane Post CSC Gamma Segment0 Index			
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_D			
Reset:	soft			
DWord	Bit	Description		
0	31:11	Reserved		
		Access:	RO	
		Format:	MBZ	
	10	Index Auto Increment		
		This field enables the index auto increment.		
		Value	Name	Description
		0b	No Increment	Do not automatically increment the index value.
	1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.	
	9:4	Reserved		
		Access:	RO	
Format:		MBZ		
3:0	Index Value			
	Access:	Write/Read Status		
	<p>This index controls access to the segment 0 of plane post color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.</p> <p>When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range.</p> <p>While in auto increment mode, after performing reads or writes to only part of the range, the</p>			

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH		
		auto increment bit must be cleared before resetting the index value.
	Value	Name
	[0,8]	



PLANE_PRE_CSC_GAMC_DATA

PLANE_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D4h-704D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705D4h-705D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	706D4h-706D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_A
Reset:	soft
Address:	707D4h-707D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_A
Reset:	soft
Address:	714D4h-714D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715D4h-715D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	716D4h-716D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_B
Reset:	soft
Address:	717D4h-717D7h

PLANE_PRE_CSC_GAMC_DATA	
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_B
Reset:	soft
Address:	724D4h-724D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725D4h-725D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_C
Reset:	soft
Address:	726D4h-726D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_C
Reset:	soft
Address:	727D4h-727D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_C
Reset:	soft
Address:	734D4h-734D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_D
Reset:	soft
Address:	735D4h-735D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_D
Reset:	soft
Address:	736D4h-736D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_6_D
Reset:	soft
Address:	737D4h-737D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_7_D
Reset:	soft
PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that	

PLANE_PRE_CSC_GAMC_DATA

determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.

The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.

For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.

For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.

For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.

For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.

Plane Pre-CSC Gamma correction gets enabled or disabled based on the 'Plane Pre CSC Gamma Enable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:19	Reserved	
		Access:	RO
		Format:	MBZ
	18:0	Gamma Value	
Default Value:		000000000000000000b	
Format:		U3.16	

PLANE_PRE_CSC_GAMC_DATA_ENH

PLANE_PRE_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D4h-701D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702D4h-702D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703D4h-703D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711D4h-711D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712D4h-712D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713D4h-713D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721D4h-721D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_C
Reset:	soft
Address:	722D4h-722D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_C

PLANE_PRE_CSC_GAMC_DATA_ENH	
Reset:	soft
Address:	723D4h-723D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_C
Reset:	soft
Address:	731D4h-731D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_D
Reset:	soft
Address:	732D4h-732D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_D
Reset:	soft
Address:	733D4h-733D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_D
Reset:	soft
<p>PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.</p> <p>The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.</p> <p>For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 129 gamma entries to create the result value. The first 128 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 129th, 130th and 131th entries are stored as 27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.</p> <p>For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 129th and 130th gamma entries to create the result value.</p> <p>For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 130th and 131st gamma entries to create the result value.</p> <p>For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.</p> <p>Pre-CSC Gamma correction gets enabled or disabled based on the "Plane Pre CSC Gamma Enable" bit in the plane color control register. The same set of values is used for gamma correction of the red, blue and green channels.</p> <p>See Pipe Gamma for an example gamma curve diagram.</p>	
Programming Notes	

PLANE_PRE_CSC_GAMC_DATA_ENH

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 129th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 130th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:27	Reserved	
		Access:	RO
	Format:	MBZ	
	26:0	Gamma Value	
Default Value:		0000000000000000000000000000b	
Format:		U3.24	



PLANE_PRE_CSC_GAMC_INDEX

PLANE_PRE_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D0h-704D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_A
Reset:	soft
Address:	705D0h-705D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_A
Reset:	soft
Address:	706D0h-706D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_A
Reset:	soft
Address:	707D0h-707D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_A
Reset:	soft
Address:	714D0h-714D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_B
Reset:	soft
Address:	715D0h-715D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_B
Reset:	soft
Address:	716D0h-716D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_B
Reset:	soft
Address:	717D0h-717D3h

PLANE_PRE_CSC_GAMC_INDEX		
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_B	
Reset:	soft	
Address:	724D0h-724D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_C	
Reset:	soft	
Address:	725D0h-725D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_C	
Reset:	soft	
Address:	726D0h-726D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_C	
Reset:	soft	
Address:	727D0h-727D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_C	
Reset:	soft	
Address:	734D0h-734D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_D	
Reset:	soft	
Address:	735D0h-735D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_D	
Reset:	soft	
Address:	736D0h-736D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_6_D	
Reset:	soft	
Address:	737D0h-737D3h	
Name:	Plane Pre CSC Gamma Index	
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_7_D	
Reset:	soft	
DWord	Bit	Description

PLANE_PRE_CSC_GAMC_INDEX										
0	31:11	Reserved								
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
	Access:	RO								
	Format:	MBZ								
	10	Index Auto Increment								
		This field enables the index auto increment.								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 60%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No Increment</td> <td>Do not automatically increment the index value.</td> </tr> <tr> <td>1b</td> <td>Auto Increment [Default]</td> <td>Increment the index value with each read or write to the data register.</td> </tr> </tbody> </table>	Value	Name	Description	0b	No Increment	Do not automatically increment the index value.	1b	Auto Increment [Default]
	Value	Name	Description							
	0b	No Increment	Do not automatically increment the index value.							
	1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.							
9:6	Reserved									
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
Access:	RO									
Format:	MBZ									
5:0	Index Value									
	Access:	Write/Read Status								
	<p>This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.</p> <p>When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.</p> <p>While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.</p>									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>[0,34]</td> <td></td> </tr> </tbody> </table>	Value	Name	[0,34]						
Value	Name									
[0,34]										

PLANE_PRE_CSC_GAMC_INDEX_ENH

PLANE_PRE_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D0h-701D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D0h-702D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D0h-703D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D0h-711D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D0h-712D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D0h-713D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D0h-721D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft
Address:	722D0h-722D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_C

PLANE_PRE_CSC_GAMC_INDEX_ENH				
Reset:	soft			
Address:	723D0h-723D3h			
Name:	Plane Pre CSC Gamma Index			
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_C			
Reset:	soft			
Address:	731D0h-731D3h			
Name:	Plane Pre CSC Gamma Index			
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_D			
Reset:	soft			
Address:	732D0h-732D3h			
Name:	Plane Pre CSC Gamma Index			
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_D			
Reset:	soft			
Address:	733D0h-733D3h			
Name:	Plane Pre CSC Gamma Index			
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_D			
Reset:	soft			
DWord	Bit	Description		
0	31:11	Reserved		
		Access:	RO	
		Format:	MBZ	
	10	Index Auto Increment		
		This field enables the index auto increment.		
		Value	Name	Description
		0b	No Increment	Do not automatically increment the index value.
	1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.	
	9:8	Reserved		
		Access:	RO	
Format:		MBZ		
7:0	Index Value			
	Access:	Write/Read Status		
<p>This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.</p> <p>When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.</p> <p>While in auto increment mode, after performing reads or writes to only part of the range, the</p>				

PLANE_PRE_CSC_GAMC_INDEX_ENH

auto increment bit must be cleared before resetting the index value.

Value	Name
[0,130]	



PLANE_SIZE

PLANE_SIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70490h-70493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_A
Reset:	soft
Address:	70590h-70593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_A
Reset:	soft
Address:	70690h-70693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_A
Reset:	soft
Address:	70790h-70793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_A
Reset:	soft
Address:	71490h-71493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_B
Reset:	soft
Address:	71590h-71593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_B
Reset:	soft
Address:	71690h-71693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_B
Reset:	soft
Address:	71790h-71793h

PLANE_SIZE	
Name:	Plane Size
ShortName:	PLANE_SIZE_7_B
Reset:	soft
Address:	72490h-72493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_C
Reset:	soft
Address:	72590h-72593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_C
Reset:	soft
Address:	72690h-72693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_C
Reset:	soft
Address:	72790h-72793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_C
Reset:	soft
Address:	73490h-73493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_D
Reset:	soft
Address:	73590h-73593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_D
Reset:	soft
Address:	73690h-73693h
Name:	Plane Size
ShortName:	PLANE_SIZE_6_D
Reset:	soft
Address:	73790h-73793h
Name:	Plane Size
ShortName:	PLANE_SIZE_7_D
Reset:	soft
Address:	70190h-70193h



PLANE_SIZE

Name: Plane Size
ShortName: PLANE_SIZE_1_A
Reset: soft

Address: 70290h-70293h
Name: Plane Size
ShortName: PLANE_SIZE_2_A
Reset: soft

Address: 70390h-70393h
Name: Plane Size
ShortName: PLANE_SIZE_3_A
Reset: soft

Address: 71190h-71193h
Name: Plane Size
ShortName: PLANE_SIZE_1_B
Reset: soft

Address: 71290h-71293h
Name: Plane Size
ShortName: PLANE_SIZE_2_B
Reset: soft

Address: 71390h-71393h
Name: Plane Size
ShortName: PLANE_SIZE_3_B
Reset: soft

Address: 72190h-72193h
Name: Plane Size
ShortName: PLANE_SIZE_1_C
Reset: soft

Address: 72290h-72293h
Name: Plane Size
ShortName: PLANE_SIZE_2_C
Reset: soft

Address: 72390h-72393h
Name: Plane Size
ShortName: PLANE_SIZE_3_C
Reset: soft

Address: 73190h-73193h

PLANE_SIZE	
Name:	Plane Size
ShortName:	PLANE_SIZE_1_D
Reset:	soft
Address:	73290h-73293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_D
Reset:	soft
Address:	73390h-73393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_D
Reset:	soft
Address:	70898h-7089Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_A
Reset:	soft
Address:	708B8h-708BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_A
Reset:	soft
Address:	708D8h-708DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_A
Reset:	soft
Address:	708F8h-708FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_A
Reset:	soft
Address:	70928h-7092Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_A
Reset:	soft
Address:	70948h-7094Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_6_A
Reset:	soft
Address:	70968h-7096Bh

PLANE_SIZE			
Name:	Selective Fetch Plane Size		
ShortName:	SEL_FETCH_PLANE_SIZE_7_A		
Reset:	soft		
<p>This register specifies the plane source size, the size of the image fetched from the frame buffer. When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.</p>			
Restriction			
<p>When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size \geq plane position + plane size.</p>			
<p>For OLED compensation plane size restrictions, refer to PIPE_MISC->OLED Compensation (bit[12]).</p>			
<p>Height and Width restrictions are specified in the following table. For formats not specified in the table, both odd and even sizes are supported.</p>			
PixelFormat	Rotate Width Height		
YUV 420 Planar - NV12	All Even Even		
YUV 420 Planar - P01x	All Even Even		
YUV 422	All Even Even		
RGB565	90, 270 Even Even		
<p>If Plane Scaling or using the Chroma Up-Sampler (CUS) for this plane, please refer to PS_CTRL or PLANE_CUS_CTL respectively, for further size restrictions.</p>			
DWord	Bit	Description	
0	31:29	Reserved	
		Access: RO	
		Format: MBZ	
	28:16	Height This specifies the height of the plane in lines. The value in the register is the height minus one. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td>The height must be at least one line when non-interlaced, two lines when interlaced. The height is limited to maximum of 4320 lines. Refer to size restrictions within PS_CTRL when plane scaling is enabled.</td> </tr> </tbody> </table>	Restriction
Restriction			
The height must be at least one line when non-interlaced, two lines when interlaced. The height is limited to maximum of 4320 lines. Refer to size restrictions within PS_CTRL when plane scaling is enabled.			
15:13	Reserved		
	Access: RO		
	Format: MBZ		
12:0	Width		
	This specifies the width of the plane in pixels. The value in the register is the width minus one.		
	<table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td>The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. For YUV4:2:0 (NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16.</td> </tr> </tbody> </table>	Restriction	The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. For YUV4:2:0 (NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16.
Restriction			
The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. For YUV4:2:0 (NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16.			

PLANE_SIZE

The width must be greater than or equal to 4 for 32bpp, YUV212 and YUV216 formats, greater than or equal to 8 for 16bpp formats, and greater than or equal to 16 for 8bpp formats.
 The width must be greater than or equal to 2 for 64bpp formats.
 The width must be greater than or equal to 8 for P010, P012 and P016 formats.
 The width should be less than or equal to the stride in pixels.

For planar YUV 420 formats, refer to chroma upsampler size restrictions in PLANE_CUS_CTL register.

Tiling format	Bytes per pixel	Max Width supported in pixels
Linear, X Tiling	1,2,4,8	5120
Y Tiling	1,2,4,8	5120



PLANE_STRIDE

PLANE_STRIDE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70488h-7048Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_A
Reset:	soft
Address:	70588h-7058Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_A
Reset:	soft
Address:	70688h-7068Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_A
Reset:	soft
Address:	70788h-7078Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_A
Reset:	soft
Address:	71488h-7148Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_B
Reset:	soft
Address:	71588h-7158Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_B
Reset:	soft
Address:	71688h-7168Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_B
Reset:	soft
Address:	71788h-7178Bh

PLANE_STRIDE	
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_B
Reset:	soft
Address:	72488h-7248Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_C
Reset:	soft
Address:	72588h-7258Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_C
Reset:	soft
Address:	72688h-7268Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_C
Reset:	soft
Address:	72788h-7278Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_C
Reset:	soft
Address:	73488h-7348Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_D
Reset:	soft
Address:	73588h-7358Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_D
Reset:	soft
Address:	73688h-7368Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_6_D
Reset:	soft
Address:	73788h-7378Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_7_D
Reset:	soft
Address:	70188h-7018Bh

PLANE_STRIDE	
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_A
Reset:	soft
Address:	70288h-7028Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_A
Reset:	soft
Address:	70388h-7038Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_A
Reset:	soft
Address:	71188h-7118Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_B
Reset:	soft
Address:	71288h-7128Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_B
Reset:	soft
Address:	71388h-7138Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_B
Reset:	soft
Address:	72188h-7218Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_C
Reset:	soft
Address:	72288h-7228Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_C
Reset:	soft
Address:	72388h-7238Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_C
Reset:	soft
Address:	73188h-7318Bh

PLANE_STRIDE									
Name:	Plane Stride								
ShortName:	PLANE_STRIDE_1_D								
Reset:	soft								
Address:	73288h-7328Bh								
Name:	Plane Stride								
ShortName:	PLANE_STRIDE_2_D								
Reset:	soft								
Address:	73388h-7338Bh								
Name:	Plane Stride								
ShortName:	PLANE_STRIDE_3_D								
Reset:	soft								
This register may be updated through MMIO writes or through command streamer initiated synchronous flips.									
DWord	Bit	Description							
0	31:18	Reserved							
		Access:	RO						
		Format:	MBZ						
	17:12	Reserved							
		Access:	RO						
		Format:	MBZ						
	11	Reserved							
		Access:	RO						
		Format:	MBZ						
	10:0	Stride							
		<p>This field specifies the stride for the plane. The field is used to determine the line to line increment for the plane.</p> <p>For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = $100 * 64 = 6400$ bytes.</p> <p>For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = $10 * 512$ (X tile width) = 5120 bytes.</p> <p>For Tile Y, if the programmed value is 10, the actual stride = $10 * 128$ (Y tile width) = 1280 bytes.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Tile Format</th> <th>Width in bytes</th> </tr> </thead> <tbody> <tr> <td>Tile X</td> <td>512</td> </tr> <tr> <td>Tile Y (legacy)</td> <td>128</td> </tr> </tbody> </table>		Tile Format	Width in bytes	Tile X	512	Tile Y (legacy)	128
		Tile Format	Width in bytes						
Tile X		512							
Tile Y (legacy)		128							
Restriction :									
For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces.									
The stride in bytes must not exceed the of the size of 8K pixels.									

PLANE_STRIDE

		Tile Format	Pixel Format	Maximum Stride in tiles
		Linear	64 bpp pixel format	1024
			32 bpp pixel format	512
			16 bpp pixel format	256
			8 bpp pixel format	128
		X Tiling	64 bpp pixel format	128
			32 bpp pixel format	64
			16 bpp pixel format	32
			8 bpp pixel format	16
		Y Tiling (Legacy)	64 bpp pixel format	512
			32 bpp pixel format	256
			16 bpp pixel format	128
			8 bpp pixel format	64

PLANE_SURF

PLANE_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint: Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled	
Address:	7049Ch-7049Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_A
Reset:	soft
Address:	7059Ch-7059Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_A
Reset:	soft
Address:	7069Ch-7069Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_A
Reset:	soft
Address:	7079Ch-7079Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_A
Reset:	soft
Address:	7149Ch-7149Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_B
Reset:	soft
Address:	7159Ch-7159Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_B
Reset:	soft
Address:	7169Ch-7169Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_B
Reset:	soft
Address:	7179Ch-7179Fh

PLANE_SURF	
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_B
Reset:	soft
Address:	7249Ch-7249Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_C
Reset:	soft
Address:	7259Ch-7259Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_C
Reset:	soft
Address:	7269Ch-7269Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_C
Reset:	soft
Address:	7279Ch-7279Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_C
Reset:	soft
Address:	7349Ch-7349Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_D
Reset:	soft
Address:	7359Ch-7359Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_D
Reset:	soft
Address:	7369Ch-7369Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_6_D
Reset:	soft
Address:	7379Ch-7379Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_7_D
Reset:	soft
Address:	7019Ch-7019Fh

PLANE_SURF	
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_A
Reset:	soft
Address:	7029Ch-7029Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_A
Reset:	soft
Address:	7039Ch-7039Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_A
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_B
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_B
Reset:	soft
Address:	7139Ch-7139Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_B
Reset:	soft
Address:	7219Ch-7219Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_C
Reset:	soft
Address:	7229Ch-7229Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_C
Reset:	soft
Address:	7239Ch-7239Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_C
Reset:	soft
Address:	7319Ch-7319Fh

PLANE_SURF

Name: Plane Surface Base Address
 ShortName: PLANE_SURF_1_D
 Reset: soft

Address: 7329Ch-7329Fh
 Name: Plane Surface Base Address
 ShortName: PLANE_SURF_2_D
 Reset: soft

Address: 7339Ch-7339Fh
 Name: Plane Surface Base Address
 ShortName: PLANE_SURF_3_D
 Reset: soft

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.

Double buffering control does not apply to PLANE_SURF updates that occur when the plane is disabled. An interrupt event is generated immediately when the PLANE_SURF is written. If the interrupt is unmasked, the interrupt is logged in the IIR.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description			
0	31:12	Surface Base Address Format: GraphicsAddress[31:12]			
	11	Reserved			
	10:7	Reserved Access: RO Format: MBZ			
	6:4	Reserved			
	3	Ring Flip Source This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">CS</td> </tr> </tbody> </table>	Value	Name	0b
Value	Name				
0b	CS				

PLANE_SURF			
	1b		BCS
	2	Reserved	
	1:0	Reserved	
		Access:	RO
		Format:	MBZ



PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	704ACh-704AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_A
Reset:	soft
Address:	704BCh-704BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_A
Reset:	soft
Address:	705ACh-705AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_A
Reset:	soft
Address:	705BCh-705BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_A
Reset:	soft
Address:	706ACh-706AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_A
Reset:	soft
Address:	706BCh-706BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_A
Reset:	soft
Address:	707ACh-707AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_A
Reset:	soft
Address:	707BCh-707BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_A
Reset:	soft

PLANE_SURFLIVE	
Address:	714ACh-714AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_B
Reset:	soft
Address:	714BCh-714BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_B
Reset:	soft
Address:	715ACh-715AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_B
Reset:	soft
Address:	715BCh-715BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_B
Reset:	soft
Address:	716ACh-716AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_B
Reset:	soft
Address:	716BCh-716BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_B
Reset:	soft
Address:	717ACh-717AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_B
Reset:	soft
Address:	717BCh-717BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_B
Reset:	soft
Address:	724ACh-724AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_C
Reset:	soft

PLANE_SURFLIVE	
Address:	724BCh-724BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_C
Reset:	soft
Address:	725ACh-725AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_C
Reset:	soft
Address:	725BCh-725BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_C
Reset:	soft
Address:	726ACh-726AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_C
Reset:	soft
Address:	726BCh-726BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_C
Reset:	soft
Address:	727ACh-727AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_C
Reset:	soft
Address:	727BCh-727BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_C
Reset:	soft
Address:	734ACh-734AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_D
Reset:	soft
Address:	734BCh-734BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_D
Reset:	soft

PLANE_SURFLIVE	
Address:	735ACh-735AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_D
Reset:	soft
Address:	735BCh-735BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_D
Reset:	soft
Address:	736ACh-736AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_6_D
Reset:	soft
Address:	736BCh-736BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_6_D
Reset:	soft
Address:	737ACh-737AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_7_D
Reset:	soft
Address:	737BCh-737BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_7_D
Reset:	soft
Address:	701ACh-701AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_A
Reset:	soft
Address:	701BCh-701BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_A
Reset:	soft
Address:	702ACh-702AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_A
Reset:	soft

PLANE_SURFLIVE	
Address:	702BCh-702BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_A
Reset:	soft
Address:	703ACh-703AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_A
Reset:	soft
Address:	703BCh-703BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_A
Reset:	soft
Address:	711ACh-711AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_B
Reset:	soft
Address:	711BCh-711BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_B
Reset:	soft
Address:	712ACh-712AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_B
Reset:	soft
Address:	712BCh-712BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_B
Reset:	soft
Address:	713ACh-713AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_B
Reset:	soft
Address:	713BCh-713BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_B
Reset:	soft

PLANE_SURFLIVE	
Address:	721ACh-721AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_C
Reset:	soft
Address:	721BCh-721BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_C
Reset:	soft
Address:	722ACh-722AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_C
Reset:	soft
Address:	722BCh-722BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_C
Reset:	soft
Address:	723ACh-723AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_C
Reset:	soft
Address:	723BCh-723BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_C
Reset:	soft
Address:	731ACh-731AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_D
Reset:	soft
Address:	731BCh-731BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_D
Reset:	soft
Address:	732ACh-732AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_D
Reset:	soft

PLANE_SURFLIVE

Address: 732BCh-732BFh
 Name: Plane Live Left Surface Base Address
 ShortName: PLANE_LEFT_SURFLIVE_2_D
 Reset: soft

Address: 733ACh-733AFh
 Name: Plane Live Surface Base Address
 ShortName: PLANE_SURFLIVE_3_D
 Reset: soft

Address: 733BCh-733BFh
 Name: Plane Live Left Surface Base Address
 ShortName: PLANE_LEFT_SURFLIVE_3_D
 Reset: soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:12	Live Surface Base Address
		Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	Reserved
		Access: RO
		Format: MBZ
	10:9	Reserved
	8:0	Reserved
		Access: RO
		Format: MBZ

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF/CUR_BASE or plane/cursor not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	70140h-70143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_A
Reset:	soft
Address:	70144h-70147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_A
Reset:	soft
Address:	70148h-7014Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_A
Reset:	soft
Address:	7014Ch-7014Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_A
Reset:	soft
Address:	70150h-70153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_A
Reset:	soft
Address:	70154h-70157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_A
Reset:	soft
Address:	70158h-7015Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_A
Reset:	soft
Address:	7015Ch-7015Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_A
Reset:	soft
Address:	70168h-7016Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_A
Reset:	soft
Address:	71140h-71143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_B
Reset:	soft
Address:	71144h-71147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_B
Reset:	soft
Address:	71148h-7114Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_B
Reset:	soft
Address:	7114Ch-7114Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_B
Reset:	soft
Address:	71150h-71153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_B
Reset:	soft
Address:	71154h-71157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_B
Reset:	soft
Address:	71158h-7115Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_B
Reset:	soft
Address:	7115Ch-7115Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_B
Reset:	soft
Address:	71168h-7116Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_B
Reset:	soft
Address:	72140h-72143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_C
Reset:	soft
Address:	72144h-72147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_C
Reset:	soft
Address:	72148h-7214Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_C
Reset:	soft
Address:	7214Ch-7214Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_C
Reset:	soft
Address:	72150h-72153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_C
Reset:	soft
Address:	72154h-72157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_C
Reset:	soft
Address:	72158h-7215Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_C
Reset:	soft
Address:	7215Ch-7215Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_C
Reset:	soft
Address:	72168h-7216Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_C
Reset:	soft
Address:	73140h-73143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_D
Reset:	soft
Address:	73144h-73147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_D
Reset:	soft
Address:	73148h-7314Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_D
Reset:	soft
Address:	7314Ch-7314Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_D
Reset:	soft
Address:	73150h-73153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_D
Reset:	soft
Address:	73154h-73157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_D
Reset:	soft
Address:	73158h-7315Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_D
Reset:	soft
Address:	7315Ch-7315Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_D
Reset:	soft
Address:	73168h-7316Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_D
Reset:	soft
Address:	70540h-70543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_A
Reset:	soft
Address:	70544h-70547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_A
Reset:	soft
Address:	70548h-7054Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_A
Reset:	soft
Address:	7054Ch-7054Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_A
Reset:	soft
Address:	70550h-70553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_A
Reset:	soft
Address:	70554h-70557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_A
Reset:	soft
Address:	70558h-7055Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_A
Reset:	soft
Address:	7055Ch-7055Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_A
Reset:	soft
Address:	70568h-7056Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_4_A
Reset:	soft
Address:	70640h-70643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_A
Reset:	soft
Address:	70644h-70647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_A
Reset:	soft
Address:	70648h-7064Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_A
Reset:	soft
Address:	7064Ch-7064Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_A
Reset:	soft
Address:	70650h-70653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_A
Reset:	soft
Address:	70654h-70657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_A
Reset:	soft
Address:	70658h-7065Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_A
Reset:	soft
Address:	7065Ch-7065Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_A
Reset:	soft
Address:	70668h-7066Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_5_A
Reset:	soft
Address:	70740h-70743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_A
Reset:	soft
Address:	70744h-70747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_A
Reset:	soft
Address:	70748h-7074Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_A
Reset:	soft
Address:	7074Ch-7074Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_A
Reset:	soft
Address:	70750h-70753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_A
Reset:	soft
Address:	70754h-70757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_A
Reset:	soft
Address:	70758h-7075Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_A
Reset:	soft
Address:	7075Ch-7075Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_A
Reset:	soft
Address:	70768h-7076Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_6_A
Reset:	soft
Address:	70840h-70843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_A
Reset:	soft
Address:	70844h-70847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_A
Reset:	soft
Address:	70848h-7084Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_A
Reset:	soft
Address:	7084Ch-7084Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_A
Reset:	soft
Address:	70850h-70853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_A
Reset:	soft
Address:	70854h-70857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_A
Reset:	soft
Address:	70858h-7085Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_A
Reset:	soft
Address:	7085Ch-7085Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_A
Reset:	soft
Address:	70868h-7086Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_7_A
Reset:	soft
Address:	71540h-71543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_B
Reset:	soft
Address:	71544h-71547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_B
Reset:	soft
Address:	71548h-7154Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_B
Reset:	soft
Address:	7154Ch-7154Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_B
Reset:	soft
Address:	71550h-71553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_B
Reset:	soft
Address:	71554h-71557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_B
Reset:	soft
Address:	71558h-7155Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_B
Reset:	soft
Address:	7155Ch-7155Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_B
Reset:	soft
Address:	71568h-7156Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_B
Reset:	soft
Address:	71640h-71643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_B
Reset:	soft
Address:	71644h-71647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_B
Reset:	soft
Address:	71648h-7164Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_B
Reset:	soft
Address:	7164Ch-7164Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_B
Reset:	soft
Address:	71650h-71653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_B
Reset:	soft
Address:	71654h-71657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_B
Reset:	soft
Address:	71658h-7165Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_B
Reset:	soft
Address:	7165Ch-7165Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_B
Reset:	soft
Address:	71668h-7166Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_B
Reset:	soft
Address:	71740h-71743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_B
Reset:	soft
Address:	71744h-71747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_B
Reset:	soft
Address:	71748h-7174Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_B
Reset:	soft
Address:	7174Ch-7174Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_B
Reset:	soft
Address:	71750h-71753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_B
Reset:	soft
Address:	71754h-71757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_B
Reset:	soft
Address:	71758h-7175Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_B
Reset:	soft
Address:	7175Ch-7175Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_B
Reset:	soft
Address:	71768h-7176Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_B
Reset:	soft
Address:	71840h-71843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_B
Reset:	soft
Address:	71844h-71847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_B
Reset:	soft
Address:	71848h-7184Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_B
Reset:	soft
Address:	7184Ch-7184Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_B
Reset:	soft
Address:	71850h-71853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_B
Reset:	soft
Address:	71854h-71857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_B
Reset:	soft
Address:	71858h-7185Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_B
Reset:	soft
Address:	7185Ch-7185Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_B
Reset:	soft
Address:	71868h-7186Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_B
Reset:	soft
Address:	72540h-72543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_C
Reset:	soft
Address:	72544h-72547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_C
Reset:	soft
Address:	72548h-7254Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_C
Reset:	soft
Address:	7254Ch-7254Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_C
Reset:	soft
Address:	72550h-72553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_C
Reset:	soft
Address:	72554h-72557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_C
Reset:	soft
Address:	72558h-7255Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_C
Reset:	soft
Address:	7255Ch-7255Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_C
Reset:	soft
Address:	72568h-7256Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_C
Reset:	soft
Address:	72640h-72643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_C
Reset:	soft
Address:	72644h-72647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_C
Reset:	soft
Address:	72648h-7264Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_C
Reset:	soft
Address:	7264Ch-7264Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_C
Reset:	soft
Address:	72650h-72653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_C
Reset:	soft
Address:	72654h-72657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_C
Reset:	soft
Address:	72658h-7265Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_C
Reset:	soft
Address:	7265Ch-7265Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_C
Reset:	soft
Address:	72668h-7266Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_C
Reset:	soft
Address:	72740h-72743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_C
Reset:	soft
Address:	72744h-72747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_C
Reset:	soft
Address:	72748h-7274Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_C
Reset:	soft
Address:	7274Ch-7274Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_C
Reset:	soft
Address:	72750h-72753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_C
Reset:	soft
Address:	72754h-72757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_C
Reset:	soft
Address:	72758h-7275Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_C
Reset:	soft
Address:	7275Ch-7275Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_C
Reset:	soft
Address:	72768h-7276Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_C
Reset:	soft
Address:	72840h-72843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_C
Reset:	soft
Address:	72844h-72847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_C
Reset:	soft
Address:	72848h-7284Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_C
Reset:	soft
Address:	7284Ch-7284Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_C
Reset:	soft
Address:	72850h-72853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_C
Reset:	soft
Address:	72854h-72857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_C
Reset:	soft
Address:	72858h-7285Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_C
Reset:	soft
Address:	7285Ch-7285Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_C
Reset:	soft
Address:	72868h-7286Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_C
Reset:	soft
Address:	73540h-73543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_D
Reset:	soft
Address:	73544h-73547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_D
Reset:	soft
Address:	73548h-7354Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_D
Reset:	soft
Address:	7354Ch-7354Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_D
Reset:	soft
Address:	73550h-73553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_D
Reset:	soft
Address:	73554h-73557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_D
Reset:	soft
Address:	73558h-7355Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_D
Reset:	soft
Address:	7355Ch-7355Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_D
Reset:	soft
Address:	73568h-7356Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_D
Reset:	soft
Address:	73640h-73643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_D
Reset:	soft
Address:	73644h-73647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_D
Reset:	soft
Address:	73648h-7364Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_D
Reset:	soft
Address:	7364Ch-7364Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_D
Reset:	soft
Address:	73650h-73653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_D
Reset:	soft
Address:	73654h-73657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_D
Reset:	soft
Address:	73658h-7365Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_D
Reset:	soft
Address:	7365Ch-7365Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_D
Reset:	soft
Address:	73668h-7366Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_D
Reset:	soft
Address:	73740h-73743h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_6_D
Reset:	soft
Address:	73744h-73747h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_6_D
Reset:	soft
Address:	73748h-7374Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_6_D
Reset:	soft
Address:	7374Ch-7374Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_6_D
Reset:	soft
Address:	73750h-73753h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_6_D
Reset:	soft
Address:	73754h-73757h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_6_D
Reset:	soft
Address:	73758h-7375Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_6_D
Reset:	soft
Address:	7375Ch-7375Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_6_D
Reset:	soft
Address:	73768h-7376Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_6_D
Reset:	soft
Address:	73840h-73843h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_7_D
Reset:	soft
Address:	73844h-73847h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_7_D
Reset:	soft
Address:	73848h-7384Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_7_D
Reset:	soft
Address:	7384Ch-7384Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_7_D
Reset:	soft
Address:	73850h-73853h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_7_D
Reset:	soft
Address:	73854h-73857h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_7_D
Reset:	soft
Address:	73858h-7385Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_7_D
Reset:	soft
Address:	7385Ch-7385Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_7_D
Reset:	soft
Address:	73868h-7386Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_7_D
Reset:	soft
Address:	70240h-70243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_A
Reset:	soft
Address:	70244h-70247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_A
Reset:	soft
Address:	70248h-7024Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_A
Reset:	soft
Address:	7024Ch-7024Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_A
Reset:	soft
Address:	70250h-70253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_A
Reset:	soft
Address:	70254h-70257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_A
Reset:	soft
Address:	70258h-7025Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_A
Reset:	soft
Address:	7025Ch-7025Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_A
Reset:	soft
Address:	70268h-7026Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_A
Reset:	soft
Address:	70340h-70343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_A
Reset:	soft
Address:	70344h-70347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_A
Reset:	soft
Address:	70348h-7034Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_A
Reset:	soft
Address:	7034Ch-7034Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_A
Reset:	soft
Address:	70350h-70353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_A
Reset:	soft
Address:	70354h-70357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_A
Reset:	soft
Address:	70358h-7035Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_A
Reset:	soft
Address:	7035Ch-7035Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_A
Reset:	soft
Address:	70368h-7036Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_A
Reset:	soft
Address:	70440h-70443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_A
Reset:	soft
Address:	70444h-70447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_A
Reset:	soft
Address:	70448h-7044Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_A
Reset:	soft
Address:	7044Ch-7044Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_A
Reset:	soft
Address:	70450h-70453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_A
Reset:	soft
Address:	70454h-70457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_A
Reset:	soft
Address:	70458h-7045Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_A
Reset:	soft
Address:	7045Ch-7045Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_A
Reset:	soft
Address:	70468h-7046Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_A
Reset:	soft
Address:	71240h-71243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_B
Reset:	soft
Address:	71244h-71247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_B
Reset:	soft
Address:	71248h-7124Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_B
Reset:	soft
Address:	7124Ch-7124Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_B
Reset:	soft
Address:	71250h-71253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_B
Reset:	soft
Address:	71254h-71257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_B
Reset:	soft
Address:	71258h-7125Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_B
Reset:	soft
Address:	7125Ch-7125Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_B
Reset:	soft
Address:	71268h-7126Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_B
Reset:	soft
Address:	71340h-71343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_B
Reset:	soft
Address:	71344h-71347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_B
Reset:	soft
Address:	71348h-7134Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_B
Reset:	soft
Address:	7134Ch-7134Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_B
Reset:	soft
Address:	71350h-71353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_B
Reset:	soft
Address:	71354h-71357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_B
Reset:	soft
Address:	71358h-7135Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_B
Reset:	soft
Address:	7135Ch-7135Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_B
Reset:	soft
Address:	71368h-7136Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_B
Reset:	soft
Address:	71440h-71443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_B
Reset:	soft
Address:	71444h-71447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_B
Reset:	soft
Address:	71448h-7144Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_B
Reset:	soft
Address:	7144Ch-7144Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_B
Reset:	soft
Address:	71450h-71453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_B
Reset:	soft
Address:	71454h-71457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_B
Reset:	soft
Address:	71458h-7145Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_B
Reset:	soft
Address:	7145Ch-7145Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_B
Reset:	soft
Address:	71468h-7146Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_B
Reset:	soft
Address:	72240h-72243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_C
Reset:	soft
Address:	72244h-72247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_C
Reset:	soft
Address:	72248h-7224Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_C
Reset:	soft
Address:	7224Ch-7224Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_C
Reset:	soft
Address:	72250h-72253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_C
Reset:	soft
Address:	72254h-72257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_C
Reset:	soft
Address:	72258h-7225Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_C
Reset:	soft
Address:	7225Ch-7225Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_C
Reset:	soft
Address:	72268h-7226Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_C
Reset:	soft
Address:	72340h-72343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_C
Reset:	soft
Address:	72344h-72347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_C
Reset:	soft
Address:	72348h-7234Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_C
Reset:	soft
Address:	7234Ch-7234Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_C
Reset:	soft
Address:	72350h-72353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_C
Reset:	soft
Address:	72354h-72357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_C
Reset:	soft
Address:	72358h-7235Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_C
Reset:	soft
Address:	7235Ch-7235Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_C
Reset:	soft
Address:	72368h-7236Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_C
Reset:	soft
Address:	72440h-72443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_C
Reset:	soft
Address:	72444h-72447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_C
Reset:	soft
Address:	72448h-7244Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_C
Reset:	soft
Address:	7244Ch-7244Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_C
Reset:	soft
Address:	72450h-72453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_C
Reset:	soft
Address:	72454h-72457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_C
Reset:	soft
Address:	72458h-7245Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_C
Reset:	soft
Address:	7245Ch-7245Fh



PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_C
Reset:	soft
Address:	72468h-7246Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_C
Reset:	soft
Address:	73240h-73243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_D
Reset:	soft
Address:	73244h-73247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_D
Reset:	soft
Address:	73248h-7324Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_D
Reset:	soft
Address:	7324Ch-7324Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_D
Reset:	soft
Address:	73250h-73253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_D
Reset:	soft
Address:	73254h-73257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_D
Reset:	soft
Address:	73258h-7325Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_D
Reset:	soft
Address:	7325Ch-7325Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_D
Reset:	soft
Address:	73268h-7326Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_D
Reset:	soft
Address:	73340h-73343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_D
Reset:	soft
Address:	73344h-73347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_D
Reset:	soft
Address:	73348h-7334Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_D
Reset:	soft
Address:	7334Ch-7334Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_D
Reset:	soft
Address:	73350h-73353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_D
Reset:	soft
Address:	73354h-73357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_D
Reset:	soft
Address:	73358h-7335Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_D
Reset:	soft
Address:	7335Ch-7335Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_D
Reset:	soft
Address:	73368h-7336Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_D
Reset:	soft
Address:	73440h-73443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_D
Reset:	soft
Address:	73444h-73447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_D
Reset:	soft
Address:	73448h-7344Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_D
Reset:	soft
Address:	7344Ch-7344Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_D
Reset:	soft
Address:	73450h-73453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_D
Reset:	soft
Address:	73454h-73457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_D
Reset:	soft
Address:	73458h-7345Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_D
Reset:	soft
Address:	7345Ch-7345Fh

PLANE_WM			
Name:	Plane Watermarks		
ShortName:	PLANE_WM_7_3_D		
Reset:	soft		
Address:	73468h-7346Bh		
Name:	Plane Transition Watermarks		
ShortName:	PLANE_WM_TRANS_3_D		
Reset:	soft		
Programming Notes			
There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.			
Restriction			
For minimum watermark requirements refer to Display Watermark Programming section.			
DWord	Bit	Description	
0	31	Enable This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used.	
		Value	Name
		1b	Enable
		0b	Disable
	30	Reserved	
	29:27	Reserved	
		Access:	RO
		Format:	MBZ
	26:19	Reserved	
		Access:	RO
	Format:	MBZ	
18:14	Lines		
	Default Value:	01h	
This field contains the watermark value in lines. Hardware ignores the lines for the transition watermark.			
13:12	Reserved		
	Access:	RO	
	Format:	MBZ	

PLANE_WM		
	11	Reserved
		Access: RO
		Format: MBZ
	10:0	Blocks
		Default Value: 007h
	This field contains the watermark value in blocks of 8 cachelines.	

POISON DATA HANDLING ENABLE

POISON_DATA_HANDLING_ENABLE - POISON DATA HANDLING ENABLE						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
SOC_Consumer:	BIOS					
Address:	100120h					
This register holds the enable for Poison data detection and corking behavior for Gunit.						
DWord	Bit	Description				
0	31:1	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
0	0	ERROR CONTROL				
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
		Access:	R/W			
		_Custom_GTIReset:	BUS			
		Enable Poison Data detection and Corking behavior for Gunit				
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>[Default]</td> </tr> <tr> <td>1b</td> <td></td> </tr> </tbody> </table>	Value	Name	0b	[Default]	1b	
Value	Name					
0b	[Default]					
1b						



POISON DATA STATUS

DWord		Bit	Description	
Register Space:		MMIO: 0/2/0		
Size (in bits):		32		
SOC_Consumer:		BIOS		
Address:		100124h		
This register holds the sticky bit which when set will indicate a Poisoned data has been received on IOSF-Primary.				
0	31:9	Reserved		
		Access:	RO	
		Format:	MBZ	
	8	DEDICATED PATH ERROR STATUS		
		Access:	R/W One Clear	
		_Custom_GTIRreset:	DEV	
		Set to 1 when Poisoned data has been received from IOSF-Primary on Dedicated memory path. This sticky bit must survive Platform/SoC level reset.		
			Value	Name
		0b	[Default]	
	1b			
	7:1	Reserved		
		Access:	RO	
Format:		MBZ		
0	ERROR STATUS			
	Access:	R/W One Clear		
	_Custom_GTIRreset:	DEV		
	Set to 1 when Poisoned data has been received from IOSF-Primary. This sticky bit must survive Platform/SoC level reset.			
		Value	Name	
	0b	[Default]		
1b				

PORT_CL_DW5

PORT_CL_DW5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162014h-162017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_A	
Reset:	global	
Address:	6C014h-6C017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_B	
Reset:	global	
Address:	160014h-160017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_C	
Reset:	global	
DWord	Bit	Description
0	31:24	Force Default Value: 00010010b
	23	Reserved Access: RO Format: MBZ
	22	Fusevalid Reset
	21	Fusevalid Override
	20	Fuse Repull
	19:16	CRI Clock Count Max Default Value: 0100b
	15	Reserved Access: RO Format: MBZ
	14:13	IOSF PD Count
	12	Reserved Access: RO Format: MBZ

PORT_CL_DW5							
11:9	IOSF ClkDiv Sel <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">010b</td> </tr> </table>	Default Value:	010b				
Default Value:	010b						
8	DL Broadcast Enable This field causes all Tx's to get programmed when writing to a group access offset for a single Tx.						
7	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
6	Enable Port Staggering <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> </table>	Default Value:	1b				
Default Value:	1b						
5	PG Staggering Control Disable <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> </table>	Default Value:	1b				
Default Value:	1b						
4	CL Power Down Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						
3	CRI Clock Select <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> </table>	Default Value:	1b				
Default Value:	1b						
2	Phy Power Ack Override						
1:0	SUS Clock Config						

PORT_CL_DW10

PORT_CL_DW10			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	162028h-16202Bh		
Name:	PORT_CL_DW10		
ShortName:	PORT_CL_DW10_A		
Reset:	global		
Address:	6C028h-6C02Bh		
Name:	PORT_CL_DW10		
ShortName:	PORT_CL_DW10_B		
Reset:	global		
Address:	160028h-16002Bh		
Name:	PORT_CL_DW10		
ShortName:	PORT_CL_DW10_C		
Reset:	global		
DWord	Bit	Description	
0	31:27	Reserved	
		Access:	RO
		Format:	MBZ
	26:25	PG Seq Delay Override PG Sequential Delay Override	
	24	PG Seq Delay Override Enable PG Sequential Delay Override Enable	
		Value	Name
		0b	Disable
		1b	Enable
	23	ohvpg_ctrl_mipia MIPI A HVPG Control	
	22	spare 22 Spare 22	
21:16	ospare_cri_ret		
	Default Value:	000011b	
		ospare_cri_ret[6:0]	

PORT_CL_DW10

PORT_CL_DW10			
15:12	Reserved		
	Access:	RO	
	Format:	MBZ	
	11	Spare 11 Spare 11	
	10	Spare 10 Spare 10	
	9	Spare 9 Spare 9	
	8	Spare 8 Spare 8	
	7:4	Static Power Down This field powers down individual lanes for the DDI that is accessed through this instance of the register. To save power, unused lanes should be powered down after link training is complete.	
		Value	Name
		0000b	Power up all lanes
		1100b	Power down lanes 3,2
		1110b	Power down lanes 3,2,1
		0011b	Power down lanes 1,0
		0111b	Power down lanes 2,1,0
		1011b	Power down lanes 3,1,0
	1010b	Power down lanes 3,1	
	1000b	Power down lane 3	
3	o_edp4k2k_mode_ovrd_en eDP power optimized setting		
	Value	Name	
	1b	Enable [Default]	
	0b	Disable	
2	o_edp4k2k_mode_ovrd_val eDP power optimized setting. Valid only when corresponding enable bit (o_edp4k2k_mode_ovrd_en) is set and specific voltage swing programming is used.		
	Value	Name	
	1b	Optimized	
	0b	Non-optimized	
1	o_rterm100en_h_ovrd_en rterm override enable		
	Value	Name	
	1b	[Default]	

PORT_CL_DW10							
	0b						
0	o_rterm100en_h_ovrd_val rterm override val valid only when corresponding enable bit (o_rterm100en_h_ovrd_en) is set.						
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>150 Ohms</td> </tr> <tr> <td>1b</td> <td>100 Ohms</td> </tr> </tbody> </table>	Value	Name	0b	150 Ohms	1b	100 Ohms
Value	Name						
0b	150 Ohms						
1b	100 Ohms						



PORT_CL_DW12

PORT_CL_DW12			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	162030h-162033h		
Name:	PORT_CL_DW12		
ShortName:	PORT_CL_DW12_A		
Reset:	global		
Address:	6C030h-6C033h		
Name:	PORT_CL_DW12		
ShortName:	PORT_CL_DW12_B		
Reset:	global		
Address:	160030h-160033h		
Name:	PORT_CL_DW12		
ShortName:	PORT_CL_DW12_C		
Reset:	global		
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
	29	MIPI Lane Enable	
		Value	Name
		0b	Disable
	1b	Enable	
	28	Reserved	
		Access:	RO
		Format:	MBZ
	27	MIPI Mode Override Enable	
		Value	Name
		0b	
	1b		
	26	MIPI Mode Override	
		Value	Name
0b			
1b			

PORT_CL_DW12								
	25:18	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
	Format:	MBZ						
	17:16	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
	Format:	MBZ						
	15:12	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
	Access:	RO						
	Format:	MBZ						
	11	Pwr Req Override AUX <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td></td> </tr> <tr> <td>1b</td> <td></td> </tr> </tbody> </table>	Value	Name	0b		1b	
	Value	Name						
	0b							
1b								
10	Pwr Req Override Enable AUX <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable	
Value	Name							
0b	Disable							
1b	Enable							
9:7	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							
6	Phy Status AUX <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO					
Access:	RO							
5	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							
4	Power Ack AUX <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table>	Access:	RO					
Access:	RO							
3:1	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							
0	Lane Enable AUX <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable	
Value	Name							
0b	Disable							
1b	Enable							



PORT_CL_DW15

PORT_CL_DW15				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	16203Ch-16203Fh			
Name:	PORT_CL_DW15			
ShortName:	PORT_CL_DW15_A			
Reset:	global			
Address:	6C03Ch-6C03Fh			
Name:	PORT_CL_DW15			
ShortName:	PORT_CL_DW15_B			
Reset:	global			
Address:	16003Ch-16003Fh			
Name:	PORT_CL_DW15			
ShortName:	PORT_CL_DW15_C			
Reset:	global			
DWord	Bit	Description		
0	31:30	Reserved		
		Access:	RO	
		Format:	MBZ	
	29		HVPG Power Ack	
			Access:	RO
			Value	Name
			0b	
	1b			
	28		HVPG Enable Status	
			Access:	RO
			Value	Name
			0b	
1b				
27		Power Ack MIPI		
		Access:	RO	
		Value	Name	

PORT_CL_DW15		
	0b	
	1b	
26:22	Reserved	
	Access:	RO
	Format:	MBZ
21	Power Req AUX	
	Access:	RO
	Value	Name
	0b	
	1b	
20:18	Reserved	
	Access:	RO
	Format:	MBZ
17	Power Ack AUX	
	Access:	RO
	Value	Name
	0b	
	1b	
16:0	Reserved	
	Access:	RO
	Format:	MBZ



PORT_CL_DW16

PORT_CL_DW16		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162040h-162043h	
Name:	PORT_CL_DW16	
ShortName:	PORT_CL_DW16_A	
Reset:	global	
Address:	6C040h-6C043h	
Name:	PORT_CL_DW16	
ShortName:	PORT_CL_DW16_B	
Reset:	global	
Address:	160040h-160043h	
Name:	PORT_CL_DW16	
ShortName:	PORT_CL_DW16_C	
Reset:	global	
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
		Format: MBZ
	15	o_hd_ddib_sel_ovrden DDI B HD Port select override enable
	14	o_hd_ddib_sel_ovrd DDI B HD Port select override
	13	o_hd_ddic_sel_ovrden DDI C HD Port select override enable
	12	o_hd_ddic_sel_ovrd DDI C HD Port select override
	11	o_hd_ddid_sel_ovrden DDI D HD Port select override enable
	10	o_hd_ddid_sel_ovrd DDI D HD Port select override
	9:8	Reserved
		Access: RO Format: MBZ
	7:4	ospare_cri[3:0] reserved

PORT_CL_DW16		
	3	o_comp_pwrdown_ovrd Comp Power Down Override
	2	o_comp_pwrdown_ovrden Comp Power Down Override Enable
	1	o_cri_wake_ovrd CRI Wake Override
	0	o_cri_wake_ovrden CRI Wake Override Enable



PORT_COMP_DW0

PORT_COMP_DW0							
Register Space:	MMIO: 0/2/0						
Access:	R/W						
Size (in bits):	32						
Address:	162100h-162103h						
Name:	PORT_COMP_DW0						
ShortName:	PORT_COMP_DW0_A						
Reset:	global						
Address:	6C100h-6C103h						
Name:	PORT_COMP_DW0						
ShortName:	PORT_COMP_DW0_B						
Reset:	global						
Address:	160100h-160103h						
Name:	PORT_COMP_DW0						
ShortName:	PORT_COMP_DW0_C						
Reset:	global						
DWord	Bit	Description					
0	31	Comp Init					
	30:29	Tx Slew Ctl					
	28:27	Tx Drvsw On					
	26	Tx Drvsw Ctl					
	25:24	Comp Spare					
	23	Procmon clock Sel					
	22:20	Reserved					
		Access:	RO				
		Format:	MBZ				
	19:8	Periodic Comp Counter Periodic comp programmable counter.					
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>05Fh</td> <td>1.25ms [Default]</td> <td>Period of ~ 1.25ms w.r.t sus clock frequency of 19.2MHz.</td> </tr> </tbody> </table>	Value	Name	Description	05Fh	1.25ms [Default]	Period of ~ 1.25ms w.r.t sus clock frequency of 19.2MHz.
Value	Name	Description					
05Fh	1.25ms [Default]	Period of ~ 1.25ms w.r.t sus clock frequency of 19.2MHz.					
7:0	Reserved						
	Access:	RO					
	Format:	MBZ					

PORT_COMP_DW1

PORT_COMP_DW1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162104h-162107h	
Name:	PORT_COMP_DW1	
ShortName:	PORT_COMP_DW1_A	
Reset:	global	
Address:	6C104h-6C107h	
Name:	PORT_COMP_DW1	
ShortName:	PORT_COMP_DW1_B	
Reset:	global	
Address:	160104h-160107h	
Name:	PORT_COMP_DW1	
ShortName:	PORT_COMP_DW1_C	
Reset:	global	
DWord	Bit	Description
0	31	ldo_bypass Default Value: 1b
	30	fcomp_ovrd_en
	29	fcomp_capratio
	28	fcomp_bias_sel
	27:26	fcomp_inputssel_ovrd
	25	fcomp_polaritysel
	24	rcomp_en Default Value: 1b
	23:22	p_ref_highval[9:8] Default Value: 01b
	21:20	p_ref_lowval[9:8]
	19:18	n_ref_highval[9:8] Default Value: 01b
	17:16	n_ref_lowval[9:8]
	15:14	phvt_ref_highval[9:8]
	13:12	phvt_ref_lowval[9:8]

PORT_COMP_DW1		
	11:10	nhvt_ref_highval[9:8] Default Value: 01h
	9:8	nhvt_ref_lowval[9:8]
	7:6	plvt_ref_highval[9:8] Default Value: 01b
	5:4	plvt_ref_lowval[9:8]
	3:2	nlvt_ref_highval[9:8] Default Value: 01b
	1:0	nlvt_ref_lowval[9:8]

PORT_COMP_DW3

PORT_COMP_DW3			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	16210Ch-16210Fh		
Name:	PORT_COMP_DW3		
ShortName:	PORT_COMP_DW3_A		
Reset:	global		
Address:	6C10Ch-6C10Fh		
Name:	PORT_COMP_DW3		
ShortName:	PORT_COMP_DW3_B		
Reset:	global		
Address:	16010Ch-16010Fh		
Name:	PORT_COMP_DW3		
ShortName:	PORT_COMP_DW3_C		
Reset:	global		
DWord	Bit	Description	
0	31:29	Reserved	
		Access:	RO
		Format:	MBZ
	28:26	Process Info	
		Value	Name
		000b	dot-0
		001b	dot-1
	25:24	Voltage Info	
		Value	Name
		00b	0.85V
01b		0.95V	
23	23	PLL DDI Pwr Ack	
	22	First Comp Done	
	21	Procmon Done	
	20	Icomp Code Maxout	
	19	Icomp Code Minout	

PORT_COMP_DW3		
	18:15	Reserved
		Access: RO
		Format: MBZ
	14:8	Icomp Code
	7	Lpdn Code Maxout
	6	Lpdn Code Minout
5:0	MIPI Lpdn Code	

PORT_COMP_DW8

PORT_COMP_DW8			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	162120h-162123h		
Name:	PORT_COMP_DW8		
ShortName:	PORT_COMP_DW8_A		
Reset:	global		
Address:	6C120h-6C123h		
Name:	PORT_COMP_DW8		
ShortName:	PORT_COMP_DW8_B		
Reset:	global		
Address:	160120h-160123h		
Name:	PORT_COMP_DW8		
ShortName:	PORT_COMP_DW8_C		
Reset:	global		
DWord	Bit	Description	
0	31:25	Reserved	
		Access:	RO
		Format:	MBZ
	24	irefgen	
		Value	Name
		1b	Enable
	0b	Disable	
	23:15	Reserved	
		Access:	RO
		Format:	MBZ
	14	prdic_icom_dis disable periodic icomp	
		Value	Name
		0b	Enable
	1b	Disable	
	13:0	Reserved	
		Access:	RO
Format:		MBZ	



PORT_COMP_DW9

PORT_COMP_DW9		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162124h-162127h	
Name:	PORT_COMP_DW9	
ShortName:	PORT_COMP_DW9_A	
Reset:	global	
Address:	6C124h-6C127h	
Name:	PORT_COMP_DW9	
ShortName:	PORT_COMP_DW9_B	
Reset:	global	
Address:	160124h-160127h	
Name:	PORT_COMP_DW9	
ShortName:	PORT_COMP_DW9_C	
Reset:	global	
DWord	Bit	Description
0	31:24	n_ref_lowval[7:0] Default Value: 11011010b
	23:16	n_ref_highval[7:0] Default Value: 10001100b
	15:8	p_ref_lowval[7:0] Default Value: 11011100b
	7:0	p_ref_highval[7:0] Default Value: 10100101b

PORT_COMP_DW10

PORT_COMP_DW10		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162128h-16212Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_A	
Reset:	global	
Address:	6C128h-6C12Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_B	
Reset:	global	
Address:	160128h-16012Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_C	
Reset:	global	
DWord	Bit	Description
0	31:24	nlvt_ref_lowval[7:0] Default Value: 10101010b
	23:16	nlvt_ref_highval[7:0] Default Value: 00111101b
	15:8	plvt_ref_lowval[7:0] Default Value: 10101000b
	7:0	plvt_ref_highval[7:0] Default Value: 01010011b



PORT_PCS_DW1

PORT_PCS_DW1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162304h-162307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_A
Reset:	global
Address:	162604h-162607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_A
Reset:	global
Address:	162804h-162807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_A
Reset:	global
Address:	162904h-162907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_A
Reset:	global
Address:	162A04h-162A07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_A
Reset:	global
Address:	162B04h-162B07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN3_A
Reset:	global
Address:	6C304h-6C307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_B
Reset:	global
Address:	6C604h-6C607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_B

PORT_PCS_DW1	
Reset:	global
Address:	6C804h-6C807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_B
Reset:	global
Address:	6C904h-6C907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_B
Reset:	global
Address:	6CA04h-6CA07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_B
Reset:	global
Address:	6CB04h-6CB07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN3_B
Reset:	global
Address:	160304h-160307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_C
Reset:	global
Address:	160604h-160607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_C
Reset:	global
Address:	160804h-160807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_C
Reset:	global
Address:	160904h-160907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_C
Reset:	global
Address:	160A04h-160A07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_C

PORT_PCS_DW1

Reset: global
 Address: 160B04h-160B07h
 Name: PORT_PCS_DW1
 ShortName: PORT_PCS_DW1_LN3_C
 Reset: global

DWord	Bit	Description	
0	31:29	Reserved	
		Access: RO	
		Format: MBZ	
	28	cmnkeeper_enable_in_pg	
		Value	Name
		1b	enable [Default]
		0b	disable
	27	pg_pwrdownen PG Power Down Enable	
		Value	Name
		1b	enable [Default]
		0b	disable
	26	cmnkeeper_enable Common Keeper Enable	
		Value	Name
		1b	enable [Default]
		0b	disable
25:24	cmnkeep_biasctr Common Keeper Bias Control		
23:22	Reserved		
	Access: RO		
	Format: MBZ		
21:20	DCC Mode Select		
	Value	Name	
	00b	Run DCC once [Default]	
	01b	Run DCC every 100us	
	10b	Run DCC every 1ms	
	11b	Run DCC continuously	
19	reg_dcc_bypass		
	Default Value: 0b		
Setting this bit will bypass the DCC calibration and will also bypass the DFx RX calibration since			

PORT_PCS_DW1

	both are triggered using same signal in PCS	
18	reg_dcc_calib_wake_en	
	Default Value:	0b
	Asserting this bit will run DCC again during DL wake up from powerdown	
17	tx_dcc_calib_enable	
	Default Value:	0b
	Force Tx DCC Calibration Enable (Should be used only after initial boot is done)	
16	Reserved	
15:14	Reserved	
	Access:	RO
	Format:	MBZ
13:12	txhigh	
11:10	Reserved	
	Access:	RO
	Format:	MBZ
9:8	clkreq	
7	tbc_as_symbclk	
	Select tbc clock to be used as symbol clock internal to the data lane	
6	txfifo_rst_main_ovrden	
	Override enable for Tx main resets	
5	txfifo_rst_main_ovrd	
	Reset Main Override for Tx	
4	txdeemp	
	Deemphasis Value	
3:2	latencyoptim	
	Default Value:	01b
	Latency Optim	
1	softreset_enable	
	Allow soft_reset_n to reset the lanes	
	Value	Name
	1b	enable
	0b	disable
0	soft_reset_n	
	Default Value:	1b
	Active low soft reset override	



PORT_PCS_DW9

PORT_PCS_DW9	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162324h-162327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_A
Reset:	global
Address:	162624h-162627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_A
Reset:	global
Address:	162824h-162827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_A
Reset:	global
Address:	162924h-162927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_A
Reset:	global
Address:	162A24h-162A27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_A
Reset:	global
Address:	162B24h-162B27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN3_A
Reset:	global
Address:	6C324h-6C327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_B
Reset:	global
Address:	6C624h-6C627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_B

PORT_PCS_DW9	
Reset:	global
Address:	6C824h-6C827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_B
Reset:	global
Address:	6C924h-6C927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_B
Reset:	global
Address:	6CA24h-6CA27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_B
Reset:	global
Address:	6CB24h-6CB27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN3_B
Reset:	global
Address:	160324h-160327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_C
Reset:	global
Address:	160624h-160627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_C
Reset:	global
Address:	160824h-160827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_C
Reset:	global
Address:	160924h-160927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_C
Reset:	global
Address:	160A24h-160A27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_C

PORT_PCS_DW9						
Reset:	global					
Address:	160B24h-160B27h					
Name:	PORT_PCS_DW9					
ShortName:	PORT_PCS_DW9_LN3_C					
Reset:	global					
DWord	Bit	Description				
0	31:28	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
	27:16	Strong CM Count Ovrđ <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>301h</td> </tr> </table>	Default Value:	301h		
	Default Value:	301h				
	15:11	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
10:8	Stagger Mult <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>001b</td> </tr> </table>	Default Value:	001b			
Default Value:	001b					
7:6	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
5	Stagger Override					
4:0	Stagger					

PORT_TX_DFLEXDPCSSS

PORT_TX_DFLEXDPCSSS			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	163894h-163897h		
Name:	PORT_TX_DFLEXDPCSSS		
ShortName:	PORT_TX_DFLEXDPCSSS_FIA1		
Reset:	global		
Address:	16E894h-16E897h		
Name:	PORT_TX_DFLEXDPCSSS		
ShortName:	PORT_TX_DFLEXDPCSSS_FIA2		
Reset:	global		
Address:	16F894h-16F897h		
Name:	PORT_TX_DFLEXDPCSSS		
ShortName:	PORT_TX_DFLEXDPCSSS_FIA3		
Reset:	global		
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	Displayport Phy Mode Status for Type-C Connector 7 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 7.	
	6	Displayport Phy Mode Status for Type-C Connector 6 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 6.	
	5	Displayport Phy Mode Status for Type-C Connector 5 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 5.	
	4	Displayport Phy Mode Status for Type-C Connector 4 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 4.	
	3	Displayport Phy Mode Status for Type-C Connector 3 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 3.	
	2	Displayport Phy Mode Status for Type-C Connector 2 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 2.	
	1	Displayport Phy Mode Status for Type-C Connector 1 Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 1.	
0	Displayport Phy Mode Status for Type-C Connector 0 Displayport Phy Mode Status for Type-C Connector 0 (DPPMSTC0):		

PORT_TX_DFLEXDPCSSS		
	Value	Name
	1b	DP Controller is not in safe state
	0b	DP controller is in safe state

PORT_TX_DFLEXDPMLE1

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1																	
Register Space:	MMIO: 0/2/0																
Access:	R/W																
Size (in bits):	32																
Reset:	soft																
Address:	1638C0h-1638C3h																
Name:	PORT_TX_DFLEXDPMLE1																
ShortName:	PORT_TX_DFLEXDPMLE1_FIA1																
Reset:	soft																
Address:	16E8C0h-16E8C3h																
Name:	PORT_TX_DFLEXDPMLE1																
ShortName:	PORT_TX_DFLEXDPMLE1_FIA2																
Reset:	soft																
Address:	16F8C0h-16F8C3h																
Name:	PORT_TX_DFLEXDPMLE1																
ShortName:	PORT_TX_DFLEXDPMLE1_FIA3																
Reset:	soft																
<p>Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware uses this information for PHY to Controller signal mapping. For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lanes in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program 0001b to this register. For x2 and x4, Display Driver will program 0011b and 1111b, respectively.</p> <p>Note that display driver should not use its internal lane reversal feature with Type-C ALT connections.</p> <p>Display Driver is expected to write to this register when the DDI Interface between DP Controller and FIA is in the Safe Mode, e.g. pllen=pwrreq=lane_enable=0. Display Driver writes to this register and then only it brings up the DP Controller, i.e. to bring the DDI interface out from Safe Mode. A mode set is required to switch the number of DP lanes. This register is applicable in both Type-C connector's Alternate mode and also DP connector mode.</p>																	
DWord	Bit	Description															
0	31:28	<p>Displayport Main Link Enable for Type-C Connector 7 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 7.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]	
Value	Name	Description															
0001b	ML0																
0011b	ML[1:0]																
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.															
1111b	ML[3:0]																

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

	27:24	Displayport Main Link Enable for Type-C Connector 6 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 6.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]	
	Value	Name	Description														
	0001b	ML0															
	0011b	ML[1:0]															
	1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.														
	1111b	ML[3:0]															
	23:20	Displayport Main Link Enable for Type-C Connector 5 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 5.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]	
	Value	Name	Description														
	0001b	ML0															
	0011b	ML[1:0]															
	1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.														
	1111b	ML[3:0]															
	19:16	Displayport Main Link Enable for Type-C Connector 4 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 4.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]	
	Value	Name	Description														
	0001b	ML0															
	0011b	ML[1:0]															
	1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.														
1111b	ML[3:0]																
15:12	Displayport Main Link Enable for Type-C Connector 3 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 3.																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]		
Value	Name	Description															
0001b	ML0																
0011b	ML[1:0]																
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.															
1111b	ML[3:0]																
11:8	Displayport Main Link Enable for Type-C Connector 2 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 2.																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>ML0</td> <td></td> </tr> <tr> <td>0011b</td> <td>ML[1:0]</td> <td></td> </tr> <tr> <td>1100b</td> <td>ML[3:2]</td> <td>This setting should not be used with Type-C ALT connections.</td> </tr> <tr> <td>1111b</td> <td>ML[3:0]</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	0001b	ML0		0011b	ML[1:0]		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.	1111b	ML[3:0]		
Value	Name	Description															
0001b	ML0																
0011b	ML[1:0]																
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.															
1111b	ML[3:0]																
7:4	Displayport Main Link Enable for Type-C Connector 1 Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 1.																

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

		Value	Name	Description
		0001b	ML0	
		0011b	ML[1:0]	
		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
		1111b	ML[3:0]	
3:0	<p>Displayport Main Link Enable for Type-C Connector 0</p> <p>Display Port Main Link Enable for Type-C Connector 0 (DPMLETC0): 4 bits correspond to 4 Main Link in DP Controller. Bit [0] is ML0, bit [1] is ML1 and so on. The Type-C Connector number is logical number. Its not physical lane numbers. Refer to the SOC block diagram for the mapping of Type-C Connector number to the actual physical lane number of the PHY.</p> <p>Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware use this information for PHY to Controller signal mapping.</p> <p>For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lane in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program 0001b to this register. For x2 and x4, Display Driver will program 0011b and 1111b, respectively.</p>			
		Value	Name	Description
		0001b	ML0	
		0011b	ML[1:0]	
		1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
		1111b	ML[3:0]	

PORT_TX_DFLEXDPPMS

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Reset:	soft		
Address:	163890h-163893h		
Name:	PORT_TX_DFLEXDPPMS		
ShortName:	PORT_TX_DFLEXDPPMS_FIA1		
Reset:	soft		
Address:	16E890h-16E893h		
Name:	PORT_TX_DFLEXDPPMS		
ShortName:	PORT_TX_DFLEXDPPMS_FIA2		
Reset:	soft		
Address:	16F890h-16F893h		
Name:	PORT_TX_DFLEXDPPMS		
ShortName:	PORT_TX_DFLEXDPPMS_FIA3		
Reset:	soft		
DWord	Bit	Description	
0	31:16	Reserved	
		Access:	RO
		Format:	MBZ
	15	Display Port PHY Mode status for Type-C connector 15 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 15.	
	14	Display Port PHY Mode status for Type-C connector 14 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 14.	
	13	Display Port PHY Mode status for Type-C connector 13 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 13.	
	12	Display Port PHY Mode status for Type-C connector 12 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 12.	
	11	Display Port PHY Mode status for Type-C connector 11 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 11.	
	10	Display Port PHY Mode status for Type-C connector 10 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 10.	
	9	Display Port PHY Mode status for Type-C connector 9 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 9.	
8	Display Port PHY Mode status for Type-C connector 8 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 8.		

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS

7	Display Port PHY Mode status for Type-C connector 7 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 7.						
6	Display Port PHY Mode status for Type-C connector 6 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 6.						
5	Display Port PHY Mode status for Type-C connector 5 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 5.						
4	Display Port PHY Mode status for Type-C connector 4 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 4.						
3	Display Port PHY Mode status for Type-C connector 3 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 3.						
2	Display Port PHY Mode status for Type-C connector 2 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 2.						
1	Display Port PHY Mode status for Type-C connector 1 Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 1.						
0	Display Port PHY Mode status for Type-C connector 0 DFLEXDPPMS.DPPMSTC0 PD FW writes 1 to this bit to tell DP Driver that PHY is ready. PD FW writes '0' to this bit to tell DP Driver that PHY is not ready. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Not Completed</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Completed</td> </tr> </tbody> </table>	Value	Name	0b	Not Completed	1b	Completed
Value	Name						
0b	Not Completed						
1b	Completed						



PORT_TX_DFLEXDPSP

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Reset:	soft
Address:	1638A0h-1638A3h
Name:	PORT_TX_DFLEXDPSP1
ShortName:	PORT_TX_DFLEXDPSP1_FIA1
Reset:	soft
Address:	1638A4h-1638A7h
Name:	PORT_TX_DFLEXDPSP2
ShortName:	PORT_TX_DFLEXDPSP2_FIA1
Reset:	soft
Address:	1638A8h-1638ABh
Name:	PORT_TX_DFLEXDPSP3
ShortName:	PORT_TX_DFLEXDPSP3_FIA1
Reset:	soft
Address:	1638ACh-1638AFh
Name:	PORT_TX_DFLEXDPSP4
ShortName:	PORT_TX_DFLEXDPSP4_FIA1
Reset:	soft
Address:	16E8A0h-16E8A3h
Name:	PORT_TX_DFLEXDPSP1
ShortName:	PORT_TX_DFLEXDPSP1_FIA2
Reset:	soft
Address:	16E8A4h-16E8A7h
Name:	PORT_TX_DFLEXDPSP2
ShortName:	PORT_TX_DFLEXDPSP2_FIA2
Reset:	soft
Address:	16E8A8h-16E8ABh
Name:	PORT_TX_DFLEXDPSP3
ShortName:	PORT_TX_DFLEXDPSP3_FIA2
Reset:	soft
Address:	16E8ACh-16E8AFh
Name:	PORT_TX_DFLEXDPSP4

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP																	
ShortName:	PORT_TX_DFLEXDPSP4_FIA2																
Reset:	soft																
Address:	16F8A0h-16F8A3h																
Name:	PORT_TX_DFLEXDPSP1																
ShortName:	PORT_TX_DFLEXDPSP1_FIA3																
Reset:	soft																
Address:	16F8A4h-16F8A7h																
Name:	PORT_TX_DFLEXDPSP2																
ShortName:	PORT_TX_DFLEXDPSP2_FIA3																
Reset:	soft																
Address:	16F8A8h-16F8ABh																
Name:	PORT_TX_DFLEXDPSP3																
ShortName:	PORT_TX_DFLEXDPSP3_FIA3																
Reset:	soft																
Address:	16F8ACh-16F8AFh																
Name:	PORT_TX_DFLEXDPSP4																
ShortName:	PORT_TX_DFLEXDPSP4_FIA3																
Reset:	soft																
Dynamic FlexIO DP Scratch Pad (Type-C)																	
See the TypeC Programming section for information on how the connector number here maps to the port instance.																	
DWord	Bit	Description															
0	31:29	TC3 Live State															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>No HPD</td> <td>No HPD connect for TypeC (DP alternate) or TBT</td> </tr> <tr> <td>001b</td> <td>TypeC HPD</td> <td>HPD connect for TypeC (DP alternate)</td> </tr> <tr> <td>010b</td> <td>TBT HPD</td> <td>HPD connect for TBT</td> </tr> <tr> <td>011b</td> <td>Invalid</td> <td>Invalid</td> </tr> </tbody> </table>	Value	Name	Description	000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT	001b	TypeC HPD	HPD connect for TypeC (DP alternate)	010b	TBT HPD	HPD connect for TBT	011b	Invalid	Invalid
		Value	Name	Description													
		000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT													
		001b	TypeC HPD	HPD connect for TypeC (DP alternate)													
	010b	TBT HPD	HPD connect for TBT														
	011b	Invalid	Invalid														
	28	Reserved															
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ											
	Access:	RO															
Format:	MBZ																
27:24	Display Port x4 TX Lane Assignment for Type-C Connector 3																
	Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 3. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>PHY TX[0]</td> </tr> </tbody> </table>	Value	Name	0001b	PHY TX[0]												
Value	Name																
0001b	PHY TX[0]																

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

		0010b	PHY TX[1]
		0011b	PHY TX[1:0]
		0100b	PHY TX[2]
		0101b	PHY TX[2] TX[0]
		1000b	PHY TX[3]
		1100b	PHY TX[3:2]
		1111b	PHY TX[3:0]
23:21	TC2 Live State		
	Value	Name	Description
	000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
	001b	TypeC HPD	HPD connect for TypeC (DP alternate)
	010b	TBT HPD	HPD connect for TBT
	011b	Invalid	Invalid
20	Reserved		
	Access:		RO
	Format:		MBZ
19:16	Display Port x4 TX Lane Assignment for Type-C Connector 2		
	Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 2.		
	Value	Name	
	0001b	PHY TX[0]	
	0010b	PHY TX[1]	
	0011b	PHY TX[1:0]	
	0100b	PHY TX[2]	
	0101b	PHY TX[2] TX[0]	
	1000b	PHY TX[3]	
	1100b	PHY TX[3:2]	
	1111b	PHY TX[3:0]	
15:13	TC1 Live State		
	Value	Name	Description
	000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
	001b	TypeC HPD	HPD connect for TypeC (DP alternate)
	010b	TBT HPD	HPD connect for TBT
	011b	Invalid	Invalid
12	IOM FW version		
	This field identifies the IOM firmware that is used.		

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

		Value	Name	
		0b	old IOM FW	
		1b	IOM FW with MFD Gen2 support	
11:8	Display Port x4 TX Lane Assignment for Type-C Connector 1 Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 1.			
		Value	Name	
		0001b	PHY TX[0]	
		0010b	PHY TX[1]	
		0011b	PHY TX[1:0]	
		0100b	PHY TX[2]	
		0101b	PHY TX[2] TX[0]	
		1000b	PHY TX[3]	
		1100b	PHY TX[3:2]	
		1111b	PHY TX[3:0]	
7:5	TC0 Live state			
		Value	Name	Description
		000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
		001b	TypeC HPD	HPD connect for TypeC (DP alternate)
		010b	TBT HPD	HPD connect for TBT
		011b	Invalid	Invalid
4	Modular FIA (MF)			
	Description			
	This bit is set by IOM FW and read by Display Driver. It tells the Display Driver if Modular FIA is used in the SOC. If Modular FIA is used in the SOC, then Display Driver will access the additional instances of FIA based on pre-assigned offset in GTTMADDR space. Each Modular FIA instance houses only 2 Type-C Ports. If Modular FIA is not used in the SOC, then a single monolithic FIA is used to house all the Type-C Ports which has only one IOSF Sideband Port ID. Modular FIA is always used. IOM FW will program the MF bit in all FIA instances.			
		Value	Name	
		0b	Monolithic FIA	
		1b	Modular FIA	
3:0	Display Port x4 TX Lane Assignment for Type-C Connector 0 DPX4TXLATC0 SOC FW writes to these bits to tell display software the Lane Assignment, which it generates			

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

based on the DP Pin Assignment and the Connector Orientation. Display software uses this value to determine the number of lanes that can be enabled, and along with other registers, to determine the DP mode programming. See the Typec PHY DDI Buffer page for DP mode programming.

The 4 bits correspond to 4 TX, i.e. TX[3:0] Lane in PHY.

Lower 2 bits correspond to the 2 lower TX lane on the PHY of Type-C connector.

Upper 2 bits correspond to the upper 2 TX lane on the PHY of Type-C connector.

For example, in DP Pin Assignment D (Multi function) and Flip case, the x2 TX lane are on the upper TypeC Lane, hence the value written into this register will be 1100b.

Another example, in DP Pin Assignment B (Multi function) Active Gen2 cable and Flip case, the x1 TX lane is on the 1st TX of upper TypeC Lane, hence the value written into this register will be 0100b.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

PORT_TX_DFLEXNPCPMS

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Reset:	soft	
Address:	163480h-163483h	
Name:	PORT_TX_DFLEXNPCPMS	
ShortName:	PORT_TX_DFLEXNPCPMS_FIA1	
Reset:	soft	
Address:	16E480h-16E483h	
Name:	PORT_TX_DFLEXNPCPMS	
ShortName:	PORT_TX_DFLEXNPCPMS_FIA2	
Reset:	soft	
Address:	16F480h-16F483h	
Name:	PORT_TX_DFLEXNPCPMS	
ShortName:	PORT_TX_DFLEXNPCPMS_FIA3	
Reset:	soft	
SW writes to these bits to control the Combo Ports mode. This register governs the Phy status tracking handling that could be different for different controllers.		
DWord	Bit	Description
0	31:28	Combo Port 7 Next Phy Combo Port Mode Select (CP7NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 7.
	27:24	Combo Port 6 Next Phy Combo Port Mode Select (CP6NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 6.
	23:20	Combo Port 5 Next Phy Combo Port Mode Select (CP5NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 5.
	19:16	Combo Port 4 Next Phy Combo Port Mode Select (CP4NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 4.
	15:12	Combo Port 3 Next Phy Combo Port Mode Select (CP3NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 3.
	11:8	Combo Port 2 Next Phy Combo Port Mode Select (CP2NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 2.
	7:4	Combo Port 1 Next Phy Combo Port Mode Select (CP1NPCPMS): Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 1.
	3:0	Combo Port 0 Next Phy Combo Port Mode Select (CP0NPCPMS): The Combo Port number is logical. Its not physical lane numbers. 0h: Port Mode is NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 1h: Port Mode is Owner 1 (default owner)

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS

	<p>2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved Others: Reserved</p> <p>SW mode: SW writes to these bits to control the Combo Ports mode. This register governs the Phy status tracking handling that could be different for different controller.</p> <p>HW mode: These bits have no impact to HW when written. The reset default is dependent on the internal HW mux select bits though its being indicated as soft-straps. The mux selects bits retain their context across Sx and will be reloaded back into this field.</p>
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PORT_TX_DFLEXPA1

PORT_TX_DFLEXPA1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	163880h-163883h	
Name:	PORT_TX_DFLEXPA1	
ShortName:	PORT_TX_DFLEXPA1_FIA1	
Reset:	global	
Address:	16E880h-16E883h	
Name:	PORT_TX_DFLEXPA1	
ShortName:	PORT_TX_DFLEXPA1_FIA2	
Reset:	global	
Address:	16F880h-16F883h	
Name:	PORT_TX_DFLEXPA1	
ShortName:	PORT_TX_DFLEXPA1_FIA3	
Reset:	global	
<p>FIA has per Connector register to govern the Pin Assignment of each Type-C Connector. For example, DFLEXPA1.DPPATC0 is used to govern the Pin Assignment of Type-C Connector 0. The Type-C Connector number (e.g. "0" in register DPPATC0) is logical number.</p>		
DWord	Bit	Description
0	31:28	Displayport Pin Assignment for Type-C Connector 7 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 7.
	27:24	Displayport Pin Assignment for Type-C Connector 6 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 6.
	23:20	Displayport Pin Assignment for Type-C Connector 5 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 5.
	19:16	Displayport Pin Assignment for Type-C Connector 4 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 4.
	15:12	Displayport Pin Assignment for Type-C Connector 3 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 3.
	11:8	Displayport Pin Assignment for Type-C Connector 2 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 2.
	7:4	Displayport Pin Assignment for Type-C Connector 1 Similar to register DFLEXPA1.DPPATC0 but this register is for Type-C Connector 1.
	3:0	Displayport Pin Assignment for Type-C Connector 0 Display Port Pin Assignment for Type-C Connector 0 (DPPATC0): Assignments Cand E have 4 lanes for DP alternate mode. Assignments D has2 lanes for DP alternate mode.

PORT_TX_DFLEXP1

		Value	Name
		0000b	No Pin Assignment (For Non Type-C/static/fixed/legacy connections)
		0011b	Pin Assignment C
		0100b	Pin Assignment D
		0101b	Pin Assignment E

PORT_TX_DFLEXPA2

PORT_TX_DFLEXPA2 - PORT_TX_DFLEXPA2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Reset:	soft	
Address:	163884h-163887h	
Name:	PORT_TX_DFLEXPA2	
ShortName:	PORT_TX_DFLEXPA2_FIA1	
Reset:	soft	
Address:	16E884h-16E887h	
Name:	PORT_TX_DFLEXPA2	
ShortName:	PORT_TX_DFLEXPA2_FIA2	
Reset:	soft	
Address:	16F884h-16F887h	
Name:	PORT_TX_DFLEXPA2	
ShortName:	PORT_TX_DFLEXPA2_FIA3	
Reset:	soft	
<p>FIA has per Connector register to govern the Pin Assignment of each Type-C Connector. For example, DFLEXPA1.DPPATC0 is used to govern the Pin Assignment of Type-C Connector 0. The Type-C Connector number (e.g. 0 in register DPPATC0) is logical number.</p>		
DWord	Bit	Description
0	31:28	Displayport Pin Assignment for Type-C Connector 15 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 15.
	27:24	Displayport Pin Assignment for Type-C Connector 14 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 14.
	23:20	Displayport Pin Assignment for Type-C Connector 13 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 13.
	19:16	Displayport Pin Assignment for Type-C Connector 12 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 12.
	15:12	Displayport Pin Assignment for Type-C Connector 11 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 11.
	11:8	Displayport Pin Assignment for Type-C Connector 10 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 10.
	7:4	Displayport Pin Assignment for Type-C Connector 9 Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 9.
	3:0	Displayport Pin Assignment for Type-C Connector 8 Display Port Pin Assignment for Type-C Connector 8 (DPPATC8): 0000 : No Pin Assignment (For Non Type-C DP)

PORT_TX_DFLEXP2 - PORT_TX_DFLEXP2	
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	0001 : Pin Assignment A 0010 : Pin Assignment B 0011 : Pin Assignment C 0100 : Pin Assignment D 0101 : Pin Assignment E 0110 : Pin Assignment F 0111-1111 : Reserved
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PORT_TX_DW0

PORT_TX_DW0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162380h-162383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_A
Reset:	global
Address:	162680h-162683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_A
Reset:	global
Address:	162880h-162883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_A
Reset:	global
Address:	162980h-162983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_A
Reset:	global
Address:	162A80h-162A83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_A
Reset:	global
Address:	162B80h-162B83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN3_A
Reset:	global
Address:	6C380h-6C383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_B
Reset:	global
Address:	6C680h-6C683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_B

PORT_TX_DW0	
Reset:	global
Address:	6C880h-6C883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_B
Reset:	global
Address:	6C980h-6C983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_B
Reset:	global
Address:	6CA80h-6CA83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_B
Reset:	global
Address:	6CB80h-6CB83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN3_B
Reset:	global
Address:	160380h-160383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_C
Reset:	global
Address:	160680h-160683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_C
Reset:	global
Address:	160880h-160883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_C
Reset:	global
Address:	160980h-160983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_C
Reset:	global
Address:	160A80h-160A83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_C

PORT_TX_DW0			
Reset:	global		
Address:	160B80h-160B83h		
Name:	PORT_TX_DW0		
ShortName:	PORT_TX_DW0_LN3_C		
Reset:	global		
This register controls Tx Equalization within the Combo-PHY's AFE.			
Restriction : Do not change the default Cursor Coefficient values within this register since that will change the equalization being applied by the PHY			
DWord	Bit	Description	
0	31	MIPI EQ Select This bit controls the Tx Equalization level of the PHY This bit is equivalent to the TxEqLevelHS PPI pin, but it is only used by the PHY when both the MIPI EQ Override Enable and MIPI EQ Enable bits are set.	
		Value	Name
		0b	Low Level Equalization (3.5 dB)
		1b	High Level Equalization (7 dB)
	30	MIPI EQ Enable This bit represents the Tx Equalization active state (i.e. enable) This bit is equivalent to the TxEqActiveHS PPI pin, but it is only used by the PHY when the MIPI EQ Override Enable is set	
		Value	Name
		0b	Tx Equalization Disabled
		1b	Tx Equalization Enabled
	29:24	Post Cursor Coeff 0 Default Value: bh Default post cursor coeff Restriction : Do not change the default value	
	23	MIPI EQ Override Enable This bit controls whether the PPI Tx Equalization pins are driving the equalization logic, or the override bits from this register	
Value		Name	
0b		PPI inputs drive EQ logic	
1b		This register drives EQ logic	
22:6	Reserved		
	Access:	RO	
	Format:	MBZ	
5:0	Cursor Coeff 0 Default Value: 34h Default cursor coeff Restriction : Do not change the default value		



PORT_TX_DW1

PORT_TX_DW1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162384h-162387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_A
Reset:	global
Address:	162684h-162687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_A
Reset:	global
Address:	162884h-162887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_A
Reset:	global
Address:	162984h-162987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_A
Reset:	global
Address:	162A84h-162A87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_A
Reset:	global
Address:	162B84h-162B87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN3_A
Reset:	global
Address:	6C384h-6C387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_B
Reset:	global
Address:	6C684h-6C687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_B

PORT_TX_DW1	
Reset:	global
Address:	6C884h-6C887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_B
Reset:	global
Address:	6C984h-6C987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_B
Reset:	global
Address:	6CA84h-6CA87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_B
Reset:	global
Address:	6CB84h-6CB87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN3_B
Reset:	global
Address:	160384h-160387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_C
Reset:	global
Address:	160684h-160687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_C
Reset:	global
Address:	160884h-160887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_C
Reset:	global
Address:	160984h-160987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_C
Reset:	global
Address:	160A84h-160A87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_C

PORT_TX_DW1		
Reset:	global	
Address:	160B84h-160B87h	
Name:	PORT_TX_DW1	
ShortName:	PORT_TX_DW1_LN3_C	
Reset:	global	
DWord	Bit	Description
0	31:8	Reserved
		Access: RO
		Format: MBZ
	7	o_iref_config ICOMP Config bit from COMP routed to Txana
	6:5	o_iref_ctrl control to change the ratio of tx iboost
	4:3	o_tx_slew_ctrl Used for MIPI HSTX Slew rate control config
	2	o_vref_low_en LDO Feedback path enable for low vref
	1	o_vref_hi_en LDO Feedback path enable for hi vref
0	o_vref_nom_en LDO Feedback path enable for nominal vref	

PORT_TX_DW2

PORT_TX_DW2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162388h-16238Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_A
Reset:	global
Address:	162688h-16268Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_A
Reset:	global
Address:	162888h-16288Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_A
Reset:	global
Address:	162988h-16298Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_A
Reset:	global
Address:	162A88h-162A8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_A
Reset:	global
Address:	162B88h-162B8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN3_A
Reset:	global
Address:	6C388h-6C38Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_B
Reset:	global
Address:	6C688h-6C68Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_B

PORT_TX_DW2	
Reset:	global
Address:	6C888h-6C88Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_B
Reset:	global
Address:	6C988h-6C98Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_B
Reset:	global
Address:	6CA88h-6CA8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_B
Reset:	global
Address:	6CB88h-6CB8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN3_B
Reset:	global
Address:	160388h-16038Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_C
Reset:	global
Address:	160688h-16068Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_C
Reset:	global
Address:	160888h-16088Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_C
Reset:	global
Address:	160988h-16098Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_C
Reset:	global
Address:	160A88h-160A8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_C

PORT_TX_DW2		
Reset:	global	
Address:	160B88h-160B8Bh	
Name:	PORT_TX_DW2	
ShortName:	PORT_TX_DW2_LN3_C	
Reset:	global	
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
		Format: MBZ
	15	swing_sel upper Swing_sel bit 3
	14	cmnmode_sel Select one of the weak common modes.
	13:11	swing_sel lower
		Default Value: 010b Select the voltage swing level. Note that this field has swing_sel bits 2:0 and bit 3 is in swing_sel upper, which is not adjacent.
10:8	frclatencyoptim Enables forcing the latency optimized value for the FIFO.	
7:0	Rcomp scalar	
	Default Value: 10011000b Also called Swing Scalar. Scalar to be applied to comp code to get required termination.	



PORT_TX_DW4

PORT_TX_DW4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162390h-162393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_A
Reset:	global
Address:	162690h-162693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_A
Reset:	global
Address:	162890h-162893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_A
Reset:	global
Address:	162990h-162993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_A
Reset:	global
Address:	162A90h-162A93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_A
Reset:	global
Address:	162B90h-162B93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN3_A
Reset:	global
Address:	6C390h-6C393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_B
Reset:	global
Address:	6C690h-6C693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_B

PORT_TX_DW4	
Reset:	global
Address:	6C890h-6C893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_B
Reset:	global
Address:	6C990h-6C993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_B
Reset:	global
Address:	6CA90h-6CA93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_B
Reset:	global
Address:	6CB90h-6CB93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN3_B
Reset:	global
Address:	160390h-160393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_C
Reset:	global
Address:	160690h-160693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_C
Reset:	global
Address:	160890h-160893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_C
Reset:	global
Address:	160990h-160993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_C
Reset:	global
Address:	160A90h-160A93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_C

PORT_TX_DW4		
Reset:	global	
Address:	160B90h-160B93h	
Name:	PORT_TX_DW4	
ShortName:	PORT_TX_DW4_LN3_C	
Reset:	global	
DWord	Bit	Description
0	31	Loadgen Select
	30:24	Spare
	23	BS Comp Ovrđ
	22:18	Rterm Limit Default Value: 10000b
	17:12	Post Cursor 1 o_txscaling_coeff[17:12]
	11:6	Post Cursor 2 o_txscaling_coeff[11:6]
	5:0	Cursor Coeff Default Value: 011000b o_txscaling_coeff[5:0]

PORT_TX_DW5

PORT_TX_DW5	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162394h-162397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_A
Reset:	global
Address:	162694h-162697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_A
Reset:	global
Address:	162894h-162897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_A
Reset:	global
Address:	162994h-162997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_A
Reset:	global
Address:	162A94h-162A97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_A
Reset:	global
Address:	162B94h-162B97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN3_A
Reset:	global
Address:	6C394h-6C397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_B
Reset:	global
Address:	6C694h-6C697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_B

PORT_TX_DW5	
Reset:	global
Address:	6C894h-6C897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_B
Reset:	global
Address:	6C994h-6C997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_B
Reset:	global
Address:	6CA94h-6CA97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_B
Reset:	global
Address:	6CB94h-6CB97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN3_B
Reset:	global
Address:	160394h-160397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_C
Reset:	global
Address:	160694h-160697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_C
Reset:	global
Address:	160894h-160897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_C
Reset:	global
Address:	160994h-160997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_C
Reset:	global
Address:	160A94h-160A97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_C

PORT_TX_DW5								
Reset:	global							
Address:	160B94h-160B97h							
Name:	PORT_TX_DW5							
ShortName:	PORT_TX_DW5_LN3_C							
Reset:	global							
DWord	Bit	Description						
0	31	TX Training Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>enable</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>disable</td> </tr> </tbody> </table>	Value	Name	1b	enable	0b	disable
	Value	Name						
	1b	enable						
	0b	disable						
	30	Disable 2tap ospare2[5] <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable
	Value	Name						
	0b	Enable						
	1b	Disable						
	29	Disable 3tap ospare2[5] <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable
	Value	Name						
0b	Enable							
1b	Disable							
28:27	Spare 28 27 ospare2[4:3]							
26	Cursor Program ospare2[2] <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable	
Value	Name							
0b	Enable							
1b	Disable							
25	Coeff Polarity ospare2[1] <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable	
Value	Name							
0b	Enable							
1b	Disable							
24	Spare 24 ospare2[0]							
23:21	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							

PORT_TX_DW5				
	20:18	Scaling Mode Sel <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">010b</td> </tr> </table>	Default Value:	010b
	Default Value:	010b		
	17:16	Decode Timer Sel <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">01b</td> </tr> </table>	Default Value:	01b
	Default Value:	01b		
	15:11	CR Scaling Coef		
	10:6	Spare 10 6 o_tx_vswing[10:6]		
5:3	Rterm Select o_tx_vswing[5:3]			
2:0	Spare 2 0 o_tx_vswing[2:0]			

PORT_TX_DW6

PORT_TX_DW6 - PORT_TX_DW6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162398h-16239Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_A
Reset:	global
Address:	162698h-16269Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_A
Reset:	global
Address:	162898h-16289Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_A
Reset:	global
Address:	162998h-16299Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_A
Reset:	global
Address:	162A98h-162A9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_A
Reset:	global
Address:	162B98h-162B9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN3_A
Reset:	global
Address:	6C398h-6C39Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_B
Reset:	global
Address:	6C698h-6C69Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_B

PORT_TX_DW6 - PORT_TX_DW6	
Reset:	global
Address:	6C898h-6C89Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_B
Reset:	global
Address:	6C998h-6C99Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_B
Reset:	global
Address:	6CA98h-6CA9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_B
Reset:	global
Address:	6CB98h-6CB9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN3_B
Reset:	global
Address:	160398h-16039Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_C
Reset:	global
Address:	160698h-16069Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_C
Reset:	global
Address:	160898h-16089Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_C
Reset:	global
Address:	160998h-16099Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_C
Reset:	global
Address:	160A98h-160A9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_C

PORT_TX_DW6 - PORT_TX_DW6		
Reset:	global	
Address:	160B98h-160B9Bh	
Name:	PORT_TX_DW6	
ShortName:	PORT_TX_DW6_LN3_C	
Reset:	global	
DWord	Bit	Description
0	31:8	Reserved
		Access: RO
		Format: MBZ
	7	o_func_ovrd_en ovrd enable signal
	6:1	o_ldo_ref_sel_cri ovrd for ldo_ref_sel
0	o_ldo_bypass_cri ovrd for ldo bypass	



PORT_TX_DW7

PORT_TX_DW7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	16239Ch-16239Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_A
Reset:	global
Address:	16269Ch-16269Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_A
Reset:	global
Address:	16289Ch-16289Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_A
Reset:	global
Address:	16299Ch-16299Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_A
Reset:	global
Address:	162A9Ch-162A9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_A
Reset:	global
Address:	162B9Ch-162B9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN3_A
Reset:	global
Address:	6C39Ch-6C39Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_B
Reset:	global
Address:	6C69Ch-6C69Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_B

PORT_TX_DW7	
Reset:	global
Address:	6C89Ch-6C89Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_B
Reset:	global
Address:	6C99Ch-6C99Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_B
Reset:	global
Address:	6CA9Ch-6CA9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_B
Reset:	global
Address:	6CB9Ch-6CB9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN3_B
Reset:	global
Address:	16039Ch-16039Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_C
Reset:	global
Address:	16069Ch-16069Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_C
Reset:	global
Address:	16089Ch-16089Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_C
Reset:	global
Address:	16099Ch-16099Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_C
Reset:	global
Address:	160A9Ch-160A9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_C

PORT_TX_DW7		
Reset:	global	
Address:	160B9Ch-160B9Fh	
Name:	PORT_TX_DW7	
ShortName:	PORT_TX_DW7_LN3_C	
Reset:	global	
DWord	Bit	Description
0	31	Spare 31
	30:24	N Scalar
	Default Value: 7Fh	
	23:0	Spare 23 0

PORT_TX_DW8

PORT_TX_DW8	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1623A0h-1623A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_A
Reset:	global
Address:	1626A0h-1626A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_A
Reset:	global
Address:	1628A0h-1628A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_A
Reset:	global
Address:	1629A0h-1629A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_A
Reset:	global
Address:	162AA0h-162AA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_A
Reset:	global
Address:	162BA0h-162BA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN3_A
Reset:	global
Address:	6C3A0h-6C3A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_B
Reset:	global
Address:	6C6A0h-6C6A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_B

PORT_TX_DW8	
Reset:	global
Address:	6C8A0h-6C8A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_B
Reset:	global
Address:	6C9A0h-6C9A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_B
Reset:	global
Address:	6CAA0h-6CAA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_B
Reset:	global
Address:	6CBA0h-6CBA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN3_B
Reset:	global
Address:	1603A0h-1603A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_C
Reset:	global
Address:	1606A0h-1606A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_C
Reset:	global
Address:	1608A0h-1608A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_C
Reset:	global
Address:	1609A0h-1609A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_C
Reset:	global
Address:	160AA0h-160AA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_C

PORT_TX_DW8										
Reset:	global									
Address:	160BA0h-160BA3h									
Name:	PORT_TX_DW8									
ShortName:	PORT_TX_DW8_LN3_C									
Reset:	global									
DWord	Bit	Description								
0	31	odcc_clksel <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">0b</td> </tr> </table> DCC clock select	Default Value:	0b						
	Default Value:	0b								
	30:29	odcc_clk_div_sel <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b,01b</td> <td style="text-align: center;">div2</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">div4 [Default]</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">div8</td> </tr> </tbody> </table>	Value	Name	00b,01b	div2	10b	div4 [Default]	11b	div8
	Value	Name								
	00b,01b	div2								
	10b	div4 [Default]								
	11b	div8								
	28:24	odcc_code_ovrd <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">10000b</td> </tr> </table>	Default Value:	10000b						
	Default Value:	10000b								
	23	odcc_code_ovrd_en								
	22	odccfuse_en								
	21	Reserved								
	20:16	odcc_lower_limit <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00011b</td> </tr> </table>	Default Value:	00011b						
	Default Value:	00011b								
15	Reserved									
14:13	idcc_code_therm_4_3 <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">10b</td> </tr> </table>	Default Value:	10b							
Default Value:	10b									
12:8	idcc_code <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">10000b</td> </tr> </table>	Default Value:	10000b							
Default Value:	10000b									
7:5	idcc_code_therm_2_0									
4:0	odcc_upper_limit <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td style="text-align: center;">11100b</td> </tr> </table>	Default Value:	11100b							
Default Value:	11100b									



POSH LRCA

POSH_LRCA - POSH LRCA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021B0h-021B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_RCSUNIT
Address:	181B0h-181B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_POCSUNIT
Address:	221B0h-221B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_BCSUNIT
Address:	1C01B0h-1C01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT0
Address:	1C41B0h-1C41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT1
Address:	1C81B0h-1C81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT0
Address:	1D01B0h-1D01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT2
Address:	1D41B0h-1D41B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT3
Address:	1D81B0h-1D81B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VECSUNIT1
Address:	1E01B0h-1E01B3h
Name:	POSH LRCA
ShortName:	POSH_LRCA_VCSUNIT4

POSH_LRCA - POSH LRCA					
Address:	1E41B0h-1E41B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_VCSUNIT5				
Address:	1E81B0h-1E81B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_VECSUNIT2				
Address:	1F01B0h-1F01B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_VCSUNIT6				
Address:	1F41B0h-1F41B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_VCSUNIT7				
Address:	1F81B0h-1F81B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_VECSUNIT3				
Address:	1A1B0h-1A1B3h				
Name:	POSH LRCA				
ShortName:	POSH_LRCA_CCSUNIT0				
<p>This register contains the LRCA address for the POSH pipe to which POCS does context save/restore. LRCA address programmed in this register is only effective when "POSH Enable" field is set in CTX_SR_CTL register. This register is not functional and must not be programmed for VideoCS, VideoEnhancementCS, BlitterCS.</p>					
DWord	Bit	Description			
0	31:12	POSH Logical Ring Context Address			
	11:0	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:	RO				
Format:	MBZ				



Power Clock State Register

PWR_CLK_STATE - Power Clock State Register				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	020C8h-020CBh			
Name:	PWR_CLK_STATE			
ShortName:	PWR_CLK_STATE_RCSUNIT_BE_COMPUTE			
Address:	1A0C8h-1A0CBh			
Name:	PWR_CLK_STATE			
ShortName:	PWR_CLK_STATE_CCSUNIT_BE_COMPUTE0			
<p>This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.</p>				
Programming Notes				
<p>This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.</p>				
<p>This register must not be programmed directly through CPU MMIO cycle. Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer.</p>				
DWord	Bit	Description		
0	31:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>PBC</td> </tr> </table>	Format:	PBC
Format:	PBC			

Power Management Capabilities

PMCAP_0_2_0_PCI - Power Management Capabilities			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	000D2h		
This register provides information on the capabilities of the function related to power management.			
DWord	Bit	Description	
0	15:11	PME Support	
		Default Value:	00000b
		Access:	RO
		_Custom_GTIRreset:	BUS
			This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
	10	D2 Support	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
			Hardwired to 0 to indicate the D2 power management state is not supported.
9	D1 Support		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
		Hardwired to 0 to indicate that the D1 power management state is not supported.	
8:6	Reserved		
	Access:	RO	
	Format:	MBZ	
5	Device Specific Initialization		
	Default Value:	1b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
		Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.	
4	Reserved		
	Access:	RO	
	Format:	MBZ	

PMCAP_0_2_0_PCI - Power Management Capabilities			
	3	PME Clock	
		Default Value:	0b
		Access:	RO
		_Custom_GTIRreset:	BUS
	Hardwired to 0 to indicate IGD does not support PME# generation.		
	2:0	Version	
		Access:	RO
		_Custom_GTIRreset:	BUS
		Description	
		Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.	
Value		Name	
010b		[Default]	

Power Management Capabilities ID

PMCAPID_0_2_0_PCI - Power Management Capabilities ID								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	000D0h							
This register contains the PCI Power Management Capability ID and the next capability pointer.								
DWord	Bit	Description						
0	15:8	Next Capability Pointer <table border="1"> <tr> <td>Default Value:</td> <td>00000000b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> This is a hardwired pointer to the next item in the capabilities list.	Default Value:	00000000b	Access:	RO	_Custom_GTIReset:	BUS
	Default Value:	00000000b						
Access:	RO							
_Custom_GTIReset:	BUS							
7:0	Capability Identifier <table border="1"> <tr> <td>Default Value:</td> <td>00000001b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> Hardwired to 01h for power management.	Default Value:	00000001b	Access:	RO	_Custom_GTIReset:	BUS	
Default Value:	00000001b							
Access:	RO							
_Custom_GTIReset:	BUS							



Power Management Control and Status

PMCS_0_2_0_PCI - Power Management Control and Status			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	000D4h		
DWord	Bit	Description	
0	15	PME Status	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
	This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).		
	14:13	Data Scale	
		Default Value:	00b
		Access:	RO
		_Custom_GTIReset:	BUS
	This field is hardwired to 00 to indicate IGD does not support data register.		
	12:9	Data Select	
		Default Value:	0000b
Access:		RO	
_Custom_GTIReset:		BUS	
This field is hardwired to 0h to indicate IGD does not support data register.			
8	PME Enable		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.			
7:2	Reserved		
	Access:	RO	
	Format:	MBZ	
1:0	Power State		
	Default Value:	00b	
	Access:	R/W Variant	
	_Custom_GTIReset:	BUS	
This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section			
Bits[1:0]Power state00:D0Default01:D1Not Supported10:D2Not Supported11:D3			

PPPR

PPPR - PPPR				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
SOC_Consumer:	BIOS			
Address:	124824h			
GT uses this register to post pending page requests to software, such as x86 page faults. A write to this register triggers an MSI per the registers PRESTS, PRECTL, PREDATA, PREADR, and PREUADR.				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	POST PENDING PAGE REQUEST		
		Default Value:	0h	
		Access:	WO	
		_Custom_GTIRreset:	BUS	
		Post Pending Page Request		

PPRO

PPRO - PPRO				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
SOC_Consumer:	BIOS			
Address:	124820h			
GT uses this register to post Page Request Queue overflow faults				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	POST PAGE REQUEST OVERFLOW FAULT		
		Default Value:	0h	
		Access:	WO	
		_Custom_GTIReset:	BUS	
		Post Page Request overflow fault		

PRE_CSC_GAMC_DATA

PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A488h-4A48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_A
Reset:	soft
Address:	4AC88h-4AC8Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_B
Reset:	soft
Address:	4B488h-4B48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_C
Reset:	soft
Address:	4BC88h-4BC8Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_D
Reset:	soft
Description	
<p>PRE_CSC_GAMC_INDEX and PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the pipe pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion Gamma if desired.</p> <p>The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.</p> <p>For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.</p> <p>For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.</p> <p>For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.</p> <p>For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.</p>	

PRE_CSC_GAMC_DATA

Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the PLANE_COLOR_CTL register. The same set of values is used for gamma correction of the red, blue and green channels.

See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Recommended sRGB degamma programming:

Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Values	0	9	15	25	3A	56	78	A0	D0	10	14	18	1D	23	29	2F	36	3E	46	4F	59	63	6E	79	85	92	A0	AE	BD	CC	DD	EE2	100
	F	3	3	C	5	3	C	6	76	5F	C8	B3	25	22	AE	CB	7E	CA	B1	38	61	2E	A4	C4	92	0F	3F	25	C2	19	D	00	

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	Reserved
		Access: RO
		Format: MBZ
	26:19	Reserved
		Access: RO
		Format: MBZ
	18:0	Gamma Value
		Default Value: 000000000000000000b
		Format: U3.16

PRE_CSC_GAMC_INDEX

PRE_CSC_GAMC_INDEX										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	4A484h-4A487h									
Name:	Pipe Pre CSC Gamma Index									
ShortName:	PRE_CSC_GAMC_INDEX_A									
Reset:	soft									
Address:	4AC84h-4AC87h									
Name:	Pipe Pre CSC Gamma Index									
ShortName:	PRE_CSC_GAMC_INDEX_B									
Reset:	soft									
Address:	4B484h-4B487h									
Name:	Pipe Pre CSC Gamma Index									
ShortName:	PRE_CSC_GAMC_INDEX_C									
Reset:	soft									
Address:	4BC84h-4BC87h									
Name:	Pipe Pre CSC Gamma Index									
ShortName:	PRE_CSC_GAMC_INDEX_D									
Reset:	soft									
DWord	Bit	Description								
0	31:11	Reserved								
		Access: RO								
	Format: MBZ									
	10	Index Auto Increment This field enables the index auto increment. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No Increment</td> <td>Do not automatically increment the index value.</td> </tr> <tr> <td>1b</td> <td>Auto Increment [Default]</td> <td>Increment the index value with each read or write to the data register.</td> </tr> </tbody> </table>	Value	Name	Description	0b	No Increment	Do not automatically increment the index value.	1b	Auto Increment [Default]
Value	Name	Description								
0b	No Increment	Do not automatically increment the index value.								
1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.								
9:8	Reserved									
	Access: RO									
Format: MBZ										
7:6	Reserved									
	Access: RO									
Format: MBZ										

PRE_CSC_GAMC_INDEX

	5:0	Index Value	
		Access:	Write/Read Status
		<p>This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set.</p> <p>When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range.</p> <p>While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.</p>	
		Value	Name
		[0,34]	

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
DWord	Bit	Description
0	31:1	Reserved
		Format: PBC
	0	MI_PREDICATE_RESULT This bit is the result of the last MI_PREDICATE.



Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0241Ch-0241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT
Address:	1841Ch-1841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_POCSUNIT
Address:	2241Ch-2241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT
Address:	1C041Ch-1C041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0
Address:	1C441Ch-1C441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1
Address:	1C841Ch-1C841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT0
Address:	1D041Ch-1D041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT2
Address:	1D441Ch-1D441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT3
Address:	1D841Ch-1D841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT1
Address:	1E041Ch-1E041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT4

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1

Address:	1E441Ch-1E441Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT5		
Address:	1E841Ch-1E841Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT2		
Address:	1F041Ch-1F041Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT6		
Address:	1F441Ch-1F441Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT7		
Address:	1F841Ch-1F841Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT3		
Address:	1A41Ch-1A41Fh		
Name:	Predicate Rendering Data Result 1		
ShortName:	MI_PREDICATE_RESULT_1_CCSUNIT0		
DWord	Bit	Description	
0	31:1	Reserved	
		Format:	PBC
	0	MI_PREDICATE_RESULT_1	
		Description	
		This bit is used to predicate MI_BATCH_BUFFER_START commands in the RCS command stream. Usage Model: MI_MATH command will be used to do some ALU operations over GPR followed by a MI_LOAD_REGISTER_REGISTER to move the result from GPR to MI_PREDICATE_RESULT_1.	



Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	023BCh-023BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT
Address:	183BCh-183BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_POCSUNIT
Address:	223BCh-223BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT
Address:	1C03BCh-1C03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0
Address:	1C43BCh-1C43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1
Address:	1C83BCh-1C83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT0
Address:	1D03BCh-1D03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT2
Address:	1D43BCh-1D43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT3
Address:	1D83BCh-1D83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT1
Address:	1E03BCh-1E03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT4

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

Address:	1E43BCh-1E43BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT5		
Address:	1E83BCh-1E83BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT2		
Address:	1F03BCh-1F03BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT6		
Address:	1F43BCh-1F43BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT7		
Address:	1F83BCh-1F83BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT3		
Address:	1A3BCh-1A3BFh		
Name:	Predicate Rendering Data Result 2		
ShortName:	MI_PREDICATE_RESULT_2_CCSUNIT0		
DWord	Bit	Description	
0	31:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	MI_PREDICATE_RESULT_2 This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command.	
	Value	Name	Description
	0h	[Default]	Indicates GT2 mode and lower slice is disabled.
	1h		Indicates GT3 mode and lower slice is enabled.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
DWord	Bit	Description
0	63:32	MI_PREDICATE_DATA_UDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	MI_PREDICATE_DATA_LDW This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC0 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.



Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
DWord	Bit	Description
0	63:0	MI_PREDICATE_SRC1 This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Preemption Status

PREEMPTION_STATUS - Preemption Status	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	025ACh-025AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_RCSUNIT
Address:	185ACh-185AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_POCSUNIT
Address:	225ACh-225AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_BCSUNIT
Address:	1C05ACh-1C05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT0
Address:	1C45ACh-1C45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT1
Address:	1C85ACh-1C85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT0
Address:	1D05ACh-1D05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT2
Address:	1D45ACh-1D45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT3
Address:	1D85ACh-1D85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT1
Address:	1E05ACh-1E05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT4

PREEMPTION_STATUS - Preemption Status

Address:	1E45ACh-1E45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT5
Address:	1E85ACh-1E85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT2
Address:	1F05ACh-1F05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT6
Address:	1F45ACh-1F45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT7
Address:	1F85ACh-1F85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT3
Address:	1A5ACh-1A5AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_CCSUNIT0

This register captures the context switch status on a context switch and gets saved as part of the context image. This register doesn't get restored on a context restore. For all functional purposes this register must be read or sampled from the context image in memory and must not be sampled live from reading to this register. This register is for HW internal purpose and must not be programmed by SW.

DWord	Bit	Description
0	31:16	Reserved
		Access: RO
		Format: MBZ
	15:13	CS Engine ID This field holds the EngineID of the command streamer on which the context got recently executed.
	12:7	CS Instance ID This field holds the InstanceID of the command streamer on which the context got recently executed.
6:4	6:4	Reserved
		Access: RO
		Format: MBZ
3:2	Context Switch Status This field indicates the preemption boundary and must be inferred based on the value in "Pipeline Selection" field.	

PREEMPTION_STATUS - Preemption Status

Value	Name	Description	Exists If
0h		Command Boundary: Context switched out on a clean command boundary with no work pending from the commands executed.	
1h		Thread Group Boundary: Context got switched out in middle of workload (Media/GPGPU Walker) execution in Media or GPGPU mode of operation. Workload got preempted on a thread group boundary. HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection != 0
1h		Object Boundary: Context got switch out in middle of workload (3DPRIMITIVE) execution in 3D mode of operation. Workload got preempted on an object level boundary. HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection == 0
2h		Mid Thread Boundary: Context got switched out in middle of workload (Media/GPGPU Walker) execution in Media or GPGPU mode of operation. Workload got preempted in middle of thread execution (mid-thread boundary). HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection != 0
3h	Reserved		

1:0	Pipeline Selection	
	Access:	RO
	Format:	U2
	This bit indicates the pipeline select mode (PIPELINE_SELECT) at the time of context switch.	
	Value	Description
	0h	3D mode of operation.
1h	Media mode of operation.	
2h	GPGPU mode of operation.	
3h	Reserved	

PRERESETMessagingRegister

MSG_RESET_PRE_GCP - PRERESETMessagingRegister			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	0866Ch		
PRE RESET Messaging Register for Clocking Unit			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
	29	Request to Prepare for GSC Reset	
		Access:	R/W
		_Custom_GTIReset:	BUS
	Prepare for cgscrst_b Domain Reset (GSC).		
	28:21	Reserved	
		Access:	RO
		Format:	MBZ
20	Request to Prepare for VEBox3 Reset		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
Prepare for cvrst_b Domain Reset (vecs3unit).			
19	Request to Prepare for VEBox2 Reset		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
Prepare for cvrst_b Domain Reset (vecs2unit).			
18	Request to Prepare for VEBox1 Reset		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
Prepare for cvrst_b Domain Reset (vecs1unit).			
17	Request to Prepare for VEBox0 Reset		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
Prepare for cvrst_b Domain Reset (vecs0unit).			
16	Request to Prepare for SFC3 Reset		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
Prepare for csfcrst_b Domain Reset (vecs0unit).			

MSG_RESET_PRE_GCP - PRERESETMessagingRegister

	15	Request to Prepare for SFC2 Reset	Access:	R/W
			_Custom_GTIReset:	BUS
		Prepare for csfcrst_b Domain Reset (vecs0unit).		
	14	Request to Prepare for SFC1 Reset	Access:	R/W
			_Custom_GTIReset:	BUS
		Prepare for csfcrst_b Domain Reset (vecs0unit).		
	13	Request to Prepare for SFC0 Reset	Access:	R/W
			_Custom_GTIReset:	BUS
		Prepare for csfcrst_b Domain Reset (vecs0unit).		
	12	Request to Prepare for Media7 Reset	Access:	R/W
			_Custom_GTIReset:	BUS
		Prepare for cmrst_b Domain Reset (vcs7unit).		
	11	Request to Prepare for Media6 Reset	Access:	R/W
			_Custom_GTIReset:	BUS
		Prepare for cmrst_b Domain Reset (vcs6unit).		
10	Request to Prepare for Media5 Reset	Access:	R/W	
		_Custom_GTIReset:	BUS	
	Prepare for cmrst_b Domain Reset (vcs5unit).			
9	Request to Prepare for Media4 Reset	Access:	R/W	
		_Custom_GTIReset:	BUS	
	Prepare for cmrst_b Domain Reset (vcs4unit).			
8	Request to Prepare for Media3 Reset	Access:	R/W	
		_Custom_GTIReset:	BUS	
	Prepare for cmrst_b Domain Reset (vcs3unit).			
7	Request to Prepare for Media2 Reset	Access:	R/W	
		_Custom_GTIReset:	BUS	
	Prepare for cmrst_b Domain Reset (vcs2unit).			
6	Request to Prepare for Media1 Reset	Access:	R/W	

MSG_RESET_PRE_GCP - PRERESETMessagingRegister

		_Custom_GTIReset:	BUS
		Prepare for cmrst_b Domain Reset (vcs1unit).	
5	Request to Prepare for Media0 Reset		
		Access:	R/W
		_Custom_GTIReset:	BUS
		Prepare for cmrst_b Domain Reset (vcs0unit).	
4	Request to Prepare for Render Reset		
		Access:	R/W
		_Custom_GTIReset:	BUS
		Prepare for crrst_b Domain Reset (csunit).	
3	Reserved		
2	Request to Prepare for Blitter Reset		
		Access:	R/W
		_Custom_GTIReset:	BUS
		Prepare for crblitrst_b Domain Reset (bcsunit).	
1	Request to Prepare for Full Reset		
		Access:	R/W
		_Custom_GTIReset:	BUS
		Prepare for all the soft Domain Reset (csunit).	
0	Request to Prepare for FLR		
		Access:	R/W
		_Custom_GTIReset:	BUS
		Prepare for devrst_b Domain Reset (FLR)	
		Note: All resets except busrst_b are asserted for an FLR.	

Primary Latency Timer

MLT2_0_2_0_PCI - Primary Latency Timer								
Register Space:	PCI: 0/2/0							
Size (in bits):	8							
Address:	0000Dh							
The IGD does not support the programmability of the primary latency timer because it does not perform bursts.								
DWord	Bit	Description						
0	7:0	Primary Latency Timer Count Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Default Value:</td> <td style="text-align: center;">00000000b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> Hardwired to 0s.	Default Value:	00000000b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	00000000b							
Access:	RO							
_Custom_GTIReset:	BUS							

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02318h-0231Fh	
Name:	Primitives Generated By VF	
ShortName:	IA_PRIMITIVES_COUNT_RCSUNIT_BE_GEOMETRY	
Address:	18318h-1831Fh	
Name:	Primitives Generated By VF	
ShortName:	IA_PRIMITIVES_COUNT_POCSUNIT_BE_GEOMETRY	
This register stores the count of primitives generated by VF. This register is part of the context save and restore.		
DWord	Bit	Description
0	63:32	IA Primitives Count Report UDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	IA Primitives Count Report LDW Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

PS_ADAPTIVE_CTRL

PS_ADAPTIVE_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	681A8h-681ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_A
Reset:	soft
Address:	681ACh-681AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_A
Reset:	soft
Address:	682A8h-682ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_A
Reset:	soft
Address:	682ACh-682AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_A
Reset:	soft
Address:	689A8h-689ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_B
Reset:	soft
Address:	689ACh-689AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_B
Reset:	soft
Address:	68AA8h-68AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_B
Reset:	soft
Address:	68AACh-68AAFh

PS_ADAPTIVE_CTRL	
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_B
Reset:	soft
Address:	691A8h-691ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_C
Reset:	soft
Address:	691ACh-691AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_C
Reset:	soft
Address:	692A8h-692ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_C
Reset:	soft
Address:	692ACh-692AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_C
Reset:	soft
Address:	699A8h-699ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_D
Reset:	soft
Address:	699ACh-699AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_D
Reset:	soft
Address:	69AA8h-69AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_D
Reset:	soft
Address:	69AACh-69AAFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_D
Reset:	soft
Programming Notes	

PS_ADAPTIVE_CTRL

Recommended threshold programming:

Threshold 1: 1Eh

Threshold 2: 2Dh

Threshold 3: 3Ch

DWord	Bit	Description
0	31:24	Reserved
		Access: RO
		Format: MBZ
	23:16	Threshold 3 This field specifies the third threshold value used in adaptive filtering.
	15:8	Threshold 2 This field specifies the second threshold value used in adaptive filtering.
7:0	Threshold 1 This field specifies the first threshold value used in adaptive filtering.	



PS_COEF_DATA

PS_COEF_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	6819Ch-6819Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_A
Reset:	soft
Address:	681A4h-681A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_A
Reset:	soft
Address:	6829Ch-6829Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_A
Reset:	soft
Address:	682A4h-682A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_A
Reset:	soft
Address:	6899Ch-6899Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_B
Reset:	soft
Address:	689A4h-689A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_B
Reset:	soft
Address:	68A9Ch-68A9Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_B
Reset:	soft
Address:	68AA4h-68AA7h

PS_COEF_DATA	
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_B
Reset:	soft
Address:	6919Ch-6919Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_C
Reset:	soft
Address:	691A4h-691A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_C
Reset:	soft
Address:	6929Ch-6929Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_C
Reset:	soft
Address:	692A4h-692A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_C
Reset:	soft
Address:	6999Ch-6999Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_D
Reset:	soft
Address:	699A4h-699A7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_D
Reset:	soft
Address:	69A9Ch-69A9Fh
Name:	PS Coefficient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_D
Reset:	soft
Address:	69AA4h-69AA7h
Name:	PS Coefficient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_D
Reset:	soft
These are the coefficient values for scaler.	

PS_COEF_DATA

The scaler coefficient Index indicates the coefficients array location to be accessed through this register. The contents of the coefficient array is uninitialized until Software loads the array (i.e. the array is not resettable). Use of the coefficient array or reading from the coefficient array before Software has initialized it will result in non-deterministic behavior or read back data.

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description		
0	31:16	Coefficient2 <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td style="text-align: center;">SCALER_COEFFICIENT_FORMAT</td> </tr> </table> Specifies the value for the second coefficient stored in this dword.	Format:	SCALER_COEFFICIENT_FORMAT
	Format:	SCALER_COEFFICIENT_FORMAT		
15:0	Coefficient1 <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Format:</td> <td style="text-align: center;">SCALER_COEFFICIENT_FORMAT</td> </tr> </table> Specifies the value for the first coefficient stored in this dword.	Format:	SCALER_COEFFICIENT_FORMAT	
Format:	SCALER_COEFFICIENT_FORMAT			

PS_COEF_INDEX

PS_COEF_INDEX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	68198h-6819Bh
Name:	PS Coefficient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_A
Reset:	soft
Address:	681A0h-681A3h
Name:	PS Coefficient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_A
Reset:	soft
Address:	68298h-6829Bh
Name:	PS Coefficient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_A
Reset:	soft
Address:	682A0h-682A3h
Name:	PS Coefficient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_A
Reset:	soft
Address:	68998h-6899Bh
Name:	PS Coefficient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_B
Reset:	soft
Address:	689A0h-689A3h
Name:	PS Coefficient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_B
Reset:	soft
Address:	68A98h-68A9Bh
Name:	PS Coefficient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_B
Reset:	soft
Address:	68AA0h-68AA3h
Name:	PS Coefficient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_B



PS_COEF_INDEX

Reset:	soft		
Address:	69198h-6919Bh		
Name:	PS Coefficient Set 0 Index 1		
ShortName:	PS_COEF_SET_0_INDEX_1_C		
Reset:	soft		
Address:	691A0h-691A3h		
Name:	PS Coefficient Set 1 Index 1		
ShortName:	PS_COEF_SET_1_INDEX_1_C		
Reset:	soft		
Address:	69298h-6929Bh		
Name:	PS Coefficient Set 0 Index 1		
ShortName:	PS_COEF_SET_0_INDEX_2_C		
Reset:	soft		
Address:	692A0h-692A3h		
Name:	PS Coefficient Set 1 Index 1		
ShortName:	PS_COEF_SET_1_INDEX_2_C		
Reset:	soft		
Address:	69998h-6999Bh		
Name:	PS Coefficient Set 0 Index 1		
ShortName:	PS_COEF_SET_0_INDEX_1_D		
Reset:	soft		
Address:	699A0h-699A3h		
Name:	PS Coefficient Set 1 Index 1		
ShortName:	PS_COEF_SET_1_INDEX_1_D		
Reset:	soft		
Address:	69A98h-69A9Bh		
Name:	PS Coefficient Set 0 Index 1		
ShortName:	PS_COEF_SET_0_INDEX_2_D		
Reset:	soft		
Address:	69AA0h-69AA3h		
Name:	PS Coefficient Set 1 Index 1		
ShortName:	PS_COEF_SET_1_INDEX_2_D		
Reset:	soft		
DWord	Bit	Description	
0	31:11	Reserved	
		Access:	RO

PS_COEF_INDEX		
	Format:	MBZ
10	Index Auto Increment	
	Access:	R/W
	This field enables the index auto increment.	
	Value	Name
	Description	
0b	No Increment	Do not automatically increment the index value.
1b	Auto Increment [Default]	Increment the index value with each read or write to the data register.
9:6	Reserved	
	Access:	RO
	Format:	MBZ
5:0	Index Value	
	Access:	R/W
	This index controls access to the array of scaler coefficient values.	
	Value	Name
[0,59]		



PS_CTRL

PS_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68180h-68183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_A
Reset:	soft
Address:	68280h-68283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_A
Reset:	soft
Address:	68980h-68983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_B
Reset:	soft
Address:	68A80h-68A83h
Name:	PS Control 1
ShortName:	PS_CTRL_2_B
Reset:	soft
Address:	69180h-69183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_C
Reset:	soft
Address:	69280h-69283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_C
Reset:	soft
Address:	69980h-69983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_D
Reset:	soft
Address:	69A80h-69A83h

PS_CTRL	
Name:	PS Control 1
ShortName:	PS_CTRL_2_D
Reset:	soft
Description	
<p>The pipe scalers are used to scale the output of a display pipe or of a display plane. All pipes have two scalers each.</p> <p>The scaler preserves 8 bits of alpha and 10 bits of each color channel for plane scaling and 12 bits of each color channel for pipe scaling.</p> <p>The scalers can be assigned to any plane (except cursor) output or the output of the display pipe (after blending and color correction, before dithering and color clamping).</p> <p>Downscale usages have scale factor restrictions:</p> <ul style="list-style-type: none"> • All scaler modes support a downscale factor of less than 3.0 in each direction. • Pipe YUV 420 encoding for port output supports Y downscale factor of less than 1.5 in each direction. <p>Beyond the restrictions of the Scaler output fitting within the destination window size, there are effectively no upscale restrictions except for the following: $(\text{Scale Factor}) * 2^{15} \geq 1.0$ Where the Scale Factor = (Source Size) / (Destination Size)</p> <p>The scalers support horizontal source sizes up to 5120 and vertical source sizes up to 4096.</p>	
Programming Notes	
<p>The scalers must not be enabled when the horizontal source sizes are greater than 5120 and the vertical sizes greater than 4320.</p> <p>Driver is responsible for making sure all the plane, pipe, and scaler size registers are programmed appropriately and gets applied atomically to the same frame since hardware does not ensure an atomic update of plane, scaler, and pipe source size registers.</p> <p>When scaling a pipe, the scaler window size and position must fit within the pipe active size. If there is a seam present (i.e. PIPE_SEAM_EXCESS is non-zero), then the pipe's horizontal active size that the scaler sees is the horizontal active size defined within the TRANS_HTOTAL register plus the amount(s) specified within the PIPE_SEAM_EXCESS.</p> <p>Pipe Horizontal Active = Horizontal Active + Left Excess Amount + Right Excess Amount</p> <p>Refer to 'YUV 420 Support' page for scaler restrictions with YUV 420 pipe output.</p>	
Restriction	
<p>Down scaling (scaler input size is larger than scaler window size) can reduce the maximum supported pixel rate for a pipe as well as increase the watermark and data buffer requirements. Refer to the Display Resolution Support page and Watermark Calculations page for detailed calculations.</p> <p>Scaler 1 and 2 must not be both scaling the same plane output.</p> <p>When scaling a pipe, the scaler window size and position must fit within the pipe active size.</p> <p>When scaling a plane, the plane position must be programmed to 0 and the scaler window size and position must fit within the pipe source size.</p> <p>When scaling is enabled, the scaler input width should be a minimum of 8 pixels and the height should be minimum of 8 scanlines.</p>	

PS_CTRL

When the plane scaling is used with YUV 420 planar formats, the height should be a minimum of 16 scanlines. When using down scaling (scaler input size is larger than scaler output size) the maximum supported pixel rate will be reduced by the down scale amount.

DWord	Bit	Description																	
0	31	<p>Enable Scaler This field enables the scaler.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable											
	Value	Name																	
	0b	Disable																	
	1b	Enable																	
	30	Reserved																	
	29	<p>Scaler Mode The Planar mode must be used when non-HDR capable planes are using YUV 420 planar surface formats. In this configuration, the scaler takes care of both the chroma upsampling and scaling. The Planar mode must not be used for the HDR capable planes. They have dedicated chroma upsamplers and only use the scaler in Normal mode for scaling.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Normal</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Planar</td> </tr> </tbody> </table>	Value	Name	0b	Normal	1b	Planar											
	Value	Name																	
	0b	Normal																	
	1b	Planar																	
	28	<p>Adaptive Filtering This field enables the scaler adaptive vertical and horizontal filtering. When adaptive filtering is enabled, the adaptive threshold values must be programmed in the PS_ADAPTIVE_CTRL register and the Filter Set Select bits should be programmed.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0h	Disable	1h	Enable											
Value	Name																		
0h	Disable																		
1h	Enable																		
27:25	<p>Scaler Binding This field selects the where the scaling operation is done. When scaling a pipe, the pipe source size specifies the input size to the scaler. When scaling a plane, the PLANE_SIZE specifies the input size to the scaler. Any border around a scaled plane window will become transparent at the plane blender.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td style="text-align: center;">Pipe Scaler</td> </tr> <tr> <td style="text-align: center;">001b</td> <td style="text-align: center;">Plane 1 Scaler</td> </tr> <tr> <td style="text-align: center;">010b</td> <td style="text-align: center;">Plane 2 Scaler</td> </tr> <tr> <td style="text-align: center;">011b</td> <td style="text-align: center;">Plane 3 Scaler</td> </tr> <tr> <td style="text-align: center;">100b</td> <td style="text-align: center;">Plane 4 Scaler</td> </tr> <tr> <td style="text-align: center;">101b</td> <td style="text-align: center;">Plane 5 Scaler</td> </tr> <tr> <td style="text-align: center;">110b</td> <td style="text-align: center;">Plane 6 Scaler</td> </tr> <tr> <td style="text-align: center;">111b</td> <td style="text-align: center;">Plane 7 Scaler</td> </tr> </tbody> </table>	Value	Name	000b	Pipe Scaler	001b	Plane 1 Scaler	010b	Plane 2 Scaler	011b	Plane 3 Scaler	100b	Plane 4 Scaler	101b	Plane 5 Scaler	110b	Plane 6 Scaler	111b	Plane 7 Scaler
Value	Name																		
000b	Pipe Scaler																		
001b	Plane 1 Scaler																		
010b	Plane 2 Scaler																		
011b	Plane 3 Scaler																		
100b	Plane 4 Scaler																		
101b	Plane 5 Scaler																		
110b	Plane 6 Scaler																		
111b	Plane 7 Scaler																		

PS_CTRL

Programming Notes												
When plane scaling is enabled on planes 1 through 3, make sure that the <i>PLANE_CUS_CTL.Plane Scaling Enabled</i> (bit 30) is programmed correctly.												
Restriction												
The scaler input size should be at least 8 scanlines. Plane/Pipe scaling is not compatible with interlaced fetch mode. Plane up and down scaling is not compatible with keying. Keying can be enabled with 1:1 plane scaling. Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, or any pixel values less than 0 or greater than 1.												
24:23	FILTER SELECT This field selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1. In the programmed mode, the filter coefficients must be programmed using the PS_COEF_INDEX and PS_COEF_DATA registers and the Filter Set Select bits should be programmed.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Medium</td> </tr> <tr> <td>01b</td> <td>Programmed</td> </tr> <tr> <td>10b</td> <td>Edge Enhance</td> </tr> <tr> <td>11b</td> <td>Bilinear</td> </tr> </tbody> </table>			Value	Name	00b	Medium	01b	Programmed	10b	Edge Enhance	11b	Bilinear
Value	Name											
00b	Medium											
01b	Programmed											
10b	Edge Enhance											
11b	Bilinear											
22	ADAPTIVE FILTER SELECT This field selects the filter coefficients used for adaptive filtering. The field is ignored when adaptive filtering is not enabled.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th style="width: 70%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Medium</td> </tr> <tr> <td>1b</td> <td>Edge Enhance</td> </tr> </tbody> </table>			Value	Name	0b	Medium	1b	Edge Enhance				
Value	Name											
0b	Medium											
1b	Edge Enhance											
21	Pipe Scaler Location This field selects where the pipe scaling is done in the pipe.											
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>After Output CSC</td> <td>This is a non-linear tap point</td> </tr> <tr> <td>1b</td> <td>After CSC</td> <td>This is a linear tap point</td> </tr> </tbody> </table>			Value	Name	Description	0b	After Output CSC	This is a non-linear tap point	1b	After CSC	This is a linear tap point	
Value	Name	Description										
0b	After Output CSC	This is a non-linear tap point										
1b	After CSC	This is a linear tap point										
Restriction The HDR Mode cannot be enabled for the Pipe(PIPE_MISC[23] = 0), when the Scaler is bound to the linear tap point												
20	Reserved											

PS_CTRL							
19	Reserved						
18	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
17	Reserved						
16	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
15	Reserved						
14	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
13:12	Reserved						
11:10	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
9	Allow Double Buffer Update Disable						
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field controls whether double buffer updates are allowed to be disabled for this scaler. The DOUBLE_BUFFER_CTL register can be configured to globally disable double buffer updates for resources that allow them to be disabled.</p>	Access:	R/W				
	Access:	R/W					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Allowed</td> </tr> <tr> <td>1b</td> <td>Allowed [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Not Allowed	1b	Allowed [Default]
Value	Name						
0b	Not Allowed						
1b	Allowed [Default]						
8	Reserved						
7:5	Scaler Binding Y						
	<p>This field selects where the planar YUV420 Y plane scaling operation is done. This field is ignored if planar YUV420 plane scaling is not used.</p> <p>This field is used only for planes 4-7 when the plane scaler is used for chroma upsampling. Planes 1-3 must use the dedicated chroma up sampler (programmed in PLANE_CUS_CTL) for YUV 444 up conversion.</p>						
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>110b</td> <td>Plane 6 Scaler</td> </tr> <tr> <td>111b</td> <td>Plane 7 Scaler</td> </tr> </tbody> </table>	Value	Name	110b	Plane 6 Scaler	111b	Plane 7 Scaler
	Value	Name					
	110b	Plane 6 Scaler					
111b	Plane 7 Scaler						
	<p style="text-align: center;">Restriction</p> <p>The scaler input size should be at least 16 scanlines.</p>						

PS_CTRL							
4	<p>Y Vert Filter Set Sel</p> <p>This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component vertical filter when filtering YUV planar formats. This field is ignored with other formats.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Set 0 [Default]</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Set 1</td> </tr> </tbody> </table>	Value	Name	0b	Set 0 [Default]	1b	Set 1
Value	Name						
0b	Set 0 [Default]						
1b	Set 1						
3	<p>Y Horz Filter Set Sel</p> <p>This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component horizontal filter when filtering YUV hybrid planar formats. This field is ignored with other formats.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Set 0 [Default]</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Set 1</td> </tr> </tbody> </table>	Value	Name	0b	Set 0 [Default]	1b	Set 1
Value	Name						
0b	Set 0 [Default]						
1b	Set 1						
2	<p>UV Vert Filter Set Sel</p> <p>This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component vertical filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the vertical filter.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Set 0 [Default]</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Set 1</td> </tr> </tbody> </table>	Value	Name	0b	Set 0 [Default]	1b	Set 1
Value	Name						
0b	Set 0 [Default]						
1b	Set 1						
1	<p>UV Horz Filter Set Sel</p> <p>This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component horizontal filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the horizontal filter.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Set 0 [Default]</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Set 1</td> </tr> </tbody> </table>	Value	Name	0b	Set 0 [Default]	1b	Set 1
Value	Name						
0b	Set 0 [Default]						
1b	Set 1						
0	<p>Reserved</p> <table border="1"> <tbody> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						



PS_ECC_STAT

PS_ECC_STAT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	681D0h-681D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_A
Reset:	soft
Address:	682D0h-682D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_A
Reset:	soft
Address:	689D0h-689D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_B
Reset:	soft
Address:	68AD0h-68AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_B
Reset:	soft
Address:	691D0h-691D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_C
Reset:	soft
Address:	692D0h-692D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_C
Reset:	soft
Address:	699D0h-699D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_D
Reset:	soft
Address:	69AD0h-69AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_D

PS_ECC_STAT		
Reset:		soft
<p>Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.</p>		
DWord	Bit	Description
0	31:17	Reserved
		Access: RO
		Format: MBZ
	16	Double Error Detected
	15:1	Reserved
		Access: RO
Format: MBZ		
0	Single Error Detected	



PS_HPHASE

PS_HPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	68194h-68197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_A
Reset:	soft
Address:	68294h-68297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_A
Reset:	soft
Address:	68994h-68997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_B
Reset:	soft
Address:	68A94h-68A97h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_B
Reset:	soft
Address:	69194h-69197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_C
Reset:	soft
Address:	69294h-69297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_C
Reset:	soft
Address:	69994h-69997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_D
Reset:	soft
Address:	69A94h-69A97h

PS_HPHASE								
Name:	PS Horizontal Phase 1							
ShortName:	PS_HPHASE_2_D							
Reset:	soft							
Description								
<p>This register programs the scaler horizontal filtering initial phase. The initial phase within the -0.5 to 1.5 range is supported. Refer to PS_VPHASE for programming details.</p> <p>The programming of this register is ignored by the pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate horizontal phase when encoding the YUV420 format.</p>								
DWord	Bit	Description						
0	31:30	<p>Y Initial HPhase Int</p> <p>This field specifies the integer part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.</p>						
	29:17	<p>Y Initial HPhase Frac</p> <p>This field specifies the most significant 13 bits of the fractional part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^{13}. This field is ignored for non-YUV420 pixel formats.</p>						
16		<p>Y Initial HPhase Trip</p> <p>This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y horizontal filtering. This field is ignored for non-YUV420 pixel formats.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	1b	Enable	0b	Disable
		Value	Name					
		1b	Enable					
0b	Disable							
15:14	<p>UV or RGB Initial HPhase Int</p> <p>This field specifies the integer part of the UV or RGB horizontal filtering initial phase.</p>							
13:1	<p>UV or RGB Initial HPhase Frac</p> <p>This field specifies the most significant 13 bits of the fractional part of the UV or RGB horizontal filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^{13}.</p>							
0		<p>UV or RGB Initial HPhase Trip</p> <p>This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB horizontal filtering.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	1b	Enable	0b	Disable
		Value	Name					
		1b	Enable					
0b	Disable							



PS_HSCALE

PS_HSCALE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	68190h-68193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_A
Reset:	soft
Address:	68290h-68293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_A
Reset:	soft
Address:	68990h-68993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_B
Reset:	soft
Address:	68A90h-68A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_B
Reset:	soft
Address:	69190h-69193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_C
Reset:	soft
Address:	69290h-69293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_C
Reset:	soft
Address:	69990h-69993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_D
Reset:	soft
Address:	69A90h-69A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_D

PS_HSCALE		
Reset:		soft
DWord	Bit	Description
0	31:18	Reserved
		Access: RO
		Format: MBZ
	17:15	HScale Int
		Access: RO This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	HScale Frac
Access: RO This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int((((src width/dest width)-HSCALE_INT) * 2 ¹⁵) + 0.5)		



PS_PROG_HSCALE

PS_PROG_HSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68168h-6816Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_A
Reset:	soft
Address:	68268h-6826Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_A
Reset:	soft
Address:	68968h-6896Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_B
Reset:	soft
Address:	68A68h-68A6Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_B
Reset:	soft
Address:	69168h-6916Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_C
Reset:	soft
Address:	69268h-6926Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_C
Reset:	soft
Address:	69968h-6996Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_D
Reset:	soft
Address:	69A68h-69A6Bh

PS_PROG_HSCALE		
Name:	PS Programmed Horizontal Scale 1	
ShortName:	PS_PROG_HSCALE_2_D	
Reset:	soft	
This register is used to specify the horizontal scale factor when Programmable Scale Factor is enabled.		
DWord	Bit	Description
0	31:18	Reserved
		Access: RO
		Format: MBZ
	17:15	HScale Int This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. $HSCALE_INT = \text{int}(\text{src width}/\text{dest width})$
14:0	HScale Frac This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. $HSCALE_FRAC = \text{int}(((\text{src width}/\text{dest width}) - HSCALE_INT) * 2^{15})$	



PS_PROG_VSCALE

PS_PROG_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68164h-68167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_A
Reset:	soft
Address:	68264h-68267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_A
Reset:	soft
Address:	68964h-68967h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_B
Reset:	soft
Address:	68A64h-68A67h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_B
Reset:	soft
Address:	69164h-69167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_C
Reset:	soft
Address:	69264h-69267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_C
Reset:	soft
Address:	69964h-69967h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_D
Reset:	soft
Address:	69A64h-69A67h

PS_PROG_VSCALE		
Name:	PS Programmed Vertical Scale 1	
ShortName:	PS_PROG_VSCALE_2_D	
Reset:	soft	
This register is used to specify the vertical scale factor when Programmable Scale Factor is enabled.		
DWord	Bit	Description
0	31:18	Reserved
		Access: RO
		Format: MBZ
	17:15	VScale Int This field gives the integer part of the vertical scale factor. $VSCALE_INT = \text{int}(\text{src height}/(\text{interlace} \times \text{dest height}))$ Interlace = 1/2 in interlace modes, 1 in progressive modes.
14:0	VScale Frac This field gives the fractional part of the vertical scale factor. $VSCALE_FRAC = \text{int}((\text{src height}/(\text{interlace} \times \text{dest height}) - VSCALE_INT) \times 2^{15})$ Interlace = 1/2 in interlace modes, 1 in progressive modes.	



PS_PWR_GATE

PS_PWR_GATE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68160h-68163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_A
Reset:	soft
Address:	68260h-68263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_A
Reset:	soft
Address:	68960h-68963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_B
Reset:	soft
Address:	68A60h-68A63h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_B
Reset:	soft
Address:	69160h-69163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_C
Reset:	soft
Address:	69260h-69263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_C
Reset:	soft
Address:	69960h-69963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_D
Reset:	soft
Address:	69A60h-69A63h

PS_PWR_GATE			
Name: Power Gate Control 1			
ShortName: PS_PWR_GATE_2_D			
Reset: soft			
DWord	Bit	Description	
0	31	Reserved	
	30	Reserved	
	Access:		RO
	Format:		MBZ
	29:6	Reserved	
	Access:		RO
	Format:		MBZ
	5	Dynamic Pwr Gate Disable Disables the dynamic power gate of unused EBB's when processing low resolution source images.	
	Value		Name
	0b		Do Not Disable [Default]
1b		Disable	
4:3	Reserved		
2	Reserved		
Access:		RO	
Format:		MBZ	
1:0	Reserved		



PS_VPHASE

PS_VPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68188h-6818Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_A
Reset:	soft
Address:	68288h-6828Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_A
Reset:	soft
Address:	68988h-6898Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_B
Reset:	soft
Address:	68A88h-68A8Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_B
Reset:	soft
Address:	69188h-6918Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_C
Reset:	soft
Address:	69288h-6928Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_C
Reset:	soft
Address:	69988h-6998Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_D
Reset:	soft
Address:	69A88h-69A8Bh

PS_VPHASE

Name: PS Vertical Phase 1
 ShortName: PS_VPHASE_2_D
 Reset: soft

Description

This register programs the scaler vertical filtering initial phase. The programming of this register is ignored in the pipe scaler PF/ID fetch mode, and the pipe scaler is responsible for applying the appropriate vertical phase to the proper frame when interlacing.

The initial phase within the -0.5 to 1.5 range is supported.

Programming +ve initial phase:

- Initial Phase Trip = 1b
- Initial Phase Int = Desired Initial Phase Int
- Initial Phase Frac = Desired Initial Phase Frac

Programming -ve initial phase:

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - Desired Initial Phase Frac

For example, -0.25 initial phase should be programmed as

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - 0.25 = 0.75

The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios (chroma being filtered to the center of the pixel).

YUV 420 Chroma Siting	H Phase	V Phase	Programmed H Initial Phase	Programmed H Initial Trip	Programmed V Initial Phase	Programmed V Initial Trip
Top Left	0.25	0.25	0.25	1	0.25	1
Bottom Right (MPEG-1)	-0.25	-0.25	0.75	0	0.75	0
Bottom Center (MPEG-2)	0	-0.25	0	0	0.75	0

The programming of this register is ignored by a pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate vertical phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	Y Initial VPhase Int This field specifies the integer part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planarformats. This field is ignored for non-YUV420 pixel formats.

PS_VPHASE

29:17	<p>Y Initial VPhase Frac</p> <p>This field specifies the most significant 13 bits of the fractional part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^{13}. This field is ignored for non-YUV420 pixel formats.</p>						
16	<p>Y Initial VPhase Trip</p> <p>This field specifies the whether the initial trip, that may occur while applying the initial phase, is used in Y vertical filtering. This field is ignored for non-YUV420 pixel formats.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>Used</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>Not Used</td> </tr> </tbody> </table>	Value	Name	1b	Used	0b	Not Used
Value	Name						
1b	Used						
0b	Not Used						
15:14	<p>UV or RGB Initial VPhase Int</p> <p>This field specifies the integer part of the UV or RGB vertical filtering initial phase.</p>						
13:1	<p>UV or RGB Initial VPhase Frac</p> <p>This field specifies the most significant 13 bits of the fractional part of the UV or RGB vertical filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^{13}.</p>						
0	<p>UV or RGB Initial VPhase Trip</p> <p>This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB vertical filtering.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>Used</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>Not Used</td> </tr> </tbody> </table>	Value	Name	1b	Used	0b	Not Used
Value	Name						
1b	Used						
0b	Not Used						

PS_VSCALE

PS_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	68184h-68187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_A
Reset:	soft
Address:	68284h-68287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_A
Reset:	soft
Address:	68984h-68987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_B
Reset:	soft
Address:	68A84h-68A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_B
Reset:	soft
Address:	69184h-69187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_C
Reset:	soft
Address:	69284h-69287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_C
Reset:	soft
Address:	69984h-69987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_D
Reset:	soft
Address:	69A84h-69A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_D

PS_VSCALE		
Reset:		soft
DWord	Bit	Description
0	31:18	Reserved
		Access: RO
		Format: MBZ
	17:15	VScale Int
		Access: RO This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	VScale Frac
Access: RO This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int(((src height/(interlace x dest height)-VSCALE_INT) * 2 ¹⁵) + 0.5) Interlace = 1/2 in interlace modes, 1 in progressive modes.		

PS_WIN_POS

PS_WIN_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68170h-68173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_A
Reset:	soft
Address:	68270h-68273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_A
Reset:	soft
Address:	68970h-68973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_B
Reset:	soft
Address:	68A70h-68A73h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_B
Reset:	soft
Address:	69170h-69173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_C
Reset:	soft
Address:	69270h-69273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_C
Reset:	soft
Address:	69970h-69973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_D
Reset:	soft
Address:	69A70h-69A73h

PS_WIN_POS					
Name:	PS Window Position 1				
ShortName:	PS_WIN_POS_2_D				
Reset:	soft				
Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).					
Restriction					
When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size \geq PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size \geq PS window position + PS window size.					
DWord	Bit	Description			
0	31:29	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
28:16	XPOS				
	<p>This field specifies the horizontal coordinate in pixels of the upper left most pixel of the scaled output window.</p> <p>Restriction : This field must be even when the scaler is delivering YUV420 format for HDMI output.</p>				
15:13	Reserved				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
12:0	YPOS				
	<p>This field specifies the vertical coordinate in lines of the upper left most pixel of the scaled output window.</p>				
	<table border="1" style="width: 100%;"> <tr> <th style="text-align: center;">Restriction</th> </tr> <tr> <td>Bit 0 must be zero for interlaced modes.</td> </tr> <tr> <td>This field must be even when the scaler is delivering YUV420 format for HDMI output.</td> </tr> </table>	Restriction	Bit 0 must be zero for interlaced modes.	This field must be even when the scaler is delivering YUV420 format for HDMI output.	
Restriction					
Bit 0 must be zero for interlaced modes.					
This field must be even when the scaler is delivering YUV420 format for HDMI output.					

PS_WIN_SZ

PS_WIN_SZ	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank	
Address:	68174h-68177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_A
Reset:	soft
Address:	68274h-68277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_A
Reset:	soft
Address:	68974h-68977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_B
Reset:	soft
Address:	68A74h-68A77h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_B
Reset:	soft
Address:	69174h-69177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_C
Reset:	soft
Address:	69274h-69277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_C
Reset:	soft
Address:	69974h-69977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_D
Reset:	soft
Address:	69A74h-69A77h
Name:	PS Window Size 1

PS_WIN_SZ					
ShortName: PS_WIN_SZ_2_D					
Reset: soft					
<p>This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels.</p> <p>Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.</p>					
Restriction					
<p>When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size \geq PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size \geq PS window position + PS window size.</p>					
DWord	Bit	Description			
0	31:30	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
29:16	XSIZE				
	<p>This field specifies the horizontal size in pixels of the scaled output window.</p> <p>Restriction : When the pipe scalar is configured to output YUV 420, the X size must be even.</p>				
15:13	Reserved				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
12:0	YSIZE				
	<p>This field specifies the vertical size in scan lines of the scaled output window.</p> <p>Restriction : Bit 0 must be zero for interlaced modes.</p>				
	<table border="1" style="width: 100%;"> <tr> <th style="text-align: center;">Restriction</th> </tr> <tr> <td>When the pipe scalar is configured to output YUV 420, the Y size must be even.</td> </tr> </table>	Restriction	When the pipe scalar is configured to output YUV 420, the Y size must be even.		
Restriction					
When the pipe scalar is configured to output YUV 420, the Y size must be even.					

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02350h	
<p>This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.</p>		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	022D8h	
Name:	PS Depth Count for Slice0	
ShortName:	PS_DEPTH_COUNT_SLICE0	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	022F8h	
Name:	PS Depth Count for Slice1	
ShortName:	PS_DEPTH_COUNT_SLICE1	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02450h	
Name:	PS Depth Count for Slice2	
ShortName:	PS_DEPTH_COUNT_SLICE2	
<p>This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.</p>		
DWord	Bit	Description
0..1	63:32	<p>Depth Count UDW</p> <p>This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>
	31:0	<p>Depth Count LDW</p> <p>This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.</p>

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02460h	
Name:	PS Depth Count for Slice3	
ShortName:	PS_DEPTH_COUNT_SLICE3	
This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice4

PS_DEPTH_COUNT_SLICE4 - PS Depth Count for Slice4		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02470h	
Name:	PS Depth Count for Slice4	
ShortName:	PS_DEPTH_COUNT_SLICE4	
This register stores the value of the count of pixels that have passed the depth test in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice5

PS_DEPTH_COUNT_SLICE5 - PS Depth Count for Slice5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	024A8h	
Name:	PS Depth Count for Slice5	
ShortName:	PS_DEPTH_COUNT_SLICE5	
This register stores the value of the count of pixels that have passed the depth test in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice6

PS_DEPTH_COUNT_SLICE6 - PS Depth Count for Slice6		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	025B0h	
Name:	PS Depth Count for Slice6	
ShortName:	PS_DEPTH_COUNT_SLICE6	
This register stores the value of the count of pixels that have passed the depth test in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice7

PS_DEPTH_COUNT_SLICE7 - PS Depth Count for Slice7		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	025B8h	
Name:	PS Depth Count for Slice7	
ShortName:	PS_DEPTH_COUNT_SLICE7	
This register stores the value of the count of pixels that have passed the depth test in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02348h	
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	022C8h	
Name:	PS Invocation Count for Slice0	
ShortName:	PS_INVOCATION_COUNT_SLICE0	
<p>This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	022F0h	
Name:	PS Invocation Count for Slice1	
ShortName:	PS_INVOCATION_COUNT_SLICE1	
<p>This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).</p>		
DWord	Bit	Description
0..1	63:32	<p>PS Invocation Count UDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>
	31:0	<p>PS Invocation Count LDW</p> <p>Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.</p>

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02448h	
Name:	PS Invocation Count for Slice2	
ShortName:	PS_INVOCATION_COUNT_SLICE2	
This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02458h	
Name:	PS Invocation Count for Slice3	
ShortName:	PS_INVOCATION_COUNT_SLICE3	
This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice4

PS_INVOCATION_COUNT_SLICE4 - PS Invocation Count for Slice4		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02468h	
Name:	PS Invocation Count for Slice4	
ShortName:	PS_INVOCATION_COUNT_SLICE4	
This register stores the value of the count of pixels that get shaded in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice5

PS_INVOCATION_COUNT_SLICE5 - PS Invocation Count for Slice5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	024A0h	
Name:	PS Invocation Count for Slice5	
ShortName:	PS_INVOCATION_COUNT_SLICE5	
This register stores the value of the count of pixels that get shaded in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice6

PS_INVOCATION_COUNT_SLICE6 - PS Invocation Count for Slice6		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	025D0h	
Name:	PS Invocation Count for Slice6	
ShortName:	PS_INVOCATION_COUNT_SLICE6	
This register stores the value of the count of pixels that get shaded in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice7

PS_INVOCATION_COUNT_SLICE7 - PS Invocation Count for Slice7		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	025D8h	
Name:	PS Invocation Count for Slice7	
ShortName:	PS_INVOCATION_COUNT_SLICE7	
This register stores the value of the count of pixels that get shaded in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.		
DWord	Bit	Description
0..1	63:32	PS Invocation Count UDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	PS Invocation Count LDW Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PSR_EVENT

PSR_EVENT			
Register Space:	MMIO: 0/2/0		
Access:	R/WC		
Size (in bits):	32		
Address:	60848h-6084Bh		
Name:	Transcoder PSR Event		
ShortName:	PSR_EVENT_A		
Reset:	soft		
Address:	61848h-6184Bh		
Name:	Transcoder PSR Event		
ShortName:	PSR_EVENT_B		
Reset:	soft		
Address:	62848h-6284Bh		
Name:	Transcoder PSR Event		
ShortName:	PSR_EVENT_C		
Reset:	soft		
Address:	63848h-6384Bh		
Name:	Transcoder PSR Event		
ShortName:	PSR_EVENT_D		
Reset:	soft		
<p>This register captures the event that caused an exit from PSR or PSR2. The exit events will be set by hardware. Software will need to clear these events.</p>			
DWord	Bit	Description	
0	31:18	Reserved	
		Access:	RO
		Format:	MBZ
	17	PSR2 watch dog timer expire	
		Access:	R/WC
		This is a sticky bit which is set when the PSR2 watch dog timer expires, causing PSR exit. Clear by writing with a 1.	
		Value	Name
		0b	Condition Not Detected
	1b	Condition Detected	
	16	PSR2 Disable	
Access:		R/WC	
This is a sticky bit which is set when the PSR2 is disabled, causing PSR exit. Clear by writing with			

PSR_EVENT

PSR_EVENT									
	<p>a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected		
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
15	<p>Selective Update Dirty FIFO Underrun</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when the selective update dirty/clean FIFO Underruns, causing PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
14	<p>Selective Update CRC FIFO Underrun</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when the selective update CRC FIFO Underruns, causing PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
13	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								
12	<p>Graphics Reset</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a graphics reset causes PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
11	<p>PCH Interrupt</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a PCH Interrupt causes PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
10	<p>Memory Up</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a PCU memup up event causes PSR exit. Clear by writing with a 1.</p>	Access:	R/WC						
Access:	R/WC								

PSR_EVENT									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected		
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
9	<p>Front Buffer Modify</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a front buffer modify causes PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
8	<p>Watch dog timer expire</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when the PSR watch dog timer expires, causing PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
7	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								
6	<p>Pipe Registers Update</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a display pipe register update causes PSR exit. Clear by writing with a 1.</p>	Access:	R/WC						
Access:	R/WC								
5	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								
4	<p>Reserved</p>								
3	<p>KVMR session enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when a KVMR session is enabled, causing PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
2	<p>VBI enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when vblank or vsync interrupt is enabled, causing PSR exit. Clear</p>	Access:	R/WC						
Access:	R/WC								

PSR_EVENT									
	<p>by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected		
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
1	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								
0	<p>SRD disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set when SRD enable is cleared, causing PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								

PSR_IIR

PSR_IIR			
Register Space:	MMIO: 0/2/0		
Access:	R/WC		
Size (in bits):	32		
Address:	60818h-6081Bh		
Name:	Transcoder PSR Interrupt Identity		
ShortName:	PSR_IIR_A		
Reset:	soft		
Address:	61818h-6181Bh		
Name:	Transcoder PSR Interrupt Identity		
ShortName:	PSR_IIR_B		
Reset:	soft		
Address:	62818h-6281Bh		
Name:	Transcoder PSR Interrupt Identity		
ShortName:	PSR_IIR_C		
Reset:	soft		
Address:	63818h-6381Bh		
Name:	Transcoder PSR Interrupt Identity		
ShortName:	PSR_IIR_D		
Reset:	soft		
<p>This register holds the persistent values of the PSR interrupt bits which are unmasked by PSR_IMR. Bits set in this register will propagate to the PSR/SRD interrupt in the Display Engine Miscellaneous Interrupts.</p>			
DWord	Bit	Description	
0	31:4	Reserved	
		Access:	RO
		Format:	MBZ
	3	Push Done	
		Access:	R/WC
		This is a sticky bit which is set after double buffer update or Push done. After this interrupt, Logic is ready to receive another push frame indication. Clear by writing with a 1.	
		Value	Name
		0b	Condition Not Detected
	1b	Condition Detected	
	2	PSR Aux Error	
Access:		R/WC	
This is a sticky bit which is set on the rising edge of the PSR Aux error (receive error or timeout)			

PSR_IIR									
	<p>indication. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected		
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
1	<p>PSR Exit</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set on the first blank start after PSR exit. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Condition Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Condition Not Detected								
1b	Condition Detected								
0	<p>PSR PreWarn</p> <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This is a sticky bit which is set two display frames prior to entering PSR. Clear by writing with a 1.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Not Detected	1b	Condition Detected
Access:	R/WC								
Value	Name								
0b	Not Detected								
1b	Condition Detected								

PSR_IMR

PSR_IMR				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	60814h-60817h			
Name:	Transcoder PSR Interrupt Mask			
ShortName:	PSR_IMR_A			
Reset:	soft			
Address:	61814h-61817h			
Name:	Transcoder PSR Interrupt Mask			
ShortName:	PSR_IMR_B			
Reset:	soft			
Address:	62814h-62817h			
Name:	Transcoder PSR Interrupt Mask			
ShortName:	PSR_IMR_C			
Reset:	soft			
Address:	63814h-63817h			
Name:	Transcoder PSR Interrupt Mask			
ShortName:	PSR_IMR_D			
Reset:	soft			
This register contains a bit mask which selects the PSR events that will be reported in the PSR_IIR.				
DWord	Bit	Description		
0	31:4	Reserved		
		Access:	RO	
		Format:	MBZ	
	3	3	Mask Push Done	
			Value	Name
			0b	Not Masked
			1b	Masked [Default]
	2	2	Mask PSR Aux Error	
			Value	Name
			0b	Not Masked
			1b	Masked [Default]

PSR_IMR								
	1	Mask PSR Exit						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Not Masked	1b	Masked [Default]
		Value	Name					
	0b	Not Masked						
	1b	Masked [Default]						
	0	Mask PSR PreWarn						
	0	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Not Masked	1b	Masked [Default]
Value		Name						
0b		Not Masked						
1b	Masked [Default]							
0								

PSR_MASK

PSR_MASK														
Register Space:	MMIO: 0/2/0													
Access:	R/W													
Size (in bits):	32													
Address:	60860h-60863h													
Name:	Transcoder PSR Event Mask													
ShortName:	PSR_MASK_A													
Reset:	soft													
Address:	61860h-61863h													
Name:	Transcoder PSR Event Mask													
ShortName:	PSR_MASK_B													
Reset:	soft													
Address:	62860h-62863h													
Name:	Transcoder PSR Event Mask													
ShortName:	PSR_MASK_C													
Reset:	soft													
Address:	63860h-63863h													
Name:	Transcoder PSR Event Mask													
ShortName:	PSR_MASK_D													
Reset:	soft													
Some of the masking is controlled here and some in the PIPE_MISC register.														
Restriction														
Only bit 30 (Idle Frame Override) can be changed while PSR or PSR2 is enabled. The other fields must not be changed while PSR or PSR2 is enabled.														
DWord	Bit	Description												
0	31:30	Idle Frame Override This field overrides the entry/exit conditions to force PSR or PSR2 Deep Sleep entry/exit.												
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b,01b</td> <td>No Override</td> <td>Do not override. Use regular entry and exit conditions.</td> </tr> <tr> <td>10b</td> <td>Force Idle Frame</td> <td>Force Idle Frames to force PSR entry or PSR2 Deep Sleep</td> </tr> <tr> <td>11b</td> <td>Force Non-Idle Frame</td> <td>Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep</td> </tr> </tbody> </table>	Value	Name	Description	00b,01b	No Override	Do not override. Use regular entry and exit conditions.	10b	Force Idle Frame	Force Idle Frames to force PSR entry or PSR2 Deep Sleep	11b	Force Non-Idle Frame	Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep
		Value	Name	Description										
		00b,01b	No Override	Do not override. Use regular entry and exit conditions.										
	10b	Force Idle Frame	Force Idle Frames to force PSR entry or PSR2 Deep Sleep											
11b	Force Non-Idle Frame	Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep												
29	Reserved													
	Access:	RO												
	Format:	MBZ												

PSR_MASK

	28	Mask Max Sleep This field controls the mask for the max sleep time event.									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> </tbody> </table>		Value	Name	0b	Not Masked	1b	Masked			
	Value	Name									
	0b	Not Masked									
	1b	Masked									
	27	Mask LPSP This field controls the mask for the low power single pipe event. This field is ignored by transcoder A/B/C.									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> </tbody> </table>		Value	Name	0b	Not masked	1b	Masked			
	Value	Name									
	0b	Not masked									
	1b	Masked									
	26	Mask Memup This field controls the mask for the memory up event.									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> <td></td> </tr> <tr> <td>1b</td> <td>Masked [Default]</td> <td>Masked - will not be considered in PSR idleness tracking (default)</td> </tr> </tbody> </table>		Value	Name	Description	0b	Not Masked		1b	Masked [Default]	Masked - will not be considered in PSR idleness tracking (default)
	Value	Name	Description								
	0b	Not Masked									
	1b	Masked [Default]	Masked - will not be considered in PSR idleness tracking (default)								
	25	Mask Hotplug This field controls the mask for the hotplug event. Not used in PSR2 Deep Sleep entry/exit.									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> </tbody> </table>		Value	Name	0b	Not Masked	1b	Masked			
	Value	Name									
	0b	Not Masked									
	1b	Masked									
	24	Mask FBC Modify This field controls the mask for the FBC front buffer modify event.									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> </tbody> </table>		Value	Name	0b	Not Masked	1b	Masked			
	Value	Name									
	0b	Not Masked									
	1b	Masked									
	23:16	Reserved									
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ					
	Access:	RO									
Format:	MBZ										
15	Exit on Pixel Underrun This field controls the mask for exit on pixel underrun.										
<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked [Default]</td> </tr> </tbody> </table>		Value	Name	0b	Not Masked	1b	Masked [Default]				
Value	Name										
0b	Not Masked										
1b	Masked [Default]										
14:1	Reserved										
<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ						
Access:	RO										
Format:	MBZ										

PSR_MASK								
	0	Global Mask This field is no longer used. The global mask function moved to 0x42084 bit 0.						
		<table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0b</td><td>Not Masked</td></tr><tr><td>1b</td><td>Masked</td></tr></tbody></table>	Value	Name	0b	Not Masked	1b	Masked
Value	Name							
0b	Not Masked							
1b	Masked							



PSR2_CTL

PSR2_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	60900h-60903h							
Name:	PSR2 Control							
ShortName:	PSR2_CTL_A							
Reset:	soft							
Programming Notes								
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.								
Restriction								
PSR needs to be enabled only when at least one plane is enabled.								
PSR2 is limited to 30bpp 10:10:10, even when using the manual tracking mode.								
Only the PSR2 Enable can be changed while PSR2 is enabled. The other fields must not be changed while PSR2 is enabled. Selective Update Tracking Enable must be set before or along with PSR2 enable								
PSR2 is supported for pipe active sizes up to 5120 pixels wide and 3200 lines tall.								
DWord	Bit	Description						
0	31	<p>PSR2 Enable</p> <p>This bit enables Revision 2.0 of the Panel Self Refresh function. Updates will take place at the start of the next vertical blank. The port will send PSR2 VDMs while enabled.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>Clear the register field SRD_CTL [TP2 TP3 Select] before enabling this bit. Do not set the register field SRD_CTL [TP2 TP3 Select] while PSR2 is enabled.</p> <p style="text-align: center;">Restriction</p> <p>PSR2 must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.</p> <p>PSR2 must not be enabled together with Interlacing, Black Frame Insertion (BFI), Compression Mode, or S3D.</p> <p>Disable FBC when PSR2 is enabled.</p>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							

PSR2_CTL											
30	Selective Update Tracking Enable <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td>Double Buffered</td> </tr> <tr> <td>_Custom_Display_DoubleBufferUpdatePoint:</td> <td>Start of vertical blank OR transcoder disabled</td> </tr> </table> <p>This field enables the Selective Update Tracking Mechanism. Updates to this field will take effect at the next vertical blank.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must be enabled anytime before PSR2 Enable. It must be disabled anytime after PSR2 disable.</p>	Access:	Double Buffered	_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR transcoder disabled	Value	Name	0b	Disable	1b	Enable
	Access:	Double Buffered									
	_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR transcoder disabled									
	Value	Name									
	0b	Disable									
	1b	Enable									
	29	Context restore to PSR2 Deep Sleep State This field restores PSR2 into Deep Sleep State <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This bit should only be used with context save restore.</p>	Value	Name	0b	Disable	1b	Enable			
		Value	Name								
		0b	Disable								
		1b	Enable								
28		Block count number This field selects block count number before SU turn on sequence <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>2 blocks</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>3 blocks</td> </tr> </tbody> </table>	Value	Name	0b	2 blocks	1b	3 blocks			
	Value	Name									
	0b	2 blocks									
1b	3 blocks										
27	Aux Frame Sync Enable This field selects whether the frame sync will be sent on Aux channel. <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td>Enable</td> </tr> <tr> <td style="text-align: center;">0b</td> <td>Disable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>Must be programmed to match the panel's requirements.</p>	Value	Name	1b	Enable	0b	Disable				
	Value	Name									
	1b	Enable									
	0b	Disable									
26	Y-coordinate valid This field selects whether PSR2 Y-coordinate valid behaves as per eDP 1.4a <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Include Y-coordinate valid eDP1.4a</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Do not include Y-coordinate valid eDP 1.4</td> </tr> </tbody> </table>	Value	Name	0b	Include Y-coordinate valid eDP1.4a	1b	Do not include Y-coordinate valid eDP 1.4				
	Value	Name									
	0b	Include Y-coordinate valid eDP1.4a									
1b	Do not include Y-coordinate valid eDP 1.4										

PSR2_CTL																					
25	<p>Y-coordinate enable This field selects whether PSR2 VSC packet will include vertical line count.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td>Do not include count</td> </tr> <tr> <td style="text-align: center;">1b</td> <td>Include count</td> </tr> </tbody> </table>	Value	Name	0b	Do not include count	1b	Include count														
Value	Name																				
0b	Do not include count																				
1b	Include count																				
24:20	<p>Max SU Disable Time</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>00000b Disabled</td> </tr> </table> <p>This field is the maximum time to spend in PSR2 Selective update without fetching a full frame. It is programmed in increments of sixty frames. Programming all 1s gives 31x60 frames time.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="text-align: center;">Restriction</th> </tr> <tr> <td>Programming all 0s disable the forced fetch of a full frame in SU.</td> </tr> </table>	Default Value:	00000b Disabled	Restriction	Programming all 0s disable the forced fetch of a full frame in SU.																
Default Value:	00000b Disabled																				
Restriction																					
Programming all 0s disable the forced fetch of a full frame in SU.																					
19	Reserved																				
18	<p>PSR2 RAM power state</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> </table>	Access:	RO																		
Access:	RO																				
17:16	Reserved																				
15:13	<p>IO buffer Wake This field selects the number of lines before the Selective Update Region to wake the IO Buffers.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td>5 lines</td> </tr> <tr> <td style="text-align: center;">001b</td> <td>6 lines</td> </tr> <tr> <td style="text-align: center;">010b</td> <td>7 lines [Default]</td> </tr> <tr> <td style="text-align: center;">011b</td> <td>8 lines</td> </tr> <tr> <td style="text-align: center;">100b</td> <td>9 lines</td> </tr> <tr> <td style="text-align: center;">101b</td> <td>10 lines</td> </tr> <tr> <td style="text-align: center;">110b</td> <td>11 lines</td> </tr> <tr> <td style="text-align: center;">111b</td> <td>12 lines</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="text-align: center;">Restriction</th> </tr> <tr> <td>To program line 9 to 12, block count number bit [28] must be set.</td> </tr> </table>	Value	Name	000b	5 lines	001b	6 lines	010b	7 lines [Default]	011b	8 lines	100b	9 lines	101b	10 lines	110b	11 lines	111b	12 lines	Restriction	To program line 9 to 12, block count number bit [28] must be set.
Value	Name																				
000b	5 lines																				
001b	6 lines																				
010b	7 lines [Default]																				
011b	8 lines																				
100b	9 lines																				
101b	10 lines																				
110b	11 lines																				
111b	12 lines																				
Restriction																					
To program line 9 to 12, block count number bit [28] must be set.																					
12:10	<p>Fast Wake This field selects the number of lines before the Selective Update Region to send the Fast Wake.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td>5 lines</td> </tr> <tr> <td style="text-align: center;">001b</td> <td>6 lines</td> </tr> <tr> <td style="text-align: center;">010b</td> <td>7 lines [Default]</td> </tr> <tr> <td style="text-align: center;">011b</td> <td>8 lines</td> </tr> </tbody> </table>	Value	Name	000b	5 lines	001b	6 lines	010b	7 lines [Default]	011b	8 lines										
Value	Name																				
000b	5 lines																				
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010b	7 lines [Default]																				
011b	8 lines																				

PSR2_CTL											
	<table border="1"> <tr> <td>100b</td> <td>9 lines</td> </tr> <tr> <td>101b</td> <td>10 lines</td> </tr> <tr> <td>110b</td> <td>11 lines</td> </tr> <tr> <td>111b</td> <td>12 lines</td> </tr> </table>	100b	9 lines	101b	10 lines	110b	11 lines	111b	12 lines		
100b	9 lines										
101b	10 lines										
110b	11 lines										
111b	12 lines										
	Restriction To program line 9 to 12, block count number bit [28] must be set.										
9:8	TP2 Time This field selects the TP2 time when training the link on exit from PSR2 DeepSleep (waking). <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>500us</td> </tr> <tr> <td>01b</td> <td>100us</td> </tr> <tr> <td>10b</td> <td>2.5ms</td> </tr> <tr> <td>11b</td> <td>50us</td> </tr> </tbody> </table>	Value	Name	00b	500us	01b	100us	10b	2.5ms	11b	50us
Value	Name										
00b	500us										
01b	100us										
10b	2.5ms										
11b	50us										
7:4	Frames Before SU Entry <table border="1"> <tr> <td>Default Value:</td> <td>0001b 1 Frames Before SU Entry</td> </tr> </table> This field is the number of frames it takes to enter into Selective Update when PSR2 is enabled. Note: HW takes a minimum of 2frames, so '0' and '1' are not valid entries for this field.	Default Value:	0001b 1 Frames Before SU Entry								
Default Value:	0001b 1 Frames Before SU Entry										
3:0	Idle Frames This field is the number of idle frames required before entering PSR2 Deep Sleep. Write to this field doesn't cause a PSR2 exit and frame update. <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Deep Sleep Disabled</td> </tr> <tr> <td>0001b</td> <td>1 idle frame [Default]</td> </tr> </tbody> </table>	Value	Name	0000b	Deep Sleep Disabled	0001b	1 idle frame [Default]				
Value	Name										
0000b	Deep Sleep Disabled										
0001b	1 idle frame [Default]										



PSR2_MAN_TRK_CTL

PSR2_MAN_TRK_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	60910h-60913h							
Name:	PSR2 Manual Tracking Control							
ShortName:	PSR2_MAN_TRK_CTL_A							
Reset:	soft							
Programming Notes								
<p>The frame is divided into blocks of four scan lines each. The blocks are addressed starting from 1 for the first block of the frame and ending with $\text{ROUNDUP}[(\text{TRANS_VTOTAL Vertical Active} + 1) / 4]$ for the last block of the frame.</p> <p>Software must provide the starting and ending block address of the selective update region. The SU Region Start Address is programmed to the first block of the selective update region. The SU Region End Address is programmed to the final block of the selective update region + 1. There can be only one selective update region in a frame.</p> <p>To disable selective update, set the selective update region to the full frame by programming SU Region Start Address to the start of the frame and SU Region End Address to the end of the frame.</p>								
DWord	Bit	Description						
0	31	<p>PSR2 Manual Tracking Enable</p> <p>This bit enables the manual tracking mode for PSR2 Selective Update.</p> <p>Restriction : This field cannot be modified while PSR2_CTL bit [30] is "1". SW must make sure PSR2_CTL bit [30] is disabled before this bit is disabled.</p> <p>Restriction : This bit should not be modified without a modeset.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
30:21	<p>SU Region Start Address</p> <p>This field indicates the starting block address of the selective update region.</p>							
20:11	<p>SU Region End Address</p> <p>This field indicates the ending block address of the selective update region.</p>							
10:4	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </tbody> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							

PSR2_MAN_TRK_CTL

3	<p>SF Single full frame</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W Set</td> </tr> </table> <p>This bit will select for a single a full frame fetch, using the regular plane and cursor registers (not SEL_FETCH registers), and update when Selective Fetch is enabled. It is cleared on vblank. Do not set this bit to 1 if Selective Fetch is not enabled.</p>	Access:	R/W Set				
Access:	R/W Set						
2	<p>SF Continuous full frame</p> <p>This bit will select for full frame fetches, using the regular plane and cursor registers (not SEL_FETCH registers), and updates continuously when Selective Fetch is enabled, until disabled by software. Do not set this bit to 1 if Selective Fetch is not enabled.</p>						
1	<p>SF Partial Frame Enable</p> <p>This field enables the planes to use the SEL_FETCH registers for selective fetch on selective update frames.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						
0	<p>Allow Double Buffer Update Disable</p> <p>This field controls whether double buffer updates are allowed to be disabled for this register.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Not Allowed</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Allowed</td> </tr> </tbody> </table>	Value	Name	0b	Not Allowed	1b	Allowed
Value	Name						
0b	Not Allowed						
1b	Allowed						



PSR2_STATUS

PSR2_STATUS																																												
Register Space:	MMIO: 0/2/0																																											
Access:	RO																																											
Size (in bits):	32																																											
Address:	60940h-60943h																																											
Name:	PSR2 Status																																											
ShortName:	PSR2_STATUS_A																																											
Reset:	soft																																											
DWord	Bit	Description																																										
0	31:28	PSR2 State																																										
		Access: RO																																										
		This field indicates the live state of PSR2																																										
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>IDLE</td> <td>Reset state</td> </tr> <tr> <td>0001b</td> <td>CAPTURE</td> <td>Send capture frame</td> </tr> <tr> <td>0010b</td> <td>CPTURE_FS</td> <td>Fast sleep after capture frame is sent</td> </tr> <tr> <td>0011b</td> <td>SLEEP</td> <td>Selective Update</td> </tr> <tr> <td>0100b</td> <td>BUFON_FW</td> <td>Turn Buffer on and Send Fast wake</td> </tr> <tr> <td>0101b</td> <td>ML_UP</td> <td>Turn Main link up and send SR</td> </tr> <tr> <td>0110b</td> <td>SU_STANDBY</td> <td>Selective update or Standby state</td> </tr> <tr> <td>0111b</td> <td>FAST_SLEEP</td> <td>Send Fast sleep</td> </tr> <tr> <td>1000b</td> <td>DEEP_SLEEP</td> <td>Enter Deep sleep</td> </tr> <tr> <td>1001b</td> <td>BUF_ON</td> <td>Turn ON IO Buffer</td> </tr> <tr> <td>1010b</td> <td>TG_ON</td> <td>Turn ON Timing Generator</td> </tr> <tr> <td>1011b</td> <td>BUFON_FW_2</td> <td>Turn Buffer on and Send Fast wake for 3 Block case</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	0000b	IDLE	Reset state	0001b	CAPTURE	Send capture frame	0010b	CPTURE_FS	Fast sleep after capture frame is sent	0011b	SLEEP	Selective Update	0100b	BUFON_FW	Turn Buffer on and Send Fast wake	0101b	ML_UP	Turn Main link up and send SR	0110b	SU_STANDBY	Selective update or Standby state	0111b	FAST_SLEEP	Send Fast sleep	1000b	DEEP_SLEEP	Enter Deep sleep	1001b	BUF_ON	Turn ON IO Buffer	1010b	TG_ON	Turn ON Timing Generator	1011b	BUFON_FW_2	Turn Buffer on and Send Fast wake for 3 Block case	Others	Reserved	Reserved
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27:26		Link Status																																										
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		This field indicates the live status of the link.																																										
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11b	Reserved	Reserved																																										
25		Reserved																																										
		Access: RO																																										
		Format: MBZ																																										

PSR2_STATUS

24:20	<p>Max Sleep Time Counter</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>This field provides the live status of the sleep time counter.</p>	Access:	RO									
Access:	RO											
19:16	<p>PSR2 Deep Sleep Entry Count</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>The value in this register represents the number of times PSR2 Deep Sleep has been entered. The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.</p>	Access:	RO									
Access:	RO											
15:12	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ							
Access:	RO											
Format:	MBZ											
11:10	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ							
Access:	RO											
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9	<p>PSR2 idle frame indication</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>This bit gets set when DP link goes to sleep state and gets reset on PSR2 exit.</p>	Access:	RO									
Access:	RO											
8	<p>Sending TP2</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p style="text-align: center;">Description</p> <p>This field indicates if TP2 is currently being sent.</p> <p>Recommendation is to not use this status bit.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 35%;">Name</th> <th style="width: 40%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Sending</td> <td>Not sending TP2</td> </tr> <tr> <td>1b</td> <td>Sending</td> <td>Sending TP2</td> </tr> </tbody> </table>	Access:	RO	Value	Name	Description	0b	Not Sending	Not sending TP2	1b	Sending	Sending TP2
Access:	RO											
Value	Name	Description										
0b	Not Sending	Not sending TP2										
1b	Sending	Sending TP2										
7	Reserved											
6	Reserved											
5	<p>PSR2 deep Sleep Entry Completion</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/WC</td> </tr> </table> <p>This is a sticky bit which is set on PSR2 deep sleep entry completion. Clear this bit by writing a 1b to it.</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th style="width: 40%;">Value</th> <th style="width: 60%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not complete</td> </tr> <tr> <td>1b</td> <td>Complete</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Not complete	1b	Complete			
Access:	R/WC											
Value	Name											
0b	Not complete											
1b	Complete											

PSR2_STATUS		
4	PSR2 SU Entry Completion	
	Access: R/WC	
	This is a sticky bit which is set on PSR2 SU entry completion. Clear this bit by writing a 1b to it.	
	Value	Name
	0b	Not complete
1b	Complete	
3:0	Idle Frame Counter	
	Access: RO	
This field provides the live status of the idle frame counter.		

PSR2_SU_ECC_STAT

PSR2_SU_ECC_STAT					
Register Space:	MMIO: 0/2/0				
Access:	R/WC				
Size (in bits):	32				
Address:	60A64h-60A67h				
Name:	PSR2 Selective Update ECC Status				
ShortName:	PSR2_SU_ECC_STAT_A				
Reset:	soft				
Each of these fields is a sticky bit that gives the ECC error status for any PSR2 memory bank.					
A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.					
DWord	Bit	Description			
0	31:17	Reserved			
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
16	Double Error Any Bank				
	<table border="1"> <tr> <th>Description</th> </tr> <tr> <td>Errors in banks 8-13 are missed and not reported.</td> </tr> </table>	Description	Errors in banks 8-13 are missed and not reported.		
Description					
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15:1	Reserved				
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
0	Single Error Any Bank				
	<table border="1"> <tr> <th>Description</th> </tr> <tr> <td>Errors in banks 8-13 are missed and not reported.</td> </tr> </table>	Description	Errors in banks 8-13 are missed and not reported.		
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PSR2_SU_STATUS

PSR2_SU_STATUS		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	96	
Address:	60914h-6091Fh	
Name:	PSR2 Selective Update Status	
ShortName:	PSR2_SU_STATUS_A	
Reset:	soft	
A frame is divided into selective update blocks of four scan lines each. This register provides the count of the number of selective update blocks per frame, for the last eight frames		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
	29:20	Number of SU blocks in frame N - 2 This field indicates the number of selective update blocks in frame N - 1.
19:10	Number of SU blocks in frame N - 1 This field indicates the number of selective update blocks in frame N - 1.	
9:0	Number of SU blocks in frame N This field indicates the number of selective update blocks in frame N.	
1	31:30	Reserved
		Access: RO
		Format: MBZ
	29:20	Number of SU blocks in frame N - 5 This field indicates the number of selective update blocks in frame N - 1.
19:10	Number of SU blocks in frame N - 4 This field indicates the number of selective update blocks in frame N - 1.	
9:0	Number of SU blocks in frame N - 3 This field indicates the number of selective update blocks in frame N.	
2	31:20	Reserved
		Access: RO
	Format: MBZ	
19:10	Number of SU blocks in frame N - 7 This field indicates the number of selective update blocks in frame N - 1.	
9:0	Number of SU blocks in frame N - 6 This field indicates the number of selective update blocks in frame N.	

PTBR Number Of Pages Recorded

PTBR_NUM_PAGES_RECORDED_REGISTER - PTBR Number Of Pages Recorded			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	18594h		
Name:	Register Template Address		
ShortName:	PTBR_NUM_PAGES_RECORDED_REGISTER		
<p>This is a running count of number of pages allocated by the OVR unit for the visibility data. This includes pages that could have been allocated but were not allocated because the OVR unit early terminated the pages with out of memory marker. This register is engine context save/restored.</p>			
DWord	Bit	Description	
0	31:17	Reserved	
		Access:	RO
		Format:	MBZ
	16:0	PTBR_NUM_PAGES_RECORDED	
		Default Value:	0h
		Access:	R/W
		Format:	U17
		_Custom_GTIReset:	DEV
		<p>This is a running count of number of pages allocated by the OVR unit for the visibility data. This includes pages that could have been allocated but were not allocated because the OVR unit early terminated the pages with out of memory marker.</p>	
		Programming Notes	
SW must not write to this register.			



PTBR Page Pool Size Register

PTBR_PAGE_POOL_SIZE_REGISTER - PTBR Page Pool Size Register				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	18590h			
Name:	Register Template Address			
ShortName:	PTBR_PAGE_POOL_SIZE_REGISTER			
<p>Indicates the size of the PTBR Page Pool Size allocated by SW. The page pool size is with respect to the PTBR_PAGE_POOL_BASE_ADDRESS programmed through 3DSTATE_PTBR_PAGE_POOL_BASE_ADDRESS command. SW can do multiple writes to this register with the increased page pool size as it allocates more pages to the PTBR page pool.</p> <p>Coming out of reset or on executing PTBR_PAGE_POOL_RESTART by 3DSTATE_PTBR_PAGE_POOL_BASE_ADDRESS command, HW initializes PTBR_PAGE_POOL_SIZE to 0x0. HW on detecting a write to this register compares its current PTBR_PAGE_POOL_SIZE with that of the value programmed in this register to add more pages to the Free-List and updates itself with the latest value.</p> <p>This is a non-privileged register and engine context save/restored by HW.</p>				
Programming Notes				
<ul style="list-style-type: none"> SW must not write a value to this register less than the existing value. SW must use the Restart field of the 3DSTATE_PTBR_PAGE_POOL_ADDRESS command to decrease the size of the pool. SW must always program PTBR_PAGE_POOL_SIZE_REGISTER through MI_LOAD_REGISTER_IMM command or any other MI command to load register in the command sequence. SW must ensure following state are set in HW prior to programming this register: 3DSTATE_PTBR_PAGE_POOL_BASE_ADDRESS 3DSTATE_PTBR_FEE_LIST_BASE_ADDRESS 				
DWord	Bit	Description		
0	31:16	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
	15:0	PTBR_PAGE_POOL_SIZE		
		Default Value:	0h	
		Access:	R/W	
		Format:	U16-1	
		_Custom_GTIReset:	DEV	
		Indicates the PTBR page pool size (4KB granularity). A value of '0x0' indicates a single page and a value of 99h indicates 154 pages are available in the page pool for use by HW. Valid Range [0..65534].		

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
_Custom_GTIRreset:	DEV					
Address:	0CEF0h					
DWord	Bit	Description				
0	31:0	Repair Address High <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Fixed PTE entry is written by SW here.	Default Value:	00000000h	Access:	R/W
Default Value:	00000000h					
Access:	R/W					



PTE SW Fault Repair Low

PTESWC_L - PTE SW Fault Repair Low				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
_Custom_GTIRreset:	DEV			
Address:	0CEF4h			
DWord	Bit	Description		
0	31:0	Repair Address Low		
		Access: <table border="1"><tr><td></td><td>R/W</td></tr></table>		R/W
	R/W			
		Fixed PTE entry is written by SW here.		

PWR_WELL_CTL

PWR_WELL_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	45400h-45403h	
Name:	Power Well Control 1	
ShortName:	PWR_WELL_CTL1	
Reset:	soft	
CrashLogSaved:	true	
CrashLogPriority:	2	
CrashLogVisibility:	public	
ExternalLongName:	DE Power Well Control 1	
ExternalDescription:	Display engine power well control	
Address:	45404h-45407h	
Name:	Power Well Control 2	
ShortName:	PWR_WELL_CTL2	
Reset:	soft	
<p>This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.</p> <p>PWR_WELL_CTL1 is generally used for BIOS to control power.</p> <p>PWR_WELL_CTL2 is generally used for driver to control power.</p> <p>The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.</p> <p>When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.</p> <p>The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.</p>		
Restriction		
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.		
Power wells must be enabled and disabled following the display initialization and mode set sequences.		
DWord	Bit	Description
0	31:22	Reserved
		Access: RO
	Format: MBZ	
	21:10	Reserved
Access: RO		
Format: MBZ		

PWR_WELL_CTL								
	9	Power Well 5 Request Access: R/W This field requests power well to enable or disable. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	8	Power Well 5 State Access: RO This field indicates the status of power well. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						
	7	Power Well 4 Request Access: R/W This field requests power well to enable or disable. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	6	Power Well 4 State Access: RO This field indicates the status of power well. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						
	5	Power Well 3 Request Access: R/W This field requests power well to enable or disable. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	4	Power Well 3 State Access: RO This field indicates the status of power well. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						

PWR_WELL_CTL								
	3	Power Well 2 Request Access: R/W This field requests power well to enable or disable.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	2	Power Well 2 State Access: RO This field indicates the status of power well.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						
	1	Power Well 1 Request Access: R/W This field requests power well to enable or disable.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	0	Power Well 1 State Access: RO This field indicates the status of power well.						
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled	
Value	Name							
0b	Disabled							
1b	Enabled							



PWR_WELL_CTL_AUX

PWR_WELL_CTL_AUX						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	45440h-45443h					
Name:	Power Well Control AUX 1					
ShortName:	PWR_WELL_CTL_AUX1					
Reset:	soft					
Address:	45444h-45447h					
Name:	Power Well Control AUX 2					
ShortName:	PWR_WELL_CTL_AUX2					
Reset:	soft					
<p>This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.</p> <p>PWR_WELL_CTL_AUX1 is generally used for BIOS to control power.</p> <p>PWR_WELL_CTL_AUX2 is generally used for driver to control power.</p> <p>The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.</p> <p>When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.</p> <p>The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.</p>						
Restriction						
<p>The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.</p>						
DWord	Bit	Description				
0	31:30	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
29		AUX TBT6 IO Power Request				
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.</p>	Access:	R/W		
		Access:	R/W			
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable
Value	Name					
0b	Disable					
1b	Enable					

PWR_WELL_CTL_AUX

	28	AUX TBT6 IO Power State						
	Access: RO							
	This field indicates the status of power for this Thunderbolt Aux IO.							
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	27	AUX TBT5 IO Power Request						
	Access: R/W							
	This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.							
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	26	AUX TBT5 IO Power State						
	Access: RO							
	This field indicates the status of power for this Thunderbolt Aux IO.							
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
1b	Enable							
25	AUX TBT4 IO Power Request							
Access: R/W								
This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.								
<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable	
Value	Name							
0b	Disable							
1b	Enable							
24	AUX TBT4 IO Power State							
Access: RO								
This field indicates the status of power for this Thunderbolt Aux IO.								
<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>		Value	Name	0b	Disable	1b	Enable	
Value	Name							
0b	Disable							
1b	Enable							
23	AUX TBT3 IO Power Request							
Access: R/W								
This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.								
<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> </tbody> </table>		Value	Name	0b	Disable			
Value	Name							
0b	Disable							

PWR_WELL_CTL_AUX

	1b	Enable
22	AUX TBT3 IO Power State	
	Access:	RO
	This field indicates the status of power for this Thunderbolt Aux IO.	
	Value	Name
	0b	Disable
	1b	Enable
21	AUX TBT2 IO Power Request	
	Access:	R/W
	This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.	
	Value	Name
	0b	Disable
	1b	Enable
20	AUX TBT2 IO Power State	
	Access:	RO
	This field indicates the status of power for this Thunderbolt Aux IO.	
	Value	Name
	0b	Disable
	1b	Enable
19	AUX TBT1 IO Power Request	
	Access:	R/W
	This field requests power for this Thunderbolt Aux IO to enable or disable. This is used for typeC ports that are in thunderbolt mode.	
	Value	Name
	0b	Disable
	1b	Enable
18	AUX TBT1 IO Power State	
	Access:	RO
	This field indicates the status of power for this Thunderbolt Aux IO.	
	Value	Name
	0b	Disable
	1b	Enable
17	USBC6 IO Power Request	
	Access:	R/W
This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.		

PWR_WELL_CTL_AUX									
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable		
Value	Name								
0b	Disable								
1b	Enable								
16	<p>USBC6 IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> <p>This field indicates the status of power for this USBC Aux IO.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disable	1b	Enable
Access:	RO								
Value	Name								
0b	Disable								
1b	Enable								
15	<p>USBC5 IO Power Request</p> <table border="1"> <tr> <td>Access:</td> <td style="text-align: right;">R/W</td> </tr> </table> <p>This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W								
Value	Name								
0b	Disable								
1b	Enable								
14	<p>USBC5 IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> <p>This field indicates the status of power for this USBC Aux IO.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disable	1b	Enable
Access:	RO								
Value	Name								
0b	Disable								
1b	Enable								
13	<p>USBC4 IO Power Request</p> <table border="1"> <tr> <td>Access:</td> <td style="text-align: right;">R/W</td> </tr> </table> <p>This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W								
Value	Name								
0b	Disable								
1b	Enable								
12	<p>USBC4 IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td style="text-align: right;">RO</td> </tr> </table> <p>This field indicates the status of power for this USBC Aux IO.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disable	1b	Enable
Access:	RO								
Value	Name								
0b	Disable								
1b	Enable								

PWR_WELL_CTL_AUX

	11	USBC3 IO Power Request	Access:	R/W
	This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.			
	Value		Name	
	0b		Disable	
	1b		Enable	
	10	USBC3 IO Power State	Access:	RO
	This field indicates the status of power for this USBC Aux IO.			
	Value		Name	
	0b		Disable	
	1b		Enable	
	9	USBC2 IO Power Request	Access:	R/W
	This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.			
	Value		Name	
	0b		Disable	
	1b		Enable	
	8	USBC2 IO Power State	Access:	RO
	This field indicates the status of power for this USBC Aux IO.			
	Value		Name	
	0b		Disable	
	1b		Enable	
	7	USBC1 IO Power Request	Access:	R/W
	This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.			
	Value		Name	
	0b		Disable	
1b		Enable		
6	USBC1 IO Power State	Access:	RO	
This field indicates the status of power for this USBC Aux IO.				
Value		Name		
0b		Disabled		

PWR_WELL_CTL_AUX									
	<table border="1"> <tr> <td style="width: 50%;">1b</td> <td>Enabled</td> </tr> </table>	1b	Enabled						
1b	Enabled								
5	<p>AUX C IO Power Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field requests power for this Aux IO to enable or disable.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W								
Value	Name								
0b	Disable								
1b	Enable								
4	<p>AUX C IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field indicates the status of power for this Aux IO.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disabled	1b	Enabled
Access:	RO								
Value	Name								
0b	Disabled								
1b	Enabled								
3	<p>AUX B IO Power Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field requests power for this Aux IO to enable or disable.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W								
Value	Name								
0b	Disable								
1b	Enable								
2	<p>AUX B IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field requests power for this Aux IO to enable or disable.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disabled	1b	Enabled
Access:	RO								
Value	Name								
0b	Disabled								
1b	Enabled								
1	<p>AUX A IO Power Request</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This field requests power for this Aux IO to enable or disable.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W								
Value	Name								
0b	Disable								
1b	Enable								
0	<p>AUX A IO Power State</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field indicates the status of power for this Aux IO.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Disabled	1b	Enabled
Access:	RO								
Value	Name								
0b	Disabled								
1b	Enabled								



PWR_WELL_CTL_DDI

PWR_WELL_CTL_DDI			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	45450h-45453h		
Name:	Power Well Control DDI 1		
ShortName:	PWR_WELL_CTL_DDI1		
Reset:	soft		
Address:	45454h-45457h		
Name:	Power Well Control DDI 2		
ShortName:	PWR_WELL_CTL_DDI2		
Reset:	soft		
<p>This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power. PWR_WELL_CTL_DDI1 is generally used for BIOS to control power. PWR_WELL_CTL_DDI2 is generally used for driver to control power. The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable. When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes. The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.</p>			
Restriction			
<p>The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.</p>			
DWord	Bit	Description	
0	31:23	Reserved	
		Access: RO	
		Format: MBZ	
	22:18	Reserved	
		Access: RO	
		Format: MBZ	
	17	USBC6 IO Power Request	
		Access: R/W	
		This field requests power for USBC6 IO to enable or disable.	
Value		Name	
	0b	Disable	

PWR_WELL_CTL_DDI							
	<table border="1"> <tr> <td style="width: 50%;">1b</td> <td>Enable</td> </tr> </table>	1b	Enable				
1b	Enable						
16	USBC6 IO Power State Access: RO						
	This field indicates the status of power for USBC6 IO.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						
15	USBC5 IO Power Request Access: R/W						
	This field requests power for USBC5 IO to enable or disable.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						
14	USBC5 IO Power State Access: RO						
	This field indicates the status of power for USBC5 IO.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						
13	USBC4 IO Power Request Access: R/W						
	This field requests power for USBC4 IO to enable or disable.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						
12	USBC4 IO Power State Access: RO						
	This field indicates the status of power for USBC4 IO.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						
11	USBC3 IO Power Request Access: R/W						
	This field requests power for USBC3 IO to enable or disable.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name					
	0b	Disable					
1b	Enable						
0b	Disable						
1b	Enable						

PWR_WELL_CTL_DDI

	10	USBC3 IO Power State		
		Access:	RO	
		This field indicates the status of power for USBC3 IO.		
		Value	Name	
		0b	Disable	
		1b	Enable	
	9	USBC2 IO Power Request		
		Access:	R/W	
		This field requests power for USBC2 IO to enable or disable.		
		Value	Name	
		0b	Disable	
		1b	Enable	
	8	USBC2 IO Power State		
		Access:	RO	
		This field indicates the status of power for USBC2 IO.		
		Value	Name	
		0b	Disabled	
		1b	Enabled	
	7	USBC1 IO Power Request		
		Access:	R/W	
This field requests power for USBC1 IO to enable or disable.				
Value		Name		
	0b	Disable		
	1b	Enable		
6	USBC1 IO Power State			
	Access:	RO		
	This field indicates the status of power for USBC1 IO.			
	Value	Name		
	0b	Disabled		
	1b	Enabled		
5	DDI C IO Power Request			
	Access:	R/W		
	This field requests power for DDI C IO to enable or disable.			
	Value	Name		
	0b	Disable		
	1b	Enable		

PWR_WELL_CTL_DDI								
	4	DDI C IO Power State Access: RO This field indicates the status of power for DDI C IO. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						
	3	DDI B IO Power Request Access: R/W This field requests power for DDI B IO to enable or disable. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
	2	DDI B IO Power State Access: RO This field indicates the status of power for DDI B IO. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled
	Value	Name						
	0b	Disabled						
	1b	Enabled						
	1	DDI A IO Power Request Access: R/W This field requests power for DDI A IO to enable or disable. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
	1b	Enable						
0	DDI A IO Power State Access: RO This field indicates the status of power for DDI A IO. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled	
Value	Name							
0b	Disabled							
1b	Enabled							



PWRCTXSAVE Message Register for Boot Controller Unit

MSG_PWRCTXSAVE_MBC - PWRCTXSAVE Message Register for Boot Controller Unit			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	0850Ch		
<p>Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.</p>			
DWord	Bit	Description	
0	31:10	Reserved	
		Access:	RO
		Format:	MBZ
9		Power Context Save Request	
		Access:	R/W
		_Custom_GTIReset:	BUS
Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.			
8:0		QWord Credits for Power Context Save Request	
		Access:	R/W
		_Custom_GTIReset:	BUS
QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bit of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).			

RC6 Context Base

RC6CTXBASE - RC6 Context Base		
Register Space:	MMIO: 0/2/0	
Size (in bits):	64	
Address:	00D48h	
RC6 Location		
DWord	Bit	Description
0	31:12	RC6 Memory Base Low
		Access: R/W Lock
		_Custom_GTIReset: BUS
This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1		
11:1	Reserved	Access: RO
		Format: MBZ
0	RC6Context Base Register Lock	Access: R/W Lock
		_Custom_GTIReset: BUS
		1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes
1	31:0	RC6 Memory Base High
		Access: R/W Lock
		_Custom_GTIReset: BUS
This field is used to set the base of memory where the RC6 power context will be saved. This value MUST be above the base and below the top of stolen memory. This High Dword must be written before the low word is written with RC6MEMLOCK of 1. This register is locked (becomes read-only) when RC6MEMLOCK is 1		



RC6 LOCATION

RC6LOCATION - RC6 LOCATION			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	00D40h		
RC6 Location			
DWord	Bit	Description	
0	31	RC6Context Location Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only	
	30:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	RC6Context Location	
		Access:	RO
		_Custom_GTIReset:	BUS
1'b1 : Send context data to DRAM location specified in RC6MEMBASE (default) This will be tied to 1 with as there is no option to save context to a SRAM			

Register_HCPBitstreamOutputCABACInsertionCount

HCP_CABAC_INSERTION_COUNT - Register_HCPBitstreamOutputCABACInsertionCount						
Register Space:	MMIO: 0/2/0					
Source:	VideoCS1					
Access:	RO					
Size (in bits):	32					
_Custom_GTIReset:	BUS					
<p>This register stores the count in bytes of CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.</p>						
DWord	Bit	Description				
0	31:0	<p>HCP Cabac Insertion Count</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.</p>	Access:	RO	Format:	U32
Access:	RO					
Format:	U32					



Register_HCP_SFC_LOCK_REQUEST

HCP_SFC_LOCK_REQUEST - Register_HCP_SFC_LOCK_REQUEST		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	1C2910h	
ShortName:	HCP_SFC_LOCK_REQUEST_VCS0	
Description:	For VDBox0	
Address:	1D2910h	
ShortName:	HCP_SFC_LOCK_REQUEST_VCS2	
Description:	For VDBox2	
Address:	1E2910h	
ShortName:	HCP_SFC_LOCK_REQUEST_VCS4	
Description:	For VDBox4	
Address:	1F2910h	
ShortName:	HCP_SFC_LOCK_REQUEST_VCS6	
Description:	For VDBox6	
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
		Format: MBZ
	0	HCP_SFC_Forced_Lock
	Format: U1	
	<p>This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells HCP that a software reset is going to happen. HCP then issues a forced lock to SFC. If SFC is currently locked to HCP, SFC should not unlock itself from HCP. If SFC is NOT currently locked to HCP, SFC should not accept the lock request from HCP. Driver needs to clear this bit after the software reset sequence is complete.</p>	

Register_HCP_SFC_LOCK_STATUS

HCP_SFC_LOCK_STATUS - Register_HCP_SFC_LOCK_STATUS			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	1C2914h		
ShortName:	HCP_SFC_LOCK_STATUS_VCS0		
Description:	For VDbbox0		
Address:	1D2914h		
ShortName:	HCP_SFC_LOCK_STATUS_VCS2		
Description:	For VDBox2		
Address:	1E2914h		
ShortName:	HCP_SFC_LOCK_STATUS_VCS4		
Description:	For VDBox4		
Address:	1F2914h		
ShortName:	HCP_SFC_LOCK_STATUS_VCS6		
Description:	For VDBox6		
DWord	Bit	Description	
0	31:2	Reserved	
		Access:	RO
		Format:	MBZ
	1	HCP_SFC_Forced_Act	
		Format:	U1
	<p>This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that HCP has received HCP_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert HCP_SFC_Forced_Lock as well.</p>		
0	HCP_SFC_Usage		
	Format:	U1	
<p>This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to HCP. This bit should be set after SFC accepts the lock request from HCP. This bit should be clear once SFC finishes the workload and unlocked from HCP. In case a reset happens on HCP, this bit must be reset once a new workload is received</p>			



Render and Media Context Restore Needed

RENDER_MEDIA_NEED_RESTORE - Render and Media Context Restore Needed		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	080F0h	
DWord	Bit	Description
0	31:2	Reserved
		Access: RO
	1	Render Context Restore is needed
		Access: RO
		_Custom_GTIRreset: BUS
	Render Context Restore Needed Flag to support Render Powergating Feature This flag will let PM know if Media context need to be restored on C6 exit 1'b0: Do not proceed if Wait for VCR1 is set (default). 1'b1: Proceed to unblocking FIFO.	
0	Media Context Restore is needed	
	Access: RO	
	_Custom_GTIRreset: BUS	
Render Context Restore Needed Flag to support Render Powergating Feature This flag will let PM know if Media context need to be restored on C6 exit 1'b0: Do not proceed if Wait for VCR1 is set (default). 1'b1: Proceed to unblocking FIFO.		

Render Control Unit Mode Register

RCU_MODE - Render Control Unit Mode Register			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	14800h		
Mode register for Render Control Unit (RCU).			
DWord	Bit	Description	
0	31:16	Mask	
		Access:	WO
		Format:	Mask
			Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:5	Reserved	
		Format:	PBC
	4:3	Reserved	
Format:		PBC	
2	Disable Dual Context Limiting to Dual Queue		
	<p>This bit enables two contexts of different address space to run in parallel. By default, HW enables RenderCS and ComputeCS to run contexts concurrently only when the executing contexts are from the same address space otherwise the context execution gets serialized. Two contexts are said to be from the same address space when they have the identical Virtual Function Number and the Page Directory Pointer-0.</p> <p>This both controls disabling of the default HW behavior.</p>		
	Value	Name	Description
	0	Force Run Alone when different context [Default]	HW allows concurrent execution only when both contexts are from the same address space.
1	Enable Dual Context	Concurrent execution of context on RenderCS and ComputeCS is allowed with no address space comparison.	
1	Reserved		
	Format:	PBC	
0	Compute Engine Enable		
	<p>Description</p> <p>This bit indicates if Compute Engine (a.k.a Dual Context or Multi Context) is enabled or not. This bit must be treated as global control for enabling and disabling of compute engine. Hardware allocates required resources for the compute engine based on this bit.</p> <ul style="list-style-type: none"> Mid Thread Preemption for GPGPU workloads is not supported when compute engine is enabled. Hardware implicitly demotes the GPGPU preemption granularity to Thread Group or lower irrespective of the preemption granularity programmed through GPGPU_PREEMPTION_CONTROL 		

RCU_MODE - Render Control Unit Mode Register

mode bits.

- HW reserves 4KB of URB space per bank for Compute Engine out of the total storage available in L3. SW must consider that 4KB of storage per bank will be reduced from what is programmed for the URB space in L3 for Render Engine executed workloads. Example: When URB space programmed is 64KB (per bank) for Render Engine, the actual URB space available for operation is only 60KB (per bank). Similarly, when URB space programmed is 128KB (per bank) for render engine, the actual URB space available for operation is only 124KB (per bank). More detailed description available in "L3 Cache" section of the PRM.

In Dual Context mode of operation Compute Engine and Render Engine address space separation is based on the memory access address bit [47]. Each of the engine's addressable space is limited to 128 TB ([46:0]).

Value	Name	Description
0	[Default]	Compute engine is disabled.
1		Compute engine is enabled.

Programming Notes

This bit must be programmed when render engine is idle with no contexts getting executed.

Render Control Unit Power Clock State Register

RCU_PWR_CLK_STATE - Render Control Unit Power Clock State Register									
Register Space:	MMIO: 0/2/0								
Access:	R/W								
Size (in bits):	32								
_Custom_GTIReset:	DEV								
Address:	148C8h								
<p>This register provides a mechanism to override the PWR_CLK_STATE requested by the RenderCS or ComputeCS. Both ComputeCS and RenderCS make their R_PWR_CLK_STATE request to Render Control Unit (RCU), RCU computes the required PWR_CLK_STATE and interfaces with power management to get the desired state.</p>									
DWord	Bit	Description							
0	31	Power Clock State Enable Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>U1</td></tr></table> When enabled (set) RCU will force the PWR_CLK_STATE programmed in the RCU_PWR_CLK_STATE to Power Management instead of the PWR_CLK_STATE received from the RenderCS or ComputeCS. RCU will enforce the updated value of RCU_PWR_CLK_STATE on an engines PWR_CLK_STATE request when the requesting engine is the only active engine in the GPU, i.e RCU will ensure the other engines are not active and are not impacted on changing the PWR_CLK_STATE. (Example: Updated value in RCU_PWR_CLK_STATE will be used to override the RenderCS PWR_CLK_STATE request when ComputeCS is idle or Vice-Versa).		U1					
			U1						
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Power Clock State Disabled</td> <td>No specific power state set, bits[30:0] are ignored.</td> </tr> <tr> <td>1h</td> <td>Power Clock State Enabled</td> <td>Power state is set and bit[30:0] are valid and have the desired state. RCU will use the powe state to override the values received from RenderCS or ComputeCS.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.	1h	Power Clock State Enabled	Power state is set and bit[30:0] are valid and have the desired state. RCU will use the powe state to override the values received from RenderCS or ComputeCS.
Value	Name	Description							
0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.							
1h	Power Clock State Enabled	Power state is set and bit[30:0] are valid and have the desired state. RCU will use the powe state to override the values received from RenderCS or ComputeCS.							
	30:0	Render Power Clock State Format: <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td></td><td>U31</td></tr></table>		U31					
	U31								



Reported BitRateControl Convergence Status

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	1C928h	
ShortName:	MFX_VP8_BRC_CONVERGENCE_STATUS_VD2	
This register stores BitRateControl Convergence Status.		
DWord	Bit	Description
0	31	Reserved
	30:28	Reserved
	27	Reserved
	26:24	Reserved
	23	Reserved
	22:20	Reserved
	19	Reserved
	18:16	Reserved
	15:12	Reserved
		Access:
	Format:	MBZ
11:8	Total Num of Pass	
	Format:	U4
	This bit indicates the number of Multipass including current frame. Note that Initial Pass is not counted.	
7:2	Reserved	
	Access:	RO
	Format:	MBZ
1	Overflow OR Underflow Flag	
	Format:	U1
	This bit indicates the current frame has BRC overflow OR underflow.	
0	MB Max. Conformance Flag	
	Format:	U1
	This contains flag that indicate Inter MB or Intra MB Max. Conformance is not met. This is legacy support and this feature is not validated.	

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	1C920h	
This register stores per segment Bit Rate Control DeltaLoopFilter.		
DWord	Bit	Description
0	31	Reserved
		Access: RO
		Format: MBZ
	30:24	Segment1 CumulativeDeltaLoopFilter
		Format: S6 This contains Segment1 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	Reserved
		Access: RO
		Format: MBZ
	21:16	Segment1 LoopFilter
		Format: U6 This contains Segment1 LoopFilter used in current frame. This register is valid after a BRC pass is done.
15	Reserved	
	Access: RO	
	Format: MBZ	
14:8	Segment0 CumulativeDeltaLoopFilter	
	Format: S6 This contains Segment0 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaLoopFilter.	
7:6	Reserved	
	Access: RO	
	Format: MBZ	

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

	5:0	Segment0 LoopFilter	
		Format:	U6
		<p>This contains Segment0 LoopFilter used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects LoopFilter. If Segmentation is enabled, this field reflects Segment0 LoopFilter.</p>	

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	1C924h		
This register stores per segment Bit Rate Control DeltaLoopFilter.			
DWord	Bit	Description	
0	31	Reserved	
		Access:	RO
		Format:	MBZ
	30:24	Segment3 CumulativeDeltaLoopFilter	
		Format:	S6 This contains Segment3 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	Reserved	
		Access:	RO
		Format:	MBZ
	21:16	Segment3 LoopFilter	
		Format:	U6 This contains Segment3 LoopFilter used in current frame. This register is valid after a BRC pass is done.
15	Reserved		
	Access:	RO	
	Format:	MBZ	
14:8	Segment2 CumulativeDeltaLoopFilter		
	Format:	S6 This contains Segment2 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.	
7:6	Reserved		
	Access:	RO	
	Format:	MBZ	

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

	5:0	Segment2 LoopFilter	
		Format:	U6
<p>This contains Segment2 LoopFilter used in current frame. This register is valid after a BRC pass is done.</p>			

Reported BitRateControl CumulativeDeltaQindex and Qindex 01

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	12918h					
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB0					
Address:	1C918h					
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB1					
This register stores per segment Bit Rate Control CumulativeDeltaQindex.						
DWord	Bit	Description				
0	31:24	Segment1 CumulativeDeltaQindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment1 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.</p>	Format:	S7		
	Format:	S7				
	23	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
	22:16	Segment1 Qindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>This contains Segment1 Qindex used in current frame. This register is valid after a BRC pass is done.</p>	Format:	U7		
Format:	U7					
15:8	Segment0 CumulativeDeltaQindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment0 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaQindex. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaQindex.</p>	Format:	S7			
Format:	S7					
7	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
6:0	Segment0 Qindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>This contains Segment0 Qindex used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects Qindex. If Segmentation is enabled, this field reflects Segment0 Qindex.</p>	Format:	U7			
Format:	U7					

Reported BitRateControl CumulativeDeltaQindex and Qindex 23

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	1291Ch					
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB0					
Address:	1C91Ch					
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB1					
This register stores per segment Bit Rate Control CumulativeDeltaQindex and Qindex.						
DWord	Bit	Description				
0	31:24	Segment3 CumulativeDeltaQindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment3 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.</p>	Format:	S7		
	Format:	S7				
	23	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
	22:16	Segment3 Qindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>This contains Segment3 Qindex used in current frame. This register is valid after a BRC pass is done.</p>	Format:	U7		
Format:	U7					
15:8	Segment2 CumulativeDeltaQindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment2 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.</p>	Format:	S7			
Format:	S7					
7	Reserved <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
6:0	Segment2 Qindex <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U7</td> </tr> </table> <p>This contains Segment2 Qindex used in current frame. This register is valid after a BRC pass is done.</p>	Format:	U7			
Format:	U7					

Reported BitRateControl DeltaLoopFilter

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12914h	
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB0	
Address:	1C914h	
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB1	
This register stores per segment Bit Rate Control DeltaLoopFilter.		
DWord	Bit	Description
0	31	Reserved
		Access: RO
		Format: MBZ
	30:24	Segment3 DeltaLoopFilter
		Format: S6 This contains Segment3 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	23	Reserved
		Access: RO
		Format: MBZ
	22:16	Segment2 DeltaLoopFilter
		Format: S6 This contains Segment2 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
15	Reserved	
	Access: RO	
	Format: MBZ	
14:8	Segment1 DeltaLoopFilter	
	Format: S6 This contains Segment1 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done.	
7	Reserved	
	Access: RO	
	Format: MBZ	

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

	6:0	Segment0 DeltaLoopFilter	
		Format:	S6
<p>This contains Segment0 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 DeltaLoopFilter.</p>			

Reported BitRateControl DeltaQindex

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	12910h			
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB0			
Address:	1C910h			
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB1			
This register stores per segment Bit Rate Control DeltaQindex.				
DWord	Bit	Description		
0	31:24	Segment3 DeltaQindex <table border="1"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment3 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done</p>	Format:	S7
	Format:	S7		
	23:16	Segment2 DeltaQindex <table border="1"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment2 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done</p>	Format:	S7
	Format:	S7		
15:8	Segment1 DeltaQindex <table border="1"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment1 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done.</p>	Format:	S7	
Format:	S7			
7:0	Segment0 DeltaQindex <table border="1"> <tr> <td>Format:</td> <td>S7</td> </tr> </table> <p>This contains Segment0 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaQindex. If Segmentation is enabled, this field reflects Segment0 DeltaQindex.</p>	Format:	S7	
Format:	S7			



Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12900h	
ShortName:	MFX_VP8_CNTRL_MASK_VB0	
Address:	1C900h	
ShortName:	MFX_VP8_CNTRL_MASK_VB1	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:6	Reserved
		Access: RO
		Format: MBZ
	5	Final Bitstream Buffer Overrun Mask
	Format: U1	
	This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.	
	4	Intermediate Bitstream Buffer Overrun Mask
Format: U1		
This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.		
3	Intra MB Bit Count Conformance Mask	
Format: U1		
This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.		
2	Inter MB Bit Count Conformance Mask	
Format: U1		
This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.		
1	Frame Bit Rate Overflow Mask	
Format: U1		
This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control		

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

	0	Frame Bit Rate Underflow Mask	
		Format:	U1
		This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control	



Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12904h	
ShortName:	MFX_VP8_CNTRL_STATUS_VB0	
Address:	1C904h	
ShortName:	MFX_VP8_CNTRL_STATUS_VB1	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:8	Reserved
		Access: RO
		Format: MBZ
	7	QindexClampHigh Status
	Format: U1	
	This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.	
	6	QindexClampLow Status
	Format: U1	
This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.		
5	Final Bitstream Buffer Overrun Status	
Format: U1		
This denotes if Final bitstream buffer overrun.		
4	Intermediate Bitstream Buffer Overrun Status	
Format: U1		
This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)		
3	Intra MB Bit Count Conformance Status	
Format: U1		
This is legacy support as AVC for Intra MB Bit Count conformance. It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.		
2	Inter MB Bit Count Conformance Status	
Format: U1		
This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.		

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

	1	Frame Bit Rate Overflow Status	
	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U1</td> </tr> </table> <p>It denotes if Frame Bit Rate Overflow in current frame</p>		Format:
Format:	U1		
	0	Frame Bit Rate Underflow Status	
	<table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Format:</td> <td style="width: 20%;">U1</td> </tr> </table> <p>It denotes if Frame Bit Rate Underflow in current frame</p>		Format:
Format:	U1		



Reported Bitstream Output Bit Count for Syntax Elements Only

HCP_BITSTREAMSE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	1E9A8h			
<p>This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.</p>				
DWord	Bit	Description		
0	31:0	<p>HCP Bitstream Syntax Element Only Bit Count</p> <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.</p>	Format:	U32
Format:	U32			

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128A4h	
<p>This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.</p>		
DWord	Bit	Description
0	31:0	<p>MFC Bitstream Syntax Element Only Bit Count Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.</p>



Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128A0h	
This register stores the count of bytes of the bitstream output per frame		
DWord	Bit	Description
0	31:0	MFC Bitstream Byte Count per Frame Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Tile

HCP_BITSTREAM_BYTECOUNT_TILE - Reported Bitstream Output Byte Count per Tile				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	1E9CCh			
This register stores the count of bytes of the bitstream output per tile.				
DWord	Bit	Description		
0	31:0	HCP Bitstream Byte Count per Tile <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>Total number of bytes in the bitstream output per Tile from the encoder. This includes header/byte alignment/data bytes/EMU (emulation) bytes/. This count is updated for every time the internal bitstream counter is incremented and its reset at tile start.</p>	Format:	U32
Format:	U32			

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128A8h	
This register stores the count of number of bins per frame.		
DWord	Bit	Description
0	31:0	MFC AVC Cabac Bin Count Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	12908h			
ShortName:	MFX_VP8_FRM_BYTE_CNT_01			
Address:	1C908h			
ShortName:	MFX_VP8_FRM_BYTE_CNT_02			
This register stores the count of bytes of the bitstream output per frame				
DWord	Bit	Description		
0	31:0	Final BitStream Byte Count <table border="1"> <tr> <td>Format:</td> <td>U32</td> </tr> </table> This register contains Final Bitstream byte count	Format:	U32
Format:	U32			



Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1290Ch	
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB0	
Address:	1C90Ch	
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB1	
This register stores Frame Zero Padding Byte Count		
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
		Format: MBZ
	15:0	Frame Zero Padding Byte Count
		Format: U16
This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.		

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02358h-0235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_RCSUNIT
Address:	18358h-1835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_POCSUNIT
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT
Address:	1C0358h-1C035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1C4358h-1C435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	1C8358h-1C835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT0
Address:	1D0358h-1D035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT2
Address:	1D4358h-1D435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT3
Address:	1D8358h-1D835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT1
Address:	1E0358h-1E035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT4

TIMESTAMP - Reported Timestamp Count

Address:	1E4358h-1E435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT5
Address:	1E8358h-1E835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT2
Address:	1F0358h-1F035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT6
Address:	1F4358h-1F435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT7
Address:	1F8358h-1F835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT3
Address:	1A358h-1A35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_CCSUNIT0

This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency.

This register provides an elapsed real-time value that can be used as a timestamp. The accumulated value in this register is of the timestamp stamp granularity (base unit) defined in the Time Stamp Bases subsection in Power Management chapter.

This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.

DWord	Bit	Description			
0..1	63:36	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
35:32	Timestamp Value UN				
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>U4</td> </tr> </table> <p>This register increments for every timestamp base unit. The granularity of the time stamp base unit is defined in the Time Stamp Bases subsection in Power Management chapter. Note: This is the Upper Nibble of the Timesamp Value, a 36-bit signal.</p>	Format:	U4		
Format:	U4				

TIMESTAMP - Reported Timestamp Count			
31:0	<p>Timestamp Value LDW</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="width: 40%;">U32</td> </tr> </table> <p>This register increments for every timestamp base unit. The granularity of the time stamp base unit is defined in the Time Stamp Bases subsection in Power Management chapter.</p>	Format:	U32
Format:	U32		



Report Queue CFG HI

RPTQCFGHI - Report Queue CFG HI		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	098ACh	
Config to MCI and DFT Ring		
DWord	Bit	Description
0	31	Report fifo cfg hi valid
		Access: RO
		_Custom_GTIRreset: BUS
	30:18	RSVD_30_18
		Access: RO
		_Custom_GTIRreset: BUS
	17:16	Report fifo cfg hi bits 9_8
		Access: RO
		_Custom_GTIRreset: BUS
	15:8	RSVD_15_8
		Access: RO
		_Custom_GTIRreset: BUS
	7:0	Report fifo cfg hi bits 0_7
		Access: RO
		_Custom_GTIRreset: BUS

Report Queue CFG LO

RPTQCFGLO - Report Queue CFG LO		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	098A8h	
Config to MCI and DFT Ring		
DWord	Bit	Description
0	31:0	Report fifo cfg low
		Access: RO
		_Custom_GTIReset: BUS



Reset Control Register

RESET_CTRL - Reset Control Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020D0h-020D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_RCSUNIT
Address:	180D0h-180D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_POCSUNIT
Address:	220D0h-220D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_BCSUNIT
Address:	1C00D0h-1C00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT0
Address:	1C40D0h-1C40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT1
Address:	1C80D0h-1C80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT0
Address:	1D00D0h-1D00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT2
Address:	1D40D0h-1D40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT3
Address:	1D80D0h-1D80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT1
Address:	1E00D0h-1E00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT4

RESET_CTRL - Reset Control Register

Address: 1E40D0h-1E40D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_VCSUNIT5

Address: 1E80D0h-1E80D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_VECSUNIT2

Address: 1F00D0h-1F00D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_VCSUNIT6

Address: 1F40D0h-1F40D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_VCSUNIT7

Address: 1F80D0h-1F80D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_VECSUNIT3

Address: 1A0D0h-1A0D3h
 Name: Reset Control Register
 ShortName: RESET_CTRL_CCSUNIT0

Soft reset flow for an engine (Render, Blitter, Video, Video Enhancement) is asynchronous to the context execution in HW. SW needs a deterministic way to ensure it resets the context it intends to. One way to achieve this is to ensure HW doesn't switch out the context while SW is doing a soft reset. This is achieved by having an explicit interface between HW-SW to prepare the engine prior to the soft reset. SW sets the Request Reset in RESET_CTRL register of an engine indicating SW wants to initiate a soft reset flow for the corresponding engine. In response to Request Reset bit set, HW sets Ready for Reset bit of RESET_CTRL register indicating engine readiness for reset. As part of the reset readiness HW will not allow any context switch to take place and also ensure any ongoing context switch is paused on a clean context boundary (context save in progress is completed, Context Switch Status Buffer updates are allowed to complete). SW polls for Ready for Reset bit to be set before it does soft reset for the corresponding engine. Reading EXECLIST_STATUS register at this point provides the active context in HW that will get reset. On engine reset Request Reset bit will get reset with rest of the engine logic. Upon polling EXECLIST_STATUS register for active context SW might decide not to reset the engine and can reset the Request Reset in RESET_CTRL register. On Request Reset getting reset by SW, HW must continue with execution. SW setting Ready for Reset bit in RESET_CTRL register of an engine need not be followed by the corresponding engine reset. SW writing to Request Reset bit in RESET_CTRL register is preparing the engine for reset whereas SW writing to GDRST triggers the actual reset flow in HW.

Programming Notes

SW must not do Reset Readiness Handshake as part of the reset recovery on a CAT error.

DWord	Bit	Description
-------	-----	-------------

RESET_CTRL - Reset Control Register

0	31:16	Mask	
		Access:	WO
		Format:	Mask
	Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)		
	15:4	Reserved	
		Access:	RO
		Format:	MBZ
	3	Reserved	
		Format:	PBC
	2	Reserved	
1	Ready for Reset		
	Format:	U1	
When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.			
0	Request Reset		
	Format:	U1	
"Request Reset" bit must be read as "Readiness for Reset". When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit.			

Reset Flow Control Messages 0

RSTFCTLMSG0 - Reset Flow Control Messages 0						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
CrashLogSaved:	true					
CrashLogVisibility:	cspec					
Address:	08108h					
Soft-Reset and FLR Flow Control Message Registers						
DWord	Bit	Description				
0	31:16	Message Mask				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	RO	_Custom_GTIReset:	BUS
	Access:	RO				
	_Custom_GTIReset:	BUS				
Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000						
15:3	Reserved					
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
2	FLR Done ack from Pmunit					
	<table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>		Access:	R/W Set	_Custom_GTIReset:	BUS
	Access:	R/W Set				
_Custom_GTIReset:	BUS					
FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.						
1	Global Resource Arbitration Acknowledgement Messages					
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>		Access:	R/W	_Custom_GTIReset:	BUS
	Access:	R/W				
_Custom_GTIReset:	BUS					
Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources						
0	CP Busy / Idle Status Acknowledgement Messages					
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>		Access:	R/W	_Custom_GTIReset:	BUS
	Access:	R/W				
_Custom_GTIReset:	BUS					
CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.						



Revision Identification and Class Code register

RID2_CC_0_2_0_PCI - Revision Identification and Class Code register			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00008h		
<p>This register contains the revision number for Device #2 Functions 0 and contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.</p>			
DWord	Bit	Description	
0	31:24	Base Class Code	
		Default Value:	00000011b
		Access:	RO Variant
		_Custom_GTIRReset:	BUS
			<p>This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 03h, indicating a Display Controller Device.</p>
	23:16	Sub-Class Code	
		Default Value:	00000000b
		Access:	RO Variant
		_Custom_GTIRReset:	BUS
			<p>When MGGC0[VAMEN] is 0, this value is 00h. When MGGC0[VAMEN] is 1, this value is 80h, indicating other display device.</p>
	15:8	Programming Interface	
		Default Value:	00000000b
		Access:	RO
_Custom_GTIRReset:		BUS	
		<p>When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.</p>	
7:0	Revision Identification Number		
	Default Value:	00h	
	Access:	R/W Variant	
	_Custom_GTIRReset:	BUS	
		<p>All 8 bits of Revision ID is acquired through fuse pull as per Chassis 2.1 updates</p>	

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT
Address:	1814Ch-1814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_POCSUNIT
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT
Address:	1C014Ch-1C014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0
Address:	1C414Ch-1C414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1
Address:	1C814Ch-1C814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT0
Address:	1D014Ch-1D014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT2
Address:	1D414Ch-1D414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT3
Address:	1D814Ch-1D814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT1
Address:	1E014Ch-1E014Fh

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT4
Address:	1E414Ch-1E414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT5
Address:	1E814Ch-1E814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT2
Address:	1F014Ch-1F014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT6
Address:	1F414Ch-1F414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT7
Address:	1F814Ch-1F814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT3
Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_CCSUNIT0

This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.

This is a global register and context save/restored as part of power context image.

Preemptable Commands	Source
<ul style="list-style-type: none"> • MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection) 	RenderCS

Preemptable Commands	Source
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RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
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Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description											
0	31:21	Last Wrap Count											
	20:2	Preempted Head Offset <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td style="text-align: center;">U19</td> </tr> </table> <p>This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.</p>	Format:	U19									
	Format:	U19											
	1:0	Ring/Batch Indicator <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td>Ring</td> <td>Preemptable command was executed in ring and caused head pointer to be updated.</td> </tr> <tr> <td style="text-align: center;">1h</td> <td>Batch</td> <td>Preemptable command was executed in batch and caused head pointer to be updated.</td> </tr> <tr> <td style="text-align: center;">2h</td> <td>2nd level batch</td> <td>Preemptable command was executed in second level batch and caused head pointer to be updated.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.	1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.	2h	2nd level batch
Value	Name	Description											
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.											
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.											
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.											



Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0203Ch-0203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_RCSUNIT
Address:	1803Ch-1803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_POCSUNIT
Address:	2203Ch-2203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_BCSUNIT
Address:	1C003Ch-1C003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT0
Address:	1C403Ch-1C403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT1
Address:	1C803Ch-1C803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT0
Address:	1D003Ch-1D003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT2
Address:	1D403Ch-1D403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT3
Address:	1D803Ch-1D803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT1
Address:	1E003Ch-1E003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT4

RING_BUFFER_CTL - Ring Buffer Control													
Address:	1E403Ch-1E403Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_VCSUNIT5												
Address:	1E803Ch-1E803Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_VECSUNIT2												
Address:	1F003Ch-1F003Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_VCSUNIT6												
Address:	1F403Ch-1F403Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_VCSUNIT7												
Address:	1F803Ch-1F803Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_VECSUNIT3												
Address:	1A03Ch-1A03Fh												
Name:	Ring Buffer Control												
ShortName:	RING_BUFFER_CTL_CCSUNIT0												
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.</p>													
DWord	Bit	Description											
0	31:21	Reserved											
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ							
	Access:	RO											
	Format:	MBZ											
20:12	Buffer Length	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>U9-1</td> </tr> </table> <p>This field is written by SW to specify the length of the ring buffer in 4 KB Pages. Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 25%;">Value</th> <th style="width: 25%;">Name</th> <th style="width: 50%;">Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td></td> <td>1 page = 4 KB</td> </tr> <tr> <td>1FFh</td> <td></td> <td>512 pages = 2 MB</td> </tr> </tbody> </table>	Format:	U9-1	Value	Name	Description	0		1 page = 4 KB	1FFh		512 pages = 2 MB
		Format:	U9-1										
		Value	Name	Description									
0		1 page = 4 KB											
1FFh		512 pages = 2 MB											
11	RBWait	Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated and the RB will be returned to arbitration.											

RING_BUFFER_CTL - Ring Buffer Control

10	<p>Semaphore Wait</p> <p>Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy. Software can write a "1" to clear this bit, write of "0" has no effect.</p>																
	<p>Programming Notes</p>																
	<p>Writing a value of 1 will unconditionally cancel the semaphore wait on the next memory comparison. Memory comparison is triggered in signal mode on receiving a semaphore signal and in poll mode on wait timer getting expired.</p>																
9:3	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ											
Access:	RO																
Format:	MBZ																
2:1	<p>Automatic Report Head Pointer</p> <p>This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.</p> <p>When Execlist Enable bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr style="background-color: #e1eef6;"> <th style="width: 15%;">Value</th> <th style="width: 30%;">Name</th> <th style="width: 55%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>MI_AUTOREPORT_OFF</td> <td>Automatic reporting disabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td>MI_AUTOREPORT_64KB</td> <td>Report every 16 pages (64KB)</td> </tr> <tr> <td style="text-align: center;">2</td> <td>MI_AUTOREPORT_4KB</td> <td>Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.</td> </tr> <tr> <td style="text-align: center;">3</td> <td>MI_AUTO_REPORT_128KB</td> <td>Report every 32 pages (128KB).</td> </tr> </tbody> </table>		Value	Name	Description	0	MI_AUTOREPORT_OFF	Automatic reporting disabled	1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)	2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.	3	MI_AUTO_REPORT_128KB	Report every 32 pages (128KB).
Value	Name	Description															
0	MI_AUTOREPORT_OFF	Automatic reporting disabled															
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)															
2	MI_AUTOREPORT_4KB	Report every page (4KB) This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.															
3	MI_AUTO_REPORT_128KB	Report every 32 pages (128KB).															
0	<p>Ring Buffer Enable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid.</p>		Format:	Enable													
Format:	Enable																
	<p>Programming Notes</p>																
	<p>Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled and enabled.</p> <ul style="list-style-type: none"> SW must set the Force Wakeup bit to prevent GT from entering C6. SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should 																

RING_BUFFER_CTL - Ring Buffer Control

be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register.

- SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences).
- Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.



Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02034h-02037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_RCSUNIT
Address:	18034h-18037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_POCSUNIT
Address:	22034h-22037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_BCSUNIT
Address:	1C0034h-1C0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT0
Address:	1C4034h-1C4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT1
Address:	1C8034h-1C8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT0
Address:	1D0034h-1D0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT2
Address:	1D4034h-1D4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT3
Address:	1D8034h-1D8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT1
Address:	1E0034h-1E0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT4

RING_BUFFER_HEAD - Ring Buffer Head				
Address:	1E4034h-1E4037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VCSUNIT5			
Address:	1E8034h-1E8037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VECSUNIT2			
Address:	1F0034h-1F0037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VCSUNIT6			
Address:	1F4034h-1F4037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VCSUNIT7			
Address:	1F8034h-1F8037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_VECSUNIT3			
Address:	1A034h-1A037h			
Name:	Ring Buffer Head			
ShortName:	RING_BUFFER_HEAD_CCSUNIT0			
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.</p>				
DWord	Bit	Description		
0	31:21	<p>Wrap Count</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td style="width: 30%;">U11</td> </tr> </table> <p>This field is incremented by 1 whenever the Head Offset wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the Head Offset field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.</p>	Format:	U11
	Format:	U11		
20:2	<p>Head Offset</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Format:</td> <td style="width: 60%;">GraphicsAddress[20:2]</td> </tr> </table> <p>This field indicates the offset of the <i>next</i> instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the Tail Offset. At this point the ring buffer is considered "empty".</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Programming Notes</td> </tr> </table> <p>An RB can be enabled empty or containing some number of valid instructions.</p>	Format:	GraphicsAddress[20:2]	Programming Notes
Format:	GraphicsAddress[20:2]			
Programming Notes				

RING_BUFFER_HEAD - Ring Buffer Head						
	1:0	Reserved				
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02038h-0203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_RCSUNIT
Address:	18038h-1803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_POCSUNIT
Address:	22038h-2203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_BCSUNIT
Address:	1C0038h-1C003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT0
Address:	1C4038h-1C403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT1
Address:	1C8038h-1C803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT0
Address:	1D0038h-1D003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT2
Address:	1D4038h-1D403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT3
Address:	1D8038h-1D803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT1
Address:	1E0038h-1E003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT4

RING_BUFFER_START - Ring Buffer Start					
Address:	1E4038h-1E403Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_VCSUNIT5				
Address:	1E8038h-1E803Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_VECSUNIT2				
Address:	1F0038h-1F003Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_VCSUNIT6				
Address:	1F4038h-1F403Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_VCSUNIT7				
Address:	1F8038h-1F803Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_VECSUNIT3				
Address:	1A038h-1A03Bh				
Name:	Ring Buffer Start				
ShortName:	RING_BUFFER_START_CCSUNIT0				
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.</p>					
DWord	Bit	Description			
0	31:12	<p>Starting Address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.</p>	Format:	GraphicsAddress[31:12]	
	Format:	GraphicsAddress[31:12]			
11:0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02030h-02033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_RCSUNIT
Address:	18030h-18033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_POCSUNIT
Address:	22030h-22033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_BCSUNIT
Address:	1C0030h-1C0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT0
Address:	1C4030h-1C4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT1
Address:	1C8030h-1C8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT0
Address:	1D0030h-1D0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT2
Address:	1D4030h-1D4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT3
Address:	1D8030h-1D8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT1
Address:	1E0030h-1E0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT4

RING_BUFFER_TAIL - Ring Buffer Tail		
Address:	1E4030h-1E4033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VCSUNIT5	
Address:	1E8030h-1E8033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VECSUNIT2	
Address:	1F0030h-1F0033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VCSUNIT6	
Address:	1F4030h-1F4033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VCSUNIT7	
Address:	1F8030h-1F8033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_VECSUNIT3	
Address:	1A030h-1A033h	
Name:	Ring Buffer Tail	
ShortName:	RING_BUFFER_TAIL_CCSUNIT0	
<p>These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.</p>		
DWord	Bit	Description
0	31	Reserved
		Access: RO
		Format: MBZ
30:21	30:21	Reserved
		Access: RO
		Format: MBZ
20:3	20:3	Tail Offset
		Format: GraphicsAddress[20:3]
<p>This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer). Note that all DWords prior to the location indicated by the Tail Offset must contain valid instruction data - which may require instruction padding by software. See Head Offset for more information.</p>		

RING_BUFFER_TAIL - Ring Buffer Tail		
	2:0	Reserved
		Access: RO
		Format: MBZ



Ring Context Address Register 0 for GTI Doorbell Unit

DRBCTXADDR0 - Ring Context Address Register 0 for GTI Doorbell Unit			
Register Space:	MMIO: 0/2/0		
Size (in bits):	64		
Address:	01950h		
DWord	Bit	Description	
0..1	63:32	CTX base address 63:32	
		Access:	R/W
		_Custom_GTIReset:	BUS
		Bits [63:32] of HPA base address which MDRB will use as the offset for its context save / restore	
	31:6	CTX base address 31:6	
		Access:	R/W
		_Custom_GTIReset:	BUS
		Bits [31:6] of HPA base address which MDRB will use as the offset for its context save / restore	
	5:0	Reserved	
		Access:	RO
Format:		MBZ	

Ring Context Start Register for GTI Doorbell Unit

DRBCTXSTART - Ring Context Start Register for GTI Doorbell Unit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0194Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].

In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000.

Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	Context Save Mask
		Access: WO
		_Custom_GTIReset: BUS
This registers isn't context save/restored.		
15:2	Reserved	Access: RO
		Format: MBZ
1:0	Context start	Access: R/W Hardware Clear
		_Custom_GTIReset: BUS
		RPM will program these bits to notify MDRB to initiate either a context save or a context restore. MDRB will clear these bits once the context procedure is completed and the ACK is sent back to RPM. 2'b11 = Reserved 2'b10 = Context restore start 2'b01 = Context save start 2'b00 = Normal operation - DEFAULT Programming Note - It is assumed that this value will be static once programmed and not changed until MDRB clears the bits after ACKing the context procedure back to RPM



RMTIMEOUTREG_CAPTURE

RMTIMEOUTREG_CAPTURE		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	420E0h-420E3h	
Name:	RM TIMEOUT REGISTER OFFSET	
ShortName:	RMTIMEOUTREG_CAPTURE	
Reset:	soft	
DWord	Bit	Description
0	31:0	REGISTER OFFSET VALUE Access: RO Offset of the Register that caused RM TIMEOUT.

RSA for uOS/Soft Scratch

UOS_RSA_SCRATCH - RSA for uOS/Soft Scratch		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Description		
<p>There are 64 Dword registers (2048 bits) for RSA check for uOS code, which is performed by the on chip Boot ROM code. This RSA check is done to ensure that the full HASH check value used for Hash operation of the uOS by Shim, itself is correct. These registers can also be used as Soft Scratch registers defined for use after the RSA operation at Boot. Note that these registers contents are not context saved/restored for C6 purposes. Usage: The Host programs these 64 registers, before programming the DMA. The Boot ROM then on being initiated reads these 64 registers and starts the RSA unwrap.</p>		
DWord	Bit	Description
0	31:0	RSA/Scratch

RTADDR_LSB

RTADDR_LSB - RTADDR_LSB			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	124830h		
Register providing the base address of root-entry table.			
DWord	Bit	Description	
0	31:12	RTA	
		Default Value:	0000000h
		Access:	R/W
		_Custom_GTIReset:	BUS
			This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
	11	RTT	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
			This field specifies the type of root-table referenced by the Root Table Address (RTA) field; 0: Root Table1: Extended Root Table
10:0	Reserved		
	Access:	RO	
	Format:	MBZ	

RTADDR_MSB

RTADDR_MSB - RTADDR_MSB			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	124834h		
Register providing the base address of root-entry table.			
DWord	Bit	Description	
0	31:14	Reserved	
		Access:	RO
		Format:	MBZ
	13:7	Reserved	
		Access:	RO
		Format:	MBZ
	6:0	RTA	
		Default Value:	00h
		Access:	R/W
_Custom_GTIReset:		BUS	
<p>This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.</p>			



RTT_CR_SPARE

RTT_CR_SPARE		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	168B90h-168B93h	
Name:	RTT_CR_SPARE	
ShortName:	RTT_CR_SPARE	
Reset:	global	
Spare registers for RTT Lane		
DWord	Bit	Description
0	31:0	cfg_rtt_cr_spare
		Default Value: 0041000h cfg_rtt_cr_spare_defaultreset
		Access: R/W
		PCS_Glue::RTT_CR_SPARE::rtt_cr_spare

Sampler control register

SAMPLER_CTL - Sampler control register		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0E140h	
DWord	Bit	Description
0	31:16	ECO Reserved 1 Reserved: MBZ
	15:8	Reserved
	7	ECO Reseved 7
	6	ECO Reseved 6
	5	ECO Reseved 5
	4	ECO Reseved 4
	3	ECO Reseved 3
	2	ECO Reseved 2
	1	ECO Reseved 1
	0	ECO Reseved 0



Sampler Dummy Register

SMP_DUMMY - Sampler Dummy Register		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0E000h	
Name:	Sampler Dummy Address	
ShortName:	Sampler_Dummy_Address	
This register is defined so that a non-posted MMIO cycle to this destination would ensure all cycles are flushed on the message channel between the source and destination. This register is used in the engine context to ensure all state is delivered. The value programmed in this register must not change the behavior of the GPU.		
DWord	Bit	Description
0	31:0	Reserved
		Access: RO
		Format: MBZ

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register											
Register Space:	MMIO: 0/2/0										
Access:	R/W										
Size (in bits):	32										
_Custom_GTIReset:	DEV										
Address:	0E18Ch										
Name:	SAMPLER Mode Register										
ShortName:	SAMPLER_MODE										
<p>This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.</p>											
DWord	Bit	Description									
0	31:16	Mask									
		<table border="1"> <tr> <td>Access:</td> <td>WO</td> </tr> <tr> <td>Format:</td> <td>Mask</td> </tr> </table>	Access:	WO	Format:	Mask					
Access:	WO										
Format:	Mask										
15		enable smallPL									
		<table border="1"> <tr> <td>Format:</td> <td>enable</td> </tr> </table>	Format:	enable							
		Format:	enable								
		Programming Notes									
<p>This bit MUST be set to ensure optimal power in 3D Sampler.</p> <p>Must not be enabled if cache_flush message is sent to sampler.</p>											
14		L1 Cache Set Selection									
		This field controls how Set0 and Set1 of the Sampler L1 Cache are selected.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Extended_Tag [Default]</td> <td>When this bit is set to 0h, Sampler will use Bit 8 of the Extended Tag To Control Set selection.</td> </tr> <tr> <td>1h</td> <td>XOR_UVQ</td> <td>When this bit is set to 1h, Sampler will use an XOR of Various u, v, and q texel coordinate bits to select set</td> </tr> </tbody> </table>	Value	Name	Description	0h	Extended_Tag [Default]	When this bit is set to 0h, Sampler will use Bit 8 of the Extended Tag To Control Set selection.	1h	XOR_UVQ	When this bit is set to 1h, Sampler will use an XOR of Various u, v, and q texel coordinate bits to select set
		Value	Name	Description							
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1h	XOR_UVQ	When this bit is set to 1h, Sampler will use an XOR of Various u, v, and q texel coordinate bits to select set									
13:12		Sampler Cache Set XOR selection									
		<table border="1"> <tr> <td>Format:</td> <td>U2</td> </tr> </table>	Format:	U2							
		Format:	U2								
		<p>These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.</p>									
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>None</td> <td>No XOR.</td> </tr> <tr> <td>01b</td> <td>Scheme 1</td> <td>New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows</td> </tr> </tbody> </table>	Value	Name	Description	00b	None	No XOR.	01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows		
Value	Name	Description									
00b	None	No XOR.									
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SAMPLER_MODE - SAMPLER Mode Register

			ranging from a pitch of 1 tile to 16 tiles.
	10b	Scheme 2	<p> $\text{New_set_mask}[3] = \text{Tiled_address}[17] \wedge \text{Tiled_address}[16].$ $\text{New_set_mask}[2] = \text{Tiled_address}[16] \wedge \text{Tiled_address}[15].$ $\text{New_set_mask}[1] = \text{Tiled_address}[15] \wedge \text{Tiled_address}[14].$ $\text{New_set_mask}[0] = \text{Tiled_address}[14] \wedge \text{Tiled_address}[13].$ $\text{New_set}[3:0] \text{ less than or } = \text{New_set_mask}[3:0] \wedge \text{Old_set}[3:0].$ Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets. </p>
	11b	Scheme 3 [Default]	<p> $\text{New_set_mask}[3] = \text{Tiled_address}[22] \wedge \text{Tiled_address}[21] \wedge \text{Tiled_address}[20] \wedge \text{Tiled_address}[19].$ $\text{New_set_mask}[2] = \text{Tiled_address}[18] \wedge \text{Tiled_address}[17] \wedge \text{Tiled_address}[16].$ $\text{New_set_mask}[1] = \text{Tiled_address}[15] \wedge \text{Tiled_address}[14].$ $\text{New_set_mask}[0] = \text{Tiled_address}[13].$ $\text{New_set}[3:0] \text{ less than or } = \text{New_set_mask}[3:0] \wedge \text{Old_set}[3:0].$ Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more. </p>
Programming Notes			
This field should be programmed as "00b" corresponding to NO XOR option when 3D map performance fix in MT is enabled using the field "Sampler Set Remapping for 3D Disable" in the SAMPLER Mode Register.			
11:10	ECO Reserved 2b		
	Format:	MBZ	
9	ECO_SCRATCH_9		
	Format:	MBZ	
8	Sampler L2 Disable		
	Format:	Disable	
Will disable the L2 cache and force all access to be misses			
7	ECO Reserved 3		
	Format:	MBZ	
6	Compressed Overfill disable		
	Format:	disable	
5	Headerless Message for Pre-emptable Contexts		
	Format:	Enable	
When set to 1h, this bit enables sampler to support headerless messages for pre-emptable GPGPU contexts. When set to 0h, it reverts to the previous behavior where pre-emptable GPGPU contexts must have headers on all sampler messages.			

SAMPLER_MODE - SAMPLER Mode Register

	Value	Name	Description
	0h		Headers must be used on all sampler messages if this bit is programmed to 0h.
	1h	[Default]	Headerless sampler messages may be used for pre-emptable contexts (this is the default behavior all contexts)
4	ECO Reserved		
3	ECO Reserved 5		
	Format:		MBZ
2	ECO Reserved 4-2		
1	PL float to fix precision fix disable		
	Format:		disable
	If disabled use legacy behavior		
0	Indirect State Base Addr Override		
	Format:		Enable
	<p>This bit is used to control whether Indirect State (Border Color) to be relative to same base address as SAMPLER_STATE or relative to the DYNAMIC_STATE_BASE_ADDR</p> <p>This bit must be set to 1. Border Color must be in the Dynamic State heap in order to allow for resource copy of sampler state to work correctly.</p>		
	Value	Name	Description
	0h	OVERRIDE_DISABLE [Default]	When set to 0h, this bit allows Indirect State (.e.g Border Color) to be stored in the Bindless Sampler State heap. This bit should not be set to 0h by SW as this will prevent resource copies of sampler state from being done correct when border color is required.
	1h	OVERRIDE_ENABLE	When set to 1h, this bit allows Indirect State (e.g. Border Color) to be stored in the Dynamic State heap. This bit must be set to 1h by SW to ensure resource copies of sampler state are done correctly when border color is required.



SAMPLER READ DATA

SAMPLER_RDATA - SAMPLER READ DATA		
Register Space:	MMIO: 0/2/0	
Access:	RO Variant	
Size (in bits):	32	
Address:	0E144h	
DWord	Bit	Description
0	31:0	Reserved

SCRATCH 1 from LPFCunit

SCRATCH_LPFC1 - SCRATCH 1 from LPFCunit		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B474h	
DWord	Bit	Description
0	31:0	SCRATCH bits from LPFCunit
		Access: R/W
		_Custom_GTIReset: DEV



SCRATCH 2 for LNCFunit

SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit			
Register Space:		MMIO: 0/2/0	
Size (in bits):		32	
Address:		0B0A0h	
DWord	Bit	Description	
0	31:23	Reserved	
		Access:	RO
		Format:	MBZ
	22:3	SCRATCH 2 field for LNCFunit	
		Access:	R/W
		_Custom_GTIReset:	DEV
	2	Colored GSYNC Disable	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	DEV
	1	LNI Cross-Slice Tracking Queue Disable	
		Access:	R/W
_Custom_GTIReset:		DEV	
Value		Name	Description
0		[Default]	LNI will only use the fifth tracking queue, allow two tracking queues for cross-slice cycles
1			LNI will only allocate one tracking queue for cross-slice cycles
0		Reserved	
	Access:	RO	
	Format:	MBZ	

SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register											
Register Space:	MMIO: 0/2/0										
Access:	R/W										
Size (in bits):	32										
_Custom_GTIReset:	DEV										
Address:	0B140h										
DWord	Bit	Description									
0	31:30	SCRATCH31									
	29:28	SCRATCH29									
	27	Reserved									
		Access:	RO								
		Format:	MBZ								
	26	SBFT Physical Override This bit-field will enable DFT to control the physical(coherent) attribute of cacheline being loaded into L3 during SBFT loading. This bit-field can be set to 1 only during SBFT loading/testing. DFX will handle making sure these get set properly (ie take care of race conditions between loading and setting the bits, etc) L3 can make the assumption that no cycles will be in-flight when the values are changing. DFX will only change the value when transactions are idle.									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>[Default]</td> <td>Physical Vs. Virtual indication sent by LSQC will be used</td> </tr> <tr> <td>1</td> <td></td> <td>Coherent lines will be loaded in L3 during SBFT loading. L3 is in SBFT loading/testing phase. Can be set to 1 only during SBFT loading/testing</td> </tr> </tbody> </table>	Value	Name	Description	0	[Default]	Physical Vs. Virtual indication sent by LSQC will be used	1		Coherent lines will be loaded in L3 during SBFT loading. L3 is in SBFT loading/testing phase. Can be set to 1 only during SBFT loading/testing
	Value	Name	Description								
	0	[Default]	Physical Vs. Virtual indication sent by LSQC will be used								
	1		Coherent lines will be loaded in L3 during SBFT loading. L3 is in SBFT loading/testing phase. Can be set to 1 only during SBFT loading/testing								
25:21	SCRATCH25										
20:15	Reserved										
	Access:	RO									
	Format:	MBZ									
14:9	Reserved										
	Access:	RO									
	Format:	MBZ									
8:4	LTCD EBB Conflict L3-Read Aging count This bit-field will determine the number of EBB conflicts experienced by the L3-read in order to age in the L3 FIFO.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>10</td> <td>[Default]</td> </tr> <tr> <td>[1,31]</td> <td></td> </tr> </tbody> </table>	Value	Name	10	[Default]	[1,31]					
Value	Name										
10	[Default]										
[1,31]											

SCRATCH2 - SCRATCH2 Register

3	<p>LTCD EBB Conflict L3-Read Aging enable</p> <p>This bit-field will enable L3-Read aging in LTCD dataunit due to EBB conflicts. During EBB conflicts, L3-fill will be preferred over L3-reads, and this aggressive fill selection can hold up the reads in L3 FIFO depending on the duration of EBB conflicts. L3-read aging will ensure fairness to an L3-read cycle that has been held back due to EBB conflicts by making the L3-fills ineligible once the read has aged.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">[Default]</td> <td>LTCD EBB conflict L3-Read aging is enabled</td> </tr> <tr> <td style="text-align: center;">0</td> <td></td> <td>LTCD EBB conflict L3-Read aging is disabled</td> </tr> </tbody> </table>	Value	Name	Description	1	[Default]	LTCD EBB conflict L3-Read aging is enabled	0		LTCD EBB conflict L3-Read aging is disabled
Value	Name	Description								
1	[Default]	LTCD EBB conflict L3-Read aging is enabled								
0		LTCD EBB conflict L3-Read aging is disabled								
2	<p>SCRATCH2</p>									
1	<p>LTCD L3 FIFO OOO Disable</p> <p>This bit-field will disable L3 FIFO OOO implementation in LTCD-dataunit and revert to implementation where only one L3 FIFO was used.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">[Default]</td> <td>LTCD L3 FIFO OOO implementation is enabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td></td> <td>LTCD L3 FIFO OOO implementation is disabled</td> </tr> </tbody> </table>	Value	Name	Description	0	[Default]	LTCD L3 FIFO OOO implementation is enabled	1		LTCD L3 FIFO OOO implementation is disabled
Value	Name	Description								
0	[Default]	LTCD L3 FIFO OOO implementation is enabled								
1		LTCD L3 FIFO OOO implementation is disabled								
0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
Access:	RO									
Format:	MBZ									

SCRATCH 3 for LNCFunit

SCRATCH_LNCF3 - SCRATCH 3 for LNCFunit						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	0B0A8h					
DWord	Bit	Description				
0	31:0	SCRATCH 3 field for LNCFunit <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> Bit[0] : LSN VR MARK Performance fix Disable. 0 : (Default) Performance fix is enabled. 1 : Disables performance fix.	Access:	R/W	_Custom_GTIReset:	DEV
Access:	R/W					
_Custom_GTIReset:	DEV					



SCRATCH3 Register

SCRATCH3 - SCRATCH3 Register			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	0B154h		
DWord	Bit	Description	
0	31:13	SPARE FIELDS	
	12	Merge Disable for non-128B Compressible Writes	
		Default Value:	0
		Access:	R/W
Format:		Disable	
	_Custom_GTIReset:	DEV	
By default, if compression partial write merging support is enabled, all compressible writes can serve as mergeable parent cycles. If this bit is set, L3 will limit merging for compressible surfaces to only apply when receiving a 128B write (marked as such by the client).			
11	Force Uncacheable Big Hammer		
	Value	Name Description	
	0	[Default] All the POR rules for Cacheable vs Uncacheable are applied	
	1	<ul style="list-style-type: none"> All the POR rules for C/UC will be overridden and every L3 cycle is made as L3 Uncacheable. Note: This does not apply for URB related transactions. 	
10:8	LTCD TAG ROINV FSM WAIT TIME		
	Used to derive the number of clocks for which the ROINV FSM will wait, in a WAIT state, prior to invalidating the state arrays. Valid values start from 4 to account for time it takes ltcc to receive roinv in progress and stall its pipeline towards LTCD-TAGUNIT, to ensure that any functional cycles that sneaks in TAG for those clocks are serviced gracefully.		
	Value	Name	
	4	default [Default]	
	[4,7]	range	
7:4	LTCD DATA INIT FSM WAIT TIME		
	Used to derive the number of 2x clocks for which the DATA-INIT FSM will wait, in a WAIT state, prior to initializing the data arrays. Final-wait time = 2**this-reg-fields-value.		
	Value	Name	
	4	default [Default]	
	[4,12]	range	

SCRATCH3 - SCRATCH3 Register		
	3:0	Reserved
		Access: RO
		Format: MBZ



Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT
Address:	1813Ch-1813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_POCSUNIT
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT
Address:	1C013Ch-1C013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0
Address:	1C413Ch-1C413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1
Address:	1C813Ch-1C813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT0
Address:	1D013Ch-1D013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT2
Address:	1D413Ch-1D413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT3
Address:	1D813Ch-1D813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT1
Address:	1E013Ch-1E013Fh

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VCSUNIT4

Address: 1E413Ch-1E413Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VCSUNIT5

Address: 1E813Ch-1E813Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VECSUNIT2

Address: 1F013Ch-1F013Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VCSUNIT6

Address: 1F413Ch-1F413Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VCSUNIT7

Address: 1F813Ch-1F813Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_VECSUNIT3

Address: 1A13Ch-1A13Fh

Name: Second Level Batch Buffer Head Pointer Preemption Register

ShortName: SBB_PREEMPT_ADDR_CCSUNIT0

Description

This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred.

This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer.

Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlistin Exec-List mode of scheduling.

This is a global register and context save/restored as part of power context image.

Refer to **Preemption > Execlst Scheduling** for a list of preemptible commands.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
-------	-----	-------------

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

0	31:2	Second Level Batch Buffer Head Pointer	
		Format:	GraphicsAddress[31:2]
	This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.		
	1:0	Reserved	
Access:		RO	
Format:		MBZ	

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02114h-02117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_RCSUNIT
Address:	18114h-18117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_POCSUNIT
Address:	22114h-22117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_BCSUNIT
Address:	1C0114h-1C0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT0
Address:	1C4114h-1C4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT1
Address:	1C8114h-1C8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT0
Address:	1D0114h-1D0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT2
Address:	1D4114h-1D4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT3
Address:	1D8114h-1D8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT1
Address:	1E0114h-1E0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT4

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Address:	1E4114h-1E4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT5
Address:	1E8114h-1E8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT2
Address:	1F0114h-1F0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT6
Address:	1F4114h-1F4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT7
Address:	1F8114h-1F8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT3
Address:	1A114h-1A117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_CCSUNIT0

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description		
0	31:2	Second Level Batch Buffer Head Pointer <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Format:</td> <td>GraphicsAddress[31:2]</td> </tr> </table> <p>This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".</p>	Format:	GraphicsAddress[31:2]
		Format:	GraphicsAddress[31:2]	
	1 Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:	RO			
Format:	MBZ			
0 Valid <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>U1</td> </tr> </table>	Format:	U1		
Format:	U1			

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	Value	Name	Description
	0h	Invalid [Default]	Second Level Batch buffer Invalid
	1h	Valid	Second Batch buffer Valid.



Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02118h-0211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_RCSUNIT
Address:	18118h-1811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_POCSUNIT
Address:	22118h-2211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_BCSUNIT
Address:	1C0118h-1C011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT0
Address:	1C4118h-1C411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT1
Address:	1C8118h-1C811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT0
Address:	1D0118h-1D011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT2
Address:	1D4118h-1D411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT3
Address:	1D8118h-1D811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT1
Address:	1E0118h-1E011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT4

SBB_STATE - Second Level Batch Buffer State Register

Address:	1E4118h-1E411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT5
Address:	1E8118h-1E811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT2
Address:	1F0118h-1F011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT6
Address:	1F4118h-1F411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT7
Address:	1F8118h-1F811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT3
Address:	1A118h-1A11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_CCSUNIT0

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description			
0	31:10	Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
9		POSH Start <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Exists If:</td> <td>//RCS, POCS</td> </tr> </table> <p>This bit reflects the POSH Start value programmed by the active first level MI_BATCH_BUFFER_START command.</p>	Exists If:	//RCS, POCS	
Exists If:	//RCS, POCS				
8		POSH Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Exists If:</td> <td>//RCS, POCS</td> </tr> </table> <p>This bit reflects the POSH Enable value programmed by the active first level MI_BATCH_BUFFER_START command.</p>	Exists If:	//RCS, POCS	
Exists If:	//RCS, POCS				
7:6		Reserved			
		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
Access:	RO				
Format:	MBZ				

SBB_STATE - Second Level Batch Buffer State Register

	5	Address Space Indicator Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START.									
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th style="width: 65%;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">GGTT [Default]</td> <td>This second level batch buffer is located in GGTT memory and is privileged</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">PPGTT</td> <td>This second level batch buffer is located in PPGTT memory and is non-privileged.</td> </tr> </tbody> </table>	Value	Name	Description	0h	GGTT [Default]	This second level batch buffer is located in GGTT memory and is privileged	1h	PPGTT	This second level batch buffer is located in PPGTT memory and is non-privileged.
	Value	Name	Description								
	0h	GGTT [Default]	This second level batch buffer is located in GGTT memory and is privileged								
	1h	PPGTT	This second level batch buffer is located in PPGTT memory and is non-privileged.								
4	Reserved										
3:0	Reserved										
	Access:	RO									
	Format:	MBZ									

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02138h-0213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT
Address:	18138h-1813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_POCSUNIT
Address:	22138h-2213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT
Address:	1C0138h-1C013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0
Address:	1C4138h-1C413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1
Address:	1C8138h-1C813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT0
Address:	1D0138h-1D013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT2
Address:	1D4138h-1D413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT3
Address:	1D8138h-1D813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT1
Address:	1E0138h-1E013Bh

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT4
Address:	1E4138h-1E413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT5
Address:	1E8138h-1E813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT2
Address:	1F0138h-1F013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT6
Address:	1F4138h-1F413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT7
Address:	1F8138h-1F813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT3
Address:	1A138h-1A13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_CCSUNIT0

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:25	Reserved
		Access: RO
		Format: MBZ
	24:16	Reserved
		Access: RO
		Format: MBZ
15:0	Second Level Batch Buffer Head Pointer Upper DWORD	
	Format: GraphicsAddress[47:32]	

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0211Ch-0211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_RCSUNIT
Address:	1811Ch-1811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_POCSUNIT
Address:	2211Ch-2211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_BCSUNIT
Address:	1C011Ch-1C011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT0
Address:	1C411Ch-1C411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT1
Address:	1C811Ch-1C811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT0
Address:	1D011Ch-1D011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT2
Address:	1D411Ch-1D411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT3
Address:	1D811Ch-1D811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT1
Address:	1E011Ch-1E011Fh

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT4
Address:	1E411Ch-1E411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT5
Address:	1E811Ch-1E811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT2
Address:	1F011Ch-1F011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT6
Address:	1F411Ch-1F411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT7
Address:	1F811Ch-1F811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT3
Address:	1A11Ch-1A11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_CCSUNIT0

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space, where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Programming Notes

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description	
0	31:25	Reserved	
		Access:	RO
		Format:	MBZ
	24:16	Reserved	
		Access:	RO
		Format:	MBZ
15:0	Batch Buffer Head Pointer Upper DWORD		
	Format:	GraphicsAddress[47:32]	

SEL_FETCH_PLANE_CTL

SEL_FETCH_PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70890h-70893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_A
Reset:	soft
Address:	708B0h-708B3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_A
Reset:	soft
Address:	708D0h-708D3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_A
Reset:	soft
Address:	708F0h-708F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_A
Reset:	soft
Address:	70920h-70923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_A
Reset:	soft
Address:	70940h-70943h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_6_A
Reset:	soft
Address:	70960h-70963h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_7_A
Reset:	soft
Restriction	

SEL_FETCH_PLANE_CTL

Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description						
0	31	<p>Selective Fetch Plane Enable When this bit is set, Plane is enabled for selective fetch update.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	30:0	Spares						

Semaphore Interrupt Register

GUC_SEM_INTR - Semaphore Interrupt Register										
Register Space:	MMIO: 0/2/0									
Size (in bits):	32									
Bits are set based on the Semaphore Token number sent by Command streamer Read and cleared by the MinIA uKernel or host CPU.										
DWord	Bit	Description								
0	31:0	<table border="1"> <thead> <tr> <th colspan="2">Semaphore Token ID</th> </tr> </thead> <tbody> <tr> <td>Default Value:</td> <td>0000h</td> </tr> <tr> <td>Access:</td> <td>R/WC</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </tbody> </table>	Semaphore Token ID		Default Value:	0000h	Access:	R/WC	_Custom_GTIRreset:	BUS
Semaphore Token ID										
Default Value:	0000h									
Access:	R/WC									
_Custom_GTIRreset:	BUS									



Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0224Ch-0224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_RCSUNIT
Address:	1824Ch-1824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_POCSUNIT
Address:	2224Ch-2224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_BCSUNIT
Address:	1C024Ch-1C024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT0
Address:	1C424Ch-1C424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT1
Address:	1C824Ch-1C824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT0
Address:	1D024Ch-1D024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT2
Address:	1D424Ch-1D424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT3
Address:	1D824Ch-1D824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT1
Address:	1E024Ch-1E024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT4

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait

Address:	1E424Ch-1E424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT5
Address:	1E824Ch-1E824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT2
Address:	1F024Ch-1F024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT6
Address:	1F424Ch-1F424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT7
Address:	1F824Ch-1F824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT3
Address:	1A24Ch-1A24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_CCSUNIT0

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out. When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description				
0	31:21	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
	20:0	<p>Poll Interval</p> <p>Minimum number of micro-seconds allowed</p>				



Semaphore Signal Port

SEMAPHORE_SIGNAL_PORT - Semaphore Signal Port	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02020h-02023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_RCSUNIT
Address:	18020h-18023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_POCSUNIT
Address:	22020h-22023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_BCSUNIT
Address:	1C0020h-1C0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT0
Address:	1C4020h-1C4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT1
Address:	1C8020h-1C8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT0
Address:	1D0020h-1D0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT2
Address:	1D4020h-1D4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT3
Address:	1D8020h-1D8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT1
Address:	1E0020h-1E0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT4

SEMAPHORE_SIGNAL_PORT - Semaphore Signal Port				
Address:	1E4020h-1E4023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT5			
Address:	1E8020h-1E8023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT2			
Address:	1F0020h-1F0023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT6			
Address:	1F4020h-1F4023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT7			
Address:	1F8020h-1F8023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT3			
Address:	1A020h-1A023h			
Name:	SEMAPHORE_SIGNAL_PORT			
ShortName:	SEMAPHORE_SIGNAL_PORT_CCSUNIT0			
<p>Each engine implements SEMAPHORE_SIGNAL_PORT register for receiving semaphore signal from the scheduler (SW or FW). A write to the SEMAPHORE_SIGNAL_PORT with data as 0xFFFF_FFFF is decoded as semaphore signal by an engine. An engine waiting on un-successful MI_SEMAPHORE_WAIT (signal mode) command will reacquire the semaphore data from memory and re-evaluate the semaphore comparison on receiving the semaphore signal. SEMAPHORE_SIGNAL_PORT register is privileged. Writing to the SEMAPHORE_SIGNAL_PORT of an idle engine (no context) does not trigger any action in HW and is of no use.</p>				
DWord	Bit	Description		
0	31:0	Semaphore Signal Value <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Format:</td> <td>U32</td> </tr> </table>	Format:	U32
Format:	U32			



Semaphore Token

SEMAPHORE_TOKEN - Semaphore Token	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	022B4h-022B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_RCSUNIT
Address:	182B4h-182B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_POCSUNIT
Address:	222B4h-222B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_BCSUNIT
Address:	1C02B4h-1C02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT0
Address:	1C42B4h-1C42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT1
Address:	1C82B4h-1C82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT0
Address:	1D02B4h-1D02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT2
Address:	1D42B4h-1D42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT3
Address:	1D82B4h-1D82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT1
Address:	1E02B4h-1E02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT4

SEMAPHORE_TOKEN - Semaphore Token					
Address:	1E42B4h-1E42B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_VCSUNIT5				
Address:	1E82B4h-1E82B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_VECSUNIT2				
Address:	1F02B4h-1F02B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_VCSUNIT6				
Address:	1F42B4h-1F42B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_VCSUNIT7				
Address:	1F82B4h-1F82B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_VECSUNIT3				
Address:	1A2B4h-1A2B7h				
Name:	SEMAPHORE_TOKEN				
ShortName:	SEMAPHORE_TOKEN_CCSUNIT0				
<p>This register holds the Producer Token Number programmed by the SW. Producer Token Number is reported to the GUC by an engine on executing MI_SEMAPHORE_SIGNAL command. SEMAPHORE_TOKEN register is privileged and context save/restored.</p>					
DWord	Bit	Description			
0	31:27	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
26:0	Producer Token Number				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>U27</td> </tr> </table>	Format:	U27		
Format:	U27				
		Description			
		This field specifies the token value (bit vector) that is sent to GuC from the CS			

Slice 0 BONUS1 Reg

SLOSPCBONUS1 - Slice 0 BONUS1 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24194h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS1 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS1 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	5	BONUS1 BIT 5	
Access:		R/W	
_Custom_GTIReset:		BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS1 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS1 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SL0SPCBONUS1 - Slice 0 BONUS1 Reg				
	'1' : Initiate power up sequence (clk/rst/fwe)			
2	BONUS1 BIT 2			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Slice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req</p>	Access:	R/W	_Custom_GTIRreset:
Access:	R/W			
_Custom_GTIRreset:	BUS			
1	BONUS1 BIT 1			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)</p>	Access:	R/W	_Custom_GTIRreset:
Access:	R/W			
_Custom_GTIRreset:	BUS			
0	BONUS1 BIT 0			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Slice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req</p>	Access:	R/W	_Custom_GTIRreset:
Access:	R/W			
_Custom_GTIRreset:	BUS			

Slice 0 BONUS2 Reg

SLOSPCBONUS2 - Slice 0 BONUS2 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24198h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS2 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS2 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS2 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS2 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS2 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SL0SPCBONUS2 - Slice 0 BONUS2 Reg				
	'1' : Initiate power up sequence (clk/rst/fwe)			
2	BONUS2 BIT 2			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Slice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W			
_Custom_GTIReset:	BUS			
1	BONUS2 BIT 1			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W			
_Custom_GTIReset:	BUS			
0	BONUS2 BIT 0			
	<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Slice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W			
_Custom_GTIReset:	BUS			

Slice 0 PGFET control register with lock

SL0SPCPFETCTL - Slice 0 PGFET control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24188h		
DWord	Bit	Description	
0	31	PFET Control Lock	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
		Reserved	
30:24		Access:	RO
		Format:	MBZ
23		Power Well Status	
		Access:	RO
		_Custom_GTIRreset:	BUS
0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.			
22		Reserved	
		Access:	RO
Format:		MBZ	
21:19		Delay from enabling secondary PFETs to power good.	
		Default Value:	111b
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns			

SL0SPCPFETCTL - Slice 0 PGFET control register with lock

18:16	Strobe pulse period	
	Access:	R/W Lock
	_Custom_GTIRreset:	BUS
	Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
	Value	Name
	001b	[Default]
15:0	PFET Ladder Step Sequence	
	Access:	R/W Lock
	_Custom_GTIRreset:	BUS
	PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetldrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?.15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.	
	Value	Name
	1000011111111001b	[Default]



Slice 0 Power Context Save request

SLOPGCTXREQ - Slice 0 Power Context Save request			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24184h		
DWord	Bit	Description	
0	31:16	Message Mask	
		Access:	RO
		_Custom_GTIReset:	BUS
		Message Mask bits for lower 16 bits	
15:10	Reserved	Access:	RO
		Format:	MBZ
9	Power context save request	Access:	R/W Set
		_Custom_GTIReset:	BUS
		Power Context Save Request	
		1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.	
8:0	Power Context Save request credit count	Access:	R/W
		_Custom_GTIReset:	BUS
		QWord Credits for Power Context Save Request	
		Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).	

Slice 0 Power Down FSM control register with lock

SLOSPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24190h		
DWord	Bit	Description	
0	31	power down control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:13		Reserved	
		Access:	RO
		Format:	MBZ
12		Leave firewall disabled	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow	
11		Leave reset de-asserted	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow	
10		Leave CLKs ON	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:	

SLOSPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

		0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow	
	9	Leave FET On	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow	
	8:0	Reserved	
		Access:	RO
		Format:	MBZ

Slice 0 Power Gate Control Request

SLOPGCTLREQ - Slice 0 Power Gate Control Request				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	24180h			
Clock Gating Messages Register				
DWord	Bit	Description		
0	31:16	Message Mask		
		Access:	RO	
		_Custom_GTIRreset:	BUS	
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000		
	15:2	Reserved		
		Access:	RO	
	1	15:2	Format:	MBZ
			CLK RST FWE Request	
		Access:	R/W	
		_Custom_GTIRreset:	BUS	
	SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
	0	0	Power Gate Request	
Access:			R/W	
_Custom_GTIRreset:		BUS		
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req				



Slice 0 Power on FSM control register with lock

SLOSPCPOWERUPFSMCTL - Slice 0 Power on FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	2418Ch		
DWord	Bit	Description	
0	31	power up control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	30:9	Reserved	
		Access:	RO
		Format:	MBZ
	8:0	Reserved	
		Access:	RO
		Format:	MBZ

Slice 0 SubSlice 0 PGFET control register with lock

SSMOSPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24408h		
DWord	Bit	Description	
0	31	PFET Control Lock	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:24		Reserved	
		Access:	RO
		Format:	MBZ
23		Power Well Status	
		Access:	RO
		_Custom_GTIRreset:	BUS
		0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
22		Powergood timer error	
		Access:	RO
		_Custom_GTIRreset:	BUS
		0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
21:19		Delay from enabling secondary PFETs to power good.	
		Default Value:	101b
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns			

SSMOSPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock

		3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns						
	18:16	Strobe pulse period <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <tr> <td style="width: 70%;">Default Value:</td> <td>011b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)</p>	Default Value:	011b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	011b							
Access:	R/W Lock							
_Custom_GTIReset:	BUS							
	15:0	PFET Ladder Step Sequence <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1111111111111111b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetldrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?.15; Steps 1, 2, 3 are skipped. 15'D55h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.</p>	Default Value:	1111111111111111b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	1111111111111111b							
Access:	R/W Lock							
_Custom_GTIReset:	BUS							

Slice 0 SubSlice 1 PGFET control register with lock

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24488h		
DWord	Bit	Description	
0	31	PFET Control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
		Reserved	
30:24		Access:	RO
		Format:	MBZ
23		Power Well Status	
		Access:	RO
		_Custom_GTIReset:	BUS
0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.			
22		Powergood timer error	
		Access:	RO
		_Custom_GTIReset:	BUS
0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.			
21:19		Delay from enabling secondary PFETs to power good.	
		Default Value:	101b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns			

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock

		<p>3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns</p>						
	18:16	<p>Strobe pulse period</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>011b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)</p>	Default Value:	011b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	011b							
Access:	R/W Lock							
_Custom_GTIReset:	BUS							
	15:0	<p>PFET Ladder Step Sequence</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1111111111111111b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetldrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D55h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.</p>	Default Value:	1111111111111111b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	1111111111111111b							
Access:	R/W Lock							
_Custom_GTIReset:	BUS							

Slice 0 SubSlice 2 PGFET control register with lock

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24508h		
DWord	Bit	Description	
0	31	PFET Control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:24		Reserved	
		Access:	RO
		Format:	MBZ
23		Power Well Status	
		Access:	RO
		_Custom_GTIReset:	BUS
		0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
22		Powergood timer error	
		Access:	RO
		_Custom_GTIReset:	BUS
		0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
21:19		Delay from enabling secondary PFETs to power good.	
		Default Value:	101b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns	

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock

		3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns						
	18:16	Strobe pulse period <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <tr> <td style="width: 60%;">Default Value:</td> <td>011b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 23ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)</p>	Default Value:	011b	Access:	R/W Lock	_Custom_GTIRreset:	BUS
Default Value:	011b							
Access:	R/W Lock							
_Custom_GTIRreset:	BUS							
	15:0	PFET Ladder Step Sequence <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1111111111111111b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetldrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?15. 15'FFF1h: Ladder step goes 0, 4, 5, 6, ?15; Steps 1, 2, 3 are skipped. 15'D55h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.</p>	Default Value:	1111111111111111b	Access:	R/W Lock	_Custom_GTIRreset:	BUS
Default Value:	1111111111111111b							
Access:	R/W Lock							
_Custom_GTIRreset:	BUS							

Slice 1 - 5 BONUS1 Reg

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24214h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS1 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS1 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	5	BONUS1 BIT 5	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
4	BONUS1 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS1 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)	
	2	BONUS1 BIT 2	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
	1	BONUS1 BIT 1	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
	0	BONUS1 BIT 0	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

Slice 1 - 5 BONUS2 Reg

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24218h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS2 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS2 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	5	BONUS2 BIT 5	
Access:		R/W	
_Custom_GTIReset:		BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS2 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS2 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)	
	2	BONUS2 BIT 2	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
	1	BONUS2 BIT 1	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
	0	BONUS2 BIT 0	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

Slice 1 - 5 PGFET control register with lock

SL15SPCPFETCTL - Slice 1 - 5 PGFET control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24208h		
DWord	Bit	Description	
0	31	PFET Control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
		Reserved	
30:24		Access:	RO
		Format:	MBZ
23		Power Well Status	
		Access:	R/WC
		_Custom_GTIReset:	BUS
strbpulsprdwered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.			
22		Powergood timer error	
		Access:	R/WC
		_Custom_GTIReset:	BUS
0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.			
21:19		Delay from enabling secondary PFETs to power good.	
		Default Value:	111b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns			

SL15SPCPFETCTL - Slice 1 - 5 PGFET control register with lock

		3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns							
	18:16	Strobe pulse period <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Default Value:</td> <td>011b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)</p>		Default Value:	011b	Access:	R/W Lock	_Custom_GTIRreset:	BUS
Default Value:	011b								
Access:	R/W Lock								
_Custom_GTIRreset:	BUS								
	15:0	PFET Ladder Step Sequence <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>1111111111111111b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetldrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1'; A '0' setting for these bits is illegal. 15'FFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?.15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.</p>		Default Value:	1111111111111111b	Access:	R/W Lock	_Custom_GTIRreset:	BUS
Default Value:	1111111111111111b								
Access:	R/W Lock								
_Custom_GTIRreset:	BUS								

Slice 1 - 5 Power Down FSM control register with lock

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24210h		
DWord	Bit	Description	
0	31	power down control Lock	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		0 = Bits of Slice 1 POWERDNFSMCTL register are R/W 1 = All bits of Slice 1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:13		Reserved	
		Access:	RO
		Format:	MBZ
12		Leave firewall disabled	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow	
11		Leave reset de-asserted	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow	
10		Leave CLKs ON	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:	

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

		<p>0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow</p>							
	9	<p>Leave FET On</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow</p>		Access:	R/W Lock	_Custom_GTIReset:	BUS		
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	8:6	<p>Power Down state 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks</p>		Default Value:	010b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	010b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	5:3	<p>Power Down state 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>001b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON</p>		Default Value:	001b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	001b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

	2:0	Power Down state 1	
		Default Value:	000b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		<p>This will be the 1st state before power is turned OFF in the well</p> <p>Encodings:</p> <p>000 = Assert Reset</p> <p>001 = Firewall ON</p> <p>010 = Gate clocks</p> <p>1xx = Rsvd for future</p> <p>Default : Assert Reset</p>	



Slice 1 - 5 Power Gate Control Request

SL15PGCTLREQ - Slice 1 - 5 Power Gate Control Request			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24200h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:16	Message Mask	
		Access:	RO
		_Custom_GTIRreset:	BUS
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000	
15:2	Reserved	Access:	RO
		Format:	MBZ
1	CLK RST FWE Request	Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	Power Gate Request	Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

Slice 1 -5 Power on FSM control register with lock

SL15SPCPOWERUPFSMCTL - Slice 1 -5 Power on FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	2420Ch		
DWord	Bit	Description	
0	31	power up control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of Slice 1 POWERUPFSMCTL register are R/W 1 = All bits of Slice 1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	30:9	Reserved	
		Access:	RO
		Format:	MBZ
	8:6	Power UP state 3	
		Default Value:	010b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)	
5:3	Power UP state 2		
	Default Value:	001b	
	Access:	R/W Lock	
	_Custom_GTIReset:	BUS	
This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF			

SL15SPCPOWERUPFSMCTL - Slice 1 -5 Power on FSM control register with lock

	2:0	Power UP state 1	
		Default Value:	000b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		<p>This will be the 1st state after power is turned ON in the well</p> <p>Encodings:</p> <p>000 = Clock Ungate</p> <p>001 = Firewall OFF</p> <p>010 = De-assert resets</p> <p>1xx = Rsvd for future</p> <p>Default - Clock Ungate</p>	

Slice unit Level Clock Gating Control 94D0

SCCGCTL94D0 - Slice unit Level Clock Gating Control 94D0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
CustomGTIIs_ContextSaved:	true		
Address:	094D0h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:2	Reserved	
		Access:	RO
		Format:	MBZ
1	1	GCPunit Clock Gating Disable	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIReset:	BUS
GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
0	0	SMCRunit Clock Gating Disable	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIReset:	BUS
Graphics Documentation Intel Confidential [Build: 112015] My Dashboard Reports Filters Help SMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

Slice unit Level Clock Gating Control 94D4

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4					
Register Space:	MMIO: 0/2/0				
Size (in bits):	32				
CustomGTIs_ContextSaved:	true				
Address:	094D4h				
Unit Level Clock Gating Disable bits					
DWord	Bit	Description			
0	31	SPARE Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:
	Access:	R/W			
	_Custom_GTIReset:	BUS			
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
30	Isqcunit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
Isqcunit Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
29	ccunit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
ccunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
28	DAPunit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
27	GACBunit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
GACBunit Clock Gating Disable Control:					

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
26	GAFSRRB Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>GAFSRRB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
25	GAHSunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>GAHSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
24	GAPCunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>GAPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
23	GAPL3unit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>GAPL3unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
22	GAPSunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>GAPSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
21	GAPZunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

	<p>GAPZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>							
20	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
19	<p>HIZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS		
Access:	R/W							
_Custom_GTIRreset:	BUS							
18	<p>IZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS		
Access:	R/W							
_Custom_GTIRreset:	BUS							
17	<p>L3 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; background-color: #e6f2ff;">Programming Notes</td> </tr> <tr> <td>As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register</td> </tr> </table>		Access:	R/W	_Custom_GTIRreset:	BUS	Programming Notes	As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register
Access:	R/W							
_Custom_GTIRreset:	BUS							
Programming Notes								
As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register								
16	<p>L3 Clock Gating Disable cr2x</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; background-color: #e6f2ff;">Programming Notes</td> </tr> <tr> <td>As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register</td> </tr> </table>		Access:	R/W	_Custom_GTIRreset:	BUS	Programming Notes	As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register
Access:	R/W							
_Custom_GTIRreset:	BUS							
Programming Notes								
As a WA - Disable L3 clock gating by setting bit 16 & 17 of this register								

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

15	<p>L3Bank Clock Gating Disable cr</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>L3Bank Clock Gating Disable cr2x</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>L3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>L3BANK Clock Gating Disable cu</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>I3bank L3BANK Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>L3BANK Clock Gating Disable cu2x</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>L3BANK Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>Isnunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Isnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
10	<p>MSCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	OAADDRunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	OAADDRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
8	OASCREP Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	OASCREP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
7	RCCunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
6	RCZunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
5	Sarbunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	Sarbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
4	SBEunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	SBEunit Clock Gating Disable Control:		

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

	<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
3	<p>STCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
2	<p>SVLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
1	<p>WMBE Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>WMBE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
0	<p>WMFEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					



Slice unit Level Clock Gating Control 94D8

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8					
Register Space:	MMIO: 0/2/0				
Size (in bits):	32				
CustomGTIs_ContextSaved:	true				
Address:	094D8h				
Unit Level Clock Gating Disable bits					
DWord	Bit	Description			
0	31	SFR unit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:
	Access:	R/W			
	_Custom_GTIReset:	BUS			
	SFR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
30	SF unit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
SF unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
29	OARUNIT Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
OARUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
28	RCU unit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
RCU unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
27	POCS unit Clock Gating Disable				
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
POCS unit Clock Gating Disable Control:					

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
26	OVR unit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>OVR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
25	HS unit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
24	GS unit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
23	GAFSWRBLK unit Clock Gating Disable wmf	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFSWRBLK unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
22	GAFSWRBLK unit Clock Gating Disable vf	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFSWRBLK unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
21	GAFSWRBLK unit Clock Gating Disable 2x	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

	<p>GAFSWRBLK unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
20	<p>GAFSFFROB unit Clock Gating Disable 2xrdrtn</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFSFFROB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
19	<p>GAFSFFROB unit Clock Gating Disable 2x</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFSFFROB unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
18	<p>GAFD unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFD unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
17	<p>GAFS unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
16	<p>GAFM unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAFM unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

15	<p>CS unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>CS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>CLR unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>CLR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>CL unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>CL unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>AMFS unit Clock Gating Disable f</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>AMFS unit Clock Gating Disable c</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
10	<p>AMFS unit Clock Gating Disable d</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	GADSS unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	GADSS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	SLMBE unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SLMBE unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	SFBEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SFBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
6	LNEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	LNEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
5	LNIunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	LNIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
4	RCPBunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for	

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

	functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
3	RCPBEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	RCPBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
2	TDCunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	TDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
1	RAMdft Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	RAMdft Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
0	Reserved	



Slice unit Level Clock Gating Control 94DC

SCCGCTL94DC - Slice unit Level Clock Gating Control 94DC			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
CustomGTIIsContextSaved:	true		
Address:	094DCh		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:15	Reserved	
		Access:	RO
		_Custom_GTIReset:	BUS
		Reserved	
	14	Reserved	
		Access:	RO
		Format:	MBZ
	13:0	Reserved	
		Access:	RO
		_Custom_GTIReset:	BUS
		Reserved	

Slice unit Level Clock Gating Control 94E0

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	094E0h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31	Reserved	
		Access:	RO
		Format:	MBZ
	30	PSS Clock Gating Disable	
		Access:	R/W
	_Custom_GTIReset:	BUS	
PSS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
29	VSR Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
VSR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
28	VS Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
VS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
27	VFR Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
VFR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

26	VF Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	VF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
25	TDS Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	TDS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
24	SVGR Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SVGR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
23	SVG Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SVG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
22	SOL Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SOL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
21:20	Reserved	
	Access:	RO
	Format:	MBZ
19	OVR Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

		<p>OVR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
18	HS Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	<p>HS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
17	GS Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	<p>GS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
16	CS Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	<p>CS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
15	SPARE Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	<p>SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
14	CPSSunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	<p>CPSSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

13	PSDunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
12	BCunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	MSCunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
10	RCPFEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	RCPFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9	AVSunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	Reserved	
	Access:	RO
	Format:	MBZ

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

7	<p>HIZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>IZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
5	<p>RCCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
4	<p>RCZunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
3	<p>SBEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
2	<p>STCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
1	SVLunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
0	WMFEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Slice unit Level Clock Gating Control 94E4

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	094E4h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
29		CCS Clock Gating Disable	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	BUS
		CCS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
28		sdfifo Clock Gating Disable svg	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	BUS
		sdfifo Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
27		sdfifo Clock Gating Disable svl	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	BUS
		sdfifo Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
26		PSS unit Clock Gating Disable	
		Access:	R/W
		Format:	Disable
		_Custom_GTIReset:	BUS
		PSS Clock Gating Disable Control:	

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
25	CARB unit Clock Gating Disable	Access:	R/W
		Format:	Disable
		_Custom_GTIRreset:	BUS
	<p>CARB Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
24	ZPBE unit Clock Gating Disable	Access:	R/W
		Format:	Disable
		_Custom_GTIRreset:	BUS
	<p>ZPBE Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
23	ZSCBANK unit Clock Gating Disable	Access:	R/W
		Format:	Disable
		_Custom_GTIRreset:	BUS
	<p>ZSCBANK Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
22	ZSCCOMPUTE unit Clock Gating Disable	Access:	R/W
		Format:	Disable
		_Custom_GTIRreset:	BUS
	<p>ZSCCOMPUTE Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
21	GAFARB unit Clock Gating Disable	Access:	R/W
		Format:	Disable
		_Custom_GTIRreset:	BUS
	<p>GAFARB Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for</p>		

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
20	VSR unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
	VSR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
19	VS unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
	VS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
18	VFR unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
	VFR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
17	VFE Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
	VFE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
16	VF unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
	VF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
15	URBM unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	BUS	
	URBM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
14	TSG unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	BUS	
	TSG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
13	TETG unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	BUS	
	TETG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
12	TE unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	BUS	
	TE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
11	TDS unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIReset:	BUS	
	TDS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

10	<p>TDG unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>TDG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
9	<p>SVGR unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SVGR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
8	<p>SVG unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SVG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
7	<p>SOL unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SOL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
6	<p>gwunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>gwunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

5	<p>psdunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>psdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIRreset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIRreset:	BUS						
4	<p>hdcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>hdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIRreset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIRreset:	BUS						
3	<p>cpssunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>cpssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIRreset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIRreset:	BUS						
2	<p>besbufunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>besbufunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIRreset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIRreset:	BUS						
1	<p>BC Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>BC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIRreset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIRreset:	BUS						

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

0	tdpunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIReset:	BUS
CCS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		



Slice unit Level Clock Gating override during rstflow 94F0

SCMISCCP94F0 - Slice unit Level Clock Gating override during rstflow 94F0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	094F0h	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:0	ECO Spare Bits
		Access: R/W
		_Custom_GTIReset: BUS

SLM Bank Hash

SLM_BANKHASH - SLM Bank Hash				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	0E660h			
Name:	SLM Bank Hash			
ShortName:	SLM_BANKHASH			
Description				
Register for selecting number of SLM banks and setting XOR hashing in bank select bits.				
Restriction : To avoid data corruption, this register can only be modified when no threads are running that access SLM. Data corruption can also occur if a mid-thread preemption image with saved SLM data is restored with a different setting.				
Restriction : This register is a privileged register (not user-mode non-privileged) to ensure that one context changing it does not corrupt a simultaneously running context.				
DWord	Bit	Description		
0	31:16	Reserved		
		Access:	RO	
		Format:	MBZ	
	15	64 Bank Mode		
		Format:	U1	
		This bit selects the number of logical banks in SLM (64 or 65).		
		Value	Name	Description
		1h	B64	64 logical banks in SLM.
	0h	B65 [Default]	65 logical banks in SLM.	
	14:12	Reserved		
		Access:	RO	
		Format:	MBZ	
	11:10	bit7 Hash		
		Access:	R/W	
		Format:	U2	
Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[7] to produce new address bit[7]. Multiple bits can be set to XOR multiple address bit with bit[7].				
Value		Name	Description	
2h		A10	When set, XOR address[7] with address[10] to produce new address[7].	
1h	A13	When set, XOR address[7] with address[13] to produce new		

SLM_BANKHASH - SLM Bank Hash

			address[7].
	0h	No XOR [Default]	Address[7] is not XOR-ed with any other address bit.
9:8	bit6 Hash		
	Access:		R/W
	Format:		U2
	Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[6] to produce new address bit[6]. Multiple bits can be set to XOR multiple address bit with bit[6].		
	Value	Name	Description
	2h	A9	When set, XOR address[6] with address[9] to produce new address[6].
	1h	A12	When set, XOR address[6] with address[12] to produce new address[6].
	0h	No XOR [Default]	Address[6] is not XOR-ed with any other address bit.
7:6	bit5 Hash		
	Access:		R/W
	Format:		U2
	Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[5] to produce new address bit[5]. Multiple bits can be set to XOR multiple address bit with bit[5].		
	Value	Name	Description
	2h	A8	When set, XOR address[5] with address[8] to produce new address[5].
	1h	A11	When set, XOR address[5] with address[11] to produce new address[5].
	0h	No XOR [Default]	Address[5] is not XOR-ed with any other address bit.
5:4	bit4 Hash		
	Access:		R/W
	Format:		U2
	Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[4] to produce new address bit[4]. Multiple bits can be set to XOR multiple address bit with bit[4].		
	Value	Name	Description
	2h	A16	When set, XOR address[4] with address[16] to produce new address[4].
	1h	A10	When set, XOR address[4] with address[10] to produce new address[4].

SLM_BANKHASH - SLM Bank Hash			
	0h	No XOR [Default]	Address[4] is not XOR-ed with any other address bit.
3:2	bit3 Hash		
	Access:		R/W
	Format:		U2
	Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[3] to produce new address bit[3]. Multiple bits can be set to XOR multiple address bit with bit[3].		
	Value	Name	Description
2h	A15	When set, XOR address[3] with address[15] to produce new address[3].	
1h	A9	When set, XOR address[3] with address[9] to produce new address[3].	
0h	No XOR [Default]	Address[3] is not XOR-ed with any other address bit.	
1:0	bit2 Hash		
	Access:		R/W
	Format:		U2
	Programming this field is only valid when Bit[15] is set to 1 (64-bank mode). This field defines which address bit(s) will be XOR-ed with address bit[2] to produce new address bit[2]. Multiple bits can be set to XOR multiple address bit with bit[2].		
	Value	Name	Description
2h	A14	When set, XOR address[2] with address[14] to produce new address[2].	
1h	A8	When set, XOR address[2] with address[8] to produce new address[2].	
0h	No XOR [Default]	Address[2] is not XOR-ed with any other address bit.	



SNP_FILTER_Q_STATUS

SNP_FILTER_Q_STATUS - SNP_FILTER_Q_STATUS						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	00B00h					
Name:	SNP_FILTER_Q_STATUS					
ShortName:	SNP_FILTER_Q_STATUS					
This is a basic register template						
DWord	Bit	Description				
0	31	Reserved				
	30:29	SF_FUSE_HASH_3 <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> This bit captures the fuse_idi_hash[3:2] for GuC to use	Access:	RO	_Custom_GTIReset:	BUS
	Access:	RO				
	_Custom_GTIReset:	BUS				
	28:20	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
	19	Reserved				
	18	Reserved				
	17	Reserved				
	16	Reserved				
	15	Reserved				
	14	Reserved				
	13	Reserved				
	12	Reserved				
	11	Reserved				
	10	Reserved				
	9	Reserved				
	8	Reserved				
	7	Reserved				
	6	Reserved				
	5	Reserved				
	4	Reserved				
	3	Reserved				
2	Reserved					
1	Reserved					
0	Reserved					

Soft Scratch

SOFT_SCRATCH - Soft Scratch		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	512	
These are 16 dword software scratchpad dword registers defined for use.		
Programming Notes		
These registers are saved in the power context		
DWord	Bit	Description
0..15	511:0	Scratch



Software SCI

SWSCI_0_2_0_PCI - Software SCI			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	000E8h		
<p>This register serves 2 purposes:</p> <p>1) Support selection of SMI or SCI event source (SMISCISEL - bit15)</p> <p>2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a "0" to "1" subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a "0" to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).</p>			
DWord	Bit	Description	
0	15	SMI or SCI event select	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	0 = SMI (default) 1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.		
	14:1	Software scratch bits	
		Default Value:	000000000000000b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	Read/write bits not used by hardware.		
0	Software SCI Event		
	Default Value:	0b	
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.			

Software SMI

SWSMI_0_2_0_PCI - Software SMI			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	000E0h		
DWord	Bit	Description	
0	15:8	Software Scratch Bits	
		Default Value:	00000000b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	7:1	Software Flag	
		Default Value:	0000000b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	Used to indicate caller and SMI function desired, as well as return result.		
	0	GMCH Software SMI Event	
		Default Value:	0b
		Access:	R/W
_Custom_GTIRreset:		BUS	
When Set this bit will trigger an SMI. Software must write a "0" to clear this bit.SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.			



SRD_CTL

SRD_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	60800h-60803h	
Name:	Transcoder SRD Control	
ShortName:	SRD_CTL_A	
Reset:	soft	
Address:	61800h-61803h	
Name:	Transcoder SRD Control	
ShortName:	SRD_CTL_B	
Reset:	soft	
Address:	62800h-62803h	
Name:	Transcoder SRD Control	
ShortName:	SRD_CTL_C	
Reset:	soft	
Address:	63800h-63803h	
Name:	Transcoder SRD Control	
ShortName:	SRD_CTL_D	
Reset:	soft	
Restriction : PSR needs to be enabled only when at least one plane is enabled.		
Programming Notes		
To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.		
Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.		
Restriction		
Only the SRD Enable and Single Frame Update Enable fields can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.		
DWord	Bit	Description
0	31	SRD Enable This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled. When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can disable the link and stop fetching data from memory. When activity occurs, hardware will exit

SRD_CTL									
	<p>SRD (wake) and re-enable the link and resume fetching data from memory.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.</p> <p>SRD must not be enabled together with Interlacing, Black Frame Insertion (BFI), or audio on the same transcoder.</p>	Value	Name	0b	Disable	1b	Enable		
Value	Name								
0b	Disable								
1b	Enable								
30	<p>Single Frame Update Enable</p> <table border="1"> <tr> <td>Access:</td> <td>Double Buffered</td> </tr> </table> <p>This field enables the single frame update mode where a plane flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.</p> <p style="text-align: center;">Workaround</p> <p>When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.</p> <p style="text-align: center;">Restriction</p> <p>This mode should only be enabled with link standby.</p>	Access:	Double Buffered	Value	Name	0b	Disable	1b	Enable
Access:	Double Buffered								
Value	Name								
0b	Disable								
1b	Enable								
29	<p>Context restore to PSR Active</p> <p>This field restores eDP context to PSR Active on a context restore.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field is used for hardware communication. Software must not change this field.</p>	Value	Name	0b	Disable	1b	Enable		
Value	Name								
0b	Disable								
1b	Enable								
28	<p>Adaptive Sync Frame Update</p> <p>This field enables the Adaptive Sync Frame Update mode where a flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank. This field must be enabled with VRR enable.</p>								

SRD_CTL																			
<p>Restriction : This mode should only be enabled with the SRD Link Disable mode. This mode does not support VRR Max Shift. However, normal and flipline VRR modes are supported.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center;">Value</th> <th style="width: 50%; text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <p>Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.</p>				Value	Name	0b	Disable	1b	Enable										
Value	Name																		
0b	Disable																		
1b	Enable																		
27	<p>Link Ctrl This field controls the behavior of the link when in SRD (sleeping). The timing generator and pixel data fetches are disabled when the link is disabled. Only pixel data fetches are disabled when the link is in standby. This field is ignored by transcoder A/B/C since they only operate in standby.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%; text-align: center;">Value</th> <th style="width: 15%; text-align: center;">Name</th> <th style="width: 70%; text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> <td style="text-align: center;">Link is disabled when in SRD (sleeping)</td> </tr> </tbody> </table>			Value	Name	Description	0b	Disable	Link is disabled when in SRD (sleeping)										
Value	Name	Description																	
0b	Disable	Link is disabled when in SRD (sleeping)																	
26:25	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>			Access:	RO	Format:	MBZ												
Access:	RO																		
Format:	MBZ																		
24:20	<p>Max Sleep Time</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td style="text-align: center;">00001b 1/8 second</td> </tr> </table> <p>This field is the maximum time to spend in SRD (sleeping). It is programmed in increments of approximately 1/8 a second. Programming all 1s gives ~3.875 seconds.</p> <p style="text-align: center;">Restriction</p> <p>Programming all 0s is invalid.</p>			Default Value:	00001b 1/8 second														
Default Value:	00001b 1/8 second																		
19:17	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>			Access:	RO	Format:	MBZ												
Access:	RO																		
Format:	MBZ																		
16:14	<p>DSC CRC Last Byte This field selects the valid last byte of DSC data stream for SRD CRC calculation. Valid data byte for CRC engine can be from 0 to 5. $DSC\ CRC\ Last\ Byte = (Slice\ Per\ Line\ eDP * Bytes\ PerChunk * VActive) \bmod 6$ Below is an example with 2 slices per line on each DSC. SPL = Slices Per Line</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: left;">Case</th> <th style="width: 12.5%; text-align: center;">DSC A SPL</th> <th style="width: 12.5%; text-align: center;">DSC C SPL</th> <th style="width: 25%; text-align: center;">Slices Per Line eDP</th> </tr> </thead> <tbody> <tr> <td>CoG enable + VDSC enable (no Joiner)</td> <td style="text-align: center;">2</td> <td style="text-align: center;">2</td> <td style="text-align: center;">2 (DSC A or DSC C)</td> </tr> <tr> <td>VDSC enable + Joiner enable (no CoG)</td> <td style="text-align: center;">2</td> <td style="text-align: center;">2</td> <td style="text-align: center;">4 (DSC A + DSC C)</td> </tr> <tr> <td>VDSC standalone</td> <td style="text-align: center;">0 or 2</td> <td style="text-align: center;">2 or 0</td> <td style="text-align: center;">2</td> </tr> </tbody> </table>			Case	DSC A SPL	DSC C SPL	Slices Per Line eDP	CoG enable + VDSC enable (no Joiner)	2	2	2 (DSC A or DSC C)	VDSC enable + Joiner enable (no CoG)	2	2	4 (DSC A + DSC C)	VDSC standalone	0 or 2	2 or 0	2
Case	DSC A SPL	DSC C SPL	Slices Per Line eDP																
CoG enable + VDSC enable (no Joiner)	2	2	2 (DSC A or DSC C)																
VDSC enable + Joiner enable (no CoG)	2	2	4 (DSC A + DSC C)																
VDSC standalone	0 or 2	2 or 0	2																

SRD_CTL			
	(no Joiner, no CoG)		
13	Reserved		
12	Reserved		
11	TP2 TP3 Select This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking).		
	Value	Name	Description
	0b	TP2	Use TP1 followed by TP2
	1b	TP3	Use TP1 followed by TP3
Programming Notes			
This bit impacts PSR2. Clear it before enabling PSR2 and do not set it while PSR2 is enabled.			
10	CRC Enable This field controls whether the PSR CRC value will be placed in the VSC packet.		
	Value	Name	Description
	0b	Disable	Disable CRC output in VSC. VSC packet CRC value will be populated by VIDEO_DIP_DATA.
	1b	Enable	Enable CRC output in VSC. VSC packet CRC value will be populated by the calculated CRC value.
Programming Notes			
When CRC is enabled, the Max Sleep Timer should be disabled to provide additional power savings. Disable the Max Sleep Timer by setting register 0x6F860 bit 28 to 1. Re-enable the Max Sleep Timer by clearing register 0x6F860 bit 28 to 0.			
Workaround			
When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.			
9:8	TP2 TP3 Time This field selects the TP2 or TP3 time when training the link on exiting SRD (waking).		
	Value	Name	
	00b	500us	
	01b	100us	
	10b	2.5ms	
	11b	0us Skip TP2/TP3	
7:6	TP4 time This field selects the TP4 time when training the link on exiting SRD (waking). If this field is set to any value other than "11", TP4 pattern will be sent at PSR reentry.		
	Value	Name	Description
	00b	500 us	

SRD_CTL		
	01b	100 us
	10b	2.5 ms
	11b	0 us
	Skip TP4	
	Programming Notes	
	Always program TP4 to 11b.	
5:4	TP1 Time This field selects the TP1 time when training the link on exiting SRD (waking).	
	Value	Name
	00b	500us
	01b	100us
	10b	2.5ms
	11b	0us
	Skip TP1	
3:0	Idle Frames Default Value: 0001b 1 idle frame This field is the number of idle frames required before entering SRD (sleeping).	

SRD_PERF_CNT

SRD_PERF_CNT		
Register Space:	MMIO: 0/2/0	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	60844h-60847h	
Name:	Transcoder SRD Performance Counter	
ShortName:	SRD_PERF_CNT_A	
Reset:	soft	
Address:	61844h-61847h	
Name:	Transcoder SRD Performance Counter	
ShortName:	SRD_PERF_CNT_B	
Reset:	soft	
Address:	62844h-62847h	
Name:	Transcoder SRD Performance Counter	
ShortName:	SRD_PERF_CNT_C	
Reset:	soft	
Address:	63844h-63847h	
Name:	Transcoder SRD Performance Counter	
ShortName:	SRD_PERF_CNT_D	
Reset:	soft	
DWord	Bit	Description
0	31:24	Reserved
		Access: RO
		Format: MBZ
23:0	SRD Perf Cnt This field increments every millisecond while in SRD (sleeping) and the display CD clock is running. It will stop incrementing when out of SRD (awake), then resume when back in SRD (sleeping). The value is maintained while SRD is disabled, and counting will resume from the previous value when SRD is re-enabled. Writes to this register will set the count to the written value, then it will increment from that value onwards.	



SRD_STATUS

SRD_STATUS																																
Register Space:	MMIO: 0/2/0																															
Access:	RO																															
Size (in bits):	32																															
Address:	60840h-60843h																															
Name:	Transcoder SRD Status																															
ShortName:	SRD_STATUS_A																															
Reset:	soft																															
Address:	61840h-61843h																															
Name:	Transcoder SRD Status																															
ShortName:	SRD_STATUS_B																															
Reset:	soft																															
Address:	62840h-62843h																															
Name:	Transcoder SRD Status																															
ShortName:	SRD_STATUS_C																															
Reset:	soft																															
Address:	63840h-63843h																															
Name:	Transcoder SRD Status																															
ShortName:	SRD_STATUS_D																															
Reset:	soft																															
DWord	Bit	Description																														
0	31:29	SRD State																														
		Access: RO																														
		This field indicates the live state of SRD																														
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>IDLE</td> <td>Reset state</td> </tr> <tr> <td>001b</td> <td>SRDONACK</td> <td>Wait for TG/Stream to send on frame of data after SRD conditions are met</td> </tr> <tr> <td>010b</td> <td>SRDENT</td> <td>SRD entry with Link OFF</td> </tr> <tr> <td>011b</td> <td>BUFOFF</td> <td>Wait for buffer turn off</td> </tr> <tr> <td>100b</td> <td>BUFON</td> <td>Wait for buffer turn on</td> </tr> <tr> <td>101b</td> <td>AUXACK</td> <td>Wait for AUX to acknowledge on SRD exit</td> </tr> <tr> <td>110b</td> <td>SRDOFFACK</td> <td>Wait for TG/Stream to acknowledge the SRD VDM exit</td> </tr> <tr> <td>111b</td> <td>SRDENT_ON</td> <td>SRD entry with Link ON</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	000b	IDLE	Reset state	001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met	010b	SRDENT	SRD entry with Link OFF	011b	BUFOFF	Wait for buffer turn off	100b	BUFON	Wait for buffer turn on	101b	AUXACK	Wait for AUX to acknowledge on SRD exit	110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit	111b	SRDENT_ON	SRD entry with Link ON	Others	Reserved	Reserved
		Value	Name	Description																												
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111b	SRDENT_ON	SRD entry with Link ON																														
Others	Reserved	Reserved																														
28	Reserved																															

SRD_STATUS		
	Access:	RO
	Format:	MBZ
27:26	Link Status	
	Access:	RO
	This field indicates the live status of the link.	
	Value	Name
	Description	
	00b	Full Off
	01b	Full On
	11b	Reserved
25	Reserved	
	Access:	RO
	Format:	MBZ
24:20	Max Sleep Time Counter	
	Access:	RO
	This field provides the live status of the sleep time counter.	
19:16	SRD Entry Count	
	Access:	RO
	The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.	
15	Aux Error	
	Access:	RO
	This field indicates an error on the last SRD AUX handshake.	
	Value	Name
	Description	
	0b	No Error
	1b	Error
	AUX had no error	
	AUX error (receive error or timeout) occurred	
14:13	Reserved	
	Access:	RO
	Format:	MBZ
12	Sending Aux	
	Access:	RO
	This field indicates if the SRD AUX handshake is currently being sent.	
	Value	Name
	Description	
	0b	Not Sending
	1b	Sending
	Not sending AUX handshake	
	Sending AUX handshake	

SRD_STATUS			
11:10	Reserved		
	Access:	RO	
	Format:	MBZ	
	9	Sending Idle	
		Access:	RO
		This field indicates if idles are currently being sent.	
		Value	Name
		Description	
	0b	Not Sending	Not sending idle
	1b	Sending	Sending idle
	8	Sending TP2 TP3	
		Access:	RO
		This field indicates if TP2 or TP3 is currently being sent.	
		Value	Name
		Description	
	0b	Not Sending	Not sending TP2 or TP3
	1b	Sending	Sending TP2 or TP3
	7	Sending TP4	
Access:		RO	
This field indicates if TP4 is currently being sent.			
Value		Name	
0b		Not Sending	
1b	Sending		
6:5	Reserved		
	Access:	RO	
	Format:	MBZ	
4	Sending TP1		
	Access:	RO	
	This field indicates if TP1 is currently being sent.		
	Value	Name	
	Description		
0b	Not Sending	Not sending TP1	
1b	Sending	Sending TP1	
3:0	Idle Frame Counter		
	Access:	RO	
	This field provides the live status of the idle frame counter.		
	Programming Notes		
The value of this field is not preserved across power down states such as DC5 and up.			

SSM0 BONUS1 Reg

SSM0PCBONUS1 - SSM0 BONUS1 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24414h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS1 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS1 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS1 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS1 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS1 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM0SPCBONUS1 - SSM0 BONUS1 Reg	
	'1' : Initiate power up sequence (clk/rst/fwe)
2	BONUS1 BIT 2
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
1	BONUS1 BIT 1
	Access: R/W
	_Custom_GTIReset: BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	BONUS1 BIT 0
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

SSM0 BONUS2 Reg

SSM0PCBONUS2 - SSM0 BONUS2 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24418h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS2 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS2 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS2 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS2 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS2 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM0SPCBONUS2 - SSM0 BONUS2 Reg	
	'1' : Initiate power up sequence (clk/rst/fwe)
2	BONUS2 BIT 2
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
1	BONUS2 BIT 1
	Access: R/W
	_Custom_GTIReset: BUS
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	BONUS2 BIT 0
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

SSM1 BONUS1 Reg

SSM1SPCBONUS1 - SSM1 BONUS1 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24494h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS1 BIT 7	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS1 BIT 6	
		Access:	R/W
		_Custom_GTIRreset:	BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS1 BIT 5		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS1 BIT 4		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS1 BIT 3		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM1SPCBONUS1 - SSM1 BONUS1 Reg	
	'1' : Initiate power up sequence (clk/rst/fwe)
2	BONUS1 BIT 2
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
1	BONUS1 BIT 1
	Access: R/W
	_Custom_GTIReset: BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	BONUS1 BIT 0
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

SSM1 BONUS2 Reg

SSM1SPCBONUS2 - SSM1 BONUS2 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24498h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS2 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS2 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS2 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS2 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS2 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM1SPCBONUS2 - SSM1 BONUS2 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)	
	2	BONUS2 BIT 2	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
	1	BONUS2 BIT 1	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
	0	BONUS2 BIT 0	
		Access:	R/W
_Custom_GTIRreset:		BUS	
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			

SSM2 BONUS1 Reg

SSM2SPCBONUS1 - SSM2 BONUS1 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24514h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS1 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS1 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS1 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS1 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS1 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM2SPCBONUS1 - SSM2 BONUS1 Reg	
	'1' : Initiate power up sequence (clk/rst/fwe)
2	BONUS1 BIT 2
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
1	BONUS1 BIT 1
	Access: R/W
	_Custom_GTIReset: BUS
SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	BONUS1 BIT 0
	Access: R/W
	_Custom_GTIReset: BUS
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

SSM2 BONUS2 Reg

SSM2SPCBONUS2 - SSM2 BONUS2 Reg			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24518h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	BONUS2 BIT 7	
		Access:	R/W
		_Custom_GTIReset:	BUS
	SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)		
	6	BONUS2 BIT 6	
		Access:	R/W
		_Custom_GTIReset:	BUS
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
5	BONUS2 BIT 5		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)			
4	BONUS2 BIT 4		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			
3	BONUS2 BIT 3		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe)			

SSM2SPCBONUS2 - SSM2 BONUS2 Reg

		'1' : Initiate power up sequence (clk/rst/fwe)	
	2	BONUS2 BIT 2	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	
	1	BONUS2 BIT 1	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
	0	BONUS2 BIT 0	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

ssmcp Sub Slice Power Context Save request

SSMPCTXSAVEREQ - ssmcp Sub Slice Power Context Save request		
Register Space: MMIO: 0/2/0		
Size (in bits): 32		
CustomGTIs_ContextSaved: false		
Address: 08150h		
DWord	Bit	Description
0	31:16	Message Mask
		Access: RO
		_Custom_GTIReset: BUS
		Message Mask bots for lower 16 bits
15:10	Reserved	Access: RO
		Format: MBZ
9	Power context save request	Access: R/W Set
		_Custom_GTIReset: BUS
		Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.
8:0	Power Context Save request credit count	Access: R/W
		_Custom_GTIReset: BUS
		QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).



Stream Output 0 Num Primitives Written Counter

SO0_NUM_PRIMS_WRITTEN - Stream Output 0 Num Primitives Written Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05200h-05207h		
Name:	Stream Output 0 Num Primitives Written Counter		
ShortName:	SO0_NUM_PRIMS_WRITTEN		
<p>There is one 64-bit register for each of the 4 supported streams:</p> <ul style="list-style-type: none"> • 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) • 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) • 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) • 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3) <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume). These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Num Prims Written Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	
1	31:0	Num Prims Written Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	

Stream Output 0 Primitive Storage Needed Counter

SOO_PRIM_STORAGE_NEEDED - Stream Output 0 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05240h-05247h
Name:	Stream Output 0 Primitive Storage Needed Counter
ShortName:	SOO_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:

- 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
- 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
- 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
- 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).

These registers are part of the context save and restore.

DWord	Bit	Description	
0	31:0	Prim Storage Needed Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.			
1	31:0	Prim Storage Needed Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.			



Stream Output 0 Write Offset

SO0_WRITE_OFFSET - Stream Output 0 Write Offset				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	05280h-05283h			
Name:	Stream Output 0 Write Offset			
ShortName:	SO0_WRITE_OFFSET			
<p>There is one R/W 32-bit register for each of the 4 supported stream output buffer slots: 5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0) 5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1) 5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2) 528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)</p> <p>These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>				
Programming Notes				
<ul style="list-style-type: none"> • Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. • The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so. 				
DWord	Bit	Description		
0	31:2	Write Offset		
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Format:	U30
Format:	U30			
_Custom_GTIReset:	DEV			
	1:0	Reserved		
		Access:	RO	
		Format:	MBZ	

Stream Output 1 Num Primitives Written Counter

SO1_NUM_PRIMS_WRITTEN - Stream Output 1 Num Primitives Written Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05208h-0520Fh		
Name:	Stream Output 1 Num Primitives Written Counter		
ShortName:	SO1_NUM_PRIMS_WRITTEN		
<p>There is one 64-bit register for each of the 4 supported streams: 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Num Prims Written Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	
1	31:0	Num Prims Written Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	



Stream Output 1 Primitive Storage Needed Counter

SO1_PRIM_STORAGE_NEEDED - Stream Output 1 Primitive Storage Needed Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05248h-0524Fh		
Name:	Stream Output 1 Primitive Storage Needed Counter		
ShortName:	SO1_PRIM_STORAGE_NEEDED		
<p>There is one 64-bit register for each of the 4 supported streams: 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0) 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1) 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2) 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume). These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Prim Storage Needed Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.	
1	31:0	Prim Storage Needed Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.	

Stream Output 1 Write Offset

SO1_WRITE_OFFSET - Stream Output 1 Write Offset				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	05284h-05287h			
Name:	Stream Output 1 Write Offset			
ShortName:	SO1_WRITE_OFFSET			
<p>There is one R/W 32-bit register for each of the 4 supported stream output buffer slots: 5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0) 5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1) 5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2) 528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)</p> <p>These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>				
Programming Notes				
<ul style="list-style-type: none"> Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so. 				
DWord	Bit	Description		
0	31:2	Write Offset		
		<table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Format:	U30
Format:	U30			
_Custom_GTIReset:	DEV			
	1:0	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			

Stream Output 2 Num Primitives Written Counter

SO2_NUM_PRIMS_WRITTEN - Stream Output 2 Num Primitives Written Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05210h-05217h		
Name:	Stream Output 2 Num Primitives Written Counter		
ShortName:	SO2_NUM_PRIMS_WRITTEN		
<p>There is one 64-bit register for each of the 4 supported streams: 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Num Prims Written Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)			
1	31:0	Num Prims Written Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)			

Stream Output 2 Primitive Storage Needed Counter

SO2_PRIM_STORAGE_NEEDED - Stream Output 2 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05250h-05257h
Name:	Stream Output 2 Primitive Storage Needed Counter
ShortName:	SO2_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
 These registers are part of the context save and restore.

DWord	Bit	Description	
0	31:0	Prim Storage Needed Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.			
1	31:0	Prim Storage Needed Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.			



Stream Output 2 Write Offset

SO2_WRITE_OFFSET - Stream Output 2 Write Offset				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	05288h-0528Bh			
Name:	Stream Output 2 Write Offset			
ShortName:	SO2_WRITE_OFFSET			
<p>There is one R/W 32-bit register for each of the 4 supported stream output buffer slots: 5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0) 5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1) 5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2) 528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)</p> <p>These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>				
Programming Notes				
<ul style="list-style-type: none"> • Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. • The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so. 				
DWord	Bit	Description		
0	31:2	Write Offset		
		<table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Format:	U30
Format:	U30			
_Custom_GTIReset:	DEV			
	1:0	Reserved		
		Access:	RO	
		Format:	MBZ	

Stream Output 3 Num Primitives Written Counter

SO3_NUM_PRIMS_WRITTEN - Stream Output 3 Num Primitives Written Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05218h-0521Fh		
Name:	Stream Output 3 Num Primitives Written Counter		
ShortName:	SO3_NUM_PRIMS_WRITTEN		
<p>There is one 64-bit register for each of the 4 supported streams: 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0) 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1) 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2) 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Num Prims Written Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	
1	31:0	Num Prims Written Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)	



Stream Output 3 Primitive Storage Needed Counter

SO3_PRIM_STORAGE_NEEDED - Stream Output 3 Primitive Storage Needed Counter			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	64		
Address:	05258h-0525Fh		
Name:	Stream Output 3 Primitive Storage Needed Counter		
ShortName:	SO3_PRIM_STORAGE_NEEDED		
<p>There is one 64-bit register for each of the 4 supported streams: 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0) 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1) 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2) 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)</p> <p>These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume). These registers are part of the context save and restore.</p>			
DWord	Bit	Description	
0	31:0	Prim Storage Needed Count 0	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.	
1	31:0	Prim Storage Needed Count 1	
		Format:	U32
		_Custom_GTIReset:	DEV
		This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.	

Stream Output 3 Write Offset

SO3_WRITE_OFFSET - Stream Output 3 Write Offset				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	0528Ch-0528Fh			
Name:	Stream Output 3 Write Offset			
ShortName:	SO3_WRITE_OFFSET			
<p>There is one R/W 32-bit register for each of the 4 supported stream output buffer slots: 5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0) 5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1) 5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2) 528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)</p> <p>These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).</p> <p>These registers are part of the context save and restore.</p>				
Programming Notes				
<ul style="list-style-type: none"> Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush. The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so. 				
DWord	Bit	Description		
0	31:2	Write Offset		
		<table border="1"> <tr> <td>Format:</td> <td>U30</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <p>This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).</p>	Format:	U30
Format:	U30			
_Custom_GTIReset:	DEV			
	1:0	Reserved		
		Access:	RO	
		Format:	MBZ	

SubSlice0 Power Down FSM control register with lock

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24410h		
DWord	Bit	Description	
0	31	power down control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:13		Reserved	
		Access:	RO
		Format:	MBZ
12		Leave firewall disabled	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow	
11		Leave reset de-asserted	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow	
10		Leave CLKs ON	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:	

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

		<p>0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow</p>							
	9	<p>Leave FET On</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow</p>		Access:	R/W Lock	_Custom_GTIReset:	BUS		
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	8:6	<p>Power Down state 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks</p>		Default Value:	010b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	010b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	5:3	<p>Power Down state 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>001b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON</p>		Default Value:	001b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	001b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	2:0	<p>Power Down state 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future</p>		Default Value:	000b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	000b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								



SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock	
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	Default : Assert Reset
--	------------------------

SubSlice 0 Power Gate Control Request

SSM0PGCTLREQ - SubSlice 0 Power Gate Control Request			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24400h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:16	Message Mask	
		Access:	RO
		_Custom_GTIRreset:	BUS
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000	
	15:2	Reserved	
		Access:	RO
	1	1	CLK RST FWE Request
			Access:
		_Custom_GTIRreset:	BUS
		SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	Power Gate Request		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req			



SubSlice 0 Power on FSM control register with lock

SSM0SPCPOWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	2440Ch		
DWord	Bit	Description	
0	31	power up control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	30:9	Reserved	
		Access:	RO
		Format:	MBZ
	8:6	Power UP state 3	
		Default Value:	010b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)	
5:3	Power UP state 2		
	Default Value:	001b	
	Access:	R/W Lock	
	_Custom_GTIReset:	BUS	
This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF			

SSM0SPCPOWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

	2:0	Power UP state 1	
		Default Value:	000b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		<p>This will be the 1st state after power is turned ON in the well</p> <p>Encodings:</p> <p>000 = Clock Ungate</p> <p>001 = Firewall OFF</p> <p>010 = De-assert resets</p> <p>1xx = Rsvd for future</p> <p>Default - Clock Ungate</p>	



SubSlice 1 Power Context Save request

SSM1PGCTXREQ - SubSlice 1 Power Context Save request			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24484h		
DWord	Bit	Description	
0	31:16	Message Mask	
		Access:	RO
		_Custom_GTIReset:	BUS
		Message Mask bots for lower 16 bits	
15:10	Reserved	Access:	RO
		Format:	MBZ
9	Power context save request	Access:	R/W Set
		_Custom_GTIReset:	BUS
		Power Context Save Request	
		1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUUnit self-clears this bit upon sampling.	
8:0	Power Context Save request credit count	Access:	R/W
		_Custom_GTIReset:	BUS
		QWord Credits for Power Context Save Request	
		Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).	

SubSlice 1 Power Down FSM control register with lock

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Size (in bits): 32

Address: 24490h

DWord	Bit	Description	
0	31	power down control Lock	
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:13	Reserved	Access:	RO
		Format:	MBZ
12	Leave firewall disabled	Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow	
11	Leave reset de-asserted	Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow	
10	Leave CLKs ON	Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:	

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

		<p>0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow</p>							
	9	<p>Leave FET On</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow</p>		Access:	R/W Lock	_Custom_GTIReset:	BUS		
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	8:6	<p>Power Down state 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks</p>		Default Value:	010b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	010b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	5:3	<p>Power Down state 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>001b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON</p>		Default Value:	001b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	001b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	2:0	<p>Power Down state 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks</p>		Default Value:	000b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	000b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

		1xx = Rsvd for future Default : Assert Reset
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SubSlice 1 Power Gate Control Request

SSM1PGCTLREQ - SubSlice 1 Power Gate Control Request			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	24480h		
Clock Gating Messages Register			
DWord	Bit	Description	
0	31:16	Message Mask	
		Access:	RO
		_Custom_GTIRreset:	BUS
		Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000	
15:2	Reserved	Access:	RO
		Format:	MBZ
1	CLK RST FWE Request	Access:	R/W
		_Custom_GTIRreset:	BUS
		SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)	
0	Power Gate Request	Access:	R/W
		_Custom_GTIRreset:	BUS
		SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req	

SubSlice 1 Power on FSM control register with lock

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	2448Ch		
DWord	Bit	Description	
0	31	power up control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	30:9	Reserved	
		Access:	RO
		Format:	MBZ
	8:6	Power UP state 3	
		Default Value:	010b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
			This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
5:3	Power UP state 2		
	Default Value:	001b	
	Access:	R/W Lock	
	_Custom_GTIReset:	BUS	
		This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF	

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock

	2:0	Power UP state 1	
		Default Value:	000b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		<p>This will be the 1st state after power is turned ON in the well</p> <p>Encodings:</p> <p>000 = Clock Ungate</p> <p>001 = Firewall OFF</p> <p>010 = De-assert resets</p> <p>1xx = Rsvd for future</p> <p>Default - Clock Ungate</p>	

SubSlice 2 Power Down FSM control register with lock

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0

Size (in bits): 32

Address: 24510h

DWord	Bit	Description	
0	31	power down control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
30:13	Reserved	Access:	RO
		Format:	MBZ
12	Leave firewall disabled	Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow	
11	Leave reset de-asserted	Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow	
10	Leave CLKs ON	Access:	R/W Lock
		_Custom_GTIReset:	BUS
		When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings:	

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

		<p>0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow</p>							
	9	<p>Leave FET On</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow</p>		Access:	R/W Lock	_Custom_GTIReset:	BUS		
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	8:6	<p>Power Down state 3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>010b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks</p>		Default Value:	010b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	010b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	5:3	<p>Power Down state 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>001b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON</p>		Default Value:	001b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	001b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								
	2:0	<p>Power Down state 1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td>000b</td> </tr> <tr> <td>Access:</td> <td>R/W Lock</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future</p>		Default Value:	000b	Access:	R/W Lock	_Custom_GTIReset:	BUS
Default Value:	000b								
Access:	R/W Lock								
_Custom_GTIReset:	BUS								

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock	
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	Default : Assert Reset
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SubSlice 2 Power Gate Control Request

SSM2PGCTLREQ - SubSlice 2 Power Gate Control Request						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	24500h					
Clock Gating Messages Register						
DWord	Bit	Description				
0	31:16	Message Mask				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000</p>	Access:	RO	_Custom_GTIRreset:	BUS
	Access:	RO				
	_Custom_GTIRreset:	BUS				
15:2	Reserved					
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
1		CLK RST FWE Request				
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
	Access:	R/W				
_Custom_GTIRreset:	BUS					
0	Power Gate Request					
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

SubSlice 2 Power on FSM control register with lock

SSM2SPCPOWERUPFSMCTL - SubSlice 2 Power on FSM control register with lock			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	2450Ch		
DWord	Bit	Description	
0	31	power up control Lock	
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	30:9	Reserved	
		Access:	RO
		Format:	MBZ
	8:6	Power UP state 3	
		Default Value:	010b
		Access:	R/W Lock
		_Custom_GTIReset:	BUS
		This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)	
5:3	Power UP state 2		
	Default Value:	001b	
	Access:	R/W Lock	
	_Custom_GTIReset:	BUS	
	This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF		

SSM2SPCPOWERUPFSMCTL - SubSlice 2 Power on FSM control register with lock

	2:0	Power UP state 1	
		Default Value:	000b
		Access:	R/W Lock
		_Custom_GTIRreset:	BUS
		<p>This will be the 1st state after power is turned ON in the well</p> <p>Encodings:</p> <p>000 = Clock Ungate</p> <p>001 = Firewall OFF</p> <p>010 = De-assert resets</p> <p>1xx = Rsvd for future</p> <p>Default - Clock Ungate</p>	

SubSlice unit Level Clock Gating Control 9520

SSMCGCTL9520 - SubSlice unit Level Clock Gating Control 9520			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
CustomGTIIs_ContextSaved:	true		
Address:	09520h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:2	Reserved	
		Access:	RO
		Format:	MBZ
	1	GPCunit Clock Gating Disable	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIReset:	BUS
	GPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	0	SMCRunit Clock Gating Disable	
		Default Value:	1b
Access:		R/W	
_Custom_GTIReset:		BUS	
SMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			



SubSlice unit Level Clock Gating Control 9524

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09524h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31	EU_FPUunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	30	EU_GAunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	29	EU_TCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	28	DSS router Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		DSS router Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	27	BCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for	

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
26	Reserved	Access:	RO
		Format:	MBZ
25	CREunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	CREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
24	DGunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
23	DMunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
22	Reserved	Access:	RO
		Format:	MBZ
21	EUunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
20	FLunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	FLunit Clock Gating Disable Control:		

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	19	Reserved	
		Access:	RO
		Format:	MBZ
	18	Ftunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		<p>Ftunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	17	Reserved	
		Access:	RO
		Format:	MBZ
	16	GWunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		<p>GWunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	15:12	HDCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		<p>HDCunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	11	ICunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		<p>ICunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	10	Reserved	
		Access:	RO
		Format:	MBZ

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

9	IMEunit's Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	IMEunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
8	MAunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
7	MTunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
6	OATREPunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	OATREPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
5	PLunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
4	PSDunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	RAMDFT Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		RAMDFT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	SCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	Slunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		Slunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	SOunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

SubSlice unit Level Clock Gating Control 9528

SSMCGCTL9528 - SubSlice unit Level Clock Gating Control 9528			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09528h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:21	Reserved	
		Access:	RO
		Format:	MBZ
	20	VMESC Clock Gating Disable	
		Access:	R/W
		Format:	Disable
	19	MediaSampler arb unit2 Clock Gating Disable	
		Access:	R/W
		Format:	Disable
	18	MediaSampler arb unit1 Clock Gating Disable	
		Access:	R/W
		Format:	Disable
17	Reserved		
	Access:	RO	
	Format:	MBZ	
16	VAFE unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
15	TSL unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
14	MediaSampler arb unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	

SSMCGCTL9528 - SubSlice unit Level Clock Gating Control 9528

		_Custom_GTIReset:	BUS
13	DTOunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
12	SLMFE unit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
11	RDEunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
10	Noaunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
9	CPSSunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
8	EUunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
7	EU_EMunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
6	sbe_ssbuff Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
		_Custom_GTIReset:	BUS
5	DAPunit Clock Gating Disable		
	Access:	R/W	
		Format:	Disable

SSMCGCTL9528 - SubSlice unit Level Clock Gating Control 9528

		_Custom_GTIRreset:	BUS
4	Reserved		
	Access:	RO	
	Format:	MBZ	
3	STunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
2	SVRRunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
1	SVSMunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	
0	TDLunit Clock Gating Disable		
	Access:	R/W	
	Format:	Disable	
	_Custom_GTIRreset:	BUS	



SubSlice unit Level Clock Gating Control 9530

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09530h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:14	Reserved	
		Access:	RO
		Format:	MBZ
	13	SPARE Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
12	CPSSunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
CPSSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
11	AVSunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
AVSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
10	Reserved	Access:	RO
		Format:	MBZ
9	BCunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for			

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

	functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
8	<p>CREunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>CREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
7	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
6	<p>GAunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
5	<p>ICunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
4	<p>IMEunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>IMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
3	<p>MTunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
2	<p>PSDunit Clock Gating Disable</p>				

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

		Access:	R/W
		_Custom_GTIReset:	BUS
		PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	SCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	VSunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

SubSlice unit Level Clock Gating override during rstflow 9540

SSMMISCCP9540 - SubSlice unit Level Clock Gating override during rstflow 9540		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09540h	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:0	ECO Spare Bits
		Access: R/W
		_Custom_GTIRreset: BUS



Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	0002Eh	
This register is used to uniquely identify the subsystem where the PCI device resides.		
DWord	Bit	Description
0	15:0	Subsystem Identification
		Default Value: 0000000000000000b
		Access: R/W
		_Custom_GTIReset: BUS
		This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up.

Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification			
Register Space:	PCI: 0/2/0		
Size (in bits):	16		
Address:	0002Ch		
This register is used to uniquely identify the subsystem where the PCI device resides.			
DWord	Bit	Description	
0	15:0	Subsystem Vendor ID	
		Access:	R/W
		_Custom_GTIReset:	BUS
		This value is used to identify the vendor of the subsystem.	
		Value	Name
	0000000000000000b	[Default]	



Supported Page Sizes

SUPPORTED_PAGE_SIZES_0_2_0_PCI - Supported Page Sizes										
Register Space:	PCI: 0/2/0									
Size (in bits):	32									
Address:	0033Ch									
DWord	Bit	Description								
0	31:0	<p>SUPPORTED PAGE SIZES VALUE</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This field indicates the page sizes supported by the PF. This PF supports a page size of $2^{(n+12)}$ if bit n is Set. For example, if bit 0 is Set, the PF supports 4-KB page sizes. PFs are required to support 4-KB, 8-KB, 64-KB, 256-KB, 1-MB, and 4-MB page sizes. All other page sizes are optional, and not supported in this implementation.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00000000000000000000000010101010011b</td> <td>[Default]</td> </tr> </tbody> </table>	Access:	RO	_Custom_GTIReset:	BUS	Value	Name	00000000000000000000000010101010011b	[Default]
Access:	RO									
_Custom_GTIReset:	BUS									
Value	Name									
00000000000000000000000010101010011b	[Default]									

SVG Debug Control

SVG_CTL - SVG Debug Control			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	06400h-06403h		
DWord	Bit	Description	
0	31:16	Reserved	
		Access:	RO
		Format:	MBZ
	15:8	Debug Output Mux Select	
		Controls which 32 bits of the debug data are returned	
		Value	Name
		0	Return General State Base Address for the context that has debug enabled
		1	Return Surface State Base Address for the context that has debug enabled
		2	Return Indirect Object Base Address for the context that has debug enabled
		3	Return General State Access Upper Bound for the context that has debug enabled
4		Return Indirect Object Access Upper Bound for the context that has debug enabled	
5		Return Instruction base address for the context that has debug enabled	
6	Return Instruction address upper bound for the context that has debug enabled		
7	Return System Instruction Pointer for the context that has debug enabled		
[8,255]	Reserved: MBZ		
7:0	Reserved		
	Access:	RO	
	Format:	MBZ	



SVG Debug Return Data

SVG_RDATA - SVG Debug Return Data		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	06404h-06407h	
DWord	Bit	Description
0	31:0	SVG Debug Data Returns data based on debug output mux select.

SVL Barrier Done

SVL_BARRIER_DONE - SVL Barrier Done		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	07FF0h	
This register is used to send messages when a render barrier is done. This register may not be written from CPU.		
DWord	Bit	Description
0	31:16	Reserved
		Access: RO
		Format: MBZ
	15:8	Reserved
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
7:0	BarrierID	



SWF

SWF										
Register Space:	MMIO: 0/2/0									
Size (in bits):	32									
SOC_Consumer:	BIOS									
Address:	4F000h-4F08Fh									
Name:	Software Flags									
ShortName:	SWF_*									
<p>These registers are used as scratch pad data storage space and have no direct effect on hardware operation. There are 36 instances of this register format.</p>										
DWord	Bit	Description								
0	31:0	Software Flags <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> <tr> <td colspan="2">Software flags</td> </tr> </table>	Default Value:	00000000000000000000000000000000b	Access:	R/W	_Custom_GTIReset:	BUS	Software flags	
Default Value:	00000000000000000000000000000000b									
Access:	R/W									
_Custom_GTIReset:	BUS									
Software flags										

System Page Sizes

SYSTEM_PAGE_SIZES_0_2_0_PCI - System Page Sizes								
Register Space: PCI: 0/2/0								
Size (in bits): 32								
Address: 00340h								
Defines the System Page Size chosen by the VMM.								
DWord	Bit	Description						
0	31:0	<p>SYSTEM PAGE SIZES VALUE</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Default Value:</td> <td>00000000000000000000000000000001b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This field defines the page size the system will use to map the VFs memory addresses. Software must set the value of the System Page Size to one of the page sizes set in the Supported Page Sizes field (see Section 3.3.12). As with Supported Page Sizes, if bit n is Set in System Page Size, the VFs associated with this PF are required to support a page size of $2^{(n+12)}$. For example, if bit 1 is Set, the system is using an 8-KB page size. The results are undefined if System Page Size is zero. The results are undefined if more than one bit is set in System Page Size. The results are undefined if a bit is Set in System Page Size that is not Set in Supported Page Sizes.</p> <p>When System Page Size is set, the VF associated with this PF is required to align all BAR resources on a System Page Size boundary. Each VF BAR_n or VF BAR_n pair (see Section 3.3.14) shall be aligned on a System Page Size boundary. Each VF BAR_n or VF BAR_n pair defining a non-zero address space shall be sized to consume an integer multiple of System Page Size bytes. All data structures requiring page size alignment within a VF shall be aligned on a System Page Size boundary.</p> <p>VF Enable must be zero when System Page Size is written. The results are undefined if System Page Size is written when VF Enable is Set.</p> <p>Default value is 1h (i.e., 4 KB), and that is the only value allowed for this implementation</p>	Default Value:	00000000000000000000000000000001b	Access:	RO	_Custom_GTIRreset:	BUS
Default Value:	00000000000000000000000000000001b							
Access:	RO							
_Custom_GTIRreset:	BUS							



Tailpointer delay counter

TP_DELAY_CNTR - Tailpointer delay counter		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	1C2DA0h-1C2DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG0	
Address:	1C6DA0h-1C6DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG1	
Address:	1D2DA0h-1D2DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG2	
Address:	1D6DA0h-1D6DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG3	
Address:	1E2DA0h-1E2DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG4	
Address:	1E6DA0h-1E6DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG5	
Address:	1F2DA0h-1F2DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG6	
Address:	1F6DA0h-1F6DA3h	
Name:	Tailpointer delay counter	
ShortName:	TP_DELAY_CNTR_VDENC_REG7	
This register has stall counter for the VDENC. In an ideal case, this value should be zero		
DWord	Bit	Description
0	31:0	Tail pointer count delay Access: R/W Hardware Clear

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	0E4BCh			
This register provides the count of threads dispatched/valid in the subslice.				
DWord	Bit	Description		
0	31:6	Reserved		
		Access: RO		
	Format: MBZ			
	5:0	Thread Count		
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0-56</td> <td>Valid Range</td> </tr> </tbody> </table>		Value	Name	0-56
Value	Name			
0-56	Valid Range			



Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	0E5BCh	
This register provides the count of threads faulted in each subslice.		
DWord	Bit	Description
0	31	Canonical fault indication bit to CS The bit is set when a canonical fault on data fetch is reported by EU.
	30:6	Reserved
		Access:
	Format:	MBZ
5:0	Thread Count	
	Value	Name
	0-56	Valid Range

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	0E6B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row0, EU3, [Reserved, T6-T0]
	23:16	Row0, EU2, [Reserved, T6-T0]
	15:8	Row0, EU1, [Reserved, T6-T0]
	7:0	Row0, EU0, [Reserved, T6-T0]



Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	0E7B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0E4B8h	
This register provides the status of each thread in the SubSlice.		
DWord	Bit	Description
0	31:0	Reserved
		Access: RO
		Format: MBZ



Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0E5B8h	
This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.		
DWord	Bit	Description
0	31:24	Row1, EU3, [Reserved, T6-T0]
	23:16	Row1, EU2, [Reserved, T6-T0]
	15:8	Row1, EU1, [Reserved, T6-T0]
	7:0	Row1, EU0, [Reserved, T6-T0]

Thread Mode Register

FF_MODE - Thread Mode Register											
Register Space:	MMIO: 0/2/0										
Access:	R/W										
Size (in bits):	32										
_Custom_GTIReset:	DEV										
This register is used to program the FF shader Mode.											
DWord	Bit	Description									
0	31	TE Autostrip Disable									
		Format:	U1								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>TE will generate "autostrip" primitives (if/where possible) during tessellation.</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>TE will not generate "autostrip" primitives.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	TE will generate "autostrip" primitives (if/where possible) during tessellation.	1h	Disable	TE will not generate "autostrip" primitives.
		Value	Name	Description							
	0h	Enable [Default]	TE will generate "autostrip" primitives (if/where possible) during tessellation.								
	1h	Disable	TE will not generate "autostrip" primitives.								
	30	TDS external Cache Disable									
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable [Default]</td> <td>The external TDS Cache is enabled if there is enough handles to enable the cache.</td> </tr> <tr> <td>1b</td> <td>Disable</td> <td>The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Enable [Default]	The external TDS Cache is enabled if there is enough handles to enable the cache.	1b	Disable	The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.	
	Value	Name	Description								
	0b	Enable [Default]	The external TDS Cache is enabled if there is enough handles to enable the cache.								
1b	Disable	The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.									
29:26	DS Hit Max Value										
	Format:	U4									
	If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch.										
	Programming a value of 0 will disable the DS Hit Max counter logic and therefore partial dispatches will <u>not</u> be forced due to the number of hits seen during the accumulation of inputs for a thread dispatch.										
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>15</td> <td>[Default]</td> </tr> <tr> <td>[0,15]</td> <td></td> </tr> </tbody> </table>	Value	Name	15	[Default]	[0,15]					
Value	Name										
15	[Default]										
[0,15]											
25:20	VS Hit Max Value										
	Format:	U6									
	If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.										
	Since VS Reference Count Full Force miss enable was removed, the value can be [1,63].										

FF_MODE - Thread Mode Register

		Value	Name
		10	[Default]
		[1,63]	
19	Tessellation DOP gating Disable		
	Format:	Disable	
	Value	Name	Description
	0h	Enable [Default]	HS, TE, TETG, DS, GS and SOL units are DOP gated if all units are disabled
	1h	Disable	DOP gating is disabled for HS, TE, TETG, DS, GS and SOL units
	Programming Notes		
	Once this bit is set to a 1, it must not be cleared to a 0 until after a reset.		
18	TRI NOINSIDE Autostrip Cache Invalidate Disable		
	Format:	Disable	
	This bit can be used to control the TRI NOINSIDE Autostrip Cache Invalidate feature. By default the invalidation is ENABLED (allowing higher performance).		
	Value	Name	Description
	0h	Enable [Default]	TE will suppress the Autostrip cache invalidate for TRI NOINSIDE patches. This setting may improve performance.
	1h	Disable	TE will not suppress the Autostrip cache invalidate for TRI NOINSIDE patches.
	Programming Notes		
	<p>The setting of this field impacts the selection of the "provoking vertex" for the center triangle of TRI domains (if a center triangle exists given the tessellation factors), and this will in turn impact the generated image if any PS attributes are enabled as "flat shaded" and that/those attributes are not identical on all 3 vertices of the triangle. Given the fact that the APIs do not impose requirements on the starting/provoking vertices of the tessellation-generated triangles, the selection of provoking vertices can be arbitrary as long as it is deterministic (i.e., repeated rendering the same patch will yield the same results).</p> <p>Note: If FF_mode.TE autostrip Disable is set to 1, then TRI NOINSIDE Autostrip Cache Invalidate will also be disabled.</p>		
17	Thread fusing disable		
	Value	Name	Description
	1h	Disable	Fusing of threads will be disabled. Threads will not be fused.
	0h	[Default]	Fusing of threads will be enabled. Threads will be fused if all conditions are met to fuse a thread.

FF_MODE - Thread Mode Register		
16:15	Reserved	
	Format:	PBC
14:13	Reserved	
	Format:	PBC
12	Reserved	
	Default Value:	0h
	Format:	PBC
11:7	Reserved	
	Format:	PBC
6:5	Reserved	
	Format:	PBC
4	Reserved	
	Default Value:	0h
	Format:	PBC
3	Reserved	
	Format:	PBC
2	TDS Tracking fifo wrap fix disable	
	Format:	Disable
	Value	Name Description
	1h	Disable the tds tracking fifo wrap fix.
	0h	[Default] Enable the tds tracking fifo wrap fix.
1	Reserved	
	Format:	PBC
0	Reserved	
	Format:	PBC



Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register			
Register Space:	MMIO: 0/2/0		
Access:	WO		
Size (in bits):	32		
Address:	0E450h		
This register provides control to restart page faulted and halted threads in each subslice.			
DWord	Bit	Description	
0	31:1	Reserved	
		Access:	RO
		Format:	MBZ
0		Restart All Faulted Threads A write of 1 to this register restarts all threads that have halted due to page fault.	

Tile Cache Control Register

TCCNTLREG - Tile Cache Control Register				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	0B138h			
Name:	Tile Cache Control Register			
ShortName:	TCCNTLREG			
Address:	0B238h			
ShortName:	TCCNTLREG_CCS0			
DWord	Bit	Description		
0	31:25	Unified Tile Cache Pool		
		Access:	R/W	
		Number of ways allocated for the unified client pool. This is a combined pool for all streams.		
		Value	Name	Programming Notes
		00h	[Default]	When this field is non-zero, Z tile cache pool and C tile cache pool should be 0KB.
		[0h,68h]		
	24:18	Z Tile Cache Pool		
		Access:	R/W	
		Number of ways allocated for Z streams.		
		Value	Name	Programming Notes
		00h	[Default]	Note: This field must be 0KB if Unified Tile cache Pool is non-zero.
		[0h,68h]		
17:11	C Tile Cache Pool			
	Access:	R/W		
	Number of ways allocated for Color Streams			
	Value	Name	Programming Notes	
	00h	[Default]	Note: This field must be 0KB if Unified Tile cache Pool is non-zero.	
	[0h,68h]			
10:4	Command Streamer Allocation			
	Access:	R/W		
	Number of ways allocated for CS(Command Streamer)			
	Value	Name		
	00h	[Default]		
	[0h,68h]			

TCCNTLREG - Tile Cache Control Register			
3	Reserved		
	Access:	RO	
	Format:	MBZ	
	2	L3 Data partial write merging enable	
		Default Value:	1
		Format:	Enable
	1	Color/Z write partial write merging enable	
		Format:	Enable
		Value	Name
			Description
		0	[Default] Partial write merging optimization (in SQDB) will be disabled for Color/Z bound cycles.
	0	Reserved	
Access:		RO	
Format:		MBZ	

TILECTL

TILECTL - TILECTL			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	101000h		
Tile control and TLB control.			
DWord	Bit	Description	
0	31:2	Reserved	
		Access:	RO
		Format:	MBZ
	1	TLBPF	
		Default Value:	0b
		Access:	R/W
		_Custom_GTIReset:	BUS
	Store multiple PTE enable. 0: Only one Page Table Entry is stored in the Translation Lookaside Buffer cache. 1: Multiple Page Table Entries (8) are stored in the Translation Lookaside Buffer cache.		
	0	SWZCTL	
		Default Value:	0b
Access:		R/W	
_Custom_GTIReset:		BUS	
In order to spread DRAM accesses between multiple channels in the most efficient way, address bits can be used as a channel select. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces			



TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	04DECh					
Name:	TiledResources Invalid Tile Detection Register					
ShortName:	TRINVTILEDETCT					
DWord	Bit	Description				
0	31:0	Invalid Tile Detection Value				
		Access:	R/W			
		_Custom_GTIReset:	DEV			
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000000h</td> <td>[Default]</td> <td>A 32-bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.</td> </tr> </tbody> </table>	Value	Name	Description	00000000h
Value	Name	Description				
00000000h	[Default]	A 32-bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.				

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	04DF0h					
Name:	TiledResources VA Detection Registers					
ShortName:	TRVADR					
DWord	Bit	Description				
0	31:8	Reserved				
		Access:	RO			
		Format:	MBZ			
	7:4	TR - VA Mask Value				
		Default Value:	0000b			
		Access:	R/W			
		_Custom_GTIRreset:	DEV			
		<p>4bit MASK value that is mapped to incoming address bits[47:44] MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection). Note: The only usage model for GFX driver to set this field to "1111". Behavior of h/w for any other setting is not defined. Note: GFX driver shall use same TRVA MASK value for all contexts.</p>				
	3:0	TR- VA Data Value				
		Access:	R/W			
_Custom_GTIRreset:		DEV				
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>[Default]</td> <td>4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts</td> </tr> </tbody> </table>		Value	Name	Description	0000b	[Default]
Value	Name	Description				
0000b	[Default]	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts				

Tiled Resources Wrapper Write Data Port arbitration

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	04DF8h	
Name:	Tiled Resources Wrapper Write Data Port arbitration	
ShortName:	TRWRPARB	
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ
	12:10	L3 Max Write Request Limit Count
		Default Value: 100b
		Access: R/W
		_Custom_GTIReset: DEV
	This is the MAX number of Allowed writes from L3 before switching the priority to Z Requests Count - Minimum count value must be 1	
	9	Reserved
		Access: RO
		Format: MBZ
	8:6	Z Max Write Request Limit Count
		Default Value: 010b
		Access: R/W
		_Custom_GTIReset: DEV
	This is the MAX number of Allowed writes from Z before switching the priority to C Requests Count - Minimum count value must be = 1	
5	Reserved	
	Access: RO	
	Format: MBZ	
4:2	C Max Write Request Limit Count	
	Default Value: 010b	
	Access: R/W	
	_Custom_GTIReset: DEV	
This is the MAX number of Allowed writes from C before switching to L3 Request Count - Minimum count value = 1		

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

	1	Reserved	
		Access:	RO
		Format:	MBZ
	0	Fixed Arbitration enable	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIRreset:	DEV
		Fixed Arbitration enable when 1'b1 Programmable arbitration when 1'b0	



TIMESTAMP_CTR

TIMESTAMP_CTR		
Register Space:	MMIO: 0/2/0	
Access:	R/WC	
Size (in bits):	32	
Address:	44070h-44073h	
Name:	Time Stamp Counter	
ShortName:	TIMESTAMP_CTR	
Reset:	global	
The register is not reset by a FLR.		
DWord	Bit	Description
0	31:0	TIMESTAMP Counter This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a FLR.

TLBInvalidationRegister_BLT

BLT_TLB_INV_CR - TLBInvalidationRegister_BLT		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	DEV	
Address:	0CEE4h	
Name:	BLT TLB Invalidation Register	
ShortName:	BLT_TLB_INV_CR	
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
		Format: MBZ
	0	Invalidate TLBs on the corresponding Engine Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.



TLBInvalidationRegister_GFX

GFX_TLB_INV_CR - TLBInvalidationRegister_GFX		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIRreset:	DEV	
Address:	0CED8h	
Name:	GFX TLB Invalidation Register	
ShortName:	GFX_TLB_INV_CR	
DWord	Bit	Description
0	31:1	Reserved
		Access: RO
		Format: MBZ
0	0	Invalidate TLBs on the corresponding Engine
		Default Value: 0b
		Access: R/W
SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.		

TLBInvalidationRegister_GUC

GUC_TLB_INV_CR - TLBInvalidationRegister_GUC						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
_Custom_GTIRReset:	DEV					
_Custom_GTIHardWiredEnable:	clr_reg_ga_cee8					
Address:	0CEE8h					
Name:	GUC TLB Invalidation Register					
ShortName:	GUC_TLB_INV_CR					
_Custom_GTIHardWiredEnable:	clr_reg_ga_cee8					
DWord	Bit	Description				
0	31:1	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
0	0	Invalidate TLBs on the corresponding Engine				
		<table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Default Value:	0b	Access:	R/W
		Default Value:	0b			
Access:	R/W					
<p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.</p> <p>This bit is self clear.</p>						

TLBInvalidationRegister_OA

OA_TLB_INV_CR - TLBInvalidationRegister_OA			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIRreset:	DEV		
Address:	0CEECh		
Name:	OA TLB Invalidation Register		
ShortName:	OA_TLB_INV_CR		
DWord	Bit	Description	
0	31:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	Invalidate TLBs on the corresponding Engine	
	Default Value:	0b	
	Access:	R/W	
<p>SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.</p> <p>This bit is self clear.</p>			

Top of Low Usable DRAM Register

TOLUD_REG - Top of Low Usable DRAM Register								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	108000h							
This 32 bit register defines the Top of Low Usable DRAM. GT uses this to ensure no GT memory accesses occur between 4GB and TOLUD.								
DWord	Bit	Description						
0	31:20	<p>TOLUD</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">001h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. BIOS must set this value. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register.</p>	Default Value:	001h	Access:	R/W	_Custom_GTIReset:	BUS
	Default Value:	001h						
Access:	R/W							
_Custom_GTIReset:	BUS							
19:0	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ			
Access:	RO							
Format:	MBZ							



TOUUD_LSB_REG

TOUUD_LSB_REG - TOUUD_LSB_REG			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	108080h		
<p>This 64 bit register defines the Top of Upper Usable DRAM. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB.</p> <p>All the bits in this register have SAI policy group protection.</p>			
DWord	Bit	Description	
0	31:20	TOUUD	
		Default Value:	001h
		Access:	R/W
		_Custom_GTIReset:	BUS
	<p>This register contains the LSB portion (bits 31 to 20) of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.</p> <p>Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB.</p>		
	19:1	Reserved	
		Access:	RO
		Format:	MBZ
	0	SPARE	
		Default Value:	0b
Access:		R/W	
_Custom_GTIReset:		BUS	

TOUUD_MSB_REG

TOUUD_MSB_REG - TOUUD_MSB_REG								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	108084h							
This is the most significant 32 bits of a 64 bit register that defines the Top of Upper Usable DRAM. BIOS Restriction: Minimum value for TOUUD is 4GB.								
DWord	Bit	Description						
0	31:0	<p>TOUUD</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>This register contains bits 63 to 32 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.</p>	Default Value:	00000000h	Access:	R/W	_Custom_GTIRreset:	BUS
Default Value:	00000000h							
Access:	R/W							
_Custom_GTIRreset:	BUS							



TRANS_CLK_SEL

TRANS_CLK_SEL																								
Register Space:	MMIO: 0/2/0																							
Access:	R/W																							
Size (in bits):	32																							
Address:	46140h-46143h																							
Name:	Transcoder A Clock Select																							
ShortName:	TRANS_CLK_SEL_A																							
Reset:	soft																							
Address:	46144h-46147h																							
Name:	Transcoder B Clock Select																							
ShortName:	TRANS_CLK_SEL_B																							
Reset:	soft																							
Address:	46148h-4614Bh																							
Name:	Transcoder C Clock Select																							
ShortName:	TRANS_CLK_SEL_C																							
Reset:	soft																							
Address:	4614Ch-4614Fh																							
Name:	Transcoder D Clock Select																							
ShortName:	TRANS_CLK_SEL_D																							
Reset:	soft																							
This register maps the port clock to the transcoder.																								
DWord	Bit	Description																						
0	31:28	<p>Trans Clock Select Select which DDI clock to use for this transcoder.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0000b</td> <td>None - Clock Disabled</td> </tr> <tr> <td style="text-align: center;">0001b</td> <td>DDI A</td> </tr> <tr> <td style="text-align: center;">0010b</td> <td>DDI B</td> </tr> <tr> <td style="text-align: center;">0011b</td> <td>DDI C</td> </tr> <tr> <td style="text-align: center;">0100b</td> <td>DDI USBC1</td> </tr> <tr> <td style="text-align: center;">0101b</td> <td>DDI USBC2</td> </tr> <tr> <td style="text-align: center;">0110b</td> <td>DDI USBC3</td> </tr> <tr> <td style="text-align: center;">0111b</td> <td>DDI USBC4</td> </tr> <tr> <td style="text-align: center;">1000b</td> <td>DDI USBC5</td> </tr> <tr> <td style="text-align: center;">1001b</td> <td>DDI USBC6</td> </tr> </tbody> </table>	Value	Name	0000b	None - Clock Disabled	0001b	DDI A	0010b	DDI B	0011b	DDI C	0100b	DDI USBC1	0101b	DDI USBC2	0110b	DDI USBC3	0111b	DDI USBC4	1000b	DDI USBC5	1001b	DDI USBC6
Value	Name																							
0000b	None - Clock Disabled																							
0001b	DDI A																							
0010b	DDI B																							
0011b	DDI C																							
0100b	DDI USBC1																							
0101b	DDI USBC2																							
0110b	DDI USBC3																							
0111b	DDI USBC4																							
1000b	DDI USBC5																							
1001b	DDI USBC6																							

TRANS_CLK_SEL		
		Restriction
		This must not be changed while the transcoder is enabled.
	27:0	Reserved
		Access: RO
		Format: MBZ



TRANS_CONF

TRANS_CONF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint: Start of vertical blank (WD cap sync) OR transcoder disabled	
Address:	7E008h-7E00Bh
Name:	Transcoder WD0 Configuration
ShortName:	TRANS_CONF_WD0
Reset:	soft
Address:	7D008h-7D00Bh
Name:	Transcoder WD1 Configuration
ShortName:	TRANS_CONF_WD1
Reset:	soft
Address:	7B008h-7B00Bh
Name:	Transcoder DSI 0 Configuration
ShortName:	TRANS_CONF_DSI0
Reset:	soft
Address:	7B808h-7B80Bh
Name:	Transcoder DSI 1 Configuration
ShortName:	TRANS_CONF_DSI1
Reset:	soft
Address:	70008h-7000Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_A
Reset:	soft
Address:	71008h-7100Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_B
Reset:	soft
Address:	72008h-7200Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_C
Reset:	soft
Address:	73008h-7300Bh
Name:	Transcoder Configuration

TRANS_CONF																	
ShortName:		TRANS_CONF_D															
Reset:		soft															
DWord	Bit	Description															
0	31	Transcoder Enable Setting this bit to the value of one, turns on this transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Enabling the transcoder may be internally delayed for one frame while the display data buffers are re-configured.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable									
		Value	Name														
		0b	Disable														
1b	Enable																
Restriction																	
Timing registers must contain valid values before this bit is enabled.																	
	30	Transcoder State Access: RO This read only bit indicates the actual state of the transcoder.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Value	Name	0b	Disabled	1b	Enabled									
		Value	Name														
		0b	Disabled														
1b	Enabled																
<table border="1"> <tbody> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </tbody> </table>		Access:	RO	Format:	MBZ												
Access:	RO																
Format:	MBZ																
29:23		Reserved Access: RO Format: MBZ															
22:21		Interlaced Mode These bits control the transcoder interlaced mode. This field is ignored by WD.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>PF-PD</td> <td>Progressive Fetch with Progressive Display</td> </tr> <tr> <td>01b</td> <td>PF-ID</td> <td>Progressive Fetch with Interlaced Display</td> </tr> <tr> <td>11b</td> <td>IF-ID</td> <td>Interlaced Fetch with Interlaced Display</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	00b	PF-PD	Progressive Fetch with Progressive Display	01b	PF-ID	Progressive Fetch with Interlaced Display	11b	IF-ID	Interlaced Fetch with Interlaced Display	Others	Reserved	Reserved
		Value	Name	Description													
		00b	PF-PD	Progressive Fetch with Progressive Display													
		01b	PF-ID	Progressive Fetch with Interlaced Display													
		11b	IF-ID	Interlaced Fetch with Interlaced Display													
		Others	Reserved	Reserved													
Programming Notes																	
Progressive Fetch with Interlaced Display requires pipe scaling.																	
Restriction																	
VGA display modes do not work while in interlaced fetch mode. Progressive Fetch with Interlaced Display effectively down scales the vertical by 2X, which reduces the maximum supported pixel rate by half.																	
Interlaced fetch mode is not supported with Y Tiling. Interlaced fetch mode is not supported																	

TRANS_CONF	
	with 90/270 rotation. Interlaced fetch mode is not supported with scaling. Interlaced fetch mode is not supported with YUV 420 hybrid planar source pixel formats. In Interlaced mode, the plane height must be a minimum of 2 scanlines.
20:12	Reserved
	Access: RO
	Format: MBZ
11:8	Reserved
7	Reserved
6:0	DP Audio Symbol Watermark
	Default Value: 24h 36 entries
	This fields set the level to which the DP audio symbol RAM must fill before it starts to drain during horizontal blank. The minimum is 2 entries and the maximum is 64.

TRANS_DDI_FUNC_CTL

TRANS_DDI_FUNC_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	6B400h-6B403h							
Name:	Transcoder DSI 0 DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_DSI0							
Reset:	soft							
Address:	6BC00h-6BC03h							
Name:	Transcoder DSI 1 DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_DSI1							
Reset:	soft							
Address:	60400h-60403h							
Name:	Transcoder DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_A							
Reset:	soft							
Address:	61400h-61403h							
Name:	Transcoder DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_B							
Reset:	soft							
Address:	62400h-62403h							
Name:	Transcoder DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_C							
Reset:	soft							
Address:	63400h-63403h							
Name:	Transcoder DDI Function Control							
ShortName:	TRANS_DDI_FUNC_CTL_D							
Reset:	soft							
DWord	Bit	Description						
0	31	TRANS DDI Function Enable This bit enables the transcoder DDI function.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
	0b	Disable						
1b	Enable							
30:27	DDI Select							

TRANS_DDI_FUNC_CTL

These bits determine which DDI port this transcoder will connect to. It is not valid to enable and direct more than one transcoder to one DDI, except when using DisplayPort multistreaming.

This field is ignored by the DSI transcoders since they have a fixed DDI mapping.

Value	Name
0000b	None
0001b	DDI A
0010b	DDI B
0011b	DDI C
0100b	DDI USBC1
0101b	DDI USBC2
0110b	DDI USBC3
0111b	DDI USBC4
1000b	DDI USBC5
1001b	DDI USBC6

Restriction

This field must not be changed while the function is enabled.

26:24 TRANS DDI Mode Select

This field determines the mode of operation. HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. DVI mode will function as HDMI if DIP packets or audio are enabled.

This field does not apply to the DSI transcoder.

Value	Name	Description
000b	HDMI	Function in HDMI mode
001b	DVI	Function in DVI mode
010b	DP SST	Function in DisplayPort SST mode
011b	DP MST	Function in DisplayPort MST mode
Others	Reserved	Reserved

Restriction

This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this transcoder.

Trans DDI mode select should be programmed to MST in the same register write as MST transport select (field [11:10] in this register).

TRANS_DDI_FUNC_CTL			
23	Reserved		
	Access:	RO	
	Format:	MBZ	
	22:20	Bits Per Color	
		This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.	
		This field does not apply to the DSI transcoder. The Pixel Format for the DSI transcoder is defined within the TRANS_DSI_FUNC_CONF register.	
		Value	Name
		000b	8 bpc
		001b	10 bpc
		010b	6 bpc
		011b	12 bpc
		Others	Reserved
Restriction			
This field must not be changed while the function is enabled.			
6bpc not supported with HDMI.			
6bpc not supported with VDSC.			
19:18	Reserved		
	Access:	RO	
	Format:	MBZ	
17:16	Sync Polarity		
	This field indicates the polarity of Hsync and Vsync.		
	Field ignored by the DSI transcoder		
	Value	Name	
	00b	Low	
	01b	VS Low, HS High	
10b	VS High, HS Low		
11b	High [Default]		
15	Reserved		
	Access:	RO	
	Format:	MBZ	

TRANS_DDI_FUNC_CTL

	14:12	<p>DSI Input Select</p> <p>These bits determine the input to transcoder DSI. These bits are ignored by the other transcoders.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Pipe A</td> </tr> <tr> <td>101b</td> <td>Pipe B</td> </tr> <tr> <td>110b</td> <td>Pipe C</td> </tr> <tr> <td>111b</td> <td>Pipe D</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.</p>	Value	Name	000b	Pipe A	101b	Pipe B	110b	Pipe C	111b	Pipe D	Others	Reserved
Value	Name													
000b	Pipe A													
101b	Pipe B													
110b	Pipe C													
111b	Pipe D													
Others	Reserved													
	11:10	<p>MST Transport Select</p> <p>This field selects which DP transport the DP data from this transcoder is sent to for MST stream combining. This field is ignored when MST is disabled.</p> <p>Restriction : MST transport select should be programmed in the same register write as Trans DDI mode select (field [26:24] in this register).</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>DPTP A</td> </tr> <tr> <td>01b</td> <td>DPTP B</td> </tr> <tr> <td>10b</td> <td>DPTP C</td> </tr> <tr> <td>11b</td> <td>DPTP D</td> </tr> </tbody> </table> <p style="text-align: center;">Restriction</p> <p>This field must not be changed while the function is enabled.</p>	Value	Name	00b	DPTP A	01b	DPTP B	10b	DPTP C	11b	DPTP D		
Value	Name													
00b	DPTP A													
01b	DPTP B													
10b	DPTP C													
11b	DPTP D													
	9	Reserved												
	8	<p>DP VC Payload Allocate</p> <p>This bit enables DisplayPort Virtual Channel payload allocation. This bit is ignored by transcoder EDP since it does not support multistreaming.</p> <p>This bit is ignored by transcoder DSI since it does not support multistreaming</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Value</th> <th style="width: 50%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable						
Value	Name													
0b	Disable													
1b	Enable													

TRANS_DDI_FUNC_CTL

7	HDMI Scrambler CTS Enable This bit enables Compliance Test Specification mode on the HDMI scrambler. This bit must be set before the scrambler is enabled. This bit is ignored by transcoder DSI		
	Value	Name	
	0b	Disable	
	1b	True	
6	HDMI Scrambler Reset frequency This bit specifies the frequency at which the scrambler is reset when the HDMI Scrambler CTS Enable bit is set. This bit must be set before or along with the HDMI Scrambler CTS Enable bit.		
	Value	Name	Description
	0b	Every Line	SSCP sent on hsync of every line
	1b	Every Other Line	SSCP sent on hsync of every other line
5	Reserved		
4	High TMDS Char Rate This field enables the high TMDS character rate. It must be enabled when the HDMI link symbol rate is greater than 340 MHz. It must be disabled when the HDMI link symbol rate is less than or equal to 340 MHz.		
	Value	Name	Description
	0	Disable	TMDS Character Rate is less than or equal to 340 Mega-characters/second/channel
	1	Enable	TMDS Character Rate is greater than 340 Mega-characters/second/channel
3:1	Port Width Selection <div style="text-align: center; background-color: #e0e0e0; padding: 5px;">Description</div> This field selects the number of lanes to be enabled on the DDI link for DisplayPort and DSI. for DSI, this field specifies the number of Data lanes to use - the Clock lane is always enabled when the DSI function is enabled. This field is ignored for HDMI and DVI which always use all 4 lanes. The value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.		
	Value	Name	Description
	000b	x1	x1 Mode
	001b	x2	x2 Mode
	010b	x3	[] x3 Mode (DSI only)
	011b	x4	x4 Mode
	Others	Reserved	Reserved

TRANS_DDI_FUNC_CTL							
	<table border="1"> <thead> <tr> <th colspan="2" style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td colspan="2">This field must not be changed while the DDI is enabled.</td> </tr> </tbody> </table>	Restriction		This field must not be changed while the DDI is enabled.			
Restriction							
This field must not be changed while the DDI is enabled.							
0	<p>HDMI Scrambling Enabled Setting this bit enables scrambling over the HDMI link. Scrambling must be enabled when the HDMI link symbol rate is greater than 340 MHz. Scrambling should be enabled at lower frequencies if the receiver supports it at that speed. This must not changed while the port is enabled.</p> <table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name						
0b	Disable						
1b	Enable						

TRANS_DDI_FUNC_CTL2

TRANS_DDI_FUNC_CTL2								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	6B404h-6B407h							
Name:	Transcoder DSI 0 DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_DSI0							
Reset:	soft							
Address:	6BC04h-6BC07h							
Name:	Transcoder DSI 1 DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_DSI1							
Reset:	soft							
Address:	60404h-60407h							
Name:	Transcoder DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_A							
Reset:	soft							
Address:	61404h-61407h							
Name:	Transcoder DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_B							
Reset:	soft							
Address:	62404h-62407h							
Name:	Transcoder DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_C							
Reset:	soft							
Address:	63404h-63407h							
Name:	Transcoder DDI Function Control2							
ShortName:	TRANS_DDI_FUNC_CTL2_D							
Reset:	soft							
DWord	Bit	Description						
0	31	Genlock Enable						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Enable</td> </tr> <tr> <td>0b</td> <td>Disable</td> </tr> </tbody> </table>	Value	Name	1b	Enable	0b	Disable
		Value	Name					
	1b	Enable						
0b	Disable							
30:29	Genlock Mode							

TRANS_DDI_FUNC_CTL2																	
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>10b</td> <td>Primary</td> <td>Primary transcoder outputs frame sync for other transcoders to secondary to.</td> </tr> <tr> <td>00b</td> <td>Local Secondary</td> <td>Local secondary transcoder secondaries to frame sync from a primary transcoder in the same device. The primary transcoder is selected by Port Sync Mode Primary Select.</td> </tr> <tr> <td>01b</td> <td>Remote Secondary</td> <td>Remote secondary transcoder secondaries to frame sync from a primary transcoder in a different device.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Value	Name	Description	10b	Primary	Primary transcoder outputs frame sync for other transcoders to secondary to.	00b	Local Secondary	Local secondary transcoder secondaries to frame sync from a primary transcoder in the same device. The primary transcoder is selected by Port Sync Mode Primary Select.	01b	Remote Secondary	Remote secondary transcoder secondaries to frame sync from a primary transcoder in a different device.	11b	Reserved		
Value	Name	Description															
10b	Primary	Primary transcoder outputs frame sync for other transcoders to secondary to.															
00b	Local Secondary	Local secondary transcoder secondaries to frame sync from a primary transcoder in the same device. The primary transcoder is selected by Port Sync Mode Primary Select.															
01b	Remote Secondary	Remote secondary transcoder secondaries to frame sync from a primary transcoder in a different device.															
11b	Reserved																
28	Reserved																
	Access:	RO															
	Format:	MBZ															
27:9	Reserved																
	Access:	RO															
	Format:	MBZ															
8	Double Buffer Vactive																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Normal Vactive</td> </tr> <tr> <td>1b</td> <td>Double Buffer Vactive</td> </tr> </tbody> </table>	Value	Name	0b	Normal Vactive	1b	Double Buffer Vactive										
Value	Name																
0b	Normal Vactive																
1b	Double Buffer Vactive																
7:6	Audio Mute Override																
	This field overrides audio mutesignal in VBID.																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b,01b</td> <td>Do not override</td> <td></td> </tr> <tr> <td>10b</td> <td>Override and reset</td> <td>Override audio mute bit to '0'.</td> </tr> <tr> <td>11b</td> <td>Override and set</td> <td>Override audio mute bit to '1'.</td> </tr> </tbody> </table>	Value	Name	Description	00b,01b	Do not override		10b	Override and reset	Override audio mute bit to '0'.	11b	Override and set	Override audio mute bit to '1'.				
Value	Name	Description															
00b,01b	Do not override																
10b	Override and reset	Override audio mute bit to '0'.															
11b	Override and set	Override audio mute bit to '1'.															
5	Dual Pipe Sync Enable																
	This bit informs the DSI transcoder that while it is synchronized with another DSI transcoder, it will also be driven by a separate Pipe																
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> <td>Both transcoders are being driven by a single Pipe (Dual Link - Single Pipe)</td> </tr> <tr> <td>1b</td> <td>Enabled</td> <td>Each transcoder is being driven by a separate Pipe (Dual Link - Dual Pipe)</td> </tr> </tbody> </table>	Value	Name	Description	0b	Disabled	Both transcoders are being driven by a single Pipe (Dual Link - Single Pipe)	1b	Enabled	Each transcoder is being driven by a separate Pipe (Dual Link - Dual Pipe)							
Value	Name	Description															
0b	Disabled	Both transcoders are being driven by a single Pipe (Dual Link - Single Pipe)															
1b	Enabled	Each transcoder is being driven by a separate Pipe (Dual Link - Dual Pipe)															
4	Port Sync Mode Enable																
	This field enables the DisplayPort port sync mode on this transcoder. This mode forces two or more transcoders to be in sync; with one transcoder primary and one or more transcoder secondaries. The primary is unaware that it is operating in this mode. Only the secondary is aware that it is operating in this mode. Port sync mode is only enabled in the secondary transcoder.																
	For DSI, this bit enables DSI Transcoder 1 to be a secondary to DSI Transcoder 0. DSI																

TRANS_DDI_FUNC_CTL2

		Transcoder 0 is unaware that it is the primary of DSI Transcoder 1	
		Value	Name
		0b	Disable
		1b	Enable
		Restriction	
		<p>Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort.</p> <p>Port Sync Mode Primary Select must be programmed with a valid value when Port sync Mode is enabled.</p> <p>The secondary and primary transcoders and associated ports must have identical parameters and properties; same color format, link width (number of lanes enabled), resolution, refresh rate, PLL configuration, dot clock, TU size, M and N programming, etc. Spread spectrum clocking cannot be used when the ports use separate PLLs.</p> <p>Port Sync Mode can be enabled with DisplayPort SST and with DisplayPort MST.</p>	
3	Reserved	Access:	RO
		Format:	MBZ
2:0	Port Sync Mode Primary Select	Description	
		This field indicates which transcoder will be the primary to this transcoder when in port sync mode.	
		This field is ignored by the DSI transcoders since only DSI 0 can be the primary.	
		This field is also used for genlock for the local secondary transcoder to select a primary transcoder.	
		Value	Name
		001b	Transcoder A
		010b	Transcoder B
		011b	Transcoder C
		100b	Transcoder D
		Restriction	
		A port cannot be secondaries to itself.	
		The DSI transcoders cannot be secondary to a non-DSI transcoder - field ignored by the DSI transcoder.	



TRANS_DSI_FUNC_CONF

TRANS_DSI_FUNC_CONF						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	6B030h-6B033h					
Name:	Transcoder DSI 0 Function Configuration					
ShortName:	TRANS_DSI_FUNC_CONF_0					
Reset:	soft					
Address:	6B830h-6B833h					
Name:	Transcoder DSI 1 Function Configuration					
ShortName:	TRANS_DSI_FUNC_CONF_1					
Reset:	soft					
<p>This register defines the functional transcoder configuration that is specific to the DSI transcoders.</p> <p>Restriction : This register must be programmed before the DSI Transcoder function is enabled (i.e. TRANS DDI Function Enable) The contents of this register must not be changed while the DSI Transcoder function is enabled</p>						
DWord	Bit	Description				
0	31:30	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
0	29:28	Mode of Operation				
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W		
		Access:	R/W			
		<p>This defines whether the DSI transcoder is in Video or Command mode. In addition to the main modes, there are two sub-modes per main mode.</p> <p>For the Command sub-modes, when in the "No Gate" mode, the transcoder will begin transmitting the frame pixels as soon as they are received from the Display Engine. When in the "TE Gate" mode, the transcoder will only start transmitting the frame pixels after a TE event is received.</p> <p>For the Video sub-modes, when in the Sync Event mode only Sync Start packets (VSS/HSS) are sent to the Periphery. When in the Sync Pulse mode, both Sync Start (VSS/HSS) and Sync End (VSE/HSE) packets are sent to the Periphery.</p> <p>Note that regardless of the programming of this field, until the Transcoder Enable bit is set within the TRANS_CONF_DSI register, the DSI transcoder will not generate any timing information to the Display Engine or timing packets to the Peripheral</p>				
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Command Mode (No Gate)</td> </tr> <tr> <td>01b</td> <td>Command Mode (TE Gate)</td> </tr> </tbody> </table>	Value	Name	00b	Command Mode (No Gate)	01b	Command Mode (TE Gate)
Value	Name					
00b	Command Mode (No Gate)					
01b	Command Mode (TE Gate)					

TRANS_DSI_FUNC_CONF									
	<table border="1"> <tr> <td>10b</td> <td>Video Mode (Sync Event)</td> </tr> <tr> <td>11b</td> <td>Video Mode (Sync Pulse)</td> </tr> </table>	10b	Video Mode (Sync Event)	11b	Video Mode (Sync Pulse)				
10b	Video Mode (Sync Event)								
11b	Video Mode (Sync Pulse)								
27	<p>TE Source</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit defines the source of the TE events from the Peripheral when the Transcoder is operating in Command Mode</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>In-band TE event source</td> </tr> <tr> <td>1</td> <td>Out-of-band TE event source (i.e. GPIO)</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0	In-band TE event source	1	Out-of-band TE event source (i.e. GPIO)
Access:	R/W								
Value	Name								
0	In-band TE event source								
1	Out-of-band TE event source (i.e. GPIO)								
26	<p>TE Deglitch Enable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>When using the GPIO as the source of TE events in Command Mode, this bit will control whether the signaling from the GPIO pin is debounced or not.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0b	Disabled	1b	Enabled
Access:	R/W								
Value	Name								
0b	Disabled								
1b	Enabled								
25	<p>TE Accumulation</p> <p>This bit controls whether the TE events from two Panels are accumulated into a single event (usage would be for a Dual Link mode). The accumulated event will feed into the interrupt registers for each DSI transcoder pair (e.g. DSI0 and DSI1).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> </tr> <tr> <td>1b</td> <td>Enabled</td> </tr> </tbody> </table> <p style="text-align: center;">Programming Notes</p> <ol style="list-style-type: none"> This bit only affects the operation of the transcoder when it is operating in the Command Mode It is the responsibility of Software to set this bit accordingly (i.e. it must ensure TE events are being received from both ports) Even though the accumulated event is being fed to the interrupt registers of both transcoders, it is ultimately up to Software on how it enables the TE Interrupt across both transcoders Hardware will automatically enable this feature (i.e. it will override the bit programming) when Periodic Frame Update and Port Sync Mode are enabled for both transcoders. Hardware will use the accumulated TE events to spawn the Frame Update Requests to each transcoder 	Value	Name	0b	Disabled	1b	Enabled		
Value	Name								
0b	Disabled								
1b	Enabled								
24:21	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								

TRANS_DSI_FUNC_CONF

		TRANS_DSI_FUNC_CONF	
	20	Link Ready	
		Access:	RO
		This bit advertises whether the Link is ready to receive traffic from the DSI transcoder	
		Value	Name
		0	Link is not ready to accept traffic
		1	Link is ready to accept traffic
	19	Reserved	
		Access:	RO
		Format:	MBZ
	18:16	Pixel Format	
	Access:	R/W	
	This field defines the pixel format the DSI Transcoder will be operating in		
	Value	Name	
	000b	16-bit RGB, 5-6-5	
	001b	18-bit RGB, 6-6-6 (Packed)	
	010b	18-bit RGB, 6-6-6 (Loose)	
	011b	24-bit RGB, 8-8-8	
	100b	30-bit RGB, 10-10-10	
	101b	36-bit RGB, 12-12-12	
	110b	Compressed	
	Others	Reserved	
	Restriction		
	When in the 18-bit RGB (Packed) pixel format, the H. Active Size must be a multiple of 4 pixels		
15	BGR Transmission		
	Access:	R/W	
	This field will reverse the order of the RGB channels within the pixels received from the Display Engine		
	Value	Name	
	0	Transmit order is R-G-B	
	1	Transmit order is B-G-R	
14	Reserved		
	Access:	RO	
	Format:	MBZ	
13:12	Pixel Virtual Channel		
	Access:	R/W	
	This field defines the Virtual Channel that HW will bind to all DSI packets carrying pixel data		

TRANS_DSI_FUNC_CONF

11:10	<p>Pixel Buffer Threshold</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>This field defines the threshold of buffering needed within the Pixel Buffer before the transcoder will start internally processing the pixel stream.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>The Pixel Buffer will have to be 1/4 full</td> </tr> <tr> <td>01b</td> <td>The Pixel Buffer will have to be 1/2 full</td> </tr> <tr> <td>10b</td> <td>The Pixel Buffer will have to be 3/4 full</td> </tr> <tr> <td>11b</td> <td>The Pixel Buffer will have to be full</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	00b	The Pixel Buffer will have to be 1/4 full	01b	The Pixel Buffer will have to be 1/2 full	10b	The Pixel Buffer will have to be 3/4 full	11b	The Pixel Buffer will have to be full
Access:	R/W												
Value	Name												
00b	The Pixel Buffer will have to be 1/4 full												
01b	The Pixel Buffer will have to be 1/2 full												
10b	The Pixel Buffer will have to be 3/4 full												
11b	The Pixel Buffer will have to be full												
9:8	<p>Continuous Clock</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>This field will control the behavior of the Clock Lane and whether it is allowed to enter the LP state.</p> <p>Keeping the Clock Lane running while letting the Data Lanes go in and out of the LP state keeps the LP to HS turnaround latency to a minimum, but consumes more power.</p> <p>Certain panels may also require the Clock Lane to continuously run</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Always enter LP after Data Lanes</td> </tr> <tr> <td>10b</td> <td>Opportunistically keep Clock in HS or LP</td> </tr> <tr> <td>11b</td> <td>Continuous HS Clock</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	00b	Always enter LP after Data Lanes	10b	Opportunistically keep Clock in HS or LP	11b	Continuous HS Clock	Others	Reserved
Access:	R/W												
Value	Name												
00b	Always enter LP after Data Lanes												
10b	Opportunistically keep Clock in HS or LP												
11b	Continuous HS Clock												
Others	Reserved												
7	<p>LP Clock during LPM</p> <p>When the Clock Lane is configured for Continuous HS Clock, this bit will control whether the DSI transcoder places the Clock Lane into the LP state along with the Data Lanes when the per frame LP mode (LPM) is performed.</p> <p>This bit has no effect on the Clock Lane for the other Continuous Clock settings.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 20%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disabled</td> <td>Clock Lane does not follow the Data Lanes</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Clock Lane follows the Data Lanes</td> </tr> </tbody> </table>	Value	Name	Description	0b	Disabled	Clock Lane does not follow the Data Lanes	1b	Enable	Clock Lane follows the Data Lanes			
Value	Name	Description											
0b	Disabled	Clock Lane does not follow the Data Lanes											
1b	Enable	Clock Lane follows the Data Lanes											
6	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ								
Access:	RO												
Format:	MBZ												
5:4	<p>Link Calibration</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> </table> <p>This field will control the Link calibration of the DSI Transcoder</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 20%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Calibration Disabled</td> </tr> <tr> <td>10b</td> <td>Calibration Enabled - Initial only</td> </tr> <tr> <td>11b</td> <td>Calibration Enabled - Initial and Periodic</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	00b	Calibration Disabled	10b	Calibration Enabled - Initial only	11b	Calibration Enabled - Initial and Periodic		
Access:	R/W												
Value	Name												
00b	Calibration Disabled												
10b	Calibration Enabled - Initial only												
11b	Calibration Enabled - Initial and Periodic												

TRANS_DSI_FUNC_CONF

	Others	Reserved
	Restriction	
	Calibration can be enabled for any Link frequency, but it must be enabled when the Link frequency is operating above 1.5 Gbps	
3	Reserved	
	Access:	RO
	Format:	MBZ
2	Blanking Packet during BLLP	
	This bit will control whether the transcoder allows the link to enter the LP state during BLLP regions (assuming there is enough time), or whether it will keep the link in the HS state with a Blanking Packet	
	Value	Name
	0b	Disabled
	1b	Enabled
	Description	
	LP allowed in BLLP regions	
	Blanking packets transmitted in BLLP regions	
	Programming Notes	
	<ol style="list-style-type: none"> 1. This bit is only applicable when the transcoder is operating in the Video Mode 2. When this bit is set, then all BLLP regions will be filled with Blanking Packets regardless of where those regions are located (i.e. Vertical active or blank) 3. Regardless of the setting of this bit, if HW determines it cannot allow the link to enter the LP state between HS bursts, then it will automatically fill the region with a Blanking Packet 4. Regardless of the setting of this bit, HW will still ensure the link enters the LP state once per frame per the DSI spec 	
1	S3D Orientation	
	Access:	R/W
	This bit controls the orientation encoding of the 3DMODE field of the Stereoscopic 3D control function sent to a Panel via the Vertical Source Sync (VSS) packet when in Video Mode.	
	Value	Name
	0b	Portrait Orientation
	1b	Landscape Orientation
	Programming Notes	
	<p>This bit will only be sampled by the transcoder when Stereoscopic 3D is enabled for the transcoder</p> <p>This bit should be programmed before enabling Stereoscopic 3D for the transcoder (TRANS_STEREO3D_CTL)</p> <p>If Software changes this bit, it must also perform a write to the TRANS_STEREO3D_CTL for the change to be sent within the next VSS</p>	

TRANS_DSI_FUNC_CONF

TRANS_DSI_FUNC_CONF									
	<p>This bit is only applicable when the transcoder is operating in Video Mode. If the transcoder is operating in Command Mode, then Software will have to communicate the Stereoscopic 3D function information to the Panel through a set_3D_control DCS command using the DCS Long Write DSI packet type.</p>								
0	<p>EoTp Disabled</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>When set, the DSI transcoder will not transmit an End of Transmission packet at the end of High Speed bursts</p> <table border="1" style="width: 100%; text-align: center;"> <thead> <tr style="background-color: #e6f2ff;"> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>EoTp Enabled</td> </tr> <tr> <td>1</td> <td>EoTp Disabled</td> </tr> </tbody> </table>	Access:	R/W	Value	Name	0	EoTp Enabled	1	EoTp Disabled
Access:	R/W								
Value	Name								
0	EoTp Enabled								
1	EoTp Disabled								



TRANS_EXITLINE

TRANS_EXITLINE			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	60018h-6001Bh		
Name:	Transcoder DC3CO Exit Line		
ShortName:	TRANS_EXITLINE_A		
Reset:	soft		
Address:	61018h-6101Bh		
Name:	Transcoder DC3CO Exit Line		
ShortName:	TRANS_EXITLINE_B		
Reset:	soft		
Address:	62018h-6201Bh		
Name:	Transcoder DC3CO Exit Line		
ShortName:	TRANS_EXITLINE_C		
Reset:	soft		
Address:	63018h-6301Bh		
Name:	Transcoder DC3CO Exit Line		
ShortName:	TRANS_EXITLINE_D		
Reset:	soft		
Restriction			
This register should be programmed following the sequence to allow DC3co (i.e., anytime before DC3co is enabled).			
DWord	Bit	Description	
0	31	Enable Exit Line Enable indicates idle frame reset should be applied at exit line	
		Value	Name
		0b	Disable
	1b	Enable	
	30:13	Reserved	
		Access: RO	
		Format: MBZ	

TRANS_EXITLINE

	12:0	Exit Line This field represents the scanline at which DC3CO Exit happens. Example: DC3CO Exit time per calculation is 10 scanlines SW needs to program this field as (VACTIVE - 10).
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TRANS_HBLANK

TRANS_HBLANK		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	60004h-60007h	
Name:	Transcoder Horizontal Blank	
ShortName:	TRANS_HBLANK_A	
Reset:	soft	
Address:	61004h-61007h	
Name:	Transcoder Horizontal Blank	
ShortName:	TRANS_HBLANK_B	
Reset:	soft	
Address:	62004h-62007h	
Name:	Transcoder Horizontal Blank	
ShortName:	TRANS_HBLANK_C	
Reset:	soft	
Address:	63004h-63007h	
Name:	Transcoder Horizontal Blank	
ShortName:	TRANS_HBLANK_D	
Reset:	soft	
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
29:16	Horizontal Blank End	This field specifies Horizontal Blank End position relative to the horizontal active display start.
		Restriction
		The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
15:14	Reserved	
		Access: RO
		Format: MBZ

TRANS_HBLANK			
13:0	<p>Horizontal Blank Start This field specifies the Horizontal Blank Start position relative to the horizontal active display start.</p> <table border="1" style="width: 100%;"><thead><tr><th style="text-align: center;">Restriction</th></tr></thead><tbody><tr><td>This register must always be programmed to the same value as the Horizontal Active.</td></tr></tbody></table>	Restriction	This register must always be programmed to the same value as the Horizontal Active.
Restriction			
This register must always be programmed to the same value as the Horizontal Active.			



TRANS_HSYNC

TRANS_HSYNC		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	6B008h-6B00Bh	
Name:	Transcoder DSI 0 Horizontal Sync	
ShortName:	TRANS_HSYNC_DSI0	
Reset:	soft	
Address:	6B808h-6B80Bh	
Name:	Transcoder DSI 1 Horizontal Sync	
ShortName:	TRANS_HSYNC_DSI1	
Reset:	soft	
Address:	60008h-6000Bh	
Name:	Transcoder Horizontal Sync	
ShortName:	TRANS_HSYNC_A	
Reset:	soft	
Address:	61008h-6100Bh	
Name:	Transcoder Horizontal Sync	
ShortName:	TRANS_HSYNC_B	
Reset:	soft	
Address:	62008h-6200Bh	
Name:	Transcoder Horizontal Sync	
ShortName:	TRANS_HSYNC_C	
Reset:	soft	
Address:	63008h-6300Bh	
Name:	Transcoder Horizontal Sync	
ShortName:	TRANS_HSYNC_D	
Reset:	soft	
Restriction		
<p>This register should not be changed while the transcoder or port are enabled. HSYNC is always programmed to an even number of pixel clock cycles for YUV 4:2:0 pixel format with 10bpc and 12bpc.. HSYNC timings must be even for HDMI operating on 10bpc (regardless of format)</p>		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO

TRANS_HSYNC					
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>MBZ</td> </tr> </table>	Format:	MBZ		
Format:	MBZ				
29:16	<p>Horizontal Sync End This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with $\text{HorizontalActive} + \text{FrontPorch} + \text{Sync} - 1$</p> <p style="text-align: center;">Restriction</p> <p>This value must be greater than the horizontal sync start and less than Horizontal Total.</p> <p>For the DSI transcoder this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). As such, please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed</p>				
15:14	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
13:0	<p>Horizontal Sync Start This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with $\text{HorizontalActive} + \text{FrontPorch} - 1$</p> <p style="text-align: center;">Restriction</p> <p>This value must be greater than Horizontal Active for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode. For DSI transcoders operating on a compressed pixel stream in Video Mode, this value should be greater than the Horizontal Active size divided by the Compression Ratio ($\text{H. Blank Start} = \text{H. Active} / \text{Compression Ratio}$).</p> <p>In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16 pixels.</p> <p>For DSI transcoders, this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). When the DSI transcoder is in Video Mode, then please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed.</p>				



TRANS_HTOTAL

TRANS_HTOTAL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E000h-6E003h
Name:	Transcoder WD0 Horizontal Total
ShortName:	TRANS_HTOTAL_WD0
Reset:	soft
Address:	6E800h-6E803h
Name:	Transcoder WD1 Horizontal Total
ShortName:	TRANS_HTOTAL_WD1
Reset:	soft
Address:	6B000h-6B003h
Name:	Transcoder DSI 0 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI0
Reset:	soft
Address:	6B800h-6B803h
Name:	Transcoder DSI 1 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI1
Reset:	soft
Address:	60000h-60003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_A
Reset:	soft
Address:	61000h-61003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_B
Reset:	soft
Address:	62000h-62003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_C
Reset:	soft
Address:	63000h-63003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_D

TRANS_HTOTAL						
Reset:	soft					
Programming Notes						
For eDP CoG: $H_{total_{CoG}} = (\text{active pixels per segment}) + (\text{overlap pixels} * \text{number of segments}/2) + \text{Original Horizontal Blanking}$						
Restriction						
This register should not be changed while the transcoder or port are enabled.						
The following restriction applies only to HDMI 4:2:0. All horizontal timings should be a multiple of 4 for 8/12/16 bpc cases and multiple of 8 for 10 bpc case. This applies to full blend and bypass modes.						
All horizontal timings must be even for HDMI operating on 10bpc (regardless of format)						
DWord	Bit	Description				
0	31:30	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
29:16	Horizontal Total					
	<p>This field specifies Horizontal Total size. This field is programmed to the number of pixels desired minus one.</p> <p>This should be equal to the sum of the horizontal active and the horizontal blank sizes for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode.</p> <p>For DSI transcoders operating with compressed pixels in Video Mode, this field should be equal to the sum of the compressed horizontal active size and the horizontal blank size (H. Total = (H. Active + H. Blank size) / Compression Ratio)</p> <p>For DSI transcoders operating in Command Mode, there are no restrictions on the programming of this field.</p> <p>This field is ignored by WD transcoders.</p>					
		<table border="1"> <tr> <th colspan="2">Restriction</th> </tr> <tr> <td colspan="2">This register must always be programmed to the same value as the Horizontal Blank End.</td> </tr> </table>	Restriction		This register must always be programmed to the same value as the Horizontal Blank End.	
Restriction						
This register must always be programmed to the same value as the Horizontal Blank End.						
15:14		Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					

TRANS_HTOTAL				
13:0	<p>Horizontal Active This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #e6f2ff;">Restriction</th> </tr> </thead> <tbody> <tr> <td> <p>The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.</p> </td> </tr> <tr> <td> <p>DSI requires a minimum Horizontal Active Display of, 256 pixels. Also, when transmitting an 18-bit RGB pixel format, the one-based size must be a multiple of 4 pixels</p> </td> </tr> </tbody> </table>	Restriction	<p>The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.</p>	<p>DSI requires a minimum Horizontal Active Display of, 256 pixels. Also, when transmitting an 18-bit RGB pixel format, the one-based size must be a multiple of 4 pixels</p>
Restriction				
<p>The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.</p>				
<p>DSI requires a minimum Horizontal Active Display of, 256 pixels. Also, when transmitting an 18-bit RGB pixel format, the one-based size must be a multiple of 4 pixels</p>				

TRANS_MSA_MISC

TRANS_MSA_MISC						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	60410h-60413h					
Name:	Transcoder MSA Misc					
ShortName:	TRANS_MSA_MISC_A					
Reset:	soft					
Address:	61410h-61413h					
Name:	Transcoder MSA Misc					
ShortName:	TRANS_MSA_MISC_B					
Reset:	soft					
Address:	62410h-62413h					
Name:	Transcoder MSA Misc					
ShortName:	TRANS_MSA_MISC_C					
Reset:	soft					
Address:	63410h-63413h					
Name:	Transcoder MSA Misc					
ShortName:	TRANS_MSA_MISC_D					
Reset:	soft					
<p>This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.</p>						
Programming Notes						
See the DisplayPort specification for the details on what to program in these fields.						
DWord	Bit	Description				
0	31:16	<p>MSA Unused</p> <p>This field selects the value that will be sent in the DisplayPort MSA unused fields.</p> <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> </thead> <tbody> <tr> <td colspan="2">This should be usually programmed with all 0s.</td> </tr> </tbody> </table>	Programming Notes		This should be usually programmed with all 0s.	
	Programming Notes					
This should be usually programmed with all 0s.						
15:8	<p>MSA MISC1</p> <p>This field selects the value that will be sent in the DisplayPort MSA MISC1 field. When TRANS_STEREO3D_CTL bit FS_MSA_MISC1_Drive_En is enabled, hardware will drive MISC1 bits 2:1 (bits 10:9 of this register) with the field sequential stereo 3D left or right eye indication, and any value written to those bits here will be ignored.</p>					

TRANS_MSA_MISC			
7:0	<p>MSA_MISC0 This field selects the value that will be sent in the DisplayPort MSA_MISC0 field.</p> <table border="1" style="width: 100%;"> <tr> <td style="text-align: center;">Restriction</td> </tr> <tr> <td>Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.</td> </tr> </table>	Restriction	Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.
Restriction			
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TRANS_MULT

TRANS_MULT																	
Register Space:	MMIO: 0/2/0																
Access:	R/W																
Size (in bits):	32																
Address:	6002Ch-6002Fh																
Name:	Transcoder Multiply																
ShortName:	TRANS_MULT_A																
Reset:	soft																
Address:	6102Ch-6102Fh																
Name:	Transcoder Multiply																
ShortName:	TRANS_MULT_B																
Reset:	soft																
Address:	6202Ch-6202Fh																
Name:	Transcoder Multiply																
ShortName:	TRANS_MULT_C																
Reset:	soft																
Address:	6302Ch-6302Fh																
Name:	Transcoder Multiply																
ShortName:	TRANS_MULT_D																
Reset:	soft																
Restriction																	
This register should not be changed while the transcoder or port are enabled.																	
DWord	Bit	Description															
0	31:3	Reserved															
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ											
Access:	RO																
Format:	MBZ																
	2:0	Multiplier															
		This field specifies the data multiplier value used by HDMI and DVI.															
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>X1</td> <td>Multiply by 1</td> </tr> <tr> <td>001b</td> <td>X2</td> <td>Multiply by 2</td> </tr> <tr> <td>011b</td> <td>X4</td> <td>Multiply by 4</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Name	Description	000b	X1	Multiply by 1	001b	X2	Multiply by 2	011b	X4	Multiply by 4	Others	Reserved	Reserved
		Value	Name	Description													
		000b	X1	Multiply by 1													
		001b	X2	Multiply by 2													
011b	X4	Multiply by 4															
Others	Reserved	Reserved															



TRANS_PUSH

TRANS_PUSH			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	60A70h-60A73h		
Name:	Transcoder ASFU VRR Push		
ShortName:	TRANS_PUSH_A		
Reset:	soft		
Address:	61A70h-61A73h		
Name:	Transcoder ASFU VRR Push		
ShortName:	TRANS_PUSH_B		
Reset:	soft		
Address:	62A70h-62A73h		
Name:	Transcoder ASFU VRR Push		
ShortName:	TRANS_PUSH_C		
Reset:	soft		
Address:	63A70h-63A73h		
Name:	Transcoder ASFU VRR Push		
ShortName:	TRANS_PUSH_D		
Reset:	soft		
<p>After programming any pipe registers in ASFU/VRR cases, Software can set push bit. H/W will sync all those updates for that frame.</p>			
DWord	Bit	Description	
0	31	Push Enable This bit enables Push frame functionality. This bit should be set before ASFU/VRR enable.	
		Value	Name
		0b	Disable
		1b	Enable
29:0	30	Send Push Access: R/W Set Writing a 1b to this field hints that Frame update is desired. Vblank is asserted at the next decision boundary. This is a sticky bit. The bit will be cleared by hardware after double buffer update. Writing a 0b has no effect.	
		Reserved Access: RO	
		Format: MBZ	

TRANS_SPACE

TRANS_SPACE			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	6B024h-6B027h		
Name:	Transcoder DSI 0 Space		
ShortName:	TRANS_SPACE_DSI0		
Reset:	soft		
Address:	6B824h-6B827h		
Name:	Transcoder DSI 1 Space		
ShortName:	TRANS_SPACE_DSI1		
Reset:	soft		
Address:	60024h-60027h		
Name:	Transcoder Space		
ShortName:	TRANS_SPACE_A		
Reset:	soft		
Address:	61024h-61027h		
Name:	Transcoder Space		
ShortName:	TRANS_SPACE_B		
Reset:	soft		
Address:	62024h-62027h		
Name:	Transcoder Space		
ShortName:	TRANS_SPACE_C		
Reset:	soft		
Address:	63024h-63027h		
Name:	Transcoder Space		
ShortName:	TRANS_SPACE_D		
Reset:	soft		
Restriction			
This register should not be changed while the transcoder or port are enabled.			
DWord	Bit	Description	
0	31:12	Reserved	
		Access:	RO
		Format:	MBZ

TRANS_SPACE			
11:0	<p>Vertical Active Space</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center; color: #0070C0;">Description</th> </tr> </thead> <tbody> <tr> <td> <p>This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.</p> </td> </tr> </tbody> </table>	Description	<p>This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.</p>
Description			
<p>This field specifies Stereo 3D Vertical Active space. This determines the number of constant pixel value lines inserted between the left and right eye active video regions in the stereo 3D stacked frame mode. This field will only be used when the transcoder is in the stereo 3D stacked frame mode. This field should usually be programmed to be the same as the width of the vertical blank.</p>			

TRANS_STEREO3D_CTL

TRANS_STEREO3D_CTL				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	7B020h-7B023h			
Name:	Transcoder DSI 0 Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_DSI0			
Reset:	soft			
Address:	7B820h-7B823h			
Name:	Transcoder DSI 1 Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_DSI1			
Reset:	soft			
Address:	70020h-70023h			
Name:	Transcoder Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_A			
Reset:	soft			
Address:	71020h-71023h			
Name:	Transcoder Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_B			
Reset:	soft			
Address:	72020h-72023h			
Name:	Transcoder Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_C			
Reset:	soft			
Address:	73020h-73023h			
Name:	Transcoder Stereo 3D Control			
ShortName:	TRANS_STEREO3D_CTL_D			
Reset:	soft			
This register is sampled one line before vertical blank.				
DWord	Bit	Description		
0	31	Transcoder S3D Enable <table border="1"> <thead> <tr> <th>Description</th> </tr> </thead> <tbody> <tr> <td>This bit enables the stereo 3D modes on this transcoder. Updates will take place at the start of the next vertical blank.</td> </tr> </tbody> </table>	Description	This bit enables the stereo 3D modes on this transcoder. Updates will take place at the start of the next vertical blank.
Description				
This bit enables the stereo 3D modes on this transcoder. Updates will take place at the start of the next vertical blank.				

TRANS_STEREO3D_CTL

		Value	Name
		0b	Disable
		1b	Enable
Restriction			
<p>These modes are only for use with DisplayPort, HDMI, and DVI. HDMI/DVI: Stereo 3D can only be enabled with a mode set. It must be enabled before transcoder and port are enabled. It must be disabled after transcoder is disabled. DisplayPort: Stereo 3D can be enabled and disabled with a mode set, like HDMI and DVI, or it can be enabled after an enable mode set is complete and disabled prior to a disable mode set. VGA display modes, interlaced modes, SRD/PSR, WD, and frame buffer compression (FBC) do not work with stereo 3D. The left surface base address registers for the planes going to this transcoder must be programmed with valid addresses prior to enabling stereo 3D.</p>			
30:29	Reserved		
	Access:	RO	
	Format:	MBZ	
28:27	S3D Mode		
<p>This field selects between the stereo 3D modes.</p> <p>The stacked buffer mode combines both stereo 3D fields (left and right eye images) into a single tall frame with the left eye image on top, then a programmable space of black lines, then the right eye image on the bottom.</p> <p>The field sequential mode sends one stereo 3D field (left or right eye image) out per frame. This mode is only for use with DisplayPort. Field sequential hardware controlled mode automatically toggles between left and right eye at the start of each vertical blank. The starting field is selected using the FS_Field_Ctl register bit. Field sequential software controlled mode will manually select left or right eye using the FS_Field_Ctl register bit.</p>			
	Value	Name	Description
	00b	FS HW Auto	Hardware controlled auto-toggle between left and right eye on each vertical blank.
	01b	FS SW Manual	Software controlled selection between left and right eye
	10b	Stacked	Stacked frame mode with both left and right eye images combined in a single tall frame
	Others	Reserved	Reserved
Programming Notes			
<p>In the stacked frame mode, a vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame.</p>			
Restriction			
<p>This field should only be changed when stereo 3D is disabled.</p>			

TRANS_STEREO3D_CTL

26	FS Field Ctl	<p>The operation of this bit depends on the S3D Mode setting. This field is ignored in the S3D stacked mode. In the field sequential software controlled mode this bit selects the field sequential stereo 3D field (left or right eye). In the field sequential hardware controlled mode this bit selects the field sequential stereo 3D starting field, the field used on the frame when field sequential stereo 3D is enabled. Hardware does not wait for a specific eye when disabling.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Right Eye</td> </tr> <tr> <td>1b</td> <td>Left Eye [Default]</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">The starting field must be set to the left eye for FS HW Auto usage.</td> </tr> </tbody> </table>	Value	Name	0b	Right Eye	1b	Left Eye [Default]	Restriction	The starting field must be set to the left eye for FS HW Auto usage.			
Value	Name												
0b	Right Eye												
1b	Left Eye [Default]												
Restriction													
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25	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ							
Access:	RO												
Format:	MBZ												
24	S3D Current Field	<table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> </table> <p>This read only bit indicates the current stereo 3D field (left or right eye). This bit should be ignored when stereo 3D is not enabled.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Right Eye</td> </tr> <tr> <td>1b</td> <td>Left Eye</td> </tr> </tbody> </table>	Access:	RO	Value	Name	0b	Right Eye	1b	Left Eye			
Access:	RO												
Value	Name												
0b	Right Eye												
1b	Left Eye												
23	FS MSA MISC1 Drive En	<p>This bit enables hardware to drive the MSA MISC1 bits 2:1 with the internal field sequential stereo 3D left/right eye field indication. Hardware will drive 00 when field sequential 3D stereo mode is not enabled, 01 when enabled and the upcoming video frame is the right eye, 11 when enabled and the upcoming video frame is the left eye. This is based on the internal left/right indication which could be either generated by hardware in the HW auto mode or by software in the SW manual mode. FS_MSA_Drive_Invert can be programmed to invert the left and right eye selection in the MSA. When this bit is disabled, software may manually program TRANS_MSA_MISC to set MISC1 bits 2:1.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 10%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> <td>Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.</td> </tr> <tr> <td>1b</td> <td>Enable</td> <td>Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Disable	Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.	1b	Enable	Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.	Restriction	This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.
Value	Name	Description											
0b	Disable	Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.											
1b	Enable	Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.											
Restriction													
This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.													
22	Reserved												

TRANS_STEREO3D_CTL			
	21:0	Reserved	
		Access:	RO
		Format:	MBZ

TRANS_VBLANK

TRANS_VBLANK	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B010h-6B013h
Name:	Transcoder DSI 0 Vertical Blank
ShortName:	TRANS_VBLANK_DSI0
Reset:	soft
Address:	6B810h-6B813h
Name:	Transcoder DSI 1 Vertical Blank
ShortName:	TRANS_VBLANK_DSI1
Reset:	soft
Address:	60010h-60013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_A
Reset:	soft
Address:	61010h-61013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_B
Reset:	soft
Address:	62010h-62013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_C
Reset:	soft
Address:	63010h-63013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_D
Reset:	soft
Description	
<p>PSR ASU: This register is double buffered when Vactive double buffer bit (bit[8]) is asserted in TRANS_DDI_FUNC_CTL2.</p> <p>The transcoder will generate two Vertical Blanks to the Display Engine. A raw (or unmodified) V. Blank will be generated based off of the vertical timings defined within the TRANS_VTOTAL register (the raw V. Blank will assert after V.Active and de-asserted after V. Total). A delayed V. Blank will be generated from the vertical timings of this register. The delay is in terms of lines, and if this register is programmed with the same value as the TRANS_VTOTAL register (i.e. V. Blank Start = V. Active), then the delay will be zero.</p>	

TRANS_VBLANK					
Programming Notes					
This register is programmed in terms of lines and the values programmed should be zero-based (e.g. for the vertical blank to start on line 10, the Vertical Blank Start will be programmed to 9)					
Restriction					
This register should not be changed while the transcoder or port are enabled.					
DWord	Bit	Description			
0	31:29	Reserved			
		Access: RO			
		Format: MBZ			
	28:16	Vertical Blank End This field specifies Vertical Blank End position relative to the vertical active display start. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td>1. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines</td> </tr> <tr> <td>2. The V. Blank End must be programmed to the same value as V. Total in the TRANS_VTOTAL register</td> </tr> <tr> <td>3. The V. Blank End must be greater than the V. Blank Start</td> </tr> </tbody> </table>	Restriction	1. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines	2. The V. Blank End must be programmed to the same value as V. Total in the TRANS_VTOTAL register
Restriction					
1. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines					
2. The V. Blank End must be programmed to the same value as V. Total in the TRANS_VTOTAL register					
3. The V. Blank End must be greater than the V. Blank Start					
15:13	Reserved				
	Access: RO				
	Format: MBZ				
12:0	Vertical Blank Start This field specifies the Vertical Blank Start position relative to the vertical active display start. <table border="1" style="width: 100%; margin-top: 5px;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td>The V. Blank Start must be greater than or equal to the Vertical Active programming in TRANS_VTOTAL</td> </tr> </tbody> </table>	Restriction	The V. Blank Start must be greater than or equal to the Vertical Active programming in TRANS_VTOTAL		
	Restriction				
The V. Blank Start must be greater than or equal to the Vertical Active programming in TRANS_VTOTAL					

TRANS_VRR_CTL

TRANS_VRR_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	60420h-60423h							
Name:	VRR Control Register Transcoder							
ShortName:	TRANS_VRR_CTL_A							
Reset:	soft							
Address:	61420h-61423h							
Name:	VRR Control Register Transcoder							
ShortName:	TRANS_VRR_CTL_B							
Reset:	soft							
Address:	62420h-62423h							
Name:	VRR Control Register Transcoder							
ShortName:	TRANS_VRR_CTL_C							
Reset:	soft							
Address:	63420h-63423h							
Name:	VRR Control Register Transcoder							
ShortName:	TRANS_VRR_CTL_D							
Reset:	soft							
DWord	Bit	Description						
0	31	VRR Enable This bit enables/disables VRR feature on the fly, no mode set required.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	Ignore Max Shift This bit when set to '1' will ignore programmed Vblank max shift values (both INC and DEC), allowing Vblank to freely swing between Vmin and Vmax.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>IGNORE</td> </tr> <tr> <td>0b</td> <td>DO NOT IGNORE</td> </tr> </tbody> </table>	Value	Name	1b	IGNORE	0b	DO NOT IGNORE
		Value	Name					
	1b	IGNORE						
	0b	DO NOT IGNORE						
29	Flip Line Enable							
		<table border="1"> <thead> <tr> <th>Description</th> </tr> </thead> <tbody> <tr> <td>This bit enables/disables Flip Line feature where frame start will be generated at flip line value for VRR. Updates to this field will take effect at the next vertical blank. This field must be</td> </tr> </tbody> </table>	Description	This bit enables/disables Flip Line feature where frame start will be generated at flip line value for VRR. Updates to this field will take effect at the next vertical blank. This field must be				
Description								
This bit enables/disables Flip Line feature where frame start will be generated at flip line value for VRR. Updates to this field will take effect at the next vertical blank. This field must be								

TRANS_VRR_CTL

		enabled before VRR enable.	
		Ignore Max Shift must be set to 1 when Flip Line is enabled	
		Value	Name
		0b	Disable
		1b	Enable
28:16	Reserved		
	Access:	RO	
	Format:	MBZ	
15:11	Reserved		
	Access:	RO	
	Format:	MBZ	
10:3	FrameStart to Pipeline Full LineCount		
	Default Value:	20h	
	This 8-bit line count allows a maximum of 255 scanlines (programming 255 gives 255 scanlines duration to fill the pipeline etc.).		
	Restriction		
	Always program this field to (Transcoder VRR Vmin - Transcoder Vertical Blank Start - 4) where VRR Vmin and Transcoder Vertical Blank Start are '0' based.		
2:1	Reserved		
	Access:	RO	
	Format:	MBZ	
0	Pipeline Full Override		
	This bit tells whether to depend on HW generated signal to start Vactive or to depend on the programmed Pipeline full line count.		
	Setting this bit assumes pipeline full line count is already programmed.		
	Value	Name	
	0b	HW generated Pipeline Full Line Count	
	1b	Programmed Pipeline Full Line Count	
	Restriction		
	SW programmed pipeline full line count must be used when flip line is enabled. This will ensure that Vblank always ends at the same point.		

TRANS_VRR_FLIPLINE

TRANS_VRR_FLIPLINE		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	60438h-6043Bh	
Name:	VRR Flipline Trans	
ShortName:	TRANS_VRR_FLIPLINE_A	
Reset:	soft	
Address:	61438h-6143Bh	
Name:	VRR Flipline Trans	
ShortName:	TRANS_VRR_FLIPLINE_B	
Reset:	soft	
Address:	62438h-6243Bh	
Name:	VRR Flipline Trans	
ShortName:	TRANS_VRR_FLIPLINE_C	
Reset:	soft	
Address:	63438h-6343Bh	
Name:	VRR Flipline Trans	
ShortName:	TRANS_VRR_FLIPLINE_D	
Reset:	soft	
This register defines vertical total size to execute a flip for VRR.		
DWord	Bit	Description
0	31:20	Reserved
		Access: RO
	Format: MBZ	
	19:0	VRR FLIPLINE This field provides the vertical total size to execute flip for VRR. This is 0-based. So, value should be programmed as N-1.



TRANS_VRR_STATUS

TRANS_VRR_STATUS										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	6042Ch-6042Fh									
Name:	VRR Status Trans									
ShortName:	TRANS_VRR_STATUS_A									
Reset:	soft									
Address:	6142Ch-6142Fh									
Name:	VRR Status Trans									
ShortName:	TRANS_VRR_STATUS_B									
Reset:	soft									
Address:	6242Ch-6242Fh									
Name:	VRR Status Trans									
ShortName:	TRANS_VRR_STATUS_C									
Reset:	soft									
Address:	6342Ch-6342Fh									
Name:	VRR Status Trans									
ShortName:	TRANS_VRR_STATUS_D									
Reset:	soft									
This register provides VRR status and some additional information										
DWord	Bit	Description								
0	31	<p>Vmax Reached</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>Sticky bit is set indicating no flip has occurred when Vmax is reached. This bit needs to be polled and cleared by software. Setting of this sticky bit will not result in any interrupt.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Reached</td> </tr> <tr> <td>1b</td> <td>Reached</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	Not Reached	1b	Reached
	Access:	R/WC								
Value	Name									
0b	Not Reached									
1b	Reached									
30	<p>No flip till decision boundary</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This bit is asserted whenever frame decision boundary is reached without a flip.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td></td> </tr> <tr> <td>1b</td> <td></td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b		1b		
Access:	R/WC									
Value	Name									
0b										
1b										

TRANS_VRR_STATUS

	29	Flip before decision boundary	
	Access:		R/WC
	This bit is asserted whenever frame decision boundary is reached with a flip.		
		Value	Name
		0b	
		1b	
	28	No flip frame	
	Access:		R/WC
	This bit is asserted whenever current frame terminates without a flip.		
		Value	Name
		0b	
		1b	
	27	VRR Enable Live	
	Access:		RO
	This bit is asserted whenever pipe/plane logic is running with VRR enabled.		
		Value	Name
		0b	
		1b	
	26	flips serviced	
	Access:		R/WC
This bit represents acknowledgement from pipe to transcoder indicating that processing for all flips in the current frame is complete and any subsequent flips will be handled in the next frame.			
	Value	Name	
	0b		
	1b		
25:23	Reserved		
Access:		RO	
Format:		MBZ	
22:20	Current Region in Vblank		
Access:		RO	
This field indicates current status of VRR FSM.			
	Value	Name	Description
	000b	IDLE	Timing generator disabled.
	001b	WAIT_TILL_FDB	Wait till the flip decision boundary
	010b	WAIT_TILL_FRAMESTART	After the decision boundary, wait for framestart
	011b	WAIT_TILL_FLIP	Transition to this state when past the decision boundary, but no primary flip

TRANS_VRR_STATUS				
		100b	PIPELINE_FILL	State after framestart, waiting for a fixed num of lines
		101b	ACTIVE	
		110b	LEGACY_VBLANK	No VRR
	19:0	Reserved		
		Access:		RO
		Format:		MBZ

TRANS_VRR_STATUS2

TRANS_VRR_STATUS2				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	6043Ch-6043Fh			
Name:	VRR Status2 Trans			
ShortName:	TRANS_VRR_STATUS2_A			
Reset:	soft			
Address:	6143Ch-6143Fh			
Name:	VRR Status2 Trans			
ShortName:	TRANS_VRR_STATUS2_B			
Reset:	soft			
Address:	6243Ch-6243Fh			
Name:	VRR Status2 Trans			
ShortName:	TRANS_VRR_STATUS2_C			
Reset:	soft			
Address:	6343Ch-6343Fh			
Name:	VRR Status2 Trans			
ShortName:	TRANS_VRR_STATUS2_D			
Reset:	soft			
This register provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.				
DWord	Bit	Description		
0	31:20	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
	19:0	Vertical Line Counter Status		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.</p>	Access:	RO
Access:	RO			



TRANS_VRR_VMAX

TRANS_VRR_VMAX				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	60424h-60427h			
Name:	VRR Vmax Transcoder			
ShortName:	TRANS_VRR_VMAX_A			
Reset:	soft			
Address:	61424h-61427h			
Name:	VRR Vmax Transcoder			
ShortName:	TRANS_VRR_VMAX_B			
Reset:	soft			
Address:	62424h-62427h			
Name:	VRR Vmax Transcoder			
ShortName:	TRANS_VRR_VMAX_C			
Reset:	soft			
Address:	63424h-63427h			
Name:	VRR Vmax Transcoder			
ShortName:	TRANS_VRR_VMAX_D			
Reset:	soft			
Programming Notes				
This register is not double buffered and the changed values are reflected immediately in VRR logic. This register should not be updated while VRR mode is running.				
DWord	Bit	Description		
0	31:20	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
	19:0	VRR Vmax This field provides the maximum vertical total size for VRR. This is a 0-based counter (that is, counted 0 to N-1). This field cannot be zero when VRR is enabled. $Vmax = \text{ROUNDDOWN}(\text{Dot clock} / (\text{Htotal} * \text{Min Refresh rate}))$		

TRANS_VRR_VMAXSHIFT

TRANS_VRR_VMAXSHIFT			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	60428h-6042Bh		
Name:	VRR Vmaxshift Trans		
ShortName:	TRANS_VRR_VMAXSHIFT_A		
Reset:	soft		
Address:	61428h-6142Bh		
Name:	VRR Vmaxshift Trans		
ShortName:	TRANS_VRR_VMAXSHIFT_B		
Reset:	soft		
Address:	62428h-6242Bh		
Name:	VRR Vmaxshift Trans		
ShortName:	TRANS_VRR_VMAXSHIFT_C		
Reset:	soft		
Address:	63428h-6342Bh		
Name:	VRR Vmaxshift Trans		
ShortName:	TRANS_VRR_VMAXSHIFT_D		
Reset:	soft		
This register defines VBLANK maximum shift allowed between successive frames.			
Programming Notes			
This register is not double buffered and the changed values are reflected immediately in VRR logic. This register should not be updated while VRR mode is running.			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
	29:16	Decrement This register represents the maximum reduction.Smallest Vblank = Previous Frame Vblank End - Vblank Max Shift Decrement.	
	15:14	Reserved	
		Access:	RO
Format:		MBZ	

TRANS_VRR_VMAXSHIFT

	13:0	Increment This register represents the maximum increase. Largest Vblank = Previous Frame Vblank End + Vblank Max Shift Increment.
--	------	---

TRANS_VRR_VMIN

TRANS_VRR_VMIN				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	60434h-60437h			
Name:	VRR Vmin Transcoder			
ShortName:	TRANS_VRR_VMIN_A			
Reset:	soft			
Address:	61434h-61437h			
Name:	VRR Vmin Transcoder			
ShortName:	TRANS_VRR_VMIN_B			
Reset:	soft			
Address:	62434h-62437h			
Name:	VRR Vmin Transcoder			
ShortName:	TRANS_VRR_VMIN_C			
Reset:	soft			
Address:	63434h-63437h			
Name:	VRR Vmin Transcoder			
ShortName:	TRANS_VRR_VMIN_D			
Reset:	soft			
Programming Notes				
<p>This register is not double buffered and the changed values are reflected immediately in VRR logic. This register should not be updated while VRR mode is running.</p>				
DWord	Bit	Description		
0	31:16	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
15:0	15:0	VRR Vmin		
		<table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> </table> <p>This field provides the minimum vertical total size for VRR. This is a 0-based counter (that is, counted 0 to N-1). This field cannot be zero when VRR is enabled. Vmin = ROUNDUP(Dot clock / (Htotal * Max Refresh rate))</p>	Access:	R/W
Access:	R/W			



TRANS_VRR_VTOTAL_PREV

TRANS_VRR_VTOTAL_PREV				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
Address:	60480h-60483h			
Name:	VRR Vtotal Previous Transcoder			
ShortName:	TRANS_VRR_VTOTAL_PREV_A			
Reset:	soft			
Address:	61480h-61483h			
Name:	VRR Vtotal Previous Transcoder			
ShortName:	TRANS_VRR_VTOTAL_PREV_B			
Reset:	soft			
Address:	62480h-62483h			
Name:	VRR Vtotal Previous Transcoder			
ShortName:	TRANS_VRR_VTOTAL_PREV_C			
Reset:	soft			
Address:	63480h-63483h			
Name:	VRR Vtotal Previous Transcoder			
ShortName:	TRANS_VRR_VTOTAL_PREV_D			
Reset:	soft			
<p>This register holds the Vtotal from previous frame and other VRR status bits. If VRR is not enabled, this register will hold software programmed Vtotal.</p>				
DWord	Bit	Description		
0	31	<p>Flip Before Boundary</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>This bit indicates that a push has occurred in either Active region or in Vblank before Flip Decision Boundary and will result in a Vblank which is Previous_Frame_Vblank - Vblank_Max_Shift_Dec.</p>	Access:	RO
	Access:	RO		
	30	<p>Flip After Boundary</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>This bit indicates that the first push has occurred after Flip Decision Boundary and will result in a Vblank which is between (Previous_Frame_Vblank - Vblank_Max_Shift_Dec) and (Previous_Frame_Vblank + Vblank_Max_Shift_Inc).</p>	Access:	RO
Access:	RO			
29	<p>Flip After Double Buffer</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">RO</td> </tr> </table> <p>This bit indicates that the first push has occurred after the Double buffer update and will result in a Vblank which is (Previous_Frame_Vblank + Vblank_Max_Shift_Inc). This however will cause</p>	Access:	RO	
Access:	RO			

TRANS_VRR_VTOTAL_PREV	
	the next frame Vblank to be (Previous_Frame_Vblank - Vblank_Max_Shift_Dec).
28:20	Reserved
	Access: RO
	Format: MBZ
19:0	Vtotal Previous
	Access: RO
	Vtotal from previous frame.



TRANS_VSYNC

TRANS_VSYNC		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	6B014h-6B017h	
Name:	Transcoder DSI 0 Vertical Sync	
ShortName:	TRANS_VSYNC_DSI0	
Reset:	soft	
Address:	6B814h-6B817h	
Name:	Transcoder DSI 1 Vertical Sync	
ShortName:	TRANS_VSYNC_DSI1	
Reset:	soft	
Address:	60014h-60017h	
Name:	Transcoder Vertical Sync	
ShortName:	TRANS_VSYNC_A	
Reset:	soft	
Address:	61014h-61017h	
Name:	Transcoder Vertical Sync	
ShortName:	TRANS_VSYNC_B	
Reset:	soft	
Address:	62014h-62017h	
Name:	Transcoder Vertical Sync	
ShortName:	TRANS_VSYNC_C	
Reset:	soft	
Address:	63014h-63017h	
Name:	Transcoder Vertical Sync	
ShortName:	TRANS_VSYNC_D	
Reset:	soft	
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:29	Reserved
		Access: RO
		Format: MBZ

TRANS_VSYNC					
28:16	<p>Vertical Sync End This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Restriction</td> </tr> <tr> <td>This value must be greater than the vertical sync start and less than Vertical Total.</td> </tr> </table>	Restriction	This value must be greater than the vertical sync start and less than Vertical Total.		
Restriction					
This value must be greater than the vertical sync start and less than Vertical Total.					
15:13	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
12:0	<p>Vertical Sync Start This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Restriction</td> </tr> <tr> <td>This value must be greater than Vertical Active.</td> </tr> </table>	Restriction	This value must be greater than Vertical Active.		
Restriction					
This value must be greater than Vertical Active.					



TRANS_VSYNCSHIFT

TRANS_VSYNCSHIFT		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	6B028h-6B02Bh	
Name:	Transcoder DSI 0 Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_DSI0	
Reset:	soft	
Address:	6B828h-6B82Bh	
Name:	Transcoder DSI 1 Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_DSI1	
Reset:	soft	
Address:	60028h-6002Bh	
Name:	Transcoder Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_A	
Reset:	soft	
Address:	61028h-6102Bh	
Name:	Transcoder Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_B	
Reset:	soft	
Address:	62028h-6202Bh	
Name:	Transcoder Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_C	
Reset:	soft	
Address:	63028h-6302Bh	
Name:	Transcoder Vertical Sync Shift	
ShortName:	TRANS_VSYNCSHIFT_D	
Reset:	soft	
Restriction		
This register should not be changed while the transcoder or port are enabled.		
DWord	Bit	Description
0	31:13	Reserved
		Access: RO
		Format: MBZ

TRANS_VSYNCSHIFT

	12:0	Second Field VSync Shift This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2]Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.
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TRANS_VTOTAL

TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E00Ch-6E00Fh
Name:	Transcoder WD0 Vertical Total
ShortName:	TRANS_VTOTAL_WD0
Reset:	soft
Address:	6E80Ch-6E80Fh
Name:	Transcoder WD1 Vertical Total
ShortName:	TRANS_VTOTAL_WD1
Reset:	soft
Address:	6B00Ch-6B00Fh
Name:	Transcoder DSI 0 Vertical Total
ShortName:	TRANS_VTOTAL_DSI0
Reset:	soft
Address:	6B80Ch-6B80Fh
Name:	Transcoder DSI 1 Vertical Total
ShortName:	TRANS_VTOTAL_DSI1
Reset:	soft
Address:	6000Ch-6000Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_A
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_B
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_C
Reset:	soft
Address:	6300Ch-6300Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_D

TRANS_VTOTAL					
Reset:	soft				
Programming Notes					
PSR ASU: This register is double buffered when Vactive double buffer bit (bit[8]) is asserted in TRANS_DDI_FUNC_CTL2.					
Restriction					
This register should not be changed while the transcoder or port are enabled.					
DWord	Bit	Description			
0	31:29	Reserved			
		<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
	Format:	MBZ			
28:16	Vertical Total				
	Description				
	<p>This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This field is ignored by WD transcoders.</p> <p>Vertical total is double buffered. It updates immediately when transcoder is off. Otherwise, it updates at VBLANK rising edge.</p>				
Restriction					
This register must always be programmed to the same value as the Vertical Blank End.					
15:13	Reserved				
	<table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
12:0	Vertical Active				
	<p>This field specifies Vertical Active Display size. The first vertical active display line is considered line number# 0. This field is always programmed to the number of lines desired minus one.</p>				
	<p>Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.</p>				



TRANS_WD_FUNC_CTL

TRANS_WD_FUNC_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	6E400h-6E403h							
Name:	Transcoder WD0 Function Control							
ShortName:	TRANS_WD_FUNC_CTL_0							
Reset:	soft							
Address:	6EC00h-6EC03h							
Name:	Transcoder WD1 Function Control							
ShortName:	TRANS_WD_FUNC_CTL_1							
Reset:	soft							
DWord	Bit	Description						
0	31	WD Function Enable This bit enables the WD function.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	Triggered Capture Mode Enable This field enables the triggered capture mode where a frame is only captured after the Start Trigger Frame bit is written with 1, and hardware will ignore the transcoder frame time. This must be set before or when WD Function Enable is set. When triggered capture mode is disabled hardware will periodically capture frames following the transcoder frame time.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	29	Start Trigger Frame						
		<table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> Write a 1 to this field to start a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame starts.	Access:	R/W Set				
Access:	R/W Set							
28	Stop Trigger Frame							
	<table border="1"> <tr> <td>Access:</td> <td>R/W Set</td> </tr> </table> Write a 1 to this field to stop a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame stops. This is only intended for use in case of an error where capture is never completing and software times out. It must not be set at the same time as Start Trigger Frame. After a stop trigger, VDenc will be out of sync with WD and also need to be stopped. WD and	Access:	R/W Set					
Access:	R/W Set							

TRANS_WD_FUNC_CTL

	VDenc then need to start from the same frame number.	
27	Reserved	
26	Chroma Filtering Enable This field selects how U and V are downsampled from YUV 444 to 422. This field only applies to the YUV 422 formats.	
	Value	Name
	0	Drop
	1	Filter [Default]
25:23	Reserved	
	Access:	RO
	Format:	MBZ
22:20	WD Color Mode This field selects the capture color format.	
	Value	Name
	000b	YUV 4:4:4
	001b	YUV 4:2:2
	010b	XYUV 4:4:4
	011b	RGBX
	100b	Y410
	101b	YUY2 8b
	110b	RGB10
	Restriction	
	This field must not be changed while the function is enabled.	
19:18	Control Pointers This field controls which pointers are sent and followed. If the head pointer is ignored, then the transcoder captures frames without any pointer comparison to stall the capture.	
	Value	Name
	00b	Enable Tail and Head
	01b	Enable Tail, Disable Head
	11b	Disable Tail and Head

TRANS_WD_FUNC_CTL

17:16	<p>VDenc Session Select</p> <p>This field selects the encode session. Each enabled WD transcoder must select a unique session. It is not valid to have multiple WD transcoders select the same session.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">01b</td> <td style="text-align: center;">1</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">2</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">3</td> </tr> </tbody> </table>	Value	Name	00b	0	01b	1	10b	2	11b	3				
Value	Name														
00b	0														
01b	1														
10b	2														
11b	3														
15	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ										
Access:	RO														
Format:	MBZ														
14:12	<p>WD Input Select</p> <p>These bits determine the input to WD.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td style="text-align: center;">Pipe A</td> </tr> <tr> <td style="text-align: center;">101b</td> <td style="text-align: center;">Pipe B</td> </tr> <tr> <td style="text-align: center;">110b</td> <td style="text-align: center;">Pipe C</td> </tr> <tr> <td style="text-align: center;">111b</td> <td style="text-align: center;">Pipe D</td> </tr> <tr> <td style="text-align: center;">Others</td> <td style="text-align: center;">Reserved</td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Restriction</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.</td> </tr> </tbody> </table>	Value	Name	000b	Pipe A	101b	Pipe B	110b	Pipe C	111b	Pipe D	Others	Reserved	Restriction	This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.
Value	Name														
000b	Pipe A														
101b	Pipe B														
110b	Pipe C														
111b	Pipe D														
Others	Reserved														
Restriction															
This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.															
11:4	<p>Reserved</p>														
3:0	<p>Frame Number</p> <p>SW provided frame number. This is sent in the tail pointer message to media, to be used for synchronizing the encode with the display frame.</p>														

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT												
Register Space:	MMIO: 0/2/0											
Size (in bits):	32											
Address:	04DE8h											
Name:	TiledResources Null Tile Detection Register											
ShortName:	TRNULLDETCT											
DWord	Bit	Description										
0	31:0	Null Tile Detection Value <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>DEV</td> </tr> </table> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00000000h</td> <td>Default]</td> <td>A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.</td> </tr> </tbody> </table>	Access:	R/W	_Custom_GTIReset:	DEV	Value	Name	Description	00000000h	Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.
Access:	R/W											
_Custom_GTIReset:	DEV											
Value	Name	Description										
00000000h	Default]	A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.										



TSEG Base Memory

TSEGMB - TSEG Base Memory			
Register Space:	MMIO: 0/2/0		
Size (in bits):	64		
SOC_Consumer:	BIOS		
Address:	108400h		
This 64 bit register defines the TSEG Base.			
DWord	Bit	Description	
0..1	63:20	TSEG Memory Base	
		Access:	R/W
		_Custom_GTIReset:	BUS
		This register contains the base address of TSEG DRAM memory. Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled.	
		Value	Name
	000000000000b	[Default]	
19:0	19:0	Reserved	
		Access:	RO
		Format:	MBZ

Ungated Clock Counter for DFR Testability

SAMPLER_DFR_UNGATED_COUNT - Ungated Clock Counter for DFR Testability				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	0E148h			
For testability of DFR feature				
DWord	Bit	Description		
0	31:0	Counter Bits <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td style="text-align: center;">U32</td> </tr> </table> Count of full-speed sampler clocks	Format:	U32
Format:	U32			



Unslice unit Level Clock Gating Control 943C

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C					
Register Space: MMIO: 0/2/0					
Size (in bits): 32					
CustomGTIs_ContextSaved: true					
Address: 0943Ch					
Unit Level Clock Gating Disable bits					
DWord	Bit	Description			
0	31	hprunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:
	Access:	R/W			
	_Custom_GTIReset:	BUS			
	30	Reserved			
29:26	Reserved				
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
25		mmcdunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>mmcdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W				
_Custom_GTIReset:	BUS				
24		bfceunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>bfceunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W				
_Custom_GTIReset:	BUS				
23		ecpunit Clock Gating Disable			
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>ecpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:
Access:	R/W				
_Custom_GTIReset:	BUS				

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

22	vdlunit1 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
21	vhmeunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
20	vimeunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	vimeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
19	vcreunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
18	vdxcunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	vdxcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
17	mdcunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
16	hpunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	hpunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
15	hrsunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	hrsunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
14	ftunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	ftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
13	fqunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	fqunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
12	hleunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
11	hlcunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	hlcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for		

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

	functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
10	<p>hhiunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hhiunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
9	<p>mhfunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>mhfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
8	<p>mmcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>mmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
7	<p>mbdunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
6	<p>mpdunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
5	<p>mmxunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

	<p>mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>				
4	<p>hedunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
3	<p>hlfunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
2	<p>hmcunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
1	<p>hmxunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
0	<p>hppunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

Unslice unit Level Clock Gating Control 9430

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09430h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
	29	oaal2 Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset: BUS	
oaal2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
28	oaal3 Clock Gating Disable		
	Access:	R/W	
		_Custom_GTIReset: BUS	
oaal3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
27	mertgart Clock Gating Disable		
	Access:	R/W	
		_Custom_GTIReset: BUS	
mertgart Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
26	RCPBLAT Clock Gating Disable		
	Access:	R/W	
		_Custom_GTIReset: BUS	
RCPBLAT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

25	RCPBARB Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	RCPBARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
24	LNIC Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	LNIC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
23	LNIB Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	LNIB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
22	Reserved	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	Reserved	
21	Reserved	
	Access:	RO
	Format:	MBZ
20	SARB Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	SARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
19	DAP Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	DAP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
18	RCC Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
RCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
17	RAMRCC Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
RAMRCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
16	Reserved		
	Access:		R/W
	_Custom_GTIReset:		BUS
Reserved			
15	SRCBPPIX Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
SRCBPPIX Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
14	SCFE Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
SCFE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
13	LNEP Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
LNEP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

12	<p>MSQC wrapper 2xclk Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>MSQC wrapper 2xclk Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	1b						
Access:	R/W						
_Custom_GTIReset:	BUS						
11	<p>MSQC wrapper Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>MSQC wrapper Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	1b						
Access:	R/W						
_Custom_GTIReset:	BUS						
10	<p>GCPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	1b						
Access:	R/W						
_Custom_GTIReset:	BUS						
9	<p>SPARE6 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	1b						
Access:	R/W						
_Custom_GTIReset:	BUS						
8	<p>SPARE5 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="width: 30%;">1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	1b						
Access:	R/W						
_Custom_GTIReset:	BUS						

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7	SPARE4 Clock Gating Disable	
	Default Value:	1b
	Access:	R/W
	_Custom_GTIRreset:	BUS
SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
6	GPMunit Clock Gating Disable	
	Default Value:	1b
	Access:	R/W
	_Custom_GTIRreset:	BUS
GPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
5	MBGFunit Clock Gating Disable	
	Default Value:	1b
	Access:	R/W
	_Custom_GTIRreset:	BUS
MBGFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
4	MSQDunit Clock Gating Disable	
	Default Value:	1b
	Access:	R/W
	_Custom_GTIRreset:	BUS
MSQDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
3	MSQDunit 2xclk Clock Gating Disable	
	Default Value:	1b
	Access:	R/W
	_Custom_GTIRreset:	BUS
MSQDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

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2	MISDunits 2x Clock Gating Disable		
	Default Value:		1b
	Access:		R/W
	_Custom_GTIRreset:		BUS
	MISDunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
1	MISDunit Clock Gating Disable		
	Default Value:		1b
	Access:		R/W
	_Custom_GTIRreset:		BUS
	MISDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
0	MCRunit Clock Gating Disable		
	Default Value:		1b
	Access:		R/W
	_Custom_GTIRreset:		BUS
	MCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

Unslice unit Level Clock Gating Control 9434

UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434							
Register Space:	MMIO: 0/2/0						
Size (in bits):	32						
Address:	09434h						
Unit Level Clock Gating Disable bits							
DWord	Bit	Description					
0	31	GTlunit Clock Gating Disable					
		Access:	R/W				
		Format:	Disable				
		_Custom_GTIReset:	BUS				
			GTlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
			<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>[Default]</td> </tr> </tbody> </table>	Value	Name	1b	[Default]
	Value	Name					
	1b	[Default]					
	30	Reserved					
		Access:	RO				
			Format:	MBZ			
	29	GAMunit Clock Gating Disable					
Default Value:		1b					
Access:		R/W					
Format:		Disable					
_Custom_GTIReset:		BUS					
		GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)					
28	GABunit Clock Gating Disable						
	Access:	R/W					
	Format:	Disable					
	_Custom_GTIReset:	BUS					
			GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>[Default]</td> </tr> </tbody> </table>	Value	Name	1b	[Default]	
Value	Name						
1b	[Default]						

UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434

27	DTunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	BUS
DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
26	Reserved	
	Access:	RO
	Format:	MBZ
25	BLSunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	BUS
BLSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
24	BLBunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	BUS
BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
23	BFunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	BUS
BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
22	BDunit Clock Gating Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	BUS
BDunit Clock Gating Disable Control:		

UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434

	<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>								
21	<p>BCSunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>BCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS		
Access:	R/W								
Format:	Disable								
_Custom_GTIReset:	BUS								
20	<p>gamtlbhtarb Clock Gating Disable</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>gamtlbhtarb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Default Value:	1b								
Access:	R/W								
Format:	Disable								
_Custom_GTIReset:	BUS								
19	<p>DTOunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS		
Access:	R/W								
Format:	Disable								
_Custom_GTIReset:	BUS								
18	<p>gamtlbmisarb Clock Gating Disable</p> <table border="1"> <tr> <td>Default Value:</td> <td>1b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>gamtlbmisarb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Default Value:	1b	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Default Value:	1b								
Access:	R/W								
Format:	Disable								
_Custom_GTIReset:	BUS								
17:14	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO								
Format:	MBZ								

UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434

13	RCPBunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W							
Format:	Disable							
_Custom_GTIReset:	BUS							
12	QCunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W							
Format:	Disable							
_Custom_GTIReset:	BUS							
11:8	Reserved	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
7	cg3ddisvfg Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>cg3ddisvfg Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W							
Format:	Disable							
_Custom_GTIReset:	BUS							
6	MSPBISTunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>MSPBISTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W							
Format:	Disable							
_Custom_GTIReset:	BUS							
5	OACSunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td style="width: 50%;">R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>OACSunit Clock Gating Disable Control:</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W							
Format:	Disable							
_Custom_GTIReset:	BUS							

UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434

	<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>						
4	<p>NOAunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>NOAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
3	<p>OARUNIT Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>OARUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
2	<p>VMEunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
1	<p>BCS BE Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>BCS BE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						
0	<p>BCS FE Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>Disable</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>BCS FE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	Format:	Disable	_Custom_GTIReset:	BUS
Access:	R/W						
Format:	Disable						
_Custom_GTIReset:	BUS						



UNSLCGCTL9434 - Unslice unit Level Clock Gating Control 9434

		functionality)
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9438

UNSLCGCTL9438 - Unslice unit Level Clock Gating Control 9438			
Register Space: MMIO: 0/2/0			
Size (in bits): 32			
CustomGTIIs_ContextSaved: true			
Address: 09438h			
Unit Level Clock Gating Disable bits.			
DWord	Bit	Description	
0	31	Reserved	
		Access: RO	
		Format: MBZ	
	30:29	MSQCunit Clock Gating Disable	
		Access: R/W	
		_Custom_GTIReset: BUS	
		MSQCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
		Value	Name
		11b	[Default]
	28	VCOPunit Clock Gating Disable	
		Access: R/W	
		_Custom_GTIReset: BUS	
VCOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
LNIunit Clock Gating Disable			
Access: R/W			
27	LNIunit Clock Gating Disable		
	Access: R/W		
	_Custom_GTIReset: BUS		
	LNIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	LNEUNIT Clock Gating Disable		
	Access: R/W		
26	LNEUNIT Clock Gating Disable		
	Access: R/W		
	_Custom_GTIReset: BUS		
LNEUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for			

UNSLCGCTL9438 - Unslice unit Level Clock Gating Control 9438

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	25:20	Reserved	
		Access:	RO
		Format:	MBZ
19	RPM Clock Gating Disable		
		Access:	R/W
		_Custom_GTIReset:	BUS
	RPM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
18	OASC Clock Gating Disable		
		Access:	R/W
		_Custom_GTIReset:	BUS
	OASC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
17	VECS Clock Gating Disable		
		Access:	R/W
		_Custom_GTIReset:	BUS
	VECS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
16	GAHSV Clock Gating Disable		
		Access:	R/W
		_Custom_GTIReset:	BUS
	GAHSV Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
15	GAHSD Clock Gating Disable		
		Access:	R/W
		_Custom_GTIReset:	BUS
	GAHSD Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

UNSLCGCTL9438 - Unslice unit Level Clock Gating Control 9438

14	Reserved		
	Access:	RO	
	Format:	MBZ	
	13	GAPSL Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	GAPSL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	12	GAPSU Clock Gating Disable	
Access:		R/W	
	_Custom_GTIReset:	BUS	
GAPSU Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
11	SPMunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
SPMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
10	MUCunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
MUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
9	Reserved		
	Access:	RO	
	Format:	MBZ	
8	GUC Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
GUC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			



UNSLCGCTL9438 - Unslice unit Level Clock Gating Control 9438

	7:0	Reserved	
		Access:	RO
		Format:	MBZ

Unslice unit Level Clock Gating Control 9440

UNSLCGCTL9440 - Unslice unit Level Clock Gating Control 9440				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	09440h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31:29	Reserved		
		Access:	RO	
		Format:	MBZ	
	28	gamtlboacs Clock Gating Disable		
		Access:	R/W	
		_Custom_GTIReset:	BUS	
		gamtlboacs Clock Gating Disable Control:		
		Value	Name	Description
		1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
		0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
	27	gamtlbgfx3 Clock Gating Disable		
		Access:	R/W	
_Custom_GTIReset:		BUS		
gamtlbgfx3 Clock Gating Disable Control:				
Value		Name	Description	
1b		Clock Gating Disabled [Default]	Clocks are toggling, always.	
0b		Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
26	gamtlbgfx2 Clock Gating Disable			
	Access:	R/W		
	_Custom_GTIReset:	BUS		
	gamtlbgfx2 Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	

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25	gamdrtnunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	gamdrtnunit Clock Gating Disable Control:	
	Value	Name
		Description
	1b	Clock Gating Disabled [Default]
		Clocks are toggling, always.
	0b	Clock Gating Enabled
		Clocks can be gated when they are not required to toggle for functionality.
24	gamtlbgfx1 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	gamtlbgfx1 Clock Gating Disable Control:	
	Value	Name
		Description
	1b	Clock Gating Disabled [Default]
		Clocks are toggling, always.
	0b	Clock Gating Enabled
		Clocks can be gated when they are not required to toggle for functionality.
23	gamtlbgfx0 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	gamtlbgfx0 Clock Gating Disable Control:	
	Value	Name
		Description
	1b	Clock Gating Disabled [Default]
		Clocks are toggling, always.
	0b	Clock Gating Enabled
		Clocks can be gated when they are not required to toggle for functionality.
22	gamtlbvebox0 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	gamtlbvebox0 Clock Gating Disable Control:	
	Value	Name
		Description
	1b	Clock Gating Disabled [Default]
		Clocks are toggling, always.
	0b	Clock Gating Enabled
		Clocks can be gated when they are not required to toggle for functionality.
21	gamtlbvdbox2 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS

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	gamtlbvdbox2 Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
20	SPARE Clock Gating Disable2		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SPARE Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
19	SPARE Clock Gating Disable1		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SPARE Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
18	LSNEPunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	LSNEPUNIT Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
17	gamtlbvdbox0 Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamtlbvdbox0 Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled	Clocks are toggling, always.

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			[Default]	
		0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
16	gamtlbkcr Clock Gating Disable			
	Access:			R/W
	_Custom_GTIRreset:			BUS
	gamtlbkcr Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
15	gamtlbguc Clock Gating Disable			
	Access:			R/W
	_Custom_GTIRreset:			BUS
	gamtlbguc Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
14	gamtlbbt Clock Gating Disable			
	Access:			R/W
	_Custom_GTIRreset:			BUS
	gamtlbbt Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
13	gamtrtlb Clock Gating Disable			
	Access:			R/W
	_Custom_GTIRreset:			BUS
	gamtrtlb Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	

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12	gamstlb Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamstlb Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
11	gamccs Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamccs Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
10	GACFG Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	GACFG Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
9	GAVARBunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	GAVARBunit Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
8	gamctrl Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS

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	gamctrl Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
7	gamcmdi Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamcmdi Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
6	Reserved		
	Access:		RO
	Format:		MBZ
5	gamwkrs Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamwkrs Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
4	gamdati Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	gamdati Clock Gating Disable Control:		
	Value	Name	Description
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.

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	3	L3_CR Clock Gating Disable		
		Access:		R/W
		_Custom_GTIReset:		BUS
		L3_CR Clock Gating Disable Control:		
		Value	Name	Description
		1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
		0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.
	2	gamreqstrm Clock Gating Disable		
		Access:		R/W
		_Custom_GTIReset:		BUS
		gamreqstrm Clock Gating Disable Control:		
		Value	Name	Description
		1b	Clock Gating Disabled [Default]	Clocks are toggling, always.
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
1	ramdft Clock Gating Disable			
	Access:		R/W	
	_Custom_GTIReset:		BUS	
	ramdft Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	
0	hwmunit Clock Gating Disable			
	Access:		R/W	
	_Custom_GTIReset:		BUS	
	hwmunit Clock Gating Disable Control:			
	Value	Name	Description	
	1b	Clock Gating Disabled [Default]	Clocks are toggling, always.	
	0b	Clock Gating Enabled	Clocks can be gated when they are not required to toggle for functionality.	



Unslice unit Level Clock Gating Control 9444

UNSLCGCTL9444 - Unslice unit Level Clock Gating Control 9444			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	09444h		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:4	Reserved	
		Access:	RO
		Format:	MBZ
	3	KCRunit Clock Gating Disable	
		Access:	R/W
_Custom_GTIRreset:		BUS	
KCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
2	WCRunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
WCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
1	Isnunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
Isnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
0	warbunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
warbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

Unslice unit Level Clock Gating Control 9448

UNSLCGCTL9448 - Unslice unit Level Clock Gating Control 9448						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
Address:	09448h					
Unslice unit Level Clock Gating Control 9448 Unit Level Clock Gating Disable bits						
DWord	Bit	Description				
0	31:0	ECO Spare Bits <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> Reserved.	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					



Unslice unit Level Clock Gating Control 9450

UNSLCGCTL9450 - Unslice unit Level Clock Gating Control 9450		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09450h	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
	29	URBunit Clock Gating Disable
		Access: R/W
_Custom_GTIReset: BUS		
URBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
28:27	Reserved	
	Access: RO	
	Format: MBZ	
26	RCPBEunit Clock Gating Disable	
	Access: R/W	
	_Custom_GTIReset: BUS	
RCPBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
25	GAMunit Clock Gating Disable	
	Access: R/W	
	_Custom_GTIReset: BUS	
GAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
24	HDCunit Clock Gating Disable	
	Access: R/W	
	_Custom_GTIReset: BUS	
HDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for		

UNSLCGCTL9450 - Unslice unit Level Clock Gating Control 9450

	functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)				
23	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
22	<p>BLBunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
21	<p>BFunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
20	<p>MUCunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>MUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
19	<p>WVISunit Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>WVISunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
18	<p>WAVM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>WAVM Clock Gating Disable Control:</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

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	<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>				
17	<p>WHME Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>WHME Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
16	<p>WIME Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>WIME Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
15	<p>WMPC Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>WMPC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
14	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
13	<p>VSHM Clock Gating Disable</p> <table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VSHM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

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12	DAPRTS Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	DAPRTS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
11	Reserved	
	Access:	RO
	Format:	MBZ
10	GUC Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	GUC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
9:6	Reserved	
	Access:	RO
	Format:	MBZ
5	vdlunit1 Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	vdlunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
4	vhmeunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

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	3	vcreunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	vcreunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	2	hleunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	hleunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	1	mbdunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	mbdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	0	mmxunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	mmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

Unslice unit Level Clock Gating Control 9454

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09454h	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:22	Reserved
		Access: RO
	Format: MBZ	
	21	SPARE Clock Gating Disable2 Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
20	ram gamtm2 unit Clock Gating Disable Access: R/W _Custom_GTIReset: BUS gamtm2 unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
19	ram gamtm1 unit Clock Gating Disable Access: R/W _Custom_GTIReset: BUS gamtm1 unit Clock Gating Disable Control for ram: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
18	VDIunit Clock Gating Disable Access: R/W _Custom_GTIReset: BUS VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	

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		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	17:14	Reserved	
		Access:	RO
		Format:	MBZ
	13	GAMTGunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		GAMTGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	12	GAMTOunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		GAMTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	11:10	Reserved	
		Access:	RO
		Format:	MBZ
	9	mpdunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		mpdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	8	hedunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454

	7	hlfunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	6	hmcunit Clock Gating Disable	
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
5	hmxunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
4	hppunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			
3	hprunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)			

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454

2	hucunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	<p>hucunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
1	hwmunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	<p>hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
0	mdcunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	<p>mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

uOS Full Hash High

UOS_FULL_HASH_HI - uOS Full Hash High		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	128	
<p>The Full Hash being generated for the uOS. This register is written by Shim hardware. The update happens as the Full Hash is being generated and compared during the GfxMem --> WOPCM DMA operation. IA Writes have no effect.</p>		
Programming Notes		
This register is saved in the power context		
DWord	Bit	Description
0..3	127:0	Hash



uOS Full Hash Low

UOS_FULL_HASH_LO - uOS Full Hash Low		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	128	
<p>The Full Hash being generated for the uOS. This register is written by Shim hardware. The update happens as the Full Hash is being generated and compared during the GfxMem --> WOPCM DMA operation. IA Writes have no effect.</p>		
Programming Notes		
This register is saved in the power context		
DWord	Bit	Description
0..3	127:0	Hash

URB Runtime ECC capture Register

URB_ECC_CAPTURE_REG - URB Runtime ECC capture Register				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	0B14Ch			
This register shows the captured value of the ECC calculated by the internal logic for URB writes.				
DWord	Bit	Description		
0	31:20	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
	19:0	URB Latched ECC Value		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field holds the value of the ECC generated by the URB pipeline for the preceding write cycle.</p>	Access:	RO
Access:	RO			



URB Runtime ECC Test Control Register

URB_ECC_TEST_CTL - URB Runtime ECC Test Control Register				
Register Space:	MMIO: 0/2/0			
Access:	R/W			
Size (in bits):	32			
_Custom_GTIReset:	DEV			
Address:	0B148h			
This register is used to control the run time testing of the ECC logic in the URB pipeline.				
DWord	Bit	Description		
0	31:22	Reserved		
		Access:	RO	
		Format:	MBZ	
	21	URB ECC Latch Enable		
		Access:	R/W	
		This bit enables the latching of the ECC value generated for any write access made to the URB. The latched value of the ECC can be read from the "URB Cache Runtime ECC capture Register".		
		Value	Name	Description
		0	[Default]	Disable latching.
	1		Enable the latching	
	20	URB ECC Override Enable		
Access:		R/W		
This bit enables the overriding of the ECC value generated for any write access made to the URB. The value in the field below will be used to override the ECC internally generated.				
Value		Name	Description	
0		[Default]	Disable override of the ECC value	
1		Enable the override of the ECC value		
19:0	URB ECC Override Value			
	Default Value:	00h		
	Access:	R/W		
This is the value to be used as the override for the ECC when enabled in the bit field above.				

UTIL_PIN_BUF_CTL

UTIL_PIN_BUF_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	48404h-48407h	
Name:	Utility Pin Buffer Control	
ShortName:	UTIL_PIN_BUF_CTL	
Reset:	soft	
This register controls the display utility pin I/O buffer.		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
	29:28	Hysteresis
	27	Reserved
		Access: RO
		Format: MBZ
	26:24	Spare
	23:21	Reserved
		Access: RO
		Format: MBZ
	20:16	Pulldown Strength
	15:12	Pulldown Slew
	11:9	Reserved
Access: RO		
Format: MBZ		
8:4	Pullup Strength	
3:0	Pullup Slew	

UTIL_PIN_CTL

UTIL_PIN_CTL																
Register Space:	MMIO: 0/2/0															
Access:	R/W															
Size (in bits):	32															
Address:	48400h-48403h															
Name:	Utility Pin Control															
ShortName:	UTIL_PIN_CTL															
Reset:	soft															
This register controls the display utility pin. The maximum switching frequency is 100 KHz.																
DWord	Bit	Description														
0	31	Util Pin Enable This bit enables the utility pin. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable								
		Value	Name													
		0b	Disable													
		1b	Enable													
	30:29	Pipe Select This bit selects which pipe will be used when the utility pin is outputting timing related signals. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Pipe A</td> </tr> <tr> <td>01b</td> <td>Pipe B</td> </tr> <tr> <td>10b</td> <td>Pipe C</td> </tr> <tr> <td>11b</td> <td>Pipe D</td> </tr> </tbody> </table>	Value	Name	00b	Pipe A	01b	Pipe B	10b	Pipe C	11b	Pipe D				
		Value	Name													
		00b	Pipe A													
		01b	Pipe B													
		10b	Pipe C													
	11b	Pipe D														
Restriction																
The field should only be changed when the utility pin is disabled or not configured to use any timing signals.																
28	Reserved Access: RO Format: MBZ															
27:24	Util Pin Mode This bit configures the utility pin mode of operation for output. <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Data</td> <td>Output the Util_Pin_Output_Data value.</td> </tr> <tr> <td>0001b</td> <td>PWM</td> <td>Output from the backlight PWM circuit.</td> </tr> <tr> <td>0100b</td> <td>Vblank</td> <td>Output the vertical blank. [] This is the pipe delayed vblank.</td> </tr> <tr> <td>0101b</td> <td>Vsync</td> <td>Output the vertical sync.</td> </tr> </tbody> </table>	Value	Name	Description	0000b	Data	Output the Util_Pin_Output_Data value.	0001b	PWM	Output from the backlight PWM circuit.	0100b	Vblank	Output the vertical blank. [] This is the pipe delayed vblank.	0101b	Vsync	Output the vertical sync.
	Value	Name	Description													
	0000b	Data	Output the Util_Pin_Output_Data value.													
	0001b	PWM	Output from the backlight PWM circuit.													
	0100b	Vblank	Output the vertical blank. [] This is the pipe delayed vblank.													
0101b	Vsync	Output the vertical sync.														

UTIL_PIN_CTL			
	0110b	framestart	Output the framestart
	1000b	Right/Left Eye Level	Output the stereo 3D right/left eye level signal. Asserted for the left eye and de-asserted for the right eye.
	Others	Reserved	Reserved
Restriction			
			The field should only be changed when the utility pin is disabled.
23	Util Pin Output Data This bit selects what the value to drive as an output when in the data mode.		
	Value	Name	
	0b	0	
	1b	1	
22	Util Pin Output Polarity This bit inverts the polarity of the pin output.		
	Value	Name	
	0b	Not inverted	
	1b	Inverted	
21:20	Reserved		
	Access:	RO	
	Format:	MBZ	
19	Util Pin Direction This bit selects whether the pin is used as an output or an input.		
	Value	Name	
	0b	Output	
	1b	Input	
Restriction			
			The field should only be changed when the utility pin is disabled.
18:17	Reserved		
	Access:	RO	
	Format:	MBZ	
16	Util Pin Input Data		
	Access:	RO	
	This bit gives the value received on the pin. This is only valid when the utility pin is enabled and the direction is input.		
15:0	Reserved		
	Access:	RO	
	Format:	MBZ	



UTIL2_PIN_BUF_CTL

UTIL2_PIN_BUF_CTL		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	4840Ch-4840Fh	
Name:	Utility2 Pin Buffer Control	
ShortName:	UTIL2_PIN_BUF_CTL	
Reset:	soft	
This register controls the display utility2 pin I/O buffer.		
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
	29:28	Hysteresis
	27	Reserved
		Access: RO
		Format: MBZ
	26:24	Spare
	23:21	Reserved
		Access: RO
		Format: MBZ
	20:16	Pulldown Strength
	15:12	Pulldown Slew
	11:9	Reserved
Access: RO		
Format: MBZ		
8:4	Pullup Strength	
3:0	Pullup Slew	

UTIL2_PIN_CTL

UTIL2_PIN_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	48408h-4840Bh							
Name:	Utility2 Pin Control							
ShortName:	UTIL2_PIN_CTL							
Reset:	soft							
This register controls the display utility2 pin.								
DWord	Bit	Description						
0	31	Util Pin Enable This bit enables the utility pin.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	Util Pin Direction This bit selects whether the pin is used as an output or an input.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Output</td> </tr> <tr> <td>1b</td> <td>Input</td> </tr> </tbody> </table>	Value	Name	0b	Output	1b	Input
		Value	Name					
		0b	Output					
	1b	Input						
Restriction								
The field should only be changed when the utility pin is disabled.								
29:0	Reserved							
	Access:	RO						
	Format:	MBZ						



Valid Bit Vector 3 for RCC Register

CCTLB_VLD_3 - Valid Bit Vector 3 for RCC Register								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
Address:	04DACH							
This register contains the valid bits for entries 0-31 of RCCTLB.								
DWord	Bit	Description						
0	31:0	Valid Bit Vector 3 for RCC <table border="1"><tr><td>Default Value:</td><td>00000000h</td></tr><tr><td>Access:</td><td>RO</td></tr><tr><td>_Custom_GTIReset:</td><td>DEV</td></tr></table> Valid Bits per Entry.	Default Value:	00000000h	Access:	RO	_Custom_GTIReset:	DEV
Default Value:	00000000h							
Access:	RO							
_Custom_GTIReset:	DEV							

VCS CSB

VCS_CSB - VCS CSB				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
SW reads this offset to read the CSB entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64 bit CSB entry. The second read pops the entry off the CSB fifo.				
DWord	Bit	Description		
0	31:0	Context Status Buffer DW <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.</p>	Access:	RO
Access:	RO			



VCS CSB Fifo Status Register

VCS_CSБ_FSR - VCS CSB Fifo Status Register		
Register Space: MMIO: 0/2/0		
Size (in bits): 32		
This RO register holds status of the CSB fifo.		
DWord	Bit	Description
0	31	Not Empty
		Default Value: 0000000000000000b
		Access: RO
	30:16	Reserved
		Access: RO
		Format: MBZ
15:8	FIFO Maximum Occupancy Count This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.	
7:0	Fifo Occupancy Count	
	Access: RO	

VDBox TLB Invalidation Register

VD_TLB_INV_CR - VDBox TLB Invalidation Register			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
_Custom_GTIRreset:	DEV		
Address:	0CEDCh		
DWord	Bit	Description	
0	31:16	Mask Bits	
		Default Value:	0000000000000000b
		Access:	R/W
	15:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	Invalidate VDBox TLBs bit7	
		Default Value:	0b
		Access:	R/W
		<p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>	
	6	Invalidate VDBox TLBs bit6	
		Default Value:	0b
Access:		R/W	
<p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>			
5	Invalidate VDBox TLBs bit5		
	Default Value:	0b	
	Access:	R/W	
	<p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>		

VD_TLB_INV_CR - VDBox TLB Invalidation Register

4	<p>Invalidate VDBox TLBs bit4</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
3	<p>Invalidate VDBox TLBs bit3</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
2	<p>Invalidate VDBox TLBs bit2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
1	<p>Invalidate VDBox TLBs bit1</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
0	<p>Invalidate VDBox TLBs bit0</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Default Value:</td> <td style="text-align: center;">0b</td> </tr> <tr> <td>Access:</td> <td style="text-align: center;">R/W</td> </tr> </table> <p>SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses.</p>	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				

VD_TLB_INV_CR - VDBox TLB Invalidation Register

		Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
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Vdbox unit Level Clock Gating Control 3F0C

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CustomGTIIs_ContextSaved:	true	
Address:	1C3F0Ch-1C3F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX0	
Address:	1C7F0Ch-1C7F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX1	
Address:	1D3F0Ch-1D3F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX2	
Address:	1D7F0Ch-1D7F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX3	
Address:	1E3F0Ch-1E3F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX4	
Address:	1E7F0Ch-1E7F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX5	
Address:	1F3F0Ch-1F3F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX6	
Address:	1F7F0Ch-1F7F0Fh	
Name:	VDbox registers4	
ShortName:	VDCGCTL3F0C_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	SPARE Clock Gating Disable12
		Access: R/W
		_Custom_GTIReset: BUS
SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for		

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
30	SPARE Clock Gating Disable11		
	Access:		R/W
	_Custom_GTIReset:		BUS
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
29	SPARE Clock Gating Disable10		
	Access:		R/W
	_Custom_GTIReset:		BUS
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
28	SPARE Clock Gating Disable9		
	Access:		R/W
	_Custom_GTIReset:		BUS
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
27	VNCunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	VNCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
26	VMXunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
25	VMTSunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	VMTSunit Clock Gating Disable Control:		

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	24	VMPcunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		<p>VMPcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	23	VMDunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		<p>VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	22	VMCRunit Clock Gating Disable	
		Default Value:	1b
		Access:	R/W
		_Custom_GTIReset:	BUS
		<p>VMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	21	VMCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		<p>VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
	20	VMBunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		<p>VMBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

19	<p>VLFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
18	<p>VITunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
17	<p>VISunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VISunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
16	<p>VIPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VIPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
15	<p>VID6 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID6 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

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14	<p>VID5 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID5 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>VID4 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID4 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>VID3 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>VID2 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
10	<p>VID1 Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VID1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

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9	<p>VIMEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VIMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
8	<p>VHRunit's Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VHRunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
7	<p>VHMEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VHMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>VFTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
5	<p>VDXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

4	<p>VDSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
3	<p>vd1unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>vd1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
2	<p>Csunit's Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>Csunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
1	<p>VCREunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
0	<p>VCPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

Vdbox unit Level Clock Gating Control 3F04

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CustomGTIIs_ContextSaved:	true	
Address:	1C3F04h-1C3F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX0	
Address:	1C7F04h-1C7F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX1	
Address:	1D3F04h-1D3F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX2	
Address:	1D7F04h-1D7F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX3	
Address:	1E3F04h-1E3F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX4	
Address:	1E7F04h-1E7F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX5	
Address:	1F3F04h-1F3F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX6	
Address:	1F7F04h-1F7F07h	
Name:	VDbox registers2	
ShortName:	VDCGCTL3F04_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	spare Clock Gating Disable4
		Access: R/W
		_Custom_GTIReset: BUS
SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for		

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	30	spare Clock Gating Disable3	
		Access:	R/W
		_Custom_GTIReset:	BUS
		SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	29	spare Clock Gating Disable2	
		Access:	R/W
		_Custom_GTIReset:	BUS
		SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	28	HVSHAREunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		HVSHAREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	27	HFTunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		HFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	26	HFQunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
		HFQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

25	HCRESunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HCRESunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
24	HCRESunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HCRESunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
23	HCRESunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HCRESunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
22	MEDunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
21	GACXunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GACXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

20	GACunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>GACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
19	ECPunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>ECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
18	BSPunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>BSPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
17	vmmunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
16	VHLFunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

15	<p>VDKMXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>VDKMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>HWMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HWMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>HUCMXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HUCMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>HUCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>HSSEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HSSEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

10	<p>HSFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HSFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
9	<p>HPRunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
8	<p>HPPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HPPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
7	<p>HMXFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HMXFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>HMXBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HMXBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

5	<p>HMCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
4	<p>HITunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HITunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
3	<p>HHLFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
2	<p>HFCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HFCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
1	<p>HEDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

0	HBEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	<p>HBEunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

Vdbox unit Level Clock Gating Control 3F08

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CustomGTIIs_ContextSaved:	true	
Address:	1C3F08h-1C3F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX0	
Address:	1C7F08h-1C7F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX1	
Address:	1D3F08h-1D3F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX2	
Address:	1D7F08h-1D7F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX3	
Address:	1E3F08h-1E3F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX4	
Address:	1E7F08h-1E7F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX5	
Address:	1F3F08h-1F3F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX6	
Address:	1F7F08h-1F7F0Bh	
Name:	VDbox registers3	
ShortName:	VDCGCTL3F08_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	SPARE Clock Gating Disable8
		Access: R/W
		_Custom_GTIReset: BUS
		SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
30	SPARE Clock Gating Disable7		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
29	SPARE Clock Gating Disable6		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
28	spare Clock Gating Disable5		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
27	VClunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	VClunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
26	VCDunit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIRreset:	BUS	
	VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

25	vbspunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>vbspunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
24	VBPunits Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
23	VAMunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
22	VADuit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VADuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
21	VACunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

20	<p>USBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>USBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
19	<p>SECunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
18	<p>RDOFunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>RDOFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
17	<p>RDOBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>RDOBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
16	<p>QRCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>QRCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

15	<p>MEDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>MPCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>MDCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>MDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>jusbunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>JPGunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>JPGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

10	<p>HWOPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HWOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
9	<p>MARB Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>MARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
8	<p>HVDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HVDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
7	<p>HTQunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HTQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>HSAOunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>HSAOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

5	<p>HRSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HRSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
4	<p>HPOunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HPOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
3	<p>HMDCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HMDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
2	<p>HLEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HLEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
1	<p>HLCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>HLCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

0	HIMEunit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIRreset:	BUS
	<p>HIMEunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	

Vdbox unit Level Clock Gating Control 3F10

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CustomGTIIs_ContextSaved:	true	
Address:	1C3F10h-1C3F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX0	
Address:	1C7F10h-1C7F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX1	
Address:	1D3F10h-1D3F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX2	
Address:	1D7F10h-1D7F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX3	
Address:	1E3F10h-1E3F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX4	
Address:	1E7F10h-1E7F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX5	
Address:	1F3F10h-1F3F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX6	
Address:	1F7F10h-1F7F13h	
Name:	VDbox registers5	
ShortName:	VDCGCTL3F10_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	Reserved
		Access: RO
		Format: MBZ

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

30	VFWunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VFWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
29	VEOunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
28	ECSunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>ECSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
27	VDNunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDNunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
26	VDMunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

25	VDlunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
24	VCWunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
23	VCUSunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCUSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
22	IECPunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
21	GAVARBunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAVARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

20	GAVunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>GAVunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
19	dec400 unit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>dec400 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
18	decsubunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>decsubunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
17	SFXunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					
16	SFOunit Clock Gating Disable	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W					
_Custom_GTIRreset:	BUS					

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

15	<p>SFMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>SFlunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SFlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>SFEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>SFDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SFDunitClock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>SFAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

10	<p>hmxbrouterunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>hmxbrouterunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
9	<p>RAMDFTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>RAMDFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
8	<p>Reserved</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
7	<p>SWPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SWPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>VTQunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VTQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
5	<p>VSLunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VSLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

	<p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
4	<p>VSECunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VSECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
3	<p>VRTunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VRTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
2	<p>VPRunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
1	<p>VOPunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					
0	<p>VNEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>VNEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W					
_Custom_GTIReset:	BUS					



Vdbox unit Level Clock Gating Control 3F14

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
CustomGTIIs_ContextSaved:	true	
Address:	1C3F14h-1C3F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX0	
Address:	1C7F14h-1C7F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX1	
Address:	1D3F14h-1D3F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX2	
Address:	1D7F14h-1D7F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX3	
Address:	1E3F14h-1E3F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX4	
Address:	1E7F14h-1E7F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX5	
Address:	1F3F14h-1F3F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX6	
Address:	1F7F14h-1F7F17h	
Name:	VDbox registers6	
ShortName:	VDCGCTL3F14_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	VDIunit Clock Gating Disable
		Access: R/W
		_Custom_GTIReset: BUS
		VDIunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
30	SFMunit Clock Gating Disable1		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SFMunit Clock Gating Disable Control:		
<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
29	SFEunit Clock Gating Disable1		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SFEunit Clock Gating Disable Control:		
<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
28	SFDunits Clock Gating Disable1		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SFDunits Clock Gating Disable Control:		
<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>			
27	SFAunit Clock Gating Disable1		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	SFAunit Clock Gating Disable Control:		
<p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>			

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	26	VEOunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		VEOunit Clock Gating Disable Control:	
		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	25	VNCunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		VNCunit Clock Gating Disable Control:	
		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	24	VMXunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		VMXunit Clock Gating Disable Control:	
		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	23	vmpcunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		vmpcunit Clock Gating Disable Control:	
		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)	
		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

22	vmmunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	vmmunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
21	VMCunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	VMCunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
20	VLfunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	VLfunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
19	VISunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	VISunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

18	vhmeunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	vhmeunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
17	vhlfunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	vhlfunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
16	VCWunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	VCWunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
15	vcreunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	vcreunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

14	<p>USBunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>USBunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
13	<p>QRCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>QRCunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
12	<p>MPCunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>MPCunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
11	<p>mdcunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>mdcunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

10	<p>HWMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>HWMunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
9	<p>IECPuit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>IECPuit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
8	<p>HVDunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>HVDunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				
7	<p>HUCMXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="width: 20%;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>HUCMXunit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIReset:	BUS
Access:	R/W				
_Custom_GTIReset:	BUS				

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

6	HUCunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	HUCunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
5	HTQunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	HTQunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
4	HSAOunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	HSAOunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
3	HPRunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIRreset:		BUS
	HPRunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

2	HPPunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	HPPunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
1	HHLFunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	HHLFunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
0	HFCunit Clock Gating Disable		
	Access:		R/W
	_Custom_GTIReset:		BUS
	HFCunit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		

Vdbox unit Level Clock Gating Control 3F18

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	1C3F18h-1C3F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX0	
Address:	1C7F18h-1C7F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX1	
Address:	1D3F18h-1D3F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX2	
Address:	1D7F18h-1D7F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX3	
Address:	1E3F18h-1E3F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX4	
Address:	1E7F18h-1E7F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX5	
Address:	1F3F18h-1F3F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX6	
Address:	1F7F18h-1F7F1Bh	
Name:	VDbox registers7	
ShortName:	VDCGCTL3F18_VDBOX7	
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31:27	Reserved
		Access: RO
	Format: MBZ	
	26	VECS BE unit Clock Gating Disable
Access: R/W		
_Custom_GTIReset: BUS		

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

		<p>VECS BE unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>					
25	<p>VECS FE unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VECS FE unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>			Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
24	<p>VCS BE unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCS BE unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>			Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
23	<p>VCS FE unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCS FE unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>			Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
22	<p>amx router unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 75%;">Access:</td> <td style="width: 25%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>amxb router unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for</p>			Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

		functionality)	
		'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
21	amx unit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	amx unit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)		
20	splt unit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	splt unit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)		
19	tbc unit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	tbc unit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)		
18	vd1is unit Clock Gating Disable		
	Access:	R/W	
	_Custom_GTIReset:	BUS	
	vd1is unit Clock Gating Disable Control:		
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)		
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)		

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

17	lbc unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	lbc unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
16	amxb unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	amxb unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
15	Reserved	
	Access:	RO
	Format:	MBZ
14	awm unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	awm unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
13	aln unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	aln unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

12	<p>alf unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>alf unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>apr unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>apr unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
10	<p>amc unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>amc unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
9	<p>ait unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td style="text-align: center;">BUS</td> </tr> </table> <p>ait unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

8	<p>app unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>app unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
7	<p>aed unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>aed unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
6	<p>hfe unit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>hfe unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
5	<p>scr unit Clock Gating Disable 2</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>scr unit Clock Gating Disable Control:</p> <p>'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)</p> <p>'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

4	scr unit Clock Gating Disable 1	
	Access:	R/W
	_Custom_GTIReset:	BUS
	scr unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
3	scr unit Clock Gating Disable 0	
	Access:	R/W
	_Custom_GTIReset:	BUS
	scr unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
2	scr unit Clock Gating Disable 3	
	Access:	R/W
	_Custom_GTIReset:	BUS
	scr unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	
1	Reserved	
	Access:	RO
	Format:	MBZ
0	kin unit Clock Gating Disable	
	Access:	R/W
	_Custom_GTIReset:	BUS
	kin unit Clock Gating Disable Control:	
	'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)	
	'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)	



Vdbox unit Level Clock Gating override during rstflow

VDMISCCP3F20 - Vdbox unit Level Clock Gating override during rstflow								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
Address:	1C3F20h-1C3F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX0							
Address:	1C7F20h-1C7F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX1							
Address:	1D3F20h-1D3F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX2							
Address:	1D7F20h-1D7F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX3							
Address:	1E3F20h-1E3F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX4							
Address:	1E7F20h-1E7F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX5							
Address:	1F3F20h-1F3F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX6							
Address:	1F7F20h-1F7F23h							
Name:	Vdbox registers9							
ShortName:	VDMISCCP3F20_VDBOX7							
Unit Level Clock Gating Disable bits								
DWord	Bit	Description						
0	31:0	ECO Spare Bits <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Access:</td> <td style="text-align: center;">R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td style="text-align: center;">BUS</td> </tr> <tr> <td colspan="2">Reserved</td> </tr> </table>	Access:	R/W	_Custom_GTIReset:	BUS	Reserved	
Access:	R/W							
_Custom_GTIReset:	BUS							
Reserved								

VDENC current encoded bitstream quality

CUR_ENC_BITS_QUALITY - VDENC current encoded bitstream quality		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	128	
_Custom_GTIReset:	BUS	
Address:	1C2D80h-1C2D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG0	
Address:	1C6D80h-1C6D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG1	
Address:	1D2D80h-1D2D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG2	
Address:	1D6D80h-1D6D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG3	
Address:	1E2D80h-1E2D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG4	
Address:	1E6D80h-1E6D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG5	
Address:	1F2D80h-1F2D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG6	
Address:	1F6D80h-1F6D8Fh	
Name:	Current Encoded bitstream quality for LCU rows	
ShortName:	CUR_ENC_BITS_QUALITY_VDENC_REG7	
Current frame row quality. Each bit in this register indicates the quality of current encoded bitstream. This is the status information derived based on Maximum QP used for any CU in the LCU row.		
DWord	Bit	Description
0	31:0	Current encoded bitstream quality vector
Access:		RO

CUR_ENC_BITS_QUALITY - VDENC current encoded bitstream quality				
		<p>This register indicates the quality of current frame for 32 consecutive LCU rows starting from LCU row 0.</p>		
1	31:0	<p>Current encoded bitstream quality vector</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register indicates the quality of current frame for 32 consecutive LCU rows starting from LCU row 32.</p>	Access:	RO
Access:	RO			
2	31:0	<p>Current encoded bitstream quality vector</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register indicates the quality of current frame for 32 consecutive LCU rows starting from LCU row 64.</p>	Access:	RO
Access:	RO			
3	31:0	<p>Current encoded bitstream quality vector</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This register indicates the quality of current frame for 32 consecutive LCU rows starting from LCU row 96.</p>	Access:	RO
Access:	RO			

VDENC FPAK Tile completion message

VDENC_FPAK_TILE_CMPL_MSG - VDENC FPAK Tile completion message		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	1C2D98h-1C2D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG0	
Address:	1C6D98h-1C6D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG1	
Address:	1D2D98h-1D2D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG2	
Address:	1D6D98h-1D6D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG3	
Address:	1E2D98h-1E2D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG4	
Address:	1E6D98h-1E6D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG5	
Address:	1F2D98h-1F2D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG6	
Address:	1F6D98h-1F6D9Bh	
Name:	VDENC FPAK Tile Completion message	
ShortName:	VDENC_FPAK_TILE_CMPL_MSG_VDENC_REG7	
A write to this register with a value of 1 would result in head pointer update to Display .		
DWord	Bit	Description
0	31:1	Frame num and time num for FPAK
		Access: R/W Hardware Clear
0	0	Tile completion Msg to FPAK
		Access: R/W Hardware Clear

VDENC_FPAK_TILE_CMPL_MSG - VDENC FPAK Tile completion message

Value	Name	Description										
1		<p>A write with 1 would result in Tile completion message to FPAK. Reading this register would result in zero.</p> <p>Tile completion message happens through config write to address 2005_0530 for session id 0 and config write to address 2005_0630 for session id 1.</p> <p>The data for the tile completion message uses the following format.</p> <table border="1" style="margin-left: 20px;"> <tr> <td style="text-align: center;">31:15</td> <td>Zeros</td> </tr> <tr> <td style="text-align: center;">14:9</td> <td>Tile Number</td> </tr> <tr> <td style="text-align: center;">8:5</td> <td>Frame number</td> </tr> <tr> <td style="text-align: center;">4</td> <td>Reserved</td> </tr> <tr> <td style="text-align: center;">3:0</td> <td>Opcode 0001 - Tail pointer update 1000 - Start of frame indicator</td> </tr> </table>	31:15	Zeros	14:9	Tile Number	8:5	Frame number	4	Reserved	3:0	Opcode 0001 - Tail pointer update 1000 - Start of frame indicator
31:15	Zeros											
14:9	Tile Number											
8:5	Frame number											
4	Reserved											
3:0	Opcode 0001 - Tail pointer update 1000 - Start of frame indicator											
0	[Default]	A write with 0 is ignored.										

VDENC X_Y_POS

VDENC X_Y_POS - VDENC X_Y_POS				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
_Custom_GTIReset:	BUS			
Address:	1C2DA8h-1C2DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG0			
Address:	1C6DA8h-1C6DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG1			
Address:	1D2DA8h-1D2DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG2			
Address:	1D6DA8h-1D6DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG3			
Address:	1E2DA8h-1E2DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG4			
Address:	1E6DA8h-1E6DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG5			
Address:	1F2DA8h-1F2DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG6			
Address:	1F6DA8h-1F6DABh			
Name:	VDENC X_Y_POS			
ShortName:	VDENC_X_Y_POS_VDENC_REG7			
<p>This register is used to indicate the VDENC processed X and Y position. This change was introduced for Streamin buffer implementation for fulsim to detect till what point VDENC has processed the data.</p>				
DWord	Bit	Description		
0	31:8	vdenc_x_pos_map <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="text-align: center;">RO</td> </tr> </table>	Access:	RO
	Access:	RO		
7:0	vdenc_y_pos <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;">Access:</td> <td style="text-align: center;">RO</td> </tr> </table>	Access:	RO	
Access:	RO			



VDMBDFBARKVM

VDMBDFBARKVM - VDMBDFBARKVM		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SOC_Consumer:	BIOS	
Address:	101070h	
Allows indirection of KVM traffic for manageability.		
DWord	Bit	Description
0	31:19	Reserved
		Access: RO
		Format: MBZ
	18:16	BARNUM
		Default Value: 111b
Access: R/W		
_Custom_GTIReset: BUS Indicates to which base address register VDM packets should be addressed.		
15:8	BUSNUM	
	Default Value: 00000000b	
	Access: R/W	
	_Custom_GTIReset: BUS Indicates to which bus number VDM packets should be addressed.	
7:3	DEVNUM	
	Default Value: 10110b	
	Access: R/W	
	_Custom_GTIReset: BUS Indicates to which Device number VDM packets should be addressed.	
2:0	FUNNUM	
	Default Value: 000b	
	Access: R/W	
	_Custom_GTIReset: BUS Indicates to which Function number VDM packets should be addressed.	

VEBOX TLB Invalidation Register

VE_TLB_INV_CR - VEBOX TLB Invalidation Register				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	0CEE0h			
DWord	Bit	Description		
0	31:16	Mask Bits		
		Default Value:	0000000000000000b	
		Access:	R/W	
		_Custom_GTIRreset:	DEV	
	15:4	Reserved		
		Access:	RO	
	3	3	Invalidate VEBox TLBs bit3	
			Default Value:	0b
			Access:	R/W
		_Custom_GTIRreset:	DEV	
	SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxes. These bits self clear.			
	2	2	Invalidate VEBox TLBs bit2	
Default Value:			0b	
Access:			R/W	
_Custom_GTIRreset:		DEV		
SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxes. These bits self clear.				
1	1	Invalidate VEBox TLBs bit1		
		Default Value:	0b	
		Access:	R/W	
	_Custom_GTIRreset:	DEV		
SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the				

VE_TLB_INV_CR - VEBOX TLB Invalidation Register

		<p>corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxes. These bits self clear.</p>	
0	Invalidate VEBox TLBs bit0		
	Default Value:	0b	
	Access:	R/W	
	_Custom_GTIRreset:	DEV	
	<p>SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxes. These bits self clear.</p>		

Vebox unit Level Clock Gating Control 3F04

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	1CBF04h-1CBF07h		
Name:	VEbox registers		
ShortName:	VECGCTL3F04_VEBOX0		
Address:	1DBF04h-1DBF07h		
Name:	VEbox registers		
ShortName:	VECGCTL3F04_VEBOX1		
Address:	1EBF04h-1EBF07h		
Name:	VEbox registers		
ShortName:	VECGCTL3F04_VEBOX2		
Address:	1FBF04h-1FBF07h		
Name:	VEbox registers		
ShortName:	VECGCTL3F04_VEBOX3		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:24	Reserved	
		Access:	RO
		Format:	MBZ
	23	ramdftunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	ramdftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	22	cg3ddis_spare2 Clock Gating Disable	
		Access:	R/W
		_Custom_GTIReset:	BUS
	cg3ddis_spare2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	21	cg3ddis_spare1 Clock Gating Disable	
Access:		R/W	
_Custom_GTIReset:		BUS	

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		<p>cg3ddis_spare1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	
20	MCRunit Clock Gating Disable	Default Value:	1b
		Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>MCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
19	VFWunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>VFWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
18	VEOunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
17	ECSunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>ECSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		
16	VDNunit Clock Gating Disable	Access:	R/W
		_Custom_GTIRreset:	BUS
	<p>VDNunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

15	<p>VDMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
14	<p>VDIunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
13	<p>VCWunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
12	<p>VCUSunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>VCUSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
11	<p>SFXunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				
10	<p>SFOunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)</p>	Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W				
_Custom_GTIRreset:	BUS				

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	9	SFMunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	8	SFlunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SFlunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	7	SFEunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	6	SFDunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SFDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	5	SFAunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	4	NOAunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		NOAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for	

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	3	IECPunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	2	GCPunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	1	GAVARBunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		GAVARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	
	0	GAVunit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
		GAVunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	



Vebox unit Level Clock Gating Control 3F08

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	1CBF08h-1CBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX0		
Address:	1DBF08h-1DBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX1		
Address:	1EBF08h-1EBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX2		
Address:	1FBF08h-1FBF0Bh		
Name:	VEbox registers		
ShortName:	VECGCTL3F08_VEBOX3		
Unit Level Clock Gating Disable bits			
DWord	Bit	Description	
0	31:8	Reserved	
		Access:	RO
		Format:	MBZ
	7	VEUnit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	VEUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	6	VDUnit Clock Gating Disable	
		Access:	R/W
		_Custom_GTIRreset:	BUS
	VDUnit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)		
	5	VCWUnit Clock Gating Disable	
Access:		R/W	
_Custom_GTIRreset:		BUS	

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08

		<p>VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>					
4		<p>SFMunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
3		<p>SFEunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
2		<p>SFDunits Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFDunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
1		<p>SFAunit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						
0		<p>IECPuit Clock Gating Disable</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%;">R/W</td> </tr> <tr> <td>_Custom_GTIRreset:</td> <td>BUS</td> </tr> </table> <p>IECPuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)</p>		Access:	R/W	_Custom_GTIRreset:	BUS
Access:	R/W						
_Custom_GTIRreset:	BUS						



Vebox unit Level Clock Gating override during rstflow

VEMISCCP3F10 - Vebox unit Level Clock Gating override during rstflow				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
Address:	03F10h			
Unit Level Clock Gating Disable bits				
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	miscp Clock Gating Disable during rstflow		
		Default Value:	1b	
		Access:	R/W	
		_Custom_GTIReset:	BUS	
miscp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Randomizing this bit will result in X flush not completing during the simulation				

VECS CSB

VECS_CSB - VECS CSB				
Register Space:	MMIO: 0/2/0			
Size (in bits):	32			
SW reads this offset to read the CSB entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64 bit entry. The second read pops the entry off the CSB fifo.				
DWord	Bit	Description		
0	31:0	Context Status Buffer DW <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">RO</td> </tr> </table> <p>This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.</p>	Access:	RO
Access:	RO			



VECS CSB Fifo Status Register

VECS_CS_B_FSR - VECS CSB Fifo Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This RO register holds status of the CSB fifo		
DWord	Bit	Description
0	31	Not Empty Access: RO
	30:16	Reserved Access: RO
		Format: MBZ
	15:8	Fifo Maximum Occupancy Count This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
7:0	FIFO Occupancy Count Access: RO	

Vendor Identification

VID2_0_2_0_PCI - Vendor Identification								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	00000h							
This register combined with the Device Identification register uniquely identifies any PCI device.								
DWord	Bit	Description						
0	15:0	Vendor Identification Number <table border="1"> <tr> <td>Default Value:</td> <td>1000000010000110b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> PCI standard identification for Intel.	Default Value:	1000000010000110b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	1000000010000110b							
Access:	RO							
_Custom_GTIReset:	BUS							



VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA054h	
ShortName:	VEO_CURRENT0_XY_01	
Address:	1DA054h	
ShortName:	VEO_CURRENT0_XY_02	
Address:	1EA054h	
ShortName:	VEO_CURRENT0_XY_03	
Address:	1FA054h	
ShortName:	VEO_CURRENT0_XY_04	
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
	Format: MBZ	
	29:16	Current Input Pipe 0 X
		Default Value: 0h
	15	Reserved
		Access: RO
		Format: MBZ
14:0	Current Input Pipe 0 Y	
	Default Value: 0h	

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA04Ch	
ShortName:	VEO_DN0_XY_01	
Address:	1DA04Ch	
ShortName:	VEO_DN0_XY_02	
Address:	1EA04Ch	
ShortName:	VEO_DN0_XY_03	
Address:	1FA04Ch	
ShortName:	VEO_DN0_XY_04	
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
	Format: MBZ	
	29:16	DN Pipe 0 X
Default Value: 0h dn_input_x[13:0]		
15	Reserved	
	Access: RO	
Format: MBZ		
14:0	DN Pipe 0 Y	
	Default Value: 0h dn_input_y[14:0]	



VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA050h	
ShortName:	VEO_DN1_XY_01	
Address:	1DA050h	
ShortName:	VEO_DN1_XY_02	
Address:	1EA050h	
ShortName:	VEO_DN1_XY_03	
Address:	1FA050h	
ShortName:	VEO_DN1_XY_04	
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
	Format: MBZ	
	29:16	DN Pipe 1 X
		Default Value: 0h
	15	Reserved
		Access: RO
	Format: MBZ	
14:0	DN Pipe 1 Y	
	Default Value: 0h	

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA044h	
ShortName:	VEO_DV_COUNT_01	
Address:	1DA044h	
ShortName:	VEO_DV_COUNT_02	
Address:	1EA044h	
ShortName:	VEO_DV_COUNT_03	
Address:	1FA044h	
ShortName:	VEO_DV_COUNT_04	
DWord	Bit	Description
0	31:24	Pipe1 Motion History DV/Hold Maxcount Default Value: 0h
	23:16	Pipe1 Pixel History DV/Hold Maxcount Default Value: 0h
	15:8	Pipe0 Motion History DV/Hold Maxcount Default Value: 0h
	7:0	Pipe0 Pixel History DV/Hold Maxcount Default Value: 0h



VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	1CA05Ch			
ShortName:	VEO_DVHOLD_01			
Address:	1DA05Ch			
ShortName:	VEO_DVHOLD_02			
Address:	1EA05Ch			
ShortName:	VEO_DVHOLD_03			
Address:	1FA05Ch			
ShortName:	VEO_DVHOLD_04			
Datavalid/Hold signals for VEO interface				
DWord	Bit	Description		
0	31	vdn_p0_veo_pixel_dv <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
	30	veo_vdn_p0_pixel_hold <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
	29	vdn_p0_veo_mh_dv <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
	28	veo_vdn_p0_mh_hold <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
	27	vdn_p0_veo_bne_luma_dv <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h
	Default Value:	0h		
26	veo_vdn_p0_bne_luma_hold <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h	
Default Value:	0h			
25	vdn_p0_veo_bne_chroma_dv <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h	
Default Value:	0h			
24	veo_vdn_p0_bne_chroma_hold <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h	
Default Value:	0h			
23	vdi_p0_veo_pixel_dv <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h	
Default Value:	0h			
22	veo_vdi_p0_pixel_hold <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%; text-align: center;">0h</td> </tr> </table>	Default Value:	0h	
Default Value:	0h			

VEO_DVHOLD - VEO DV Hold Register

	21	vdi_p0_veo_stmm_dv	Default Value:	0h
	20	veo_vdi_p0_stmm_hold	Default Value:	0h
	19	vdi_p0_veo_fmd_dv	Default Value:	0h
	18	veo_vdi_p0_fmd_hold	Default Value:	0h
	17	iecp_p0_veo_dv	Default Value:	0h
	16	veo_iecp_p0_hold	Default Value:	0h
	15	vdn_p1_veo_pixel_dv	Default Value:	0h
	14	veo_vdn_p1_pixel_hold	Default Value:	0h
	13	vdn_p1_veo_mh_dv	Default Value:	0h
	12	veo_vdn_p1_mh_hold	Default Value:	0h
	11	vdn_p1_veo_bne_luma_dv	Default Value:	0h
	10	veo_vdn_p1_bne_luma_hold	Default Value:	0h
	9	vdn_p1_veo_bne_chroma_dv	Default Value:	0h
	8	veo_vdn_p1_bne_chroma_hold	Default Value:	0h
	7	vdi_p1_veo_pixel_dv	Default Value:	0h
	6	veo_vdi_p1_pixel_hold	Default Value:	0h
5	vdi_p1_veo_stmm_dv	Default Value:	0h	
4	veo_vdi_p1_stmm_hold	Default Value:	0h	

VEO_DVHOLD - VEO DV Hold Register		
	3	vdi_p1_veo_fmd_dv Default Value: 0h
	2	veo_vdi_p1_fmd_hold Default Value: 0h
	1	iecp_p1_veo_dv Default Value: 0h
	0	veo_iecp_p1_hold Default Value: 0h

VEO IECP DV Count Register

VEO_IECP_DV_COUNT - VEO IECP DV Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA048h	
ShortName:	VEO_IECP_DV_COUNT_01	
Address:	1DA048h	
ShortName:	VEO_IECP_DV_COUNT_02	
Address:	1EA048h	
ShortName:	VEO_IECP_DV_COUNT_03	
Address:	1FA048h	
ShortName:	VEO_IECP_DV_COUNT_04	
DWord	Bit	Description
0	31:24	IECP DV/Hold Maxcount Default Value: 0h
	23:16	DI/FMD DV/Hold Maxcount Default Value: 0h
	15:8	DI/STMM DV/Hold Maxcount Default Value: 0h
	7:0	DI Pixel DV/Hold Maxcount Default Value: 0h



VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA058h	
ShortName:	VEO_PREVIOUS0_XY_01	
Address:	1DA058h	
ShortName:	VEO_PREVIOUS0_XY_02	
Address:	1EA058h	
ShortName:	VEO_PREVIOUS0_XY_03	
Address:	1FA058h	
ShortName:	VEO_PREVIOUS0_XY_04	
DWord	Bit	Description
0	31:30	Reserved
		Access: RO
		Format: MBZ
	29:16	Previous Input Pipe 0 X
		Default Value: 0h
	15	Reserved
		Access: RO
		Format: MBZ
14:0	Previous Input Pipe 0 Y	
	Default Value: 0h	

VEO State Register

VEO_STATE - VEO State Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA040h	
ShortName:	VEO_STATE_01	
Address:	1DA040h	
ShortName:	VEO_STATE_02	
Address:	1EA040h	
ShortName:	VEO_STATE_03	
Address:	1FA040h	
ShortName:	VEO_STATE_04	
Data valids and holds for the statistics interface		
DWord	Bit	Description
0	31	iecp_p0_veo_his_dv Default Value: 0h
	30	iecp_p0_veo_skin_dv Default Value: 0h
	29	iecp_p0_veo_rgb_his_dv Default Value: 0h
	28	iecp_p0_veo_out_dist_dv Default Value: 0h
	27	iecp_p1_veo_his_dv Default Value: 0h
	26	iecp_p1_veo_skin_dv Default Value: 0h
	25	iecp_p1_veo_out_dist_dv Default Value: 0h
	24	veo_iecp_p0_rgb_his_hold Default Value: 0h
	23	Reserved Access: RO Format: MBZ

VEO_STATE - VEO State Register	
22:19	VSC_FSM_State Default Value: 0h State of the VEO_VSC_CNTRL state machine
	GAV Command Credit Count Default Value: 4h
	GAV Data Credit Count Default Value: 8h
	Reserved Access: RO Format: MBZ
	GAV Stall Clk Cnt Max Default Value: 0h The longest stall from GAV since the beginning of the frame.

VE SFC Forced Lock Acknowledgement Register

VE_SFC_FORCED_LOCK_ACK - VE SFC Forced Lock Acknowledgement Register				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	1CA018h			
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS0			
Address:	1DA018h			
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS1			
Address:	1EA018h			
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS2			
Address:	1FA018h			
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS3			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	VE_SFC_FORCED_LOCK_ACK		
		<table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that VE has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert VE_SFC_Forced_Lock as well.</p>	Format:	U1
Format:	U1			



VE SFC Forced Lock Register

VE_SFC_FORCED_LOCK - VE SFC Forced Lock Register				
Register Space:	MMIO: 0/2/0			
Access:	WO			
Size (in bits):	32			
Address:	1CA01Ch			
ShortName:	VE_SFC_FORCED_LOCK_01			
Address:	1DA01Ch			
ShortName:	VE_SFC_FORCED_LOCK_02			
Address:	1EA01Ch			
ShortName:	VE_SFC_FORCED_LOCK_03			
Address:	1FA01Ch			
ShortName:	VE_SFC_FORCED_LOCK_04			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	VE_SFC_FORCED_LOCK		
		<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells VEBox that a software reset is going to happen. VE then issues a forced lock to SFC. If SFC is currently locked to VE, SFC should not unlock itself from VE. If SFC is NOT currently locked to VE, SFC should not accept the lock request from VE. Driver needs to clear this bit after the software reset sequence is complete.</p>	Format:	U1
Format:	U1			

VE VFW SFC Usage Register

VE_SFC_USAGE - VE VFW SFC Usage Register				
Register Space:	MMIO: 0/2/0			
Access:	RO			
Size (in bits):	32			
Address:	1CA014h			
ShortName:	VE_SFC_USAGE_VECS0			
Address:	1DA014h			
ShortName:	VE_SFC_USAGE_VECS1			
Address:	1EA014h			
ShortName:	VE_SFC_USAGE_VECS2			
Address:	1FA014h			
ShortName:	VE_SFC_USAGE_VECS3			
DWord	Bit	Description		
0	31:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	VE_SFC_USAGE		
		<table border="1"> <tr> <td>Format:</td> <td>U1</td> </tr> </table> <p>This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to VE. This bit should be set after SFC accepts the lock request from VE. This bit should be clear once SFC finishes the workload and unlocked from VEBox. In case a reset happens on MFX, this bit must be reset once a new workload is received</p>	Format:	U1
Format:	U1			



VF_CAPABILITY_REGISTER

VF_CAP_REG - VF_CAPABILITY_REGISTER						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
SOC_Consumer:	BIOS					
Address:	1901F8h					
This register is used to communicate information about the VF to the VM Drivers. The same offset (0x1901F8) is used for all VF and the PF.						
DWord	Bit	Description				
0	31:1	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
0	0	Virtual Function				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table>	Access:	RO	_Custom_GTIReset:	BUS
		Access:	RO			
		_Custom_GTIReset:	BUS			
<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Physical Function [Default]</td> </tr> <tr> <td>1b</td> <td>Virtual Function</td> </tr> </tbody> </table>	Value	Name	0b	Physical Function [Default]	1b	Virtual Function
Value	Name					
0b	Physical Function [Default]					
1b	Virtual Function					

VF_SW_FLAG

VF_SW_FLAG								
Register Space:	MMIO: 0/2/0							
Size (in bits):	32							
SOC_Consumer:	BIOS							
Address:	190240h							
Name:	VF_SW_FLAG_0							
ShortName:	VF_SW_FLAG_0							
Address:	190244h							
Name:	VF_SW_FLAG_1							
ShortName:	VF_SW_FLAG_1							
Address:	190248h							
Name:	VF_SW_FLAG_2							
ShortName:	VF_SW_FLAG_2							
Address:	19024Ch							
Name:	VF_SW_FLAG_3							
ShortName:	VF_SW_FLAG_3							
Each Virtual Function has 4x32bit Software Flag registers, which can be used as scratch registers.								
DWord	Bit	Description						
0	31:0	<p>Data</p> <table border="1"> <tr> <td>Default Value:</td> <td>00000000h</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>The format of this register is defined by Software.</p>	Default Value:	00000000h	Access:	R/W	_Custom_GTIReset:	BUS
Default Value:	00000000h							
Access:	R/W							
_Custom_GTIReset:	BUS							



VF BAR0 LDW

VF_BAR0_LDW_0_2_0_PCI - VF BAR0 LDW			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00344h		
Lower DW of the BAR that defines the base Host Physical Address (HPA) of GTTMMADR for all VFs. The HPA of the GTTMMADR for Virtual Function n = VF GTTMMADDR (Upper and Lower DW) + (n - 1) * (16MB * num Tiles)			
DWord	Bit	Description	
0	31:24	VF GTTMMADDR Lower DW	
		Default Value:	00000000b
		Access:	R/W
		Mask:	VF GTTMMADDR Lower DW Mask
		Format:	PhysicalAddress[31:24]
		_Custom_GTIReset:	BUS
			VF GTTMMADDR Lower DW
	23:4	VF GTTMMADDR Lower DW Mask	
		Default Value:	000000000000000000000000b
		Access:	RO
		_Custom_GTIReset:	BUS
			VF GTTMMADDR Lower DW Mask
	3	Prefetchable	
		Default Value:	0b
		Access:	RO
		_Custom_GTIReset:	BUS
		Prefetchable	
2:1	Type		
	Default Value:	10b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
		Type. Value 10 indicates 64 bit BAR	

VF_BAR0_LDW_0_2_0_PCI - VF BAR0 LDW								
	0	Memory Space Indicator <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 80%;">Default Value:</td> <td style="width: 20%;">0b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Memory space Indicator. Value 0 indicates memory space.</p>	Default Value:	0b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	0b							
Access:	RO							
_Custom_GTIReset:	BUS							



VF BAR0 UDW

VF_BAR0_UDW_0_2_0_PCI - VF BAR0 UDW										
Register Space:	PCI: 0/2/0									
Size (in bits):	32									
Address:	00348h									
Upper DW of the BAR that defines the base Host Physical Address of the GTTMMADR for all VFs										
DWord	Bit	Description								
0	31:0	VF GTTMMADDR Upper DWord <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>GraphicsAddress[63:32]</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> VF GTTMMADDR Upper DW	Default Value:	00000000000000000000000000000000b	Access:	R/W	Format:	GraphicsAddress[63:32]	_Custom_GTIReset:	BUS
Default Value:	00000000000000000000000000000000b									
Access:	R/W									
Format:	GraphicsAddress[63:32]									
_Custom_GTIReset:	BUS									

VF BAR1 LDW

VF_BAR1_LDW_0_2_0_PCI - VF BAR1 LDW			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	0034Ch		
Lower DW of the BAR that defines the base Host Physical Address of GMADR for all VFs.			
DWord	Bit	Description	
0	31:29	VF GMADDR Lower DW	
		Default Value:	000b
		Access:	R/W
		Mask:	VF GMADDR Lower DW Mask
		Format:	PhysicalAddress[31:29]
		_Custom_GTIRreset:	BUS
			VF GMADDR Lower DW
	28:4	VF GMADDR Lower DW Mask	
		Default Value:	00000000000000000000b
		Access:	RO
		_Custom_GTIRreset:	BUS
			VF GMADDR Lower DW Mask
	3	Prefetchable	
		Default Value:	1b
		Access:	RO
		_Custom_GTIRreset:	BUS
			Prefetchable
	2:1	Type	
		Default Value:	10b
		Access:	RO
_Custom_GTIRreset:		BUS	
		Type. Value 10 indicates 64 bit BAR	
0	Memory Space Indicator		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIRreset:	BUS	
		Memory space Indicator. Value 0 indicates memory space.	



VF BAR1 UDW

VF_BAR1_UDW_0_2_0_PCI - VF BAR1 UDW										
Register Space:	PCI: 0/2/0									
Size (in bits):	32									
Address:	00350h									
Upper DW of the BAR that defines the base Host Physical Address of GMADR for all VFs										
DWord	Bit	Description								
0	31:0	VF GMADDR Upper DWord <table border="1"> <tr> <td>Default Value:</td> <td>00000000000000000000000000000000b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> <tr> <td>Format:</td> <td>PhysicalAddress[63:32]</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> VF GMADDR Upper DW	Default Value:	00000000000000000000000000000000b	Access:	R/W	Format:	PhysicalAddress[63:32]	_Custom_GTIReset:	BUS
Default Value:	00000000000000000000000000000000b									
Access:	R/W									
Format:	PhysicalAddress[63:32]									
_Custom_GTIReset:	BUS									

VF BAR2 LDW

VF_BAR2_LDW_0_2_0_PCI - VF BAR2 LDW			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00354h		
Lower DW of Unused BAR			
DWord	Bit	Description	
0	31:0	Reserved Bar	
		Default Value:	00000000000000000000000000000000b
		Access:	RO
		_Custom_GTIReset:	BUS
		Reserved	



VF BAR2 UDW

VF_BAR2_UDW_0_2_0_PCI - VF BAR2 UDW		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	00358h	
Upper DW of Unused BAR		
DWord	Bit	Description
0	31:0	Reserved Bar
		Default Value: 00000000000000000000000000000000b
		Access: RO
		_Custom_GTIReset: BUS
		Reserved

VF Device ID

VF_DEVICEID_0_2_0_PCI - VF Device ID												
Register Space:	PCI: 0/2/0											
Size (in bits):	16											
Address:	0033Ah											
Defines the Device ID to be used by all Virtual Functions												
DWord	Bit	Description										
0	15:0	VF DEVICE ID VALUE <table border="1"> <tr> <td>Access:</td> <td>RO Variant</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> <tr> <td colspan="2">Mirror the same device ID as the PF</td> </tr> <tr> <th>Value</th> <th>Name</th> </tr> <tr> <td>1001101001000000b</td> <td>[Default]</td> </tr> </table>	Access:	RO Variant	_Custom_GTIReset:	BUS	Mirror the same device ID as the PF		Value	Name	1001101001000000b	[Default]
Access:	RO Variant											
_Custom_GTIReset:	BUS											
Mirror the same device ID as the PF												
Value	Name											
1001101001000000b	[Default]											



VF Migration State Array Offset

VF_MIGST_OFFSET_0_2_0_PCI - VF Migration State Array Offset			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	0035Ch		
Defines offset from a PF BAR to the VF Migration State Array. VF Migration not supported in this implementation			
DWord	Bit	Description	
0	31:0	Reserved bits	
		Default Value:	00000000000000000000000000000000b
		Access:	RO
		_Custom_GTIReset:	BUS
		Reserved	

VF Scratch Pad

VFSKPD - VF Scratch Pad										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	083A8h-083ABh									
Name:	VF Scratch Pad									
ShortName:	VFSKPD_VFUNIT									
Address:	16EA8h-16EABh									
Name:	VF Scratch Pad									
ShortName:	VFSKPD_VFRUNIT									
DWord	Bit	Description								
0	31:16	Mask								
		Access:	WO							
		Format:	Mask							
		_Custom_GTIReset:	DEV							
	Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)									
	15	Reserved								
		Access:	RO							
	14	Reserved								
		Access:	R/W							
		Format:	PBC							
	13	Mid Object Preemption Topology Fix Disable								
		Access:	R/W							
Format:		Disable								
12	Index Buffer Fetch Enhancement Disable									
	Access:	R/W								
	Format:	Disable								
	<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>VF replay topology fix is enabled - VF will output correct topology after Object Level Pre-emption.</td> </tr> <tr> <td>1h</td> <td></td> <td>VF replay topology fix is disabled</td> </tr> </tbody> </table>		Value	Name	Description	0h	Enable [Default]	VF replay topology fix is enabled - VF will output correct topology after Object Level Pre-emption.	1h	
Value	Name	Description								
0h	Enable [Default]	VF replay topology fix is enabled - VF will output correct topology after Object Level Pre-emption.								
1h		VF replay topology fix is disabled								

VFSKPD - VF Scratch Pad

		DEV									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>The index buffer fetch enhancement is enabled. If the number of vertex per instance is less than the index buffer depth, VF will only fetch the indices from the index buffer on the first instance. All other instances will re-use the indices stored in the index buffer.</td> </tr> <tr> <td>1h</td> <td></td> <td>The index fetch enhancement is disabled. All indices are always fetched.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	The index buffer fetch enhancement is enabled. If the number of vertex per instance is less than the index buffer depth, VF will only fetch the indices from the index buffer on the first instance. All other instances will re-use the indices stored in the index buffer.	1h		The index fetch enhancement is disabled. All indices are always fetched.	
Value	Name	Description									
0h	Enable [Default]	The index buffer fetch enhancement is enabled. If the number of vertex per instance is less than the index buffer depth, VF will only fetch the indices from the index buffer on the first instance. All other instances will re-use the indices stored in the index buffer.									
1h		The index fetch enhancement is disabled. All indices are always fetched.									
11	POLYGON PrimitiveID Fix Disable										
	Access:	R/W									
	Format:	Disable									
	_Custom_GTIReset:	DEV									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>PrimitiveID is constant across all triangles of a POLYGON.</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>PrimitiveID is incremented for each triangle of a POLYGON.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	PrimitiveID is constant across all triangles of a POLYGON.	1h	Disable	PrimitiveID is incremented for each triangle of a POLYGON.	
Value	Name	Description									
0h	Enable [Default]	PrimitiveID is constant across all triangles of a POLYGON.									
1h	Disable	PrimitiveID is incremented for each triangle of a POLYGON.									
10	VF POSH Starvation Disable										
	Access:	R/W									
	Format:	Disable									
	_Custom_GTIReset:	DEV									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>The VF will inform OVR when it is starved for POSH token data.</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>The VF will not inform OVR when it is starved for POSH token data.</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	The VF will inform OVR when it is starved for POSH token data.	1h	Disable	The VF will not inform OVR when it is starved for POSH token data.	
Value	Name	Description									
0h	Enable [Default]	The VF will inform OVR when it is starved for POSH token data.									
1h	Disable	The VF will not inform OVR when it is starved for POSH token data.									
9	Partial Autostrip Disable										
	Access:	R/W									
	Format:	Disable									
	_Custom_GTIReset:	DEV									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 75%;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Enable [Default]</td> <td>The VF can generate "partial autostrip" primitives from TRILIST inputs (if/when possible).</td> </tr> <tr> <td>1h</td> <td>Disable</td> <td>VF will not generate "partial autostrip" primitives</td> </tr> </tbody> </table>	Value	Name	Description	0h	Enable [Default]	The VF can generate "partial autostrip" primitives from TRILIST inputs (if/when possible).	1h	Disable	VF will not generate "partial autostrip" primitives	
Value	Name	Description									
0h	Enable [Default]	The VF can generate "partial autostrip" primitives from TRILIST inputs (if/when possible).									
1h	Disable	VF will not generate "partial autostrip" primitives									
8	Reserved										
	Access:	R/W									
	Format:	PBC									
	_Custom_GTIReset:	DEV									

VFSKPD - VF Scratch Pad

7	Reserved	
	Access:	R/W
	Format:	PBC
	_Custom_GTIRreset:	DEV
6	Autostrip Disable	
	Access:	R/W
	Format:	U1
	_Custom_GTIRreset:	DEV
	Value	Name
	Description	
	0h	Enable [Default]
		The VF can generate "autostrip" primitives from TRILIST inputs (if/when possible).
	1h	Disable
		VF will not generate "autostrip" primitives.
5	TLB Prefetch Enable	
	Access:	R/W
	Format:	U1
	_Custom_GTIRreset:	DEV
	Value	Name
	Description	
	0h	Disable [Default]
		The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
	1h	Enable
		VF will disable prefetch of TLB entries.
4	4th Vertex Data Pipe Disable	
	Access:	R/W
	Format:	Disable
	_Custom_GTIRreset:	DEV
	Value	Name
	Description	
	0h	[Default]
		The 4th Vertex Data Pipe is enabled.
	1h	
		The 4th Vertex Data Pipe is disabled.
	Programming Notes	
	This is only valid when there are 3 or more vertex data pipes.	
3	Nullprim early credit release disable	
	Access:	R/W
	_Custom_GTIRreset:	DEV

VFSKPD - VF Scratch Pad

	Value	Name	Description
	0h	[Default]	The nullprim credit release will be returned to csunit when the upper pipe of vfunit is empty.
	1h		The nullprim credit release will be returned to csunit when the upper pipe and the lower pipe of vfunit are empty.
2	Vertex Cache Implicit Disable Inhibit		
	Access:		R/W
	Format:		U1
	_Custom_GTIRreset:		DEV
	Value	Name	Description
	0h	[Default]	Allow VF to disable VS0 when Sequential index or Prim ID is a valid Element.
	1h		VF never implicitly disables the vertex cache. Software must disable the VS0 Cache when required.
1	Disable Over Fetch Cache		
	Access:		R/W
	_Custom_GTIRreset:		DEV
	Value	Name	Description
	0h	[Default]	Cache will check for data in cache before making a request to memory
	1h		Always re-fetch new data from memory.
Programming Notes			
Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.			
0	Disable Multiple Miss Read squash		
	Access:		R/W
	Format:		Disable
	_Custom_GTIRreset:		DEV
	Value	Name	Description
	0h	[Default]	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
	1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

VF Stride

VF_STRIDE_0_2_0_PCI - VF Stride								
Register Space:	PCI: 0/2/0							
Size (in bits):	16							
Address:	00336h							
Defines the stride of the function number from one VF to the next.								
DWord	Bit	Description						
0	15:0	<p>VF STRIDE VALUE</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>0000000000000001b</td> </tr> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>_Custom_GTIReset:</td> <td>BUS</td> </tr> </table> <p>Defines the Routing ID offset from one VF to the next one for all VFs associated with the PF that contains this Capability structure. The next VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the current VF, ignoring any carry, using unsigned 16-bit arithmetic. The value of this field is hardwired to 0001h.</p>	Default Value:	0000000000000001b	Access:	RO	_Custom_GTIReset:	BUS
Default Value:	0000000000000001b							
Access:	RO							
_Custom_GTIReset:	BUS							



VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA010h	
ShortName:	VFW_CREDIT_CNT_01	
Address:	1DA010h	
ShortName:	VFW_CREDIT_CNT_02	
Address:	1EA010h	
ShortName:	VFW_CREDIT_CNT_03	
Address:	1FA010h	
ShortName:	VFW_CREDIT_CNT_04	
DWord	Bit	Description
0	31:8	Reserved
		Access: RO
	Format: MBZ	
	7:0	Credit Count
	Default Value: 4h	
	The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.	

VGA_CONTROL

VGA_CONTROL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	41000h-41003h							
Name:	VGA Control							
ShortName:	VGA_CONTROL							
Reset:	global							
Restriction								
VGA requires panel fitting to be enabled. VGA is always connected to pipe A.VGA cannot be enabled while the display power well is powered down. VGA display should only be enabled if all display planes other than VGA are disabled.								
DWord	Bit	Description						
0	31	VGA Display Disable This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings.						
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Enable</td> </tr> <tr> <td>1b</td> <td>Disable [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Enable	1b	Disable [Default]
		Value	Name					
		0b	Enable					
1b	Disable [Default]							
Restriction								
The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.								
	30:27	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
		Access:	RO					
Format:	MBZ							
26	VGA Border Enable This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data.							
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable</td> </tr> <tr> <td>1b</td> <td>Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable
Value	Name							
0b	Disable							
1b	Enable							
	25	DBuf Clock Gate <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W				
		Access:	R/W					
The bit controls the Display buffer clocking when VGA is used. Software must set this bit to 0b before enabling VGA and set it to 1b after VGA gets disabled.								

VGA_CONTROL		
24	Pipe CSC Enable	
	This bit enables pipe color space conversion and the pipe pre-CSC gamma for the VGA pixel data.	
	Value	Name
	0b	Disable
	1b	Enable
23:21 Reserved		
	Access:	RO
	Format:	MBZ
20	Legacy 8Bit Palette En	
	This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path.	
	Value	Name
	0b	6 bit DAC
	1b	8 bit DAC
19 Reserved		
18 Reserved		
17:16 Reserved		
	Access:	RO
	Format:	MBZ
15:12 Reserved		
11:8 Reserved		
7:6	Blink Duty Cycle	
	Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.	
	Value	Name
	00b	100%
	01b	25%
10b	50%	
11b	75%	
Description		
100% Duty Cycle, Full Cursor Rate		
25% Duty Cycle, 1/2 Cursor Rate		
50% Duty Cycle, 1/2 Cursor Rate		
75% Duty Cycle, 1/2 Cursor Rate		
5:0	VSYNC Blink Rate	
	Controls the VGA blink rate in terms of the number of VSYNCS per on/off cycle.	
	Programming Notes	
Program with (VSYNCS/cycle)/2-1		

VIDEO_DIP_CTL

VIDEO_DIP_CTL								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	60200h-60203h							
Name:	Transcoder Video Data Island Packet Control							
ShortName:	VIDEO_DIP_CTL_A							
Reset:	soft							
Address:	61200h-61203h							
Name:	Transcoder Video Data Island Packet Control							
ShortName:	VIDEO_DIP_CTL_B							
Reset:	soft							
Address:	62200h-62203h							
Name:	Transcoder Video Data Island Packet Control							
ShortName:	VIDEO_DIP_CTL_C							
Reset:	soft							
Address:	63200h-63203h							
Name:	Transcoder Video Data Island Packet Control							
ShortName:	VIDEO_DIP_CTL_D							
Reset:	soft							
Each type of Video DIP will be sent once each frame while it is enabled.								
DWord	Bit	Description						
0	31:29	Reserved						
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
28		DRM DIP enable						
		<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table>	Access:	R/W				
		Access:	R/W					
		This bit enables the output of the DRM DIP.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>DRM DIP enable</td> </tr> <tr> <td>0b</td> <td>DRM DIP disable</td> </tr> </tbody> </table>	Value	Name	1b	DRM DIP enable	0b	DRM DIP disable
		Value	Name					
1b	DRM DIP enable							
0b	DRM DIP disable							
Programming Notes								
This needs to be enabled with HDMI only.								

VIDEO_DIP_CTL													
27	PSR PSR2 VSC bit 7 This bit manually sets PSR VSC bit for future specification changes.												
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Do not set</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Set</td> </tr> </tbody> </table>	Value	Name	0b	Do not set	1b	Set						
	Value	Name											
	0b	Do not set											
1b	Set												
0b	Do not set												
1b	Set												
26:25	VSC select Select between hardware and software control of the VSC DIP data and header. When hardware controls it will send PSR1 header and data values when PSR1 is enabled, and PSR2 + Y-coordinate header and data values when PSR2 is enabled. If PSR2/SU SDP without Y-coordinate is enabled SW must set the header bits of the VSC packet to the PSR2 without Y-coordinate value from the eDP standard.												
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td style="text-align: center;">Header and Data</td> <td>Hardware controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when PSR is enabled and software is not using VSC for other types of data.</td> </tr> <tr> <td style="text-align: center;">10b</td> <td style="text-align: center;">Data Only</td> <td>Software controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when software is sending data with VSC. If PSR is enabled, software must configure the header to include the PSR revision and byte count.</td> </tr> <tr> <td style="text-align: center;">11b</td> <td style="text-align: center;">None</td> <td>Software controls all headers bytes. Software controls all data bytes. Not recommended for use.</td> </tr> </tbody> </table>	Value	Name	Description	00b	Header and Data	Hardware controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when PSR is enabled and software is not using VSC for other types of data.	10b	Data Only	Software controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when software is sending data with VSC. If PSR is enabled, software must configure the header to include the PSR revision and byte count.	11b	None	Software controls all headers bytes. Software controls all data bytes. Not recommended for use.
	Value	Name	Description										
	00b	Header and Data	Hardware controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when PSR is enabled and software is not using VSC for other types of data.										
	10b	Data Only	Software controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when software is sending data with VSC. If PSR is enabled, software must configure the header to include the PSR revision and byte count.										
11b	None	Software controls all headers bytes. Software controls all data bytes. Not recommended for use.											
00b	Header and Data	Hardware controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when PSR is enabled and software is not using VSC for other types of data.											
10b	Data Only	Software controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when software is sending data with VSC. If PSR is enabled, software must configure the header to include the PSR revision and byte count.											
11b	None	Software controls all headers bytes. Software controls all data bytes. Not recommended for use.											
24	VDIP Enable PPS Access: R/W												
	This field controls enable/disable of PPS DIP. It should be enabled prior to enabling VDSC. SW should enable DSC hardware feature only after programming PPS. Hardware still sends PPS once at the beginning of enable cycle in disable PPS case. PPS DIP can only be enabled with DisplayPort.												
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable						
	Value	Name											
0b	Disable												
1b	Enable												
0b	Disable												
1b	Enable												
23:22	Reserved Access: RO												
	Format: MBZ												
21	Reserved Access: RO												
	Format: MBZ												

VIDEO_DIP_CTL							
20	VDIP Enable VSC						
	Access: R/W						
	This bit enables the output of the Video Stream Configuration DIP.						
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable VSC DIP</td> </tr> <tr> <td>1b</td> <td>Enable VSC DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable VSC DIP	1b	Enable VSC DIP
	Value	Name					
	0b	Disable VSC DIP					
	1b	Enable VSC DIP					
	Restriction						
	VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.						
	19:17	Reserved					
Access: RO							
Format: MBZ							
16	VDIP Enable GCP						
	Access: R/W						
	This bit enables the output of the General Control Packet (GCP) DIP. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP.						
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable GCP DIP</td> </tr> <tr> <td>1b</td> <td>Enable GCP DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable GCP DIP	1b	Enable GCP DIP
	Value	Name					
	0b	Disable GCP DIP					
	1b	Enable GCP DIP					
	Restriction						
	GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL						
	15:13	Reserved					
Access: RO							
Format: MBZ							
12	VDIP Enable AVI						
	Access: R/W						
	This bit enables the output of the Auxiliary Video Information DIP.						
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable AVI DIP</td> </tr> <tr> <td>1b</td> <td>Enable AVI DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable AVI DIP	1b	Enable AVI DIP
	Value	Name					
	0b	Disable AVI DIP					
1b	Enable AVI DIP						
Restriction							
Only enable with HDMI.							

VIDEO_DIP_CTL							
11:9	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
8	VDIP Enable VS						
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit enables the output of the Vendor Specific (VS) DIP.</p>	Access:	R/W				
	Access:	R/W					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable VS DIP</td> </tr> <tr> <td>1b</td> <td>Enable VS DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable VS DIP	1b	Enable VS DIP
	Value	Name					
	0b	Disable VS DIP					
1b	Enable VS DIP						
Restriction							
Only enable with HDMI.							
7:5	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
4	VDIP Enable GMP						
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit enables the output of the Gamut Metadata Packet (GMP) DIP. GMP can be enabled with either DisplayPort or HDMI.</p>	Access:	R/W				
	Access:	R/W					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable GMP DIP</td> </tr> <tr> <td>1b</td> <td>Enable GMP DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable GMP DIP	1b	Enable GMP DIP
	Value	Name					
0b	Disable GMP DIP						
1b	Enable GMP DIP						
3:1	Reserved						
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO						
Format:	MBZ						
0	VDIP Enable SPD						
	<table border="1"> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> <p>This bit enables the output of the Source Product Description (SPD) DIP.</p>	Access:	R/W				
	Access:	R/W					
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Disable SPD DIP</td> </tr> <tr> <td>1b</td> <td>Enable SPD DIP</td> </tr> </tbody> </table>	Value	Name	0b	Disable SPD DIP	1b	Enable SPD DIP
	Value	Name					
	0b	Disable SPD DIP					
1b	Enable SPD DIP						
Restriction							
Only enable with HDMI.							

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60220h-60223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_A
Reset:	soft
Address:	60224h-60227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_A
Reset:	soft
Address:	60228h-6022Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_A
Reset:	soft
Address:	6022Ch-6022Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_A
Reset:	soft
Address:	60230h-60233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_A
Reset:	soft
Address:	60234h-60237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_A
Reset:	soft
Address:	60238h-6023Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_A
Reset:	soft
Address:	6023Ch-6023Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_A



VIDEO_DIP_DATA	
Reset:	soft
Address:	60260h-60263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_A
Reset:	soft
Address:	60264h-60267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_A
Reset:	soft
Address:	60268h-6026Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_A
Reset:	soft
Address:	6026Ch-6026Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_A
Reset:	soft
Address:	60270h-60273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_A
Reset:	soft
Address:	60274h-60277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_A
Reset:	soft
Address:	60278h-6027Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_A
Reset:	soft
Address:	6027Ch-6027Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_A
Reset:	soft
Address:	602A0h-602A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_A

VIDEO_DIP_DATA	
Reset:	soft
Address:	602A4h-602A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_A
Reset:	soft
Address:	602A8h-602ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_A
Reset:	soft
Address:	602ACh-602AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_A
Reset:	soft
Address:	602B0h-602B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_A
Reset:	soft
Address:	602B4h-602B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_A
Reset:	soft
Address:	602B8h-602BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_A
Reset:	soft
Address:	602BCh-602BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_A
Reset:	soft
Address:	602E0h-602E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_A
Reset:	soft
Address:	602E4h-602E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_A



VIDEO_DIP_DATA	
Reset:	soft
Address:	602E8h-602EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_A
Reset:	soft
Address:	602ECh-602EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_A
Reset:	soft
Address:	602F0h-602F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_A
Reset:	soft
Address:	602F4h-602F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_A
Reset:	soft
Address:	602F8h-602FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_A
Reset:	soft
Address:	602FCh-602FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_A
Reset:	soft
Address:	60300h-60303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_A
Reset:	soft
Address:	60320h-60323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_A
Reset:	soft
Address:	60324h-60327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_A

VIDEO_DIP_DATA	
Reset:	soft
Address:	60328h-6032Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_A
Reset:	soft
Address:	6032Ch-6032Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_A
Reset:	soft
Address:	60330h-60333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_A
Reset:	soft
Address:	60334h-60337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_A
Reset:	soft
Address:	60338h-6033Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_A
Reset:	soft
Address:	6033Ch-6033Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_A
Reset:	soft
Address:	60340h-60343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_A
Reset:	soft
Address:	61220h-61223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_B
Reset:	soft
Address:	61224h-61227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_B



VIDEO_DIP_DATA

Reset:	soft
Address:	61228h-6122Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_B
Reset:	soft
Address:	6122Ch-6122Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_B
Reset:	soft
Address:	61230h-61233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_B
Reset:	soft
Address:	61234h-61237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_B
Reset:	soft
Address:	61238h-6123Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_B
Reset:	soft
Address:	6123Ch-6123Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_B
Reset:	soft
Address:	61260h-61263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_B
Reset:	soft
Address:	61264h-61267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_B
Reset:	soft
Address:	61268h-6126Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_B

VIDEO_DIP_DATA	
Reset:	soft
Address:	6126Ch-6126Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_B
Reset:	soft
Address:	61270h-61273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_B
Reset:	soft
Address:	61274h-61277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_B
Reset:	soft
Address:	61278h-6127Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_B
Reset:	soft
Address:	6127Ch-6127Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_B
Reset:	soft
Address:	612A0h-612A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_B
Reset:	soft
Address:	612A4h-612A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_B
Reset:	soft
Address:	612A8h-612ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_B
Reset:	soft
Address:	612ACh-612AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_B



VIDEO_DIP_DATA

Reset:	soft
Address:	612B0h-612B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_B
Reset:	soft
Address:	612B4h-612B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_B
Reset:	soft
Address:	612B8h-612BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_B
Reset:	soft
Address:	612BCh-612BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_B
Reset:	soft
Address:	612E0h-612E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_B
Reset:	soft
Address:	612E4h-612E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_B
Reset:	soft
Address:	612E8h-612EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_B
Reset:	soft
Address:	612ECh-612EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_B
Reset:	soft
Address:	612F0h-612F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_B

VIDEO_DIP_DATA	
Reset:	soft
Address:	612F4h-612F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_B
Reset:	soft
Address:	612F8h-612FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_B
Reset:	soft
Address:	612FCh-612FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_B
Reset:	soft
Address:	61300h-61303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_B
Reset:	soft
Address:	61320h-61323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_B
Reset:	soft
Address:	61324h-61327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_B
Reset:	soft
Address:	61328h-6132Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_B
Reset:	soft
Address:	6132Ch-6132Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_B
Reset:	soft
Address:	61330h-61333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_B



VIDEO_DIP_DATA

Reset:	soft
Address:	61334h-61337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_B
Reset:	soft
Address:	61338h-6133Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_B
Reset:	soft
Address:	6133Ch-6133Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_B
Reset:	soft
Address:	61340h-61343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_B
Reset:	soft
Address:	62220h-62223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_C
Reset:	soft
Address:	62224h-62227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_C
Reset:	soft
Address:	62228h-6222Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_C
Reset:	soft
Address:	6222Ch-6222Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_C
Reset:	soft
Address:	62230h-62233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_C

VIDEO_DIP_DATA	
Reset:	soft
Address:	62234h-62237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_C
Reset:	soft
Address:	62238h-6223Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_C
Reset:	soft
Address:	6223Ch-6223Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_C
Reset:	soft
Address:	62260h-62263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_C
Reset:	soft
Address:	62264h-62267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_C
Reset:	soft
Address:	62268h-6226Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_C
Reset:	soft
Address:	6226Ch-6226Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_C
Reset:	soft
Address:	62270h-62273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_C
Reset:	soft
Address:	62274h-62277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_C



VIDEO_DIP_DATA

Reset:	soft
Address:	62278h-6227Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_C
Reset:	soft
Address:	6227Ch-6227Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_C
Reset:	soft
Address:	622A0h-622A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_C
Reset:	soft
Address:	622A4h-622A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_C
Reset:	soft
Address:	622A8h-622ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_C
Reset:	soft
Address:	622ACh-622AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_C
Reset:	soft
Address:	622B0h-622B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_C
Reset:	soft
Address:	622B4h-622B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_C
Reset:	soft
Address:	622B8h-622BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_C

VIDEO_DIP_DATA	
Reset:	soft
Address:	622BCh-622BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_C
Reset:	soft
Address:	622E0h-622E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_C
Reset:	soft
Address:	622E4h-622E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_C
Reset:	soft
Address:	622E8h-622EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_C
Reset:	soft
Address:	622ECh-622EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_C
Reset:	soft
Address:	622F0h-622F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_C
Reset:	soft
Address:	622F4h-622F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_C
Reset:	soft
Address:	622F8h-622FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_C
Reset:	soft
Address:	622FCh-622FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_C



VIDEO_DIP_DATA	
Reset:	soft
Address:	62300h-62303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_C
Reset:	soft
Address:	62320h-62323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_C
Reset:	soft
Address:	62324h-62327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_C
Reset:	soft
Address:	62328h-6232Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_C
Reset:	soft
Address:	6232Ch-6232Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_C
Reset:	soft
Address:	62330h-62333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_C
Reset:	soft
Address:	62334h-62337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_C
Reset:	soft
Address:	62338h-6233Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_C
Reset:	soft
Address:	6233Ch-6233Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_C

VIDEO_DIP_DATA	
Reset:	soft
Address:	62340h-62343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_C
Reset:	soft
Address:	63220h-63223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_D
Reset:	soft
Address:	63224h-63227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_D
Reset:	soft
Address:	63228h-6322Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_D
Reset:	soft
Address:	6322Ch-6322Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_D
Reset:	soft
Address:	63230h-63233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_D
Reset:	soft
Address:	63234h-63237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_D
Reset:	soft
Address:	63238h-6323Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_D
Reset:	soft
Address:	6323Ch-6323Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_D



VIDEO_DIP_DATA	
Reset:	soft
Address:	63260h-63263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_D
Reset:	soft
Address:	63264h-63267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_D
Reset:	soft
Address:	63268h-6326Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_D
Reset:	soft
Address:	6326Ch-6326Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_D
Reset:	soft
Address:	63270h-63273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_D
Reset:	soft
Address:	63274h-63277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_D
Reset:	soft
Address:	63278h-6327Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_D
Reset:	soft
Address:	6327Ch-6327Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_D
Reset:	soft
Address:	632A0h-632A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_D

VIDEO_DIP_DATA	
Reset:	soft
Address:	632A4h-632A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_D
Reset:	soft
Address:	632A8h-632ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_D
Reset:	soft
Address:	632ACh-632AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_D
Reset:	soft
Address:	632B0h-632B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_D
Reset:	soft
Address:	632B4h-632B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_D
Reset:	soft
Address:	632B8h-632BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_D
Reset:	soft
Address:	632BCh-632BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_D
Reset:	soft
Address:	632E0h-632E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_D
Reset:	soft
Address:	632E4h-632E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_D



VIDEO_DIP_DATA	
Reset:	soft
Address:	632E8h-632EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_D
Reset:	soft
Address:	632ECh-632EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_D
Reset:	soft
Address:	632F0h-632F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_D
Reset:	soft
Address:	632F4h-632F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_D
Reset:	soft
Address:	632F8h-632FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_D
Reset:	soft
Address:	632FCh-632FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_D
Reset:	soft
Address:	63300h-63303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_D
Reset:	soft
Address:	63320h-63323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_D
Reset:	soft
Address:	63324h-63327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_D

VIDEO_DIP_DATA										
Reset:	soft									
Address:	63328h-6332Bh									
Name:	Transcoder Video Data Island Packet VSC Data 2									
ShortName:	VIDEO_DIP_VSC_DATA_2_D									
Reset:	soft									
Address:	6332Ch-6332Fh									
Name:	Transcoder Video Data Island Packet VSC Data 3									
ShortName:	VIDEO_DIP_VSC_DATA_3_D									
Reset:	soft									
Address:	63330h-63333h									
Name:	Transcoder Video Data Island Packet VSC Data 4									
ShortName:	VIDEO_DIP_VSC_DATA_4_D									
Reset:	soft									
Address:	63334h-63337h									
Name:	Transcoder Video Data Island Packet VSC Data 5									
ShortName:	VIDEO_DIP_VSC_DATA_5_D									
Reset:	soft									
Address:	63338h-6333Bh									
Name:	Transcoder Video Data Island Packet VSC Data 6									
ShortName:	VIDEO_DIP_VSC_DATA_6_D									
Reset:	soft									
Address:	6333Ch-6333Fh									
Name:	Transcoder Video Data Island Packet VSC Data 7									
ShortName:	VIDEO_DIP_VSC_DATA_7_D									
Reset:	soft									
Address:	63340h-63343h									
Name:	Transcoder Video Data Island Packet VSC Data 8									
ShortName:	VIDEO_DIP_VSC_DATA_8_D									
Reset:	soft									
There are multiple instances of this register format per DIP type and per transcoder.										
DWord	Bit	Description								
0	31:0	Video DIP DATA <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/W</td> </tr> <tr> <td colspan="2">This field contains the video DIP data to be transmitted.</td> </tr> <tr> <td colspan="2" style="text-align: center;">Restriction</td> </tr> <tr> <td colspan="2">Data should be loaded before enabling the transmission through the DIP type enable bit.</td> </tr> </table>	Access:	R/W	This field contains the video DIP data to be transmitted.		Restriction		Data should be loaded before enabling the transmission through the DIP type enable bit.	
Access:	R/W									
This field contains the video DIP data to be transmitted.										
Restriction										
Data should be loaded before enabling the transmission through the DIP type enable bit.										



VIDEO_DIP_DRM_DATA

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60440h-60443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_A
Reset:	soft
Address:	60444h-60447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_A
Reset:	soft
Address:	60448h-6044Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_A
Reset:	soft
Address:	6044Ch-6044Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_A
Reset:	soft
Address:	60450h-60453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_A
Reset:	soft
Address:	60454h-60457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_A
Reset:	soft
Address:	60458h-6045Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_A
Reset:	soft
Address:	6045Ch-6045Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_A

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
Reset:	soft
Address:	61440h-61443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_B
Reset:	soft
Address:	61444h-61447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_B
Reset:	soft
Address:	61448h-6144Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_B
Reset:	soft
Address:	6144Ch-6144Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_B
Reset:	soft
Address:	61450h-61453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_B
Reset:	soft
Address:	61454h-61457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_B
Reset:	soft
Address:	61458h-6145Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_B
Reset:	soft
Address:	6145Ch-6145Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_B
Reset:	soft
Address:	62440h-62443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_C



VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA

Reset:	soft
Address:	62444h-62447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_C
Reset:	soft
Address:	62448h-6244Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_C
Reset:	soft
Address:	6244Ch-6244Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_C
Reset:	soft
Address:	62450h-62453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_C
Reset:	soft
Address:	62454h-62457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_C
Reset:	soft
Address:	62458h-6245Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_C
Reset:	soft
Address:	6245Ch-6245Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_C
Reset:	soft
Address:	63440h-63443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_D
Reset:	soft
Address:	63444h-63447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_D

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA

Reset:	soft		
Address:	63448h-6344Bh		
Name:	Transcoder Video Data Island Packet for DRM 2		
ShortName:	VIDEO_DIP_DRM_DATA_2_D		
Reset:	soft		
Address:	6344Ch-6344Fh		
Name:	Transcoder Video Data Island Packet for DRM 3		
ShortName:	VIDEO_DIP_DRM_DATA_3_D		
Reset:	soft		
Address:	63450h-63453h		
Name:	Transcoder Video Data Island Packet for DRM 4		
ShortName:	VIDEO_DIP_DRM_DATA_4_D		
Reset:	soft		
Address:	63454h-63457h		
Name:	Transcoder Video Data Island Packet for DRM 5		
ShortName:	VIDEO_DIP_DRM_DATA_5_D		
Reset:	soft		
Address:	63458h-6345Bh		
Name:	Transcoder Video Data Island Packet for DRM 6		
ShortName:	VIDEO_DIP_DRM_DATA_6_D		
Reset:	soft		
Address:	6345Ch-6345Fh		
Name:	Transcoder Video Data Island Packet for DRM 7		
ShortName:	VIDEO_DIP_DRM_DATA_7_D		
Reset:	soft		
HDMI 2.0 DRM Infoframe DIP data.			
DWord	Bit	Description	
0	31:0	DRM DIP data	
		Access:	R/W



VIDEO_DIP_DRM_ECC

VIDEO_DIP_DRM_ECC - VIDEO_DIP_DRM_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60460h-60463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_A
Reset:	soft
Address:	60464h-60467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_A
Reset:	soft
Address:	61460h-61463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_B
Reset:	soft
Address:	61464h-61467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_B
Reset:	soft
Address:	62460h-62463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_C
Reset:	soft
Address:	62464h-62467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_C
Reset:	soft
Address:	63460h-63463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_D
Reset:	soft
Address:	63464h-63467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_D

VIDEO_DIP_DRM_ECC - VIDEO_DIP_DRM_ECC		
Reset: soft		
HDMI 2.0 DRM Infoframe ECC data.		
DWord	Bit	Description
0	31:0	DRM ECC data



VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60240h-60243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_A
Reset:	soft
Address:	60244h-60247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_A
Reset:	soft
Address:	60280h-60283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_A
Reset:	soft
Address:	60284h-60287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_A
Reset:	soft
Address:	602C0h-602C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_A
Reset:	soft
Address:	602C4h-602C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_A
Reset:	soft
Address:	602D0h-602D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_A
Reset:	soft
Address:	602D4h-602D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_A

VIDEO_DIP_ECC	
Reset:	soft
Address:	602D8h-602DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_A
Reset:	soft
Address:	60304h-60307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_A
Reset:	soft
Address:	60308h-6030Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_A
Reset:	soft
Address:	6030Ch-6030Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_A
Reset:	soft
Address:	60310h-60313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_A
Reset:	soft
Address:	60314h-60317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_A
Reset:	soft
Address:	60344h-60347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_A
Reset:	soft
Address:	60348h-6034Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_A
Reset:	soft
Address:	6034Ch-6034Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_A

VIDEO_DIP_ECC	
Reset:	soft
Address:	61240h-61243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_B
Reset:	soft
Address:	61244h-61247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_B
Reset:	soft
Address:	61280h-61283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_B
Reset:	soft
Address:	61284h-61287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_B
Reset:	soft
Address:	612C0h-612C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_B
Reset:	soft
Address:	612C4h-612C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_B
Reset:	soft
Address:	612D0h-612D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_B
Reset:	soft
Address:	612D4h-612D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_B
Reset:	soft
Address:	612D8h-612DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_B

VIDEO_DIP_ECC	
Reset:	soft
Address:	61304h-61307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_B
Reset:	soft
Address:	61308h-6130Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_B
Reset:	soft
Address:	6130Ch-6130Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_B
Reset:	soft
Address:	61310h-61313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_B
Reset:	soft
Address:	61314h-61317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_B
Reset:	soft
Address:	61344h-61347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_B
Reset:	soft
Address:	61348h-6134Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_B
Reset:	soft
Address:	6134Ch-6134Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_B
Reset:	soft
Address:	62240h-62243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_C



VIDEO_DIP_ECC	
Reset:	soft
Address:	62244h-62247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_C
Reset:	soft
Address:	62280h-62283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_C
Reset:	soft
Address:	62284h-62287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_C
Reset:	soft
Address:	622C0h-622C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_C
Reset:	soft
Address:	622C4h-622C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_C
Reset:	soft
Address:	622D0h-622D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_C
Reset:	soft
Address:	622D4h-622D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_C
Reset:	soft
Address:	622D8h-622DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_C
Reset:	soft
Address:	62304h-62307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_C

VIDEO_DIP_ECC	
Reset:	soft
Address:	62308h-6230Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_C
Reset:	soft
Address:	6230Ch-6230Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_C
Reset:	soft
Address:	62310h-62313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_C
Reset:	soft
Address:	62314h-62317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_C
Reset:	soft
Address:	62344h-62347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_C
Reset:	soft
Address:	62348h-6234Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_C
Reset:	soft
Address:	6234Ch-6234Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_C
Reset:	soft
Address:	63240h-63243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_D
Reset:	soft
Address:	63244h-63247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_D



VIDEO_DIP_ECC	
Reset:	soft
Address:	63280h-63283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_D
Reset:	soft
Address:	63284h-63287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_D
Reset:	soft
Address:	632C0h-632C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_D
Reset:	soft
Address:	632C4h-632C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_D
Reset:	soft
Address:	632D0h-632D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_D
Reset:	soft
Address:	632D4h-632D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_D
Reset:	soft
Address:	632D8h-632DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_D
Reset:	soft
Address:	63304h-63307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_D
Reset:	soft
Address:	63308h-6330Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_D

VIDEO_DIP_ECC		
Reset:	soft	
Address:	6330Ch-6330Fh	
Name:	Transcoder Video Data Island Packet GMP ECC 2	
ShortName:	VIDEO_DIP_GMP_ECC_2_D	
Reset:	soft	
Address:	63310h-63313h	
Name:	Transcoder Video Data Island Packet GMP ECC 3	
ShortName:	VIDEO_DIP_GMP_ECC_3_D	
Reset:	soft	
Address:	63314h-63317h	
Name:	Transcoder Video Data Island Packet GMP ECC 4	
ShortName:	VIDEO_DIP_GMP_ECC_4_D	
Reset:	soft	
Address:	63344h-63347h	
Name:	Transcoder Video Data Island Packet VSC ECC 0	
ShortName:	VIDEO_DIP_VSC_ECC_0_D	
Reset:	soft	
Address:	63348h-6334Bh	
Name:	Transcoder Video Data Island Packet VSC ECC 1	
ShortName:	VIDEO_DIP_VSC_ECC_1_D	
Reset:	soft	
Address:	6334Ch-6334Fh	
Name:	Transcoder Video Data Island Packet VSC ECC 2	
ShortName:	VIDEO_DIP_VSC_ECC_2_D	
Reset:	soft	
There are multiple instances of this register format per DIP type and per transcoder.		
DWord	Bit	Description
0	31:0	Video DIP ECC This field contains the video DIP ECC value for read back.



VIDEO_DIP_GCP

VIDEO_DIP_GCP											
Register Space:	MMIO: 0/2/0										
Access:	R/W										
Size (in bits):	32										
Address:	60210h-60213h										
Name:	Transcoder Video Data Island Packet GCP										
ShortName:	VIDEO_DIP_GCP_A										
Reset:	soft										
Address:	61210h-61213h										
Name:	Transcoder Video Data Island Packet GCP										
ShortName:	VIDEO_DIP_GCP_B										
Reset:	soft										
Address:	62210h-62213h										
Name:	Transcoder Video Data Island Packet GCP										
ShortName:	VIDEO_DIP_GCP_C										
Reset:	soft										
Address:	63210h-63213h										
Name:	Transcoder Video Data Island Packet GCP										
ShortName:	VIDEO_DIP_GCP_D										
Reset:	soft										
DWord	Bit	Description									
0	31:3	Reserved									
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
Access:	RO										
Format:	MBZ										
2		GCP color indication									
		Access: R/W									
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Don't Indicate</td> <td>Don't indicate color depth. CD and PP bits in GCP set to zero.</td> </tr> <tr> <td>1b</td> <td>Indicate</td> <td>Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Don't Indicate	Don't indicate color depth. CD and PP bits in GCP set to zero.	1b	Indicate	Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register.
		Value	Name	Description							
		0b	Don't Indicate	Don't indicate color depth. CD and PP bits in GCP set to zero.							
1b	Indicate	Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register.									
Restriction											
This bit must be set when in HDMI deep color (>8 BPC) mode.											

VIDEO_DIP_GCP

1	GCP default phase enable				R/W																					
<p>Access:</p> <p>GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met:</p> <ol style="list-style-type: none"> 1. Htotal is a multiple of the value given in the table below 2. Hactive is an even number 3. Front and back porches for Hsync are even numbers 4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0) 																										
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 10%;">BPC</th> <th style="width: 30%;">Color Format</th> <th style="width: 60%;">Htotal Multiple Requirement</th> </tr> </thead> <tbody> <tr> <td>8</td> <td>RGB</td> <td>2</td> </tr> <tr> <td>8</td> <td>YUV420</td> <td>4</td> </tr> <tr> <td>10</td> <td>RGB</td> <td>4</td> </tr> <tr> <td>10</td> <td>YUV420</td> <td>8</td> </tr> <tr> <td>12</td> <td>RGB</td> <td>2</td> </tr> <tr> <td>12</td> <td>YUV420</td> <td>4</td> </tr> </tbody> </table>						BPC	Color Format	Htotal Multiple Requirement	8	RGB	2	8	YUV420	4	10	RGB	4	10	YUV420	8	12	RGB	2	12	YUV420	4
BPC	Color Format	Htotal Multiple Requirement																								
8	RGB	2																								
8	YUV420	4																								
10	RGB	4																								
10	YUV420	8																								
12	RGB	2																								
12	YUV420	4																								
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 15%;">Value</th> <th style="width: 15%;">Name</th> <th style="width: 70%;">Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Clear</td> <td>Default phase bit in GCP is cleared.</td> </tr> <tr> <td>1b</td> <td>Set</td> <td>Default phase bit in GCP is set.</td> </tr> </tbody> </table>						Value	Name	Description	0b	Clear	Default phase bit in GCP is cleared.	1b	Set	Default phase bit in GCP is set.												
Value	Name	Description																								
0b	Clear	Default phase bit in GCP is cleared.																								
1b	Set	Default phase bit in GCP is set.																								
Restriction																										
Do not set this bit if these requirements are not met.																										
0	Reserved																									



VIDEO_DIP_PPS_DATA

VIDEO_DIP_PPS_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60350h-60353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_A
Reset:	soft
Address:	60354h-60357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_A
Reset:	soft
Address:	60358h-6035Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_A
Reset:	soft
Address:	6035Ch-6035Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_A
Reset:	soft
Address:	60360h-60363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_A
Reset:	soft
Address:	60364h-60367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_A
Reset:	soft
Address:	60368h-6036Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_A
Reset:	soft
Address:	6036Ch-6036Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_A

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	60370h-60373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_A
Reset:	soft
Address:	60374h-60377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_A
Reset:	soft
Address:	60378h-6037Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_A
Reset:	soft
Address:	6037Ch-6037Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_A
Reset:	soft
Address:	60380h-60383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_A
Reset:	soft
Address:	60384h-60387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_A
Reset:	soft
Address:	60388h-6038Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_A
Reset:	soft
Address:	6038Ch-6038Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_A
Reset:	soft
Address:	60390h-60393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_A



VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	60394h-60397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_A
Reset:	soft
Address:	60398h-6039Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_A
Reset:	soft
Address:	6039Ch-6039Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_A
Reset:	soft
Address:	603A0h-603A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_A
Reset:	soft
Address:	603A4h-603A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_A
Reset:	soft
Address:	603A8h-603ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_A
Reset:	soft
Address:	603ACh-603AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_A
Reset:	soft
Address:	603B0h-603B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_A
Reset:	soft
Address:	603B4h-603B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_A

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	603B8h-603BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_A
Reset:	soft
Address:	603BCh-603BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_A
Reset:	soft
Address:	603C0h-603C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_A
Reset:	soft
Address:	603C4h-603C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_A
Reset:	soft
Address:	603C8h-603CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_A
Reset:	soft
Address:	603CCh-603CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_A
Reset:	soft
Address:	603D0h-603D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_A
Reset:	soft
Address:	61350h-61353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_B
Reset:	soft
Address:	61354h-61357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_B



VIDEO_DIP_PPS_DATA

Reset:	soft
Address:	61358h-6135Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_B
Reset:	soft
Address:	6135Ch-6135Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_B
Reset:	soft
Address:	61360h-61363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_B
Reset:	soft
Address:	61364h-61367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_B
Reset:	soft
Address:	61368h-6136Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_B
Reset:	soft
Address:	6136Ch-6136Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_B
Reset:	soft
Address:	61370h-61373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_B
Reset:	soft
Address:	61374h-61377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_B
Reset:	soft
Address:	61378h-6137Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	6137Ch-6137Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_B
Reset:	soft
Address:	61380h-61383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_B
Reset:	soft
Address:	61384h-61387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_B
Reset:	soft
Address:	61388h-6138Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_B
Reset:	soft
Address:	6138Ch-6138Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_B
Reset:	soft
Address:	61390h-61393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_B
Reset:	soft
Address:	61394h-61397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_B
Reset:	soft
Address:	61398h-6139Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_B
Reset:	soft
Address:	6139Ch-6139Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_B



VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	613A0h-613A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_B
Reset:	soft
Address:	613A4h-613A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_B
Reset:	soft
Address:	613A8h-613ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_B
Reset:	soft
Address:	613ACh-613AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_B
Reset:	soft
Address:	613B0h-613B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_B
Reset:	soft
Address:	613B4h-613B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_B
Reset:	soft
Address:	613B8h-613BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_B
Reset:	soft
Address:	613BCh-613BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_B
Reset:	soft
Address:	613C0h-613C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	613C4h-613C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_B
Reset:	soft
Address:	613C8h-613CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_B
Reset:	soft
Address:	613CCh-613CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_B
Reset:	soft
Address:	613D0h-613D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_B
Reset:	soft
Address:	62350h-62353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_C
Reset:	soft
Address:	62354h-62357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_C
Reset:	soft
Address:	62358h-6235Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_C
Reset:	soft
Address:	6235Ch-6235Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_C
Reset:	soft
Address:	62360h-62363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_C



VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	62364h-62367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_C
Reset:	soft
Address:	62368h-6236Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_C
Reset:	soft
Address:	6236Ch-6236Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_C
Reset:	soft
Address:	62370h-62373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_C
Reset:	soft
Address:	62374h-62377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_C
Reset:	soft
Address:	62378h-6237Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_C
Reset:	soft
Address:	6237Ch-6237Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_C
Reset:	soft
Address:	62380h-62383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_C
Reset:	soft
Address:	62384h-62387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	62388h-6238Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_C
Reset:	soft
Address:	6238Ch-6238Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_C
Reset:	soft
Address:	62390h-62393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_C
Reset:	soft
Address:	62394h-62397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_C
Reset:	soft
Address:	62398h-6239Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_C
Reset:	soft
Address:	6239Ch-6239Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_C
Reset:	soft
Address:	623A0h-623A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_C
Reset:	soft
Address:	623A4h-623A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_C
Reset:	soft
Address:	623A8h-623ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_C



VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	623ACh-623AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_C
Reset:	soft
Address:	623B0h-623B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_C
Reset:	soft
Address:	623B4h-623B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_C
Reset:	soft
Address:	623B8h-623BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_C
Reset:	soft
Address:	623BCh-623BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_C
Reset:	soft
Address:	623C0h-623C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_C
Reset:	soft
Address:	623C4h-623C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_C
Reset:	soft
Address:	623C8h-623CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_C
Reset:	soft
Address:	623CCh-623CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	623D0h-623D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_C
Reset:	soft
Address:	63350h-63353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_D
Reset:	soft
Address:	63354h-63357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_D
Reset:	soft
Address:	63358h-6335Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_D
Reset:	soft
Address:	6335Ch-6335Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_D
Reset:	soft
Address:	63360h-63363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_D
Reset:	soft
Address:	63364h-63367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_D
Reset:	soft
Address:	63368h-6336Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_D
Reset:	soft
Address:	6336Ch-6336Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_D



VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	63370h-63373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_D
Reset:	soft
Address:	63374h-63377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_D
Reset:	soft
Address:	63378h-6337Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_D
Reset:	soft
Address:	6337Ch-6337Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_D
Reset:	soft
Address:	63380h-63383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_D
Reset:	soft
Address:	63384h-63387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_D
Reset:	soft
Address:	63388h-6338Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_D
Reset:	soft
Address:	6338Ch-6338Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_D
Reset:	soft
Address:	63390h-63393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_D

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	63394h-63397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_D
Reset:	soft
Address:	63398h-6339Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_D
Reset:	soft
Address:	6339Ch-6339Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_D
Reset:	soft
Address:	633A0h-633A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_D
Reset:	soft
Address:	633A4h-633A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_D
Reset:	soft
Address:	633A8h-633ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_D
Reset:	soft
Address:	633ACh-633AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_D
Reset:	soft
Address:	633B0h-633B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_D
Reset:	soft
Address:	633B4h-633B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_D



VIDEO_DIP_PPS_DATA				
Reset:	soft			
Address:	633B8h-633BBh			
Name:	Transcoder Video Data Island Packet for PPS 26			
ShortName:	VIDEO_DIP_PPS_DATA_26_D			
Reset:	soft			
Address:	633BCh-633BFh			
Name:	Transcoder Video Data Island Packet for PPS 27			
ShortName:	VIDEO_DIP_PPS_DATA_27_D			
Reset:	soft			
Address:	633C0h-633C3h			
Name:	Transcoder Video Data Island Packet for PPS 28			
ShortName:	VIDEO_DIP_PPS_DATA_28_D			
Reset:	soft			
Address:	633C4h-633C7h			
Name:	Transcoder Video Data Island Packet for PPS 29			
ShortName:	VIDEO_DIP_PPS_DATA_29_D			
Reset:	soft			
Address:	633C8h-633CBh			
Name:	Transcoder Video Data Island Packet for PPS 30			
ShortName:	VIDEO_DIP_PPS_DATA_30_D			
Reset:	soft			
Address:	633CCh-633CFh			
Name:	Transcoder Video Data Island Packet for PPS 31			
ShortName:	VIDEO_DIP_PPS_DATA_31_D			
Reset:	soft			
Address:	633D0h-633D3h			
Name:	Transcoder Video Data Island Packet for PPS 32			
ShortName:	VIDEO_DIP_PPS_DATA_32_D			
Reset:	soft			
DWord	Bit	Description		
0	31:0	Video DIP PPS data <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">Access:</td> <td style="width: 30%; text-align: center;">R/W</td> </tr> </table> Video data island packet for PPS data.	Access:	R/W
Access:	R/W			

VIDEO_DIP_PPS_ECC

VIDEO_DIP_PPS_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	603D4h-603D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_A
Reset:	soft
Address:	603D8h-603DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_A
Reset:	soft
Address:	603DCh-603DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_A
Reset:	soft
Address:	603E0h-603E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_A
Reset:	soft
Address:	603E4h-603E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_A
Reset:	soft
Address:	603E8h-603EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_A
Reset:	soft
Address:	603ECh-603EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_A
Reset:	soft
Address:	603F0h-603F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_A



VIDEO_DIP_PPS_ECC

Reset:	soft
Address:	603F4h-603F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_A
Reset:	soft
Address:	613D4h-613D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_B
Reset:	soft
Address:	613D8h-613DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_B
Reset:	soft
Address:	613DCh-613DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_B
Reset:	soft
Address:	613E0h-613E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_B
Reset:	soft
Address:	613E4h-613E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_B
Reset:	soft
Address:	613E8h-613EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_B
Reset:	soft
Address:	613ECh-613EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_B
Reset:	soft
Address:	613F0h-613F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_B

VIDEO_DIP_PPS_ECC	
Reset:	soft
Address:	613F4h-613F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_B
Reset:	soft
Address:	623D4h-623D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_C
Reset:	soft
Address:	623D8h-623DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_C
Reset:	soft
Address:	623DCh-623DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_C
Reset:	soft
Address:	623E0h-623E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_C
Reset:	soft
Address:	623E4h-623E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_C
Reset:	soft
Address:	623E8h-623EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_C
Reset:	soft
Address:	623ECh-623EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_C
Reset:	soft
Address:	623F0h-623F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_C



VIDEO_DIP_PPS_ECC	
Reset:	soft
Address:	623F4h-623F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_C
Reset:	soft
Address:	633D4h-633D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_D
Reset:	soft
Address:	633D8h-633DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_D
Reset:	soft
Address:	633DCh-633DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_D
Reset:	soft
Address:	633E0h-633E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_D
Reset:	soft
Address:	633E4h-633E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_D
Reset:	soft
Address:	633E8h-633EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_D
Reset:	soft
Address:	633ECh-633EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_D
Reset:	soft
Address:	633F0h-633F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_D

VIDEO_DIP_PPS_ECC				
Reset:	soft			
Address:	633F4h-633F7h			
Name:	Transcoder Video DIP for PPS ECC 8			
ShortName:	VIDEO_DIP_PPS_ECC_8_D			
Reset:	soft			
This represents 36 bytes of ECC over PPS DIP.				
DWord	Bit	Description		
0	31:0	Video DIP PPS ECC <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> ECC for PPS DIP.	Access:	RO
Access:	RO			



Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address			
Register Space:	PCI: 0/2/0		
Size (in bits):	32		
Address:	00030h		
The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.			
DWord	Bit	Description	
0	31:18	ROM Base Address	
		Default Value:	00000000000000b
		Access:	RO
		_Custom_GTIReset:	BUS
			Hardwired to 0's.
	17:11	Address Mask	
		Default Value:	0000000b
		Access:	RO
		_Custom_GTIReset:	BUS
			Hardwired to 0s to indicate 256 KB address range.
	10:1	Reserved	
		Access:	RO
Format:		MBZ	
0	ROM BIOS Enable		
	Default Value:	0b	
	Access:	RO	
	_Custom_GTIReset:	BUS	
		Hardwired to 0 to indicate ROM not accessible.	

VIRTUALIZATION CONTROL REGISTER

VIRTUAL_CTRL_REG - VIRTUALIZATION CONTROL REGISTER			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
SOC_Consumer:	BIOS		
Address:	10108Ch		
This register is used to identify which Virtual Function, if any, is allowed to access or configure the Global GTT Entry.			
DWord	Bit	Description	
0	31:9	Reserved	
		Access: RO	
		Format: MBZ	
8	8	Guest Direct GGTT Update Enable	
		Access: R/W	
		_Custom_GTIReset: BUS	
		1'b0 : Guest VM can't directly update GGTT Entries via GSM range within VF GTTMMADR 1'b1 : Guest VM can modify the physical address field of a GGTT Entry if the Function Number field of that entry matches the Function Number associated with the GTTMMADR range that was targeted by the access. No other field of the GGTT Entry can be modified by the Guest VM. A Guest VM Read to a GGTT Entry is allowed if the Function Number field matches, but the Function Number field itself will read as 0 (a Guest VM should not know which VF it has been assigned to).	
		Value	Name
0b	[Default]		
	1b		
7:0	7:0	Reserved	
		Access: RO	
		Format: MBZ	



VSC_EXT_SDP_CONF

VSC_EXT_SDP_CONF			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	60288h-6028Bh		
Name:	Transcoder VSD Extended SDP Configuration		
ShortName:	VSC_EXT_SDP_CONF_A		
Reset:	soft		
Address:	61288h-6128Bh		
Name:	Transcoder VSD Extended SDP Configuration		
ShortName:	VSC_EXT_SDP_CONF_B		
Reset:	soft		
Address:	62288h-6228Bh		
Name:	Transcoder VSD Extended SDP Configuration		
ShortName:	VSC_EXT_SDP_CONF_C		
Reset:	soft		
Address:	63288h-6328Bh		
Name:	Transcoder VSD Extended SDP Configuration		
ShortName:	VSC_EXT_SDP_CONF_D		
Reset:	soft		
DWord	Bit	Description	
0	31	Chain done	
		Access:	RO
		Read by software/DSB to know if it can start sending new chain. Chained metadata straddling 2 buffers need to know this status.	
		Value	Name
		0b	HW sending previous chain
	1b	HW completed sending previous chain	
	30:25	Reserved	
		Access:	RO
		Format:	MBZ
	24	Reserved	
Access:		RO	
Format:		MBZ	

VSC_EXT_SDP_CONF

23	<p>SDP Active Error</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td style="width: 40%;">R/WC</td> </tr> </table> <p>This bit represents an error condition that not all SDPs were read when video active region is reached. HW will stop transmitting metadata once active region is reached. This bit is set by HW and cleared by SW by writing '1'. To avoid false indication of an error, SW can choose either of the following methods:</p> <ol style="list-style-type: none"> 1. Avoid programming VSC_EXT registers and setting the buffer ready bit in VSC_EXT_SDP_CTL before vblank rises. 2. Program VSC_EXT registers and set the buffer ready bit in VSC_EXT_SDP_CTL anytime, but clear the SDP Active Error at the start of vblank, so that it can be rechecked at the end of vblank to indicate real issues. <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>All SDPs transmitted in VBLANK</td> </tr> <tr> <td>1b</td> <td>All SDPs not transmitted in VBLANK</td> </tr> </tbody> </table>	Access:	R/WC	Value	Name	0b	All SDPs transmitted in VBLANK	1b	All SDPs not transmitted in VBLANK
Access:	R/WC								
Value	Name								
0b	All SDPs transmitted in VBLANK								
1b	All SDPs not transmitted in VBLANK								
22	<p>Block mode</p> <p>When this bit is set to 1, it is software responsibility to set Middle Of Chaining bit [23] and Packet sequence bits [28:24] in the header packet that it programs in metadata register. HW does not support changing this field during transmission.</p> <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th style="width: 20%;">Value</th> <th style="width: 80%;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Header values from Header register</td> </tr> <tr> <td>1b</td> <td>Header values from SW/DSB written buffer</td> </tr> </tbody> </table>	Value	Name	0b	Header values from Header register	1b	Header values from SW/DSB written buffer		
Value	Name								
0b	Header values from Header register								
1b	Header values from SW/DSB written buffer								
21:10	<p>HBLANK early indication</p> <p>In HW, this field is expressed in terms of pixels and not clocks. It provides a guardband to stop the VSC_EXT_SDP transmission from going into Hblank region (for Audio). For eg: If this field is programed to 20 pixels, then when horizontal counter reaches (HActive -20), VSC_EXT_SDP transmission stops. If a packet is in the middle of transmission, then it completes before stopping. Transmission resumes on the next HActive. In MST/DP2 this transmission can happen only when an MTP slot is available. For all SST/MST/DP2 use cases, recommendation is to use 10% of HActive.</p>								
9:0	<p>Packets per chain</p> <p>This field specifies the total number of packets (each packet has 32 bytes) in the chain. = Number of bytes/32</p>								



VSC_EXT_SDP_CTL

VSC_EXT_SDP_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60290h-60293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_A
Reset:	soft
Address:	60294h-60297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_A
Reset:	soft
Address:	61290h-61293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_B
Reset:	soft
Address:	61294h-61297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_B
Reset:	soft
Address:	62290h-62293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_C
Reset:	soft
Address:	62294h-62297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_C
Reset:	soft
Address:	63290h-63293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_D
Reset:	soft
Address:	63294h-63297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_D

VSC_EXT_SDP_CTL

Reset: soft

The VSC_EXT_VESA SDP allows a DP Source device to send video stream-related metadata aligned with the stream. A single VSC_EXT SDP is composed of four header bytes and 32 payload bytes. The VSC_EXT_VESA SDP maybe chained. Chaining framework enables a flexible metadata transportation framework to allow the transport of variable bytes of payload using a single VSC_EXT_VESA.

For transmitting frame synchronous metadata beyond 1KB, software must alternate between Buffer0 and Buffer1.

Metadata must be programmed in multiple of 32 bytes (8 dwords).

DWord	Bit	Description								
0	31	VSC extension SDP metadata enable NOTE: This field is ignored on the register instance VSC_EXT_SDP_CTL_1.								
		<table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Disable</td> </tr> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Enable</td> </tr> </tbody> </table>	Value	Name	0b	Disable	1b	Enable		
		Value	Name							
	0b	Disable								
	1b	Enable								
	30:25	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
	Access:	RO								
	Format:	MBZ								
	24	Buffer Empty <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">RO</td> </tr> </table> <p>This field is set by hardware when buffer is empty and reset when buffer has metadata to be sent over the link.</p> <p>This field is read by software (or DSB) to know when it can start writing to the buffer (buffer reuse cases included).</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">buffer empty [Default]</td> </tr> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">buffer not empty</td> </tr> </tbody> </table>	Access:	RO	Value	Name	1b	buffer empty [Default]	0b	buffer not empty
	Access:	RO								
Value	Name									
1b	buffer empty [Default]									
0b	buffer not empty									
23:17	Reserved <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td style="text-align: center;">RO</td> </tr> <tr> <td>Format:</td> <td style="text-align: center;">MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ					
Access:	RO									
Format:	MBZ									
16	Buffer Ready <table border="1" style="width: 100%;"> <tr> <td style="width: 40%;">Access:</td> <td style="text-align: center;">Write/Read Status</td> </tr> </table> <p>This field is set by software (or DSB) to indicate that the buffer is ready for hardware use. Hardware clears this field after the buffer processing is complete.</p> <p>SW can also clear this bit. Both SW clear and SW set will have higher priority over HW clear.</p> <table border="1" style="width: 100%;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1b</td> <td style="text-align: center;">Ready For HW Use</td> </tr> <tr> <td style="text-align: center;">0b</td> <td style="text-align: center;">Not ready for HW Use</td> </tr> </tbody> </table>	Access:	Write/Read Status	Value	Name	1b	Ready For HW Use	0b	Not ready for HW Use	
Access:	Write/Read Status									
Value	Name									
1b	Ready For HW Use									
0b	Not ready for HW Use									

VSC_EXT_SDP_CTL	
15	Reserved
	Access: RO
	Format: MBZ
14	Index Auto Increment This field controls the index auto increment.
13:8	Reserved
	Access: RO
	Format: MBZ
7:0	Index Value This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a write to the data register if the index auto increment bit (14) is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. 8-bit index supports up to 1KB. Examples: 00h = Dword at location 0 FFh = Dword at location 255

VSC_EXT_SDP_DATA

VSC_EXT_SDP_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60298h-6029Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_A
Reset:	soft
Address:	6029Ch-6029Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_A
Reset:	soft
Address:	61298h-6129Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_B
Reset:	soft
Address:	6129Ch-6129Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_B
Reset:	soft
Address:	62298h-6229Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_C
Reset:	soft
Address:	6229Ch-6229Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_C
Reset:	soft
Address:	63298h-6329Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_D
Reset:	soft
Address:	6329Ch-6329Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_D

VSC_EXT_SDP_DATA		
Reset:		soft
DWord	Bit	Description
0	31:0	<p>Data</p> <p>This field specifies the data for the index specified in VSC EXT SDP CTL register. Index [0-31] allows up to 1KB data.</p> <p>This register must be written only as a full 32 bit dword. Byte or word writes are not supported.</p> <p>This field can be read back only when "VSC extension SDP metadata enable" field in VSC_EXT_SDP_CTL is deasserted.</p>

VSC_EXT_SDP_HEADER

VSC_EXT_SDP_HEADER								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	6028Ch-6028Fh							
Name:	Transcoder VSD Extended SDP Header							
ShortName:	VSC_EXT_SDP_HEADER_A							
Reset:	soft							
Address:	6128Ch-6128Fh							
Name:	Transcoder VSD Extended SDP Header							
ShortName:	VSC_EXT_SDP_HEADER_B							
Reset:	soft							
Address:	6228Ch-6228Fh							
Name:	Transcoder VSD Extended SDP Header							
ShortName:	VSC_EXT_SDP_HEADER_C							
Reset:	soft							
Address:	6328Ch-6328Fh							
Name:	Transcoder VSD Extended SDP Header							
ShortName:	VSC_EXT_SDP_HEADER_D							
Reset:	soft							
DWord	Bit	Description						
0	31:29	Reserved						
		Access:	RO					
		Format:	MBZ					
	28:24	Packet sequence Range is from 0 to 31. Shall be cleared to 0 on the first SDP of a new VSC_EXT packet sequence. When bit 6 of HB2 is set to 1, this field shall increment by 1 on each subsequent chained packet. This counter rolls over to 0 when it exceeds 31.						
	23	Middle Of Chaining This bit specifies if there are any chained packets to follow. This bit has to be set if block mode(VSC_EXT_SDP_CONF[block mode]) is set.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No chained packets to follow</td> </tr> <tr> <td>1b</td> <td>Chained packet(s) to follow.</td> </tr> </tbody> </table>	Value	Name	0b	No chained packets to follow	1b	Chained packet(s) to follow.
Value	Name							
0b	No chained packets to follow							
1b	Chained packet(s) to follow.							
	22	Variable Packet Sequence Number This bit specifies how the packed sequence field is used.						

VSC_EXT_SDP_HEADER							
	<table border="1"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Packet Sequence Field is fixed</td> </tr> <tr> <td>1b</td> <td>Packet Sequence field is incremented with chained packets</td> </tr> </tbody> </table>	Value	Name	0b	Packet Sequence Field is fixed	1b	Packet Sequence field is incremented with chained packets
Value	Name						
0b	Packet Sequence Field is fixed						
1b	Packet Sequence field is incremented with chained packets						
21:18	VSC EXT VESA SDP Framework Ver 1 Specifies the VSC EXT VESA SDP Framework Version, to be left at default '0'.						
17:16	VSC EXT VESA SDP Framework Ver 0 Specifies the VSC EXT VESA SDP Framework Version, to be left at default '0'.						
15:8	SDP Type Specifies the Secondary Data Packet type. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: center;">Value</th> <th style="text-align: center;">Name</th> </tr> </thead> <tbody> <tr> <td>20h</td> <td>VESA [Default]</td> </tr> <tr> <td>21h</td> <td>CEA</td> </tr> </tbody> </table>	Value	Name	20h	VESA [Default]	21h	CEA
Value	Name						
20h	VESA [Default]						
21h	CEA						
7:0	SDP ID Specifies the Secondary Data Packet ID. Specific to stream (usually 00h).						

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	64	
_Custom_GTIReset:	DEV	
Address:	02320h-02327h	
Name:	VS Invocation Counter	
ShortName:	VS_INVOCATION_COUNT_RCSUNIT_BE_GEOMETRY	
Address:	18320h-18327h	
Name:	VS Invocation Counter	
ShortName:	VS_INVOCATION_COUNT_POCSUNIT_BE_GEOMETRY	
This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.		
DWord	Bit	Description
0..1	63:32	VS Invocation Count Report UDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	VS Invocation Count Report LDW Number of vertices that are dispatched as threads by the VS stage. Updated only when Statistics Enable is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)



VSR_PUSH_CONSTANT_BASE

VSR_PUSH_CONSTANT_BASE - VSR_PUSH_CONSTANT_BASE			
Register Space:	MMIO: 0/2/0		
Size (in bits):	32		
Address:	0E518h		
Name:	VSR_PUSH_CONSTANT_BASE		
ShortName:	VSR_PUSH_CONSTANT_BASE		
DWord	Bit	Description	
0	31:17	Reserved	
		Access:	RO
		Format:	MBZ
	16:6	VSR PUSH CONSTANT BASE	
		Default Value:	200h
		Access:	R/W
		<p style="text-align: center;">Description</p> <p>This is an 64 Byte aligned offset in to the URB indicating the base of the push constant allocation space for the push constant allocation space for VSR unit in POSH pipeline. The offset and size of the VSR allocation is relative to this base address.</p>	
	5:0	Reserved	
		Access:	RO
		Format:	MBZ

VTd Status

VTD_STATUS_0_2_0_PCI - VTd Status				
Register Space:	PCI: 0/2/0			
Size (in bits):	8			
Address:	0006Ch			
This register contains indicator bits for Graphics VTd mode.				
DWord	Bit	Description		
0	7:1	Reserved		
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO
Access:	RO			
Format:	MBZ			
0	0	GFX VTd Active		
		Default Value:	0b	
		Access:	R/W	
		_Custom_GTIReset:	BUS	
Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive. Acts as R/W register only during Punit restore - when iommu freeze bit is set. RO otherwise				



Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	022D0h-022D3h		
Name:	Wait For Event and Display Flip Flags Register		
ShortName:	SYNC_FLIP_STATUS_RCSUNIT_DISP		
Address:	222D0h-222D3h		
Name:	Wait For Event and Display Flip Flags Register		
ShortName:	SYNC_FLIP_STATUS_BCSUNIT_DISP		
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.			
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.			
DWord	Bit	Description	
0	31	Reserved	
		Access:	RO
		Format:	MBZ
	30	Display Plane 1 Asynchronous Display Flip Pending	
	Format:	Enable	
This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			
29	Display Plane 1 Synchronous Flip Display Pending		
	Format:	Enable	
This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			
28	Display Plane 4 Synchronous Flip Display Pending		
	Format:	Enable	
This field enables a wait for the duration of a Display Plane 4 "Flip Pending" condition. If a flip			

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.				
27	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
26	<p>Display Plane 2 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 2 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
25	<p>Display Plane 2 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
24	<p>Display Plane 5 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
23	<p>Display Plane 1 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Source:	RenderCS	Format:	Enable
Source:	RenderCS				
Format:	Enable				
22	<p>Display Plane 1 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending</p>	Format:	Enable		
Format:	Enable				

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	Condition (in the Device Programming Interface chapter of MI Functions).					
21	Display Plane 1 Synchronous Flip Pending Wait Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>		Format:	Enable		
Format:	Enable					
20	Display Plane 4 Synchronous Flip Pending Wait Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>		Format:	Enable		
Format:	Enable					
19	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
18	Display Pipe A Scan Line Wait Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>		Format:	Enable		
Format:	Enable					
17	Display Pipe A Vertical Blank Wait Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>		Format:	Enable		
Format:	Enable					
16	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>		Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
15	Display Plane 2 Asynchronous Performance Flip Pending Wait Enable <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending</p>		Source:	RenderCS	Format:	Enable
Source:	RenderCS					
Format:	Enable					

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

	Condition (in the Device Programming Interface chapter of MI Functions).	
14	Display Plane 2 Asynchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).	
13	Display Plane 2 Synchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).	
12	Display Plane 5 Synchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
11	Reserved	
	Access:	RO
	Format:	MBZ
10	Display Pipe B Scan Line Wait Enable	
	Format:	Enable
	This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.	
9	Display Pipe B Vertical Blank Wait Enable	
	Format:	Enable
	This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).	
8:0	Reserved	
	Access:	RO
	Format:	MBZ



Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	022D4h-022D7h		
Name:	Wait For Event and Display Flip Flags Register 1		
ShortName:	SYNC_FLIP_STATUS_1_RCSUNIT_DISP		
Address:	222D4h-222D7h		
Name:	Wait For Event and Display Flip Flags Register 1		
ShortName:	SYNC_FLIP_STATUS_1_BCSUNIT_DISP		
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.			
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.			
DWord	Bit	Description	
0	31:27	Reserved	
		Access:	RO
		Format:	MBZ
26		Display Plane 12 Synchronous Flip Pending Wait Enable	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.			
25		Display Plane 12 Synchronous Flip Display Pending	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.			

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

24	<p>Display Plane 11 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
23	<p>Display Plane 11 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
22	<p>Display Plane 10 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
21	<p>Display Plane 10 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
20	<p>Display Plane 9 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
19	<p>Display Plane 9 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

18	<p>Display Plane 8 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
17	<p>Display Plane 8 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
16	<p>Display Plane 7 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
15	<p>Display Plane 7 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
14	<p>Display Pipe C Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.</p>	Format:	Enable
Format:	Enable		
13	<p>Display Pipe B Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

12	<p>Display Pipe A Scan Line Event Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.</p>	Format:	Enable		
Format:	Enable				
11	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
10	<p>Display Plane 3 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
9	<p>Display Plane 3 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
8	<p>Display Plane 6 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
7	<p>Display Plane 3 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Source:</td> <td>RenderCS</td> </tr> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.</p>	Source:	RenderCS	Format:	Enable
Source:	RenderCS				
Format:	Enable				

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

6	<p>Display Plane 3 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
5	<p>Display Plane 3 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
4	<p>Display Plane 6 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
3	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
2	<p>Display Pipe C Scan Line Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				
1	<p>Display Pipe C Vertical Blank Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>	Format:	Enable		
Format:	Enable				
0	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				

Wait For Event and Display Flip Flags Register 2

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	022ECh-022EFh		
Name:	Wait For Event and Display Flip Flags Register 2		
ShortName:	SYNC_FLIP_STATUS_2_RCSUNIT_DISP		
Address:	222ECh-222EFh		
Name:	Wait For Event and Display Flip Flags Register 2		
ShortName:	SYNC_FLIP_STATUS_2_BCSUNIT_DISP		
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.			
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.			
DWord	Bit	Description	
0	31:27	Reserved	
		Access:	RO
		Format:	MBZ
26		Display Plane 12 Asynchronous Performance Flip Pending Wait Enable	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			
25		Display Plane 12 Asynchronous Flip Pending Wait Enable	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

24	<p>Display Plane 12 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
23	<p>Display Plane 11 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
22	<p>Display Plane 11 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
21	<p>Display Plane 11 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
20	<p>Display Plane 10 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
19	<p>Display Plane 10 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

18	<p>Display Plane 10 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
17	<p>Display Plane 9 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
16	<p>Display Plane 9 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
15	<p>Display Plane 9 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
14	<p>Display Plane 8 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
13	<p>Display Plane 8 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

12	<p>Display Plane 8 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
11	<p>Display Plane 7 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
10	<p>Display Plane 7 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
9	<p>Display Plane 7 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
8	<p>Display Plane 6 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
7	<p>Display Plane 6 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

6	<p>Display Plane 6 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
5	<p>Display Plane 5 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
4	<p>Display Plane 5 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
3	<p>Display Plane 5 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
2	<p>Display Plane 4 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
1	<p>Display Plane 4 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

0	<p>Display Plane 4 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

Wait For Event and Display Flip Flags Register 3

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	022B8h-022BBh		
Name:	SYNC_FLIP_STATUS_3		
ShortName:	SYNC_FLIP_STATUS_3_RCSUNIT_DISP		
Address:	222B8h-222BBh		
Name:	SYNC_FLIP_STATUS_3		
ShortName:	SYNC_FLIP_STATUS_3_BCSUNIT_DISP		
<p>This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</p>			
Programming Notes			
<p>Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.</p>			
<p>VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.</p>			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
29		Display Plane 18 Asynchronous Performance Flip Pending Wait Enable	
		Format:	Enable
<p>This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			
28		Display Plane 18 Asynchronous Flip Pending Wait Enable	
		Format:	Enable
<p>This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>			

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

27	<p>Display Plane 18 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
26	<p>Display Plane 18 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
25	<p>Display Plane 18 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
24	<p>Display Plane 17 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
23	<p>Display Plane 17 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
22	<p>Display Plane 17 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

21	<p>Display Plane 17 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
20	<p>Display Plane 17 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
19	<p>Display Plane 16 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 1616 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
18	<p>Display Plane 16 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
17	<p>Display Plane 16 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
16	<p>Display Plane 16 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

15	<p>Display Plane 16 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
14	<p>Display Plane 15 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
13	<p>Display Plane 15 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
12	<p>Display Plane 15 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
11	<p>Display Plane 15 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
10	<p>Display Plane 15 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

9	<p>Display Plane 14 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
8	<p>Display Plane 14 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
7	<p>Display Plane 14 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
6	<p>Display Plane 14 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
5	<p>Display Plane 14 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
4	<p>Display Plane 13 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 50%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

3	<p>Display Plane 13 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
2	<p>Display Plane 13 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
1	<p>Display Plane 13 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
0	<p>Display Plane 13 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

Wait For Event and Display Flip Flags Register 4

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	022C0h-022C3h		
Name:	SYNC_FLIP_STATUS_4		
ShortName:	SYNC_FLIP_STATUS_4_RCSUNIT_DISP		
Address:	222C0h-222C3h		
Name:	SYNC_FLIP_STATUS_4		
ShortName:	SYNC_FLIP_STATUS_4_BCSUNIT_DISP		
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.			
Programming Notes			
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.			
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.			
DWord	Bit	Description	
0	31:30	Reserved	
		Access:	RO
		Format:	MBZ
29		Display Plane 24 Asynchronous Performance Flip Pending Wait Enable	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			
28		Display Plane 24 Asynchronous Flip Pending Wait Enable	
		Format:	Enable
This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).			

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

27	<p>Display Plane 24 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
26	<p>Display Plane 24 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
25	<p>Display Plane 24 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
24	<p>Display Plane 23 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
23	<p>Display Plane 23 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
22	<p>Display Plane 23 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

21	<p>Display Plane 23 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
20	<p>Display Plane 23 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
19	<p>Display Plane 22 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
18	<p>Display Plane 22 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
17	<p>Display Plane 22 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
16	<p>Display Plane 22 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

15	<p>Display Plane 22 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
14	<p>Display Plane 21 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
13	<p>Display Plane 21 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
12	<p>Display Plane 21 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
11	<p>Display Plane 21 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
10	<p>Display Plane 21 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

9	<p>Display Plane 20 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
8	<p>Display Plane 20 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
7	<p>Display Plane 20 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
6	<p>Display Plane 20 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
5	<p>Display Plane 20 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
4	<p>Display Plane 19 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

3	<p>Display Plane 19 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
2	<p>Display Plane 19 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
1	<p>Display Plane 19 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
0	<p>Display Plane 19 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

Wait For Event and Display Flip Flags Register 5

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

Register Space: MMIO: 0/2/0
 Access: R/W
 Size (in bits): 32
 _Custom_GTIReset: DEV

Address: 022C4h-022C7h
 Name: SYNC_FLIP_STATUS_5
 ShortName: SYNC_FLIP_STATUS_5_RCSUNIT_DISP

Address: 222C4h-222C7h
 Name: SYNC_FLIP_STATUS_5
 ShortName: SYNC_FLIP_STATUS_5_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description				
0	31:30	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
	29	<p>Display Plane 30 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable					
	28	<p>Display Plane 30 Asynchronous Flip Pending Wait Enable</p> <table border="1"> <tr> <td>Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable					

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

27	<p>Display Plane 30 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
26	<p>Display Plane 30 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
25	<p>Display Plane 30 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
24	<p>Display Plane 29 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
23	<p>Display Plane 29 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
22	<p>Display Plane 29 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

21	<p>Display Plane 29 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
20	<p>Display Plane 29 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
19	<p>Display Plane 28 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
18	<p>Display Plane 28 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
17	<p>Display Plane 28 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
16	<p>Display Plane 28 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

15	<p>Display Plane 28 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
14	<p>Display Plane 27 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
13	<p>Display Plane 27 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
12	<p>Display Plane 27 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
11	<p>Display Plane 27 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
10	<p>Display Plane 27 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

9	<p>Display Plane 26 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
8	<p>Display Plane 26 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
7	<p>Display Plane 26 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
6	<p>Display Plane 26 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
5	<p>Display Plane 26 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
4	<p>Display Plane 25 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

3	<p>Display Plane 25 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
2	<p>Display Plane 25 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
1	<p>Display Plane 25 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
0	<p>Display Plane 25 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		

Wait For Event and Display Flip Flags Register 6

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	021F8h-021FBh		
Name:	SYNC_FLIP_STATUS_6		
ShortName:	SYNC_FLIP_STATUS_6_RCSUNIT_DISP		
Address:	221F8h-221FBh		
Name:	SYNC_FLIP_STATUS_6		
ShortName:	SYNC_FLIP_STATUS_6_BCSUNIT_DISP		
<p>This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.</p>			
Programming Notes			
<p>Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.</p>			
<p>VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.</p>			
DWord	Bit	Description	
0	31:19	Reserved	
		Access:	RO
		Format:	MBZ
18		Display Pipe D Scan Line Event Pending	
		Format:	Enable
<p>This field indicates scan line event operation is pending from Display Pipe D. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Pipe D and gets reset on scan line event completion for Display Plane-C.</p>			
17		Display Pipe D Scan Line Wait Enable	
		Format:	Enable
<p>This field enables a wait while a Display Pipe D Scan Line condition exists. This condition is defined as the start of the scan line specified in the Pipe D Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.</p>			

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

16	<p>Display Pipe D Vertical Blank Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait until the next Display Pipe D Vertical Blank event occurs. This event is defined as the start of the next Display Pipe D vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).</p>	Format:	Enable		
Format:	Enable				
15:10	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				
9	<p>Display Plane 32 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
8	<p>Display Plane 32 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
7	<p>Display Plane 32 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable		
Format:	Enable				
6	<p>Display Plane 32 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable		
Format:	Enable				

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

5	<p>Display Plane 32 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
4	<p>Display Plane 31 Asynchronous Performance Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
3	<p>Display Plane 31 Asynchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
2	<p>Display Plane 31 Asynchronous Display Flip Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).</p>	Format:	Enable
Format:	Enable		
1	<p>Display Plane 31 Synchronous Flip Pending Wait Enable</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		
0	<p>Display Plane 31 Synchronous Flip Display Pending</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 70%;">Format:</td> <td>Enable</td> </tr> </table> <p>This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.</p>	Format:	Enable
Format:	Enable		



Watchdog Counter

PR_CTR - Watchdog Counter	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02190h-02193h
Name:	Watchdog Counter
ShortName:	PR_CTR_RCSUNIT
Address:	18190h-18193h
Name:	Watchdog Counter
ShortName:	PR_CTR_POCSUNIT
Address:	22190h-22193h
Name:	Watchdog Counter
ShortName:	PR_CTR_BCSUNIT
Address:	1C0190h-1C0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT0
Address:	1C4190h-1C4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT1
Address:	1C8190h-1C8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT0
Address:	1D0190h-1D0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT2
Address:	1D4190h-1D4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT3
Address:	1D8190h-1D8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT1
Address:	1E0190h-1E0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT4

PR_CTR - Watchdog Counter				
Address:	1E4190h-1E4193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VCSUNIT5			
Address:	1E8190h-1E8193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VECSUNIT2			
Address:	1F0190h-1F0193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VCSUNIT6			
Address:	1F4190h-1F4193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VCSUNIT7			
Address:	1F8190h-1F8193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_VECSUNIT3			
Address:	1A190h-1A193h			
Name:	Watchdog Counter			
ShortName:	PR_CTR_CCSUNIT0			
DWord	Bit	Description		
0	31:0	<p>Counter Value</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Format:</td> <td style="text-align: center;">U32</td> </tr> </table> <p>This register reflects the render watchdog counter value itself. It cannot be written to.</p>	Format:	U32
Format:	U32			



Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02178h-0217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_RCSUNIT
Address:	18178h-1817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_POCSUNIT
Address:	22178h-2217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_BCSUNIT
Address:	1C0178h-1C017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT0
Address:	1C4178h-1C417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT1
Address:	1C8178h-1C817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT0
Address:	1D0178h-1D017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT2
Address:	1D4178h-1D417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT3
Address:	1D8178h-1D817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT1
Address:	1E0178h-1E017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT4

PR_CTR_CTL - Watchdog Counter Control										
Address:	1E4178h-1E417Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_VCSUNIT5									
Address:	1E8178h-1E817Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_VECSUNIT2									
Address:	1F0178h-1F017Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_VCSUNIT6									
Address:	1F4178h-1F417Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_VCSUNIT7									
Address:	1F8178h-1F817Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_VECSUNIT3									
Address:	1A178h-1A17Bh									
Name:	Watchdog Counter Control									
ShortName:	PR_CTR_CTL_CCSUNIT0									
Programming Notes										
<p>Ring Buffer Mode of scheduling SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesn't stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. Execution List Mode of Scheduling: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. On a context switch Watch Dog Counter Control and Watch dog Threshold are context save restored, whereas watch dog counter gets reset to 0x0 and remains disabled until it gets enabled by another context during context restore or due to explicit programming. Watch dog counter value doesn't get accumulated across multiple submissions of a given context.</p>										
<p>This register functionality is not supported and must not be programmed for Position command streamer.</p>										
DWord	Bit	Description								
0	31	<p>Count Select</p> <table border="1" style="width: 100%;"> <tr> <td>Format:</td> <td>U1</td> </tr> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> <tr> <td>0h</td> <td>[Default]</td> <td>Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the Time Stamp</td> </tr> </table>	Format:	U1	Value	Name	Description	0h	[Default]	Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the Time Stamp
Format:	U1									
Value	Name	Description								
0h	[Default]	Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the Time Stamp								

PR_CTR_CTL - Watchdog Counter Control		
		Bases subsection in Power Management chapter.
	1h	Use the fixed function clock (csclk) to increment the watchdog count
	30:0	<p>Counter Logic Op</p> <p>Default Value: 1h</p> <p>This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.</p>

Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0217Ch-0217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_RCSUNIT
Address:	1817Ch-1817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_POCSUNIT
Address:	2217Ch-2217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_BCSUNIT
Address:	1C017Ch-1C017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT0
Address:	1C417Ch-1C417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT1
Address:	1C817Ch-1C817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT0
Address:	1D017Ch-1D017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT2
Address:	1D417Ch-1D417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT3
Address:	1D817Ch-1D817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT1
Address:	1E017Ch-1E017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT4

PR_CTR_THRSH - Watchdog Counter Threshold

Address: 1E417Ch-1E417Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_VCSUNIT5

Address: 1E817Ch-1E817Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_VECSUNIT2

Address: 1F017Ch-1F017Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_VCSUNIT6

Address: 1F417Ch-1F417Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_VCSUNIT7

Address: 1F817Ch-1F817Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_VECSUNIT3

Address: 1A17Ch-1A17Fh
 Name: Watchdog Counter Threshold
 ShortName: PR_CTR_THRSH_CCSUNIT0

Programming Notes

This register functionality is not supported and must not be programmed for Position command streamer.

This register must never be programmed with zero. This will cause the watchdog counter to exceed and not allow the engine to go into IDLE state.

DWord	Bit	Description				
0	31:0	<p>Counter Logic Threshold</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 60%;">Default Value:</td> <td>00145855h</td> </tr> <tr> <td>Format:</td> <td>U32</td> </tr> </table> <p>This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.</p>	Default Value:	00145855h	Format:	U32
Default Value:	00145855h					
Format:	U32					

WD_27_M

WD_27_M								
Register Space:	MMIO: 0/2/0							
Access:	R/W							
Size (in bits):	32							
Address:	6E524h-6E527h							
Name:	WD0 27 MHz M							
ShortName:	WD_27_M_0							
Reset:	soft							
Address:	6ED24h-6ED27h							
Name:	WD1 27 MHz M							
ShortName:	WD_27_M_1							
Reset:	soft							
DWord	Bit	Description						
0	31	Counter Force This field forces the 27 MHz counter to enabled even if the WD function is disabled. This may be necessary when WD audio is used while WD video is disabled.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>1b</td> <td>Force Enabled</td> </tr> <tr> <td>0b</td> <td>Do Not Force</td> </tr> </tbody> </table>	Value	Name	1b	Force Enabled	0b	Do Not Force
		Value	Name					
		1b	Force Enabled					
	0b	Do Not Force						
	30:24	Reserved Access: RO Format: MBZ						
	23:0	WD Link M This field specifies the M value for the 27 MHz clock. Link M / Link N = 27 MHz / CD clock frequency See the Sequences for Changing CD Clock Frequency for the values to use.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000002h</td> <td>2 [Default]</td> <td>M=2</td> </tr> </tbody> </table>	Value	Name	Description	000002h	2 [Default]	M=2
	Value	Name	Description					
	000002h	2 [Default]	M=2					



WD_27_N

WD_27_N						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	6E528h-6E52Bh					
Name:	WD0 27 MHz N					
ShortName:	WD_27_N_0					
Reset:	soft					
Address:	6EC28h-6EC2Bh					
Name:	WD1 27 MHz N					
ShortName:	WD_27_N_1					
Reset:	soft					
DWord	Bit	Description				
0	31:24	Reserved				
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO					
Format:	MBZ					
0	23:0	WD Link N				
		This field specifies the N value for the 27 MHz clock. Link M / Link N = 27 MHz / CD clock frequency				
		See the Sequences for Changing CD Clock Frequency for the values to use.				
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000019h</td> <td>25 [Default]</td> <td>N=25</td> </tr> </tbody> </table>	Value	Name	Description	000019h
Value	Name	Description				
000019h	25 [Default]	N=25				

WD_FRAME_STATUS

WD_FRAME_STATUS																												
Register Space:	MMIO: 0/2/0																											
Access:	RO																											
Size (in bits):	32																											
Address:	6E568h-6E56Bh																											
Name:	WD0 Frame Status																											
ShortName:	WD_FRAME_STATUS_0																											
Reset:	soft																											
Address:	6ED68h-6ED6Bh																											
Name:	WD1 Frame Status																											
ShortName:	WD_FRAME_STATUS_1																											
Reset:	soft																											
DWord	Bit	Description																										
0	31	Frame Complete <table border="1"> <tr> <td>Access:</td> <td>R/WC</td> </tr> </table> <p>This field is a sticky bit set when WD fully completes a frame. Clear by writing a 1 to it.</p>	Access:	R/WC																								
	Access:	R/WC																										
	30:27	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ																						
	Access:	RO																										
	Format:	MBZ																										
	26:24	WD State <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> </table> <p>This field indicates the live state of WD capture.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>IDLE</td> <td>Reset state</td> </tr> <tr> <td>001b</td> <td>CAPSTART</td> <td>Start timing generator for normal capture</td> </tr> <tr> <td>010b</td> <td>FRAME_START</td> <td>Send framestart to display pipe</td> </tr> <tr> <td>011b</td> <td>CAPACTIVE</td> <td>Capturing data</td> </tr> <tr> <td>100b</td> <td>TG_DONE</td> <td>Completed writing pixels. Waiting for frame completion.</td> </tr> <tr> <td>101b</td> <td>WDX_DONE</td> <td>Fully completed frame. Waiting to start next frame.</td> </tr> <tr> <td>110b</td> <td>QUICK_CAP</td> <td>Quick capture entry</td> </tr> </tbody> </table>	Access:	RO	Value	Name	Description	000b	IDLE	Reset state	001b	CAPSTART	Start timing generator for normal capture	010b	FRAME_START	Send framestart to display pipe	011b	CAPACTIVE	Capturing data	100b	TG_DONE	Completed writing pixels. Waiting for frame completion.	101b	WDX_DONE	Fully completed frame. Waiting to start next frame.	110b	QUICK_CAP	Quick capture entry
	Access:	RO																										
	Value	Name	Description																									
	000b	IDLE	Reset state																									
	001b	CAPSTART	Start timing generator for normal capture																									
010b	FRAME_START	Send framestart to display pipe																										
011b	CAPACTIVE	Capturing data																										
100b	TG_DONE	Completed writing pixels. Waiting for frame completion.																										
101b	WDX_DONE	Fully completed frame. Waiting to start next frame.																										
110b	QUICK_CAP	Quick capture entry																										
23	Reserved																											
22:21	Reserved <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ																							
Access:	RO																											
Format:	MBZ																											
20	Reserved																											



WD_FRAME_STATUS		
	19:0	Reserved
		Access: RO
		Format: MBZ

WD_IIR

WD_IIR								
Register Space:	MMIO: 0/2/0							
Access:	R/WC							
Size (in bits):	32							
Address:	6E564h-6E567h							
Name:	WD0 Interrupt Identity							
ShortName:	WD_IIR_0							
Reset:	soft							
Address:	6ED64h-6ED67h							
Name:	WD1 Interrupt Identity							
ShortName:	WD_IIR_1							
Reset:	soft							
See the WD interrupt bit definition to find the source event for each interrupt bit.								
DWord	Bit	Description						
0	31:16	Reserved						
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ		
Access:	RO							
Format:	MBZ							
	15:0	Interrupt Identity Bits						
		This field holds the persistent values of the WD interrupt bits which are unmasked by the WD_IMR. Bits set in this register will propagate to the WD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.						
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Condition Not Detected</td> </tr> <tr> <td>1b</td> <td>Condition Detected</td> </tr> </tbody> </table>	Value	Name	0b	Condition Not Detected	1b	Condition Detected
		Value	Name					
0b	Condition Not Detected							
1b	Condition Detected							



WD_IMR

WD_IMR										
Register Space:	MMIO: 0/2/0									
Access:	R/W									
Size (in bits):	32									
Address:	6E560h-6E563h									
Name:	WD0 Interrupt Mask									
ShortName:	WD_IMR_0									
Reset:	soft									
Address:	6ED60h-6ED63h									
Name:	WD1 Interrupt Mask									
ShortName:	WD_IMR_1									
Reset:	soft									
See the WD interrupt bit definition to find the source event for each interrupt bit.										
DWord	Bit	Description								
0	31:16	Reserved								
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ				
Access:	RO									
Format:	MBZ									
	15:0	Interrupt Mask Bits								
		This field contains a bit mask which selects which WD events are reported in the WD_IIR.								
		<table border="1"> <thead> <tr> <th>Value</th> <th>Name</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not Masked</td> </tr> <tr> <td>1b</td> <td>Masked</td> </tr> <tr> <td>0000FFFFh</td> <td>All interrupts masked [Default]</td> </tr> </tbody> </table>	Value	Name	0b	Not Masked	1b	Masked	0000FFFFh	All interrupts masked [Default]
		Value	Name							
0b	Not Masked									
1b	Masked									
0000FFFFh	All interrupts masked [Default]									

WD_PERF_CNT

WD_PERF_CNT		
Register Space:	MMIO: 0/2/0	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	6E55Ch-6E55Fh	
Name:	WD0 Performance Counter	
ShortName:	WD_PERF_CNT_0	
Reset:	soft	
Address:	6ED5Ch-6ED5Fh	
Name:	WD1 Performance Counter	
ShortName:	WD_PERF_CNT_1	
Reset:	soft	
DWord	Bit	Description
0	31:24	Reserved
		Access: RO
	Format: MBZ	
	23:0	WD Perf Cnt This field increments every millisecond while capturing. It does not count the time after capture is completed and waiting for the next capsync. Writes to this register will set the count to the written value, then it will increment from that value onwards.



WD_STRIDE

WD_STRIDE					
Register Space:	MMIO: 0/2/0				
Access:	Double Buffered				
Size (in bits):	32				
_Custom_Display_DoubleBufferUpdatePoint: Start of capture sync or transcoder not enabled					
Address:	6E510h-6E513h				
Name:	WD0 Stride				
ShortName:	WD_STRIDE_0				
Reset:	soft				
Address:	6ED10h-6ED13h				
Name:	WD1 Stride				
ShortName:	WD_STRIDE_1				
Reset:	soft				
DWord	Bit	Description			
0	31:16	Reserved			
		<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:
	Access:	RO			
Format:	MBZ				
15:6	<p>WD Stride This field specifies the stride bits 15:6. This value is used to determine the line to line increment for the capture data writes. This field is programmed in units of 64 bytes.</p> <p style="text-align: center;">Programming Notes</p> <p>The stride has to be at least large enough to encompass all the pixels in a line, and rounded up to 64 byte alignment. Stride bytes \geq $\text{CEILING}[(\text{Horizontal Active} * \text{WD Color Mode bytes per pixel}) / 64] * 64$</p> <p style="text-align: center;">Restriction</p> <p>The stride is limited to a maximum of 32K bytes.</p>				
5:0	Reserved				
	<table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
Access:	RO				
Format:	MBZ				

WD_SURF

WD_SURF												
Register Space:	MMIO: 0/2/0											
Access:	Double Buffered											
Size (in bits):	32											
_Custom_Display_DoubleBufferUpdatePoint: Start of capture sync or transcoder not enabled												
Address:	6E514h-6E517h											
Name:	WD0 Surface Base Address											
ShortName:	WD_SURF_0											
Reset:	soft											
Address:	6ED14h-6ED17h											
Name:	WD1 Surface Base Address											
ShortName:	WD_SURF_1											
Reset:	soft											
Writes to this register arm WD registers.												
DWord	Bit	Description										
0	31:12	<p>WD Surface Base Address</p> <table border="1"> <tr> <td>Format:</td> <td>GraphicsAddress[31:12]</td> </tr> </table> <p>This address specifies the surface base address bits 31:12. It is mapped to physical pages through the global GTT.</p> <table border="1"> <tr> <th colspan="2" style="text-align: center;">Programming Notes</th> </tr> <tr> <td colspan="2">The mapped pages must be located outside graphics data stolen memory.</td> </tr> </table> <table border="1"> <tr> <th colspan="2" style="text-align: center;">Restriction</th> </tr> <tr> <td colspan="2">It must be at least 4KB aligned.It must use linear memory.</td> </tr> </table>	Format:	GraphicsAddress[31:12]	Programming Notes		The mapped pages must be located outside graphics data stolen memory.		Restriction		It must be at least 4KB aligned.It must use linear memory.	
	Format:	GraphicsAddress[31:12]										
Programming Notes												
The mapped pages must be located outside graphics data stolen memory.												
Restriction												
It must be at least 4KB aligned.It must use linear memory.												
11:0	<p>Reserved</p> <table border="1"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ							
Access:	RO											
Format:	MBZ											



WD_TAIL_CFG

WD_TAIL_CFG						
Register Space:	MMIO: 0/2/0					
Access:	Double Buffered					
Size (in bits):	32					
_Custom_Display_DoubleBufferArmedBy:	Write to WD_SURF or WD not enabled					
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled; after armed					
Address:	6E520h-6E523h					
Name:	WD0 Tail Pointer Config					
ShortName:	WD_TAIL_CFG_0					
Reset:	soft					
Address:	6ED20h-6ED23h					
Name:	WD1 Tail Pointer Config					
ShortName:	WD_TAIL_CFG_1					
Reset:	soft					
DWord	Bit	Description				
<p style="text-align: center;">0</p> <p>If Delay < Period; first tail pointer is sent at the next multiple of Period, after the Delay. If Delay Period; first tail pointer is set at the Period.</p> <p>The tail pointer is also sent at the end of the frame. If Delay or Period are greater than the vertical size, only the tail pointer at the end of the frame is sent.</p>	31:28	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
	Format:	MBZ				
	27:16	<p>Tail Initial Update Delay</p> <p>This field specifies the minimum number of scan lines that WD capture must wait for at the beginning of each frame before any tail pointer updates will be sent to media. This must be programmed smaller than the vertical active size.</p>				
15:12	<p>Reserved</p> <table border="1" style="width: 100%;"> <tr> <td>Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ	
Access:	RO					
Format:	MBZ					
11:4	<p>Tail Update Period</p> <table border="1" style="width: 100%;"> <tr> <td>Default Value:</td> <td>01h 16 lines</td> </tr> </table> <p>This field specifies the number of scan lines that the WD capture will write back to memory before sending each tail pointer message to media. This field is programmed in multiples of 16 scan lines.</p> <table border="1" style="width: 100%; background-color: #e6f2ff;"> <tr> <td style="text-align: center;">Restriction</td> </tr> <tr> <td>A value of 0 is not valid.</td> </tr> </table>	Default Value:	01h 16 lines	Restriction	A value of 0 is not valid.	
Default Value:	01h 16 lines					
Restriction						
A value of 0 is not valid.						

WD_TAIL_CFG		
	3:0	Reserved
		Access: RO
		Format: MBZ



WD_TAIL_CFG2

WD_TAIL_CFG2			
Register Space:	MMIO: 0/2/0		
Access:	Double Buffered		
Size (in bits):	32		
_Custom_Display_DoubleBufferArmedBy:	Write to WD_SURF or WD not enabled		
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled; after armed		
Address:	6E52Ch-6E52Fh		
Name:	WD0 Tail Pointer Config2		
ShortName:	WD_TAIL_CFG2_0		
Reset:	soft		
Address:	6ED2Ch-6ED2Fh		
Name:	WD1 Tail Pointer Config2		
ShortName:	WD_TAIL_CFG2_1		
Reset:	soft		
DWord	Bit	Description	
0	31:16	Reserved	
		Access:	RO
		Format:	MBZ
	15:4	Tail Pointer Offset If during selective read/write we are compositing to smaller than a full resolution surface, this tail pointer offset is used to synchronize with the VDEnc relative to the full resolution surface. This field is programmed in multiples of 16 scan lines.	
	3:0	Reserved	
		Access:	RO
Format:		MBZ	

WIDI Session 0

WIDI_SESSION_0 - WIDI Session 0						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
_Custom_GTIReset:	BUS					
Address:	00ED0h					
DWord	Bit	Description				
0	31:0	Static Data <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Scratch registers provided for Display/VEnc/GUC WIDI Session access	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					



WIDI Session 1

WIDI_SESSION_1 - WIDI Session 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00ED4h	
DWord	Bit	Description
0	31:0	Static Data
		Default Value: 0b
		Access: R/W
		Scratch registers provided for Display/VEnc/GUC WIDI Session access

WIDI Session 2

WIDI_SESSION_2 - WIDI Session 2						
Register Space:	MMIO: 0/2/0					
Size (in bits):	32					
_Custom_GTIReset:	BUS					
Address:	00ED8h					
DWord	Bit	Description				
0	31:0	Static Data <table border="1"> <tr> <td>Default Value:</td> <td>0b</td> </tr> <tr> <td>Access:</td> <td>R/W</td> </tr> </table> Scratch registers provided for Display/VEnc/GUC WIDI Session access	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					



WIDI Session 3

WIDI_SESSION_3 - WIDI Session 3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EDCh	
DWord	Bit	Description
0	31:0	Static Data
		Default Value: 0b
		Access: R/W
		Scratch registers provided for Display/VEnc/GUC WIDI Session access

WiDi VDEnc Stall counter

WIDI_VDENC_STALL_CNTR - WiDi VDEnc Stall counter		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	1C2D94h-1C2D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG0	
Address:	1C6D94h-1C6D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG1	
Address:	1D2D94h-1D2D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG2	
Address:	1D6D94h-1D6D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG3	
Address:	1E2D94h-1E2D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG4	
Address:	1E6D94h-1E6D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG5	
Address:	1F2D94h-1F2D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG6	
Address:	1F6D94h-1F6D97h	
Name:	WiDi mode VDENC stall counter value	
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG7	
This register has stall counter for the VDENC. In an ideal case, this value should be zero.		
DWord	Bit	Description
0	31:0	WiDi Stall clock count
Access:		RO



Window Hardware Generated Clear Value

WMHWCLRVAL - Window Hardware Generated Clear Value		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	05524h	
DWord	Bit	Description
0	31:0	WM HW Generated Clear Value Format: MBZ This register stores HW generated Z clear value.

WM_LINETIME

WM_LINETIME						
Register Space:	MMIO: 0/2/0					
Access:	R/W					
Size (in bits):	32					
Address:	45270h-45273h					
Name:	Pipe Watermark Line Time					
ShortName:	WM_LINETIME_A					
Reset:	soft					
Address:	45274h-45277h					
Name:	Pipe Watermark Line Time					
ShortName:	WM_LINETIME_B					
Reset:	soft					
Address:	45278h-4527Bh					
Name:	Pipe Watermark Line Time					
ShortName:	WM_LINETIME_C					
Reset:	soft					
Address:	4527Ch-4527Fh					
Name:	Pipe Watermark Line Time					
ShortName:	WM_LINETIME_D					
Reset:	soft					
DWord	Bit	Description				
0	31:9	Reserved <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Access:</td> <td>RO</td> </tr> <tr> <td>Format:</td> <td>MBZ</td> </tr> </table>	Access:	RO	Format:	MBZ
	Access:	RO				
Format:	MBZ					
8:0	Line Time This field specifies the line time for the current screen resolution in units of 0.125us. <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Programming Notes</th> </tr> <tr> <td>Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates.</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse; background-color: #e6f2ff;"> <tr> <th style="text-align: center;">Restriction</th> </tr> <tr> <td>The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (111111111b).</td> </tr> </table>	Programming Notes	Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates.	Restriction	The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (111111111b).	
Programming Notes						
Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer. Program the smallest line time when using multiple refresh rates.						
Restriction						
The line time value must be programmed before enabling any display low power watermark. Maximum supported line time is 63.875us (111111111b).						

WM_MISC

WM_MISC											
Register Space:	MMIO: 0/2/0										
Access:	R/W										
Size (in bits):	32										
Address:	45260h-45263h										
Name:	Watermark Miscellaneous										
ShortName:	WM_MISC										
Reset:	soft										
DWord	Bit	Description									
0	31	Reserved Format: PBC									
	30:28	Reserved									
	27	MIPI DBI Method This field controls the behavior for the TTNF calculation for MIPI DBI. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Value</th> <th style="width: 15%;">Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Calculated</td> <td>TTNF calculated in active area and all 1s outside of active. TTVBI all 1s.</td> </tr> <tr> <td>1b</td> <td>Simple</td> <td>TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.</td> </tr> </tbody> </table>	Value	Name	Description	0b	Calculated	TTNF calculated in active area and all 1s outside of active. TTVBI all 1s.	1b	Simple	TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.
	Value	Name	Description								
	0b	Calculated	TTNF calculated in active area and all 1s outside of active. TTVBI all 1s.								
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	26:20	Reserved Format: PBC									
	19:0	Reserved Access: RO Format: MBZ									