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Model of hybrid classical-quantum computing method

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Abstract

Here, a model of classical computing that uses an electric field is proposed. The model can be used to create a wireless logic circuit. In this model, an electric field is used to transfer bit signals. The transfer medium can be a semiconductor, an optical fiber, some other material, or a combination.

1) Hardware design of logic gates

The following four figures show the logic gates OR, AND, and NOT and a gate that combines AND and OR. The application of a parallel switch to the AND gate, a unique feature of the proposed concept, makes it possible to combine the AND gate with the OR gate as a single gate.

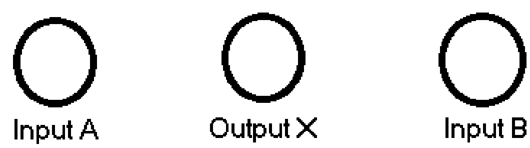


Fig. 1 OR gate. Inputs A and B each generate an electric field. The presence of an electric field indicates that the input is high. Output X conducts if either of A or B generates an electric field.

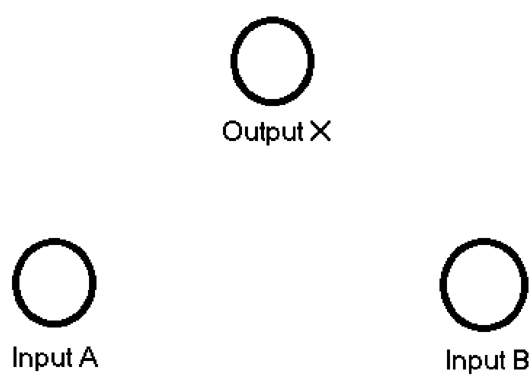


Fig. 2 AND gate. Output X is placed slightly away from inputs A and B. Therefore, it conducts only when both inputs generate an electric field at the same time.

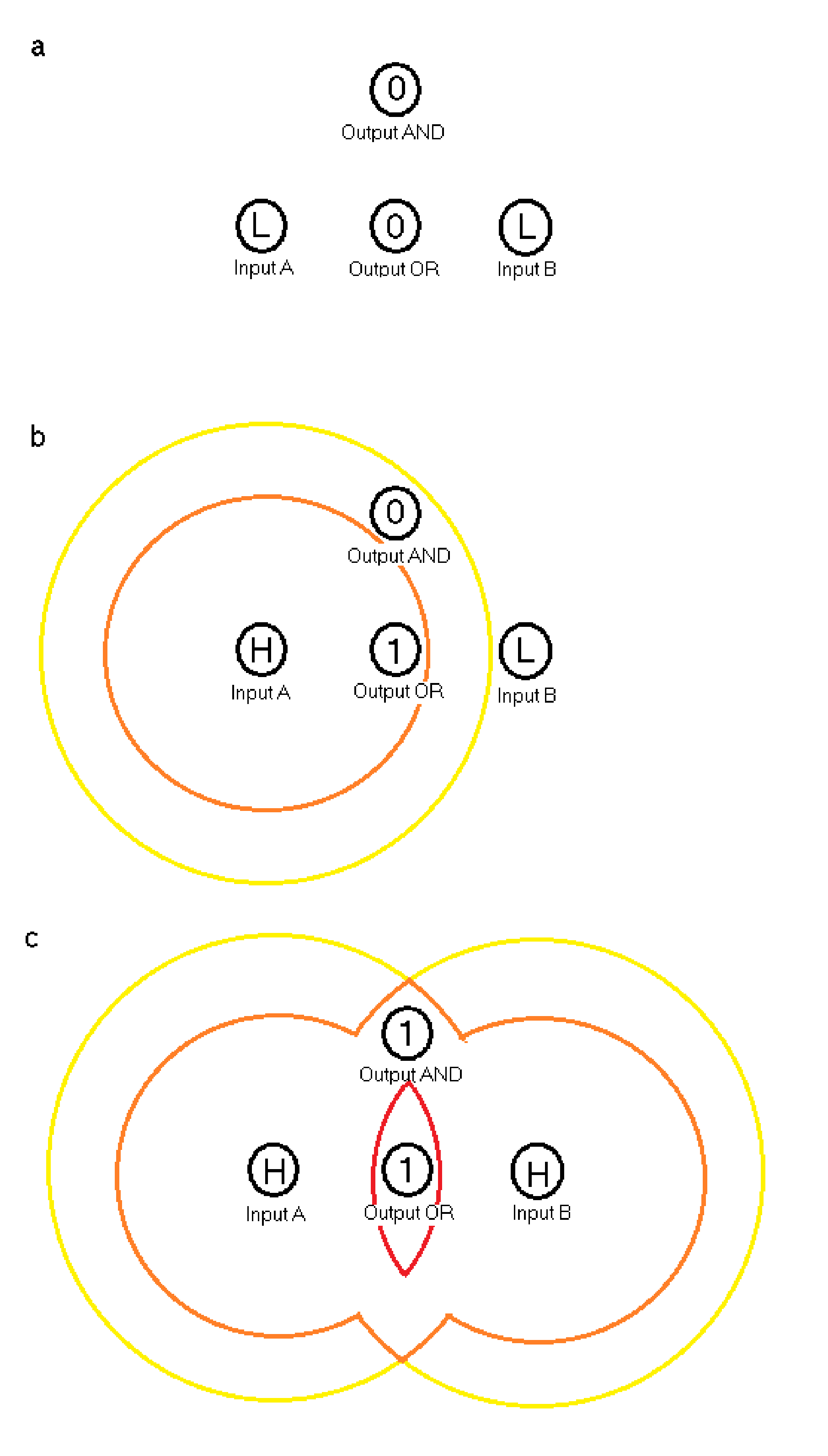


Fig. 3 Combo gate. a This gate combines an OR gate and an AND gate. **b** Input A is high and input B is low. **c** Inputs A and B are both high.

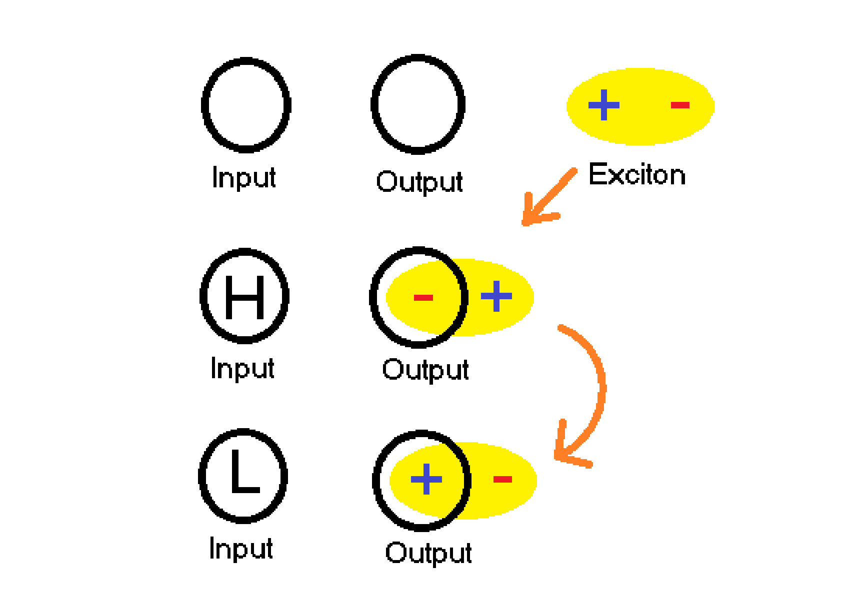


Fig. 4 NOT gate. A NOT gate could be embedded in logic boards as existing current modules or at quantum level operation. Trapping excitons at the output's edge could result in inverse output because the excitons are flipped by the electric field generated by the input.

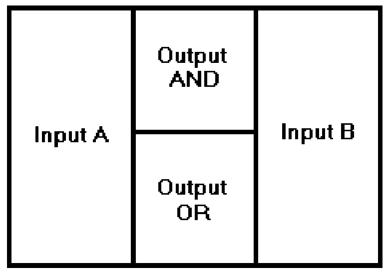
2) Conclusions

The proposed gate designs could be scaled down to the atomic scale by using graphene or carbon nanotubes. At larger scale, the proposed classical computing method may be used to overcome some existing hardware limitations.

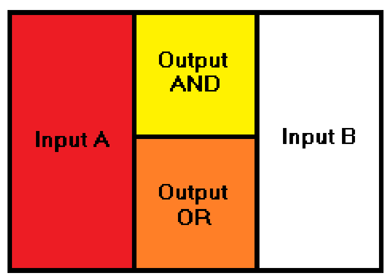
In the proposed model, the difference between the OR gate and the AND gate is the distance from the output to the inputs. The proposed concept is implemented using a semiconductor in the appendix. This makes it possible to build a gate that produces multiple outputs at once, similar to a quantum logic gate.

Appendix

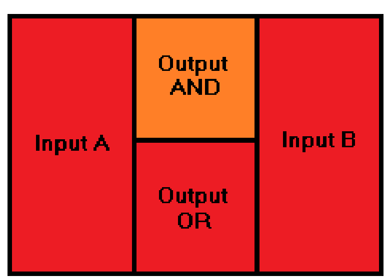
The following two figures show how existing semiconductors can be used to implement parallel switching for all outputs. This is a feasible approach that utilizes classical computing technology.



A	B	AND	OR
0	0	0	0

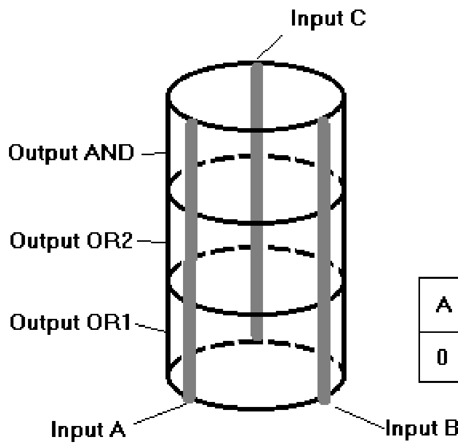


A	B	AND	OR
1	0	0	1

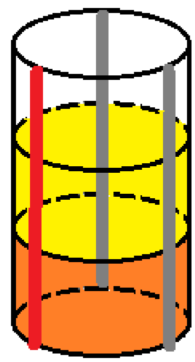


A	B	AND	OR
1	1	1	1

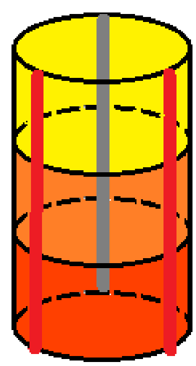
Fig. 5 Example of combo gate using a semiconductive layer. The OR block has a lower conduction threshold than that of the AND block. This is achieved using conductors with different characteristics for the two gate types.



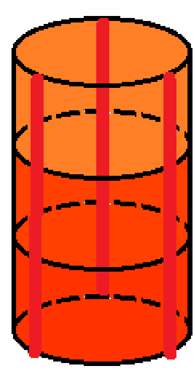
A	B	C	AND	OR1	OR2
0	0	0	0	0	0



A	B	C	AND	OR1	OR2
1	0	0	0	1	0



A	B	C	AND	OR1	OR2
1	1	0	0	1	1



A	B	C	AND	OR1	OR2
1	1	1	1	1	1

Fig. 6 Super combo (trinary) gate using semiconductive layer. The shown semiconductive layer consists of three inputs and outputs, respectively. The numbers of inputs and outputs can be changed.