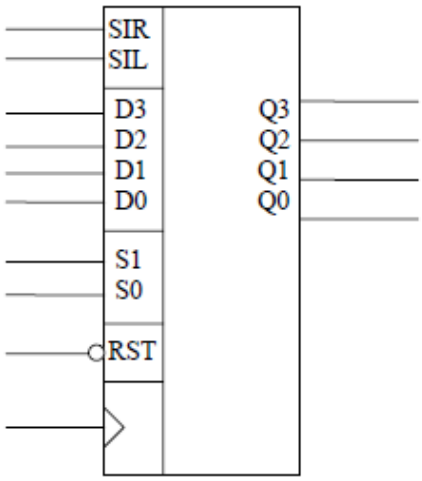
Design in VHDL a 4-bit universal shift register as presented below:



SIR – Serial Input Right
SIL – Serial Input Left
D3,…,D0 – Data Inputs
Q3,…,Q0 – Data Outputs
RST – Asynchronous Reset Input
S1,S0 – Operation Select Inputs

The operation of the universal register is described by the following truth table:

S1	S0	Action
0	0	Hold
0	1	Shift Left
1	0	Shift Right
1	1	Parallel Load