

Quartus 11.1sp2 Subscription edition (status: working)

The screenshot shows the Quartus II 64-bit IDE interface. The main window displays a Verilog HDL file named 'testing.v' with the following code:

```
1 module testing (
2     top_clkln_50, // clk in
3     rst, // sw0,
4     //sram1_signals
5     sram1_add,
6     sram1_ben,
7     sram1_oen,
8     sram1_wen,
9     sram1_data,
10    sram1_csn,
11    //sram2_signals
12    sram2_add,
13    sram2_ben,
14    sram2_oen,
15    sram2_wen,
16    sram2_data,
```

The left sidebar shows the Project Navigator with the entity 'testing' selected. The Tasks window shows the compilation process. The Messages window displays the following information:

- Info (209060): Started Programmer operation at Mon Nov 20 10:32:16 2017
- Info (209016): Configuring device index 1
- Info (209017): Device 1 contains JTAG ID code 0x020F70DD
- Info (209007): Configuration succeeded -- 1 device(s) configured
- Info (209011): Successfully performed operation(s)
- Info (209061): Ended Programmer operation at Mon Nov 20 10:32:23 2017

SignalTap in Quartus 11.1sp2 subscription edition (status: working)

The screenshot shows the SignalTap II Logic Analyzer interface. The top bar indicates 'Acquisition in progress'. The Instance Manager shows the following details:

Instance	Status	LES: 4918	Memory: 39936	Small: 0/0	Medium: 44/43	Large: 0/0
auto_s...	Offloading acq...	4918 cells	399360 bits	0 blocks	44 blocks	0 blocks

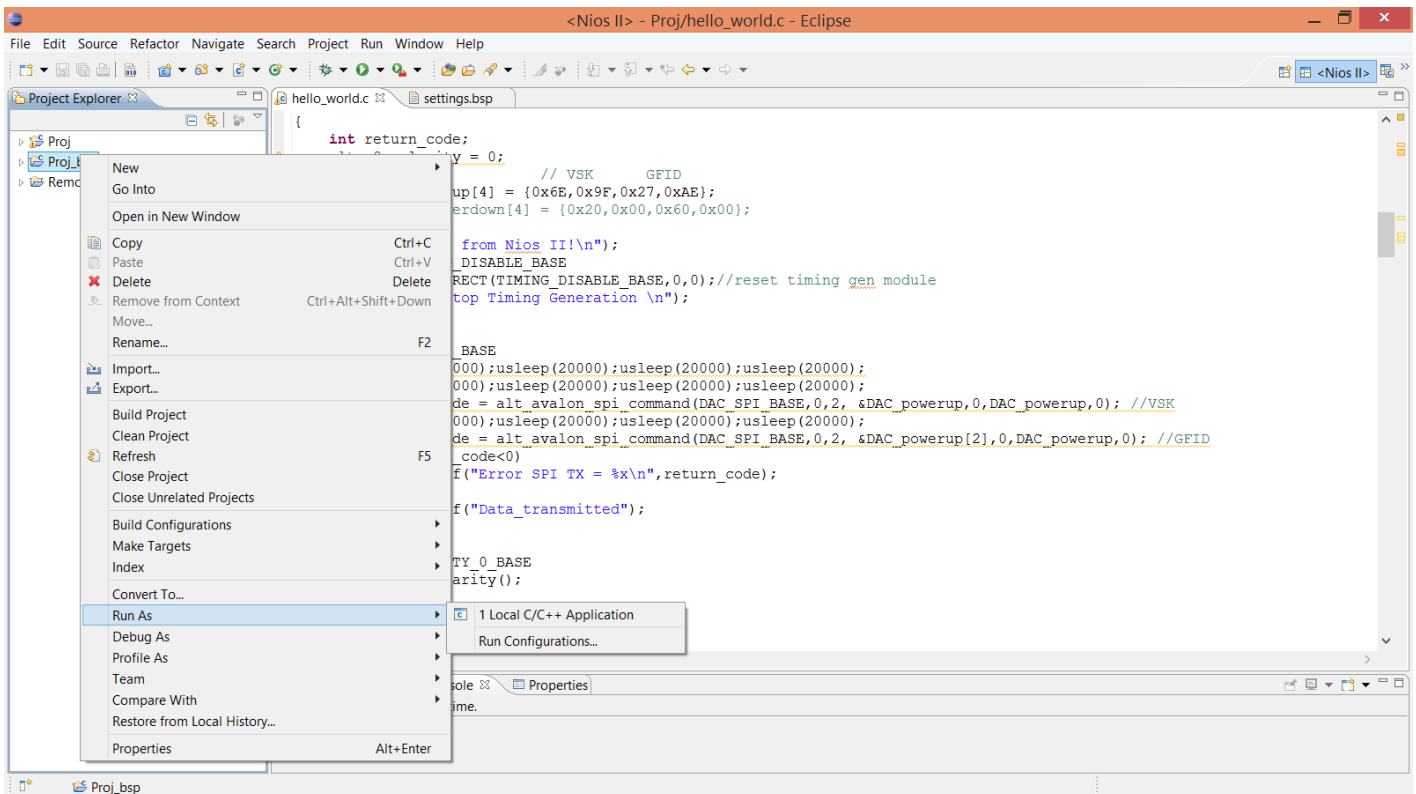
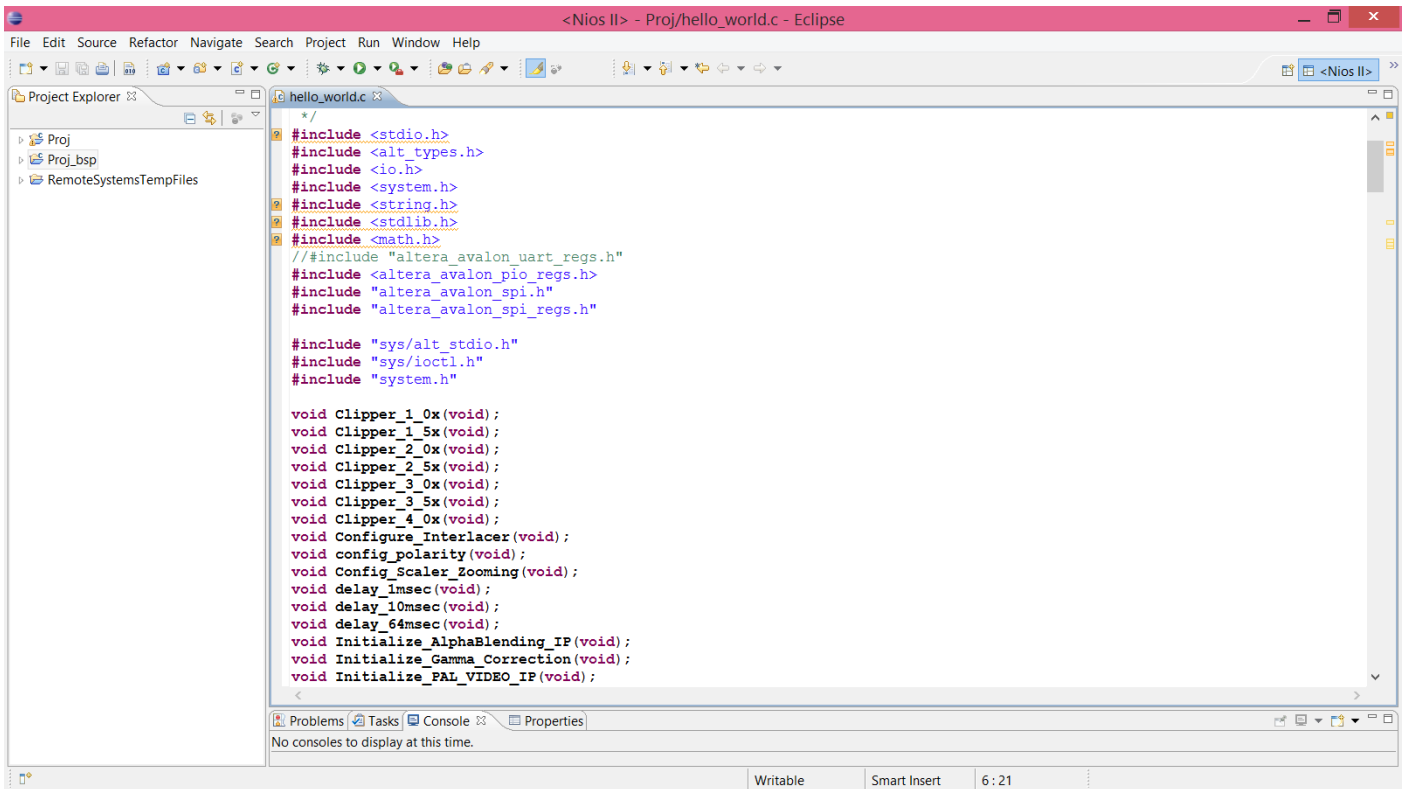
The right sidebar shows the JTAG Chain Configuration: JTAG ready. The Hardware is USB-Blaster [USB-0]. The Device is @1: EP3C120/EP4CE115 (0x). The SOF Manager is _Bring_test/testing.sof.

The main window displays a waveform capture with the following signals:

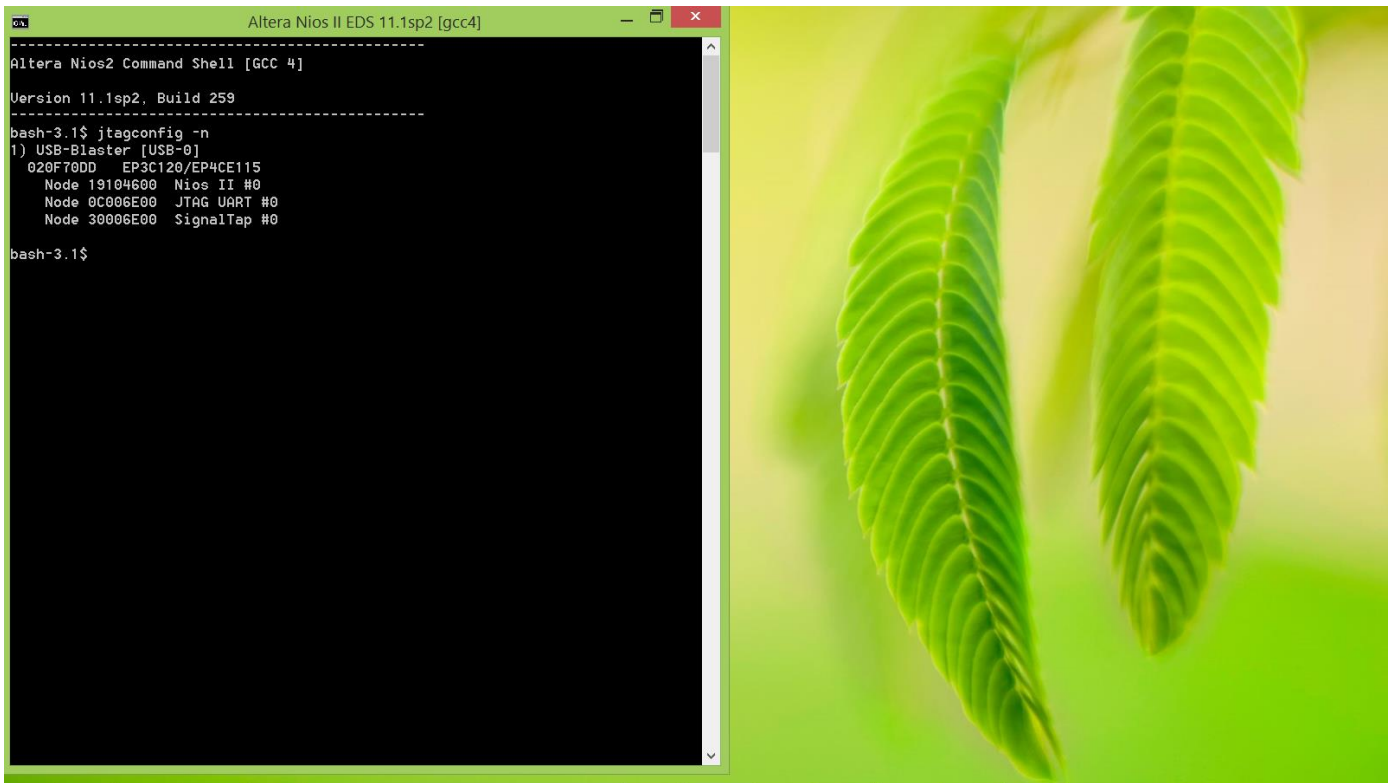
- top_clkln_50
- vid_blank
- vid_clk_out
- vid_data
- vid_sync
- bolo_video_path.u0|pal_out_clocked_video_underflow
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_data
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_ready
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_valid
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_startofpacket
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_endofpacket
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|din_ready
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|dout_data
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|dout_valid
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|dout_startofpacket
- bolo_video_path.u0|bolo_video_path_Frame_Buffer640x480.frame_buffer640x480|dout_endofpacket
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_0_ready
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_0_valid
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_0_data
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_0_startofpacket
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_0_endofpacket
- bolo_video_path.u0|bolo_video_path_Mixer.mixer|din_1_ready

The waveform shows a clock signal (top_clkln_50) and various data signals. The time axis ranges from -128 to 896. The data signals show values such as 000h, 0000h, and 1000h.

NiosII 11.1sp2 in Quartus 11.1 Subscription edition (status: not working)



NiosII 11.1sp2 Command Shell (jtagconfig command)



jtagconfig -n command

The screenshot shows a web browser window displaying the following content:

Example 4-1. jtagconfig Example Response

```
[SOPC Builder]$ jtagconfig -n  
1) USB-Blaster [USB-0]  
   020050DD EP1S40/_HARDCOPY_FPGA_PROTOTYPE  
     Node 11104600  
     Node 0C006E00
```

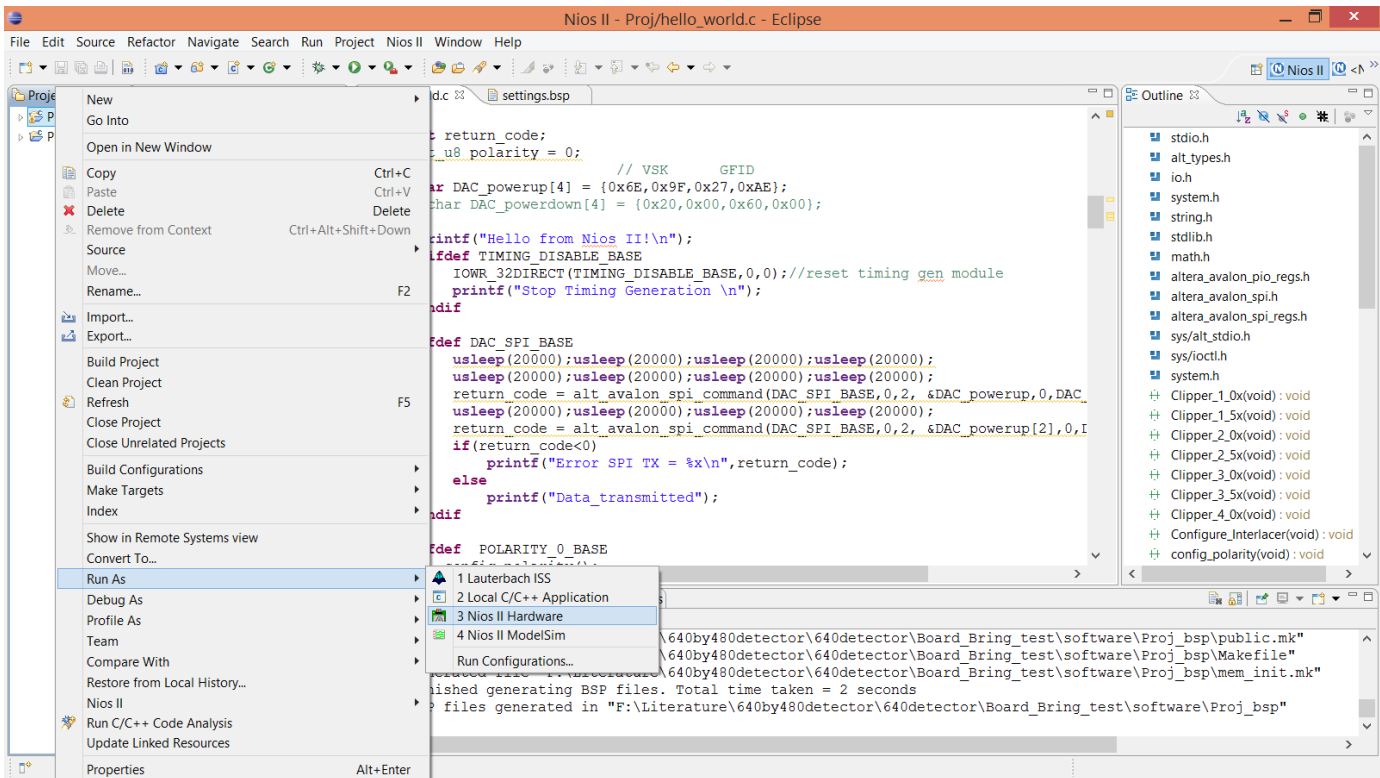
The information in the response varies, depending on the particular FPGA, its configuration, and the JTAG connection cable type. Table 4-1 describes the information that appears in the response in Example 4-1.

Table 4-1. Interpretation of jtagconfig Command Response

Value	Description
USB-Blaster [USB-0]	The type of cable. You can have multiple cables connected to your workstation.
EP1S40/_HARDCOPY_FPGA_PROTOTYPE	The device name, as identified by silicon identification number.
Node 11104600	The node number of a JTAG node inside the FPGA. The appearance of a node number between 11104600 and 11046FFF, inclusive, in this system's response confirms that you have a Nios II processor with a JTAG debug module.
Note 0C006E00	The node number of a JTAG node inside the FPGA. The appearance of a node number between 0C006E00 and 0C006EFF, inclusive, in this system's response confirms that you have a JTAG UART component.

The device name is read from the text file `pgm_parts.txt` in your Quartus® II installation. In Example 4-1, the name is `EP1S40/_HARDCOPY_FPGA_PROTOTYPE` because the silicon identification number on the JTAG chain for the FPGA device is `020050DD`, which maps to the names `EP1S40<device-specific name>`, a couple of which end in the string `_HARDCOPY_FPGA_PROTOTYPE`. The internal nodes are nodes on the system-level debug (SLD) hub. All ITAG communication to an Altera FPGA

NiosII 13.0 in Quartus 13.0 Free edition (status: working)



NiosII 13.0 Command Shell (jtagconfig command)

