



.JIC Flash programming procedure

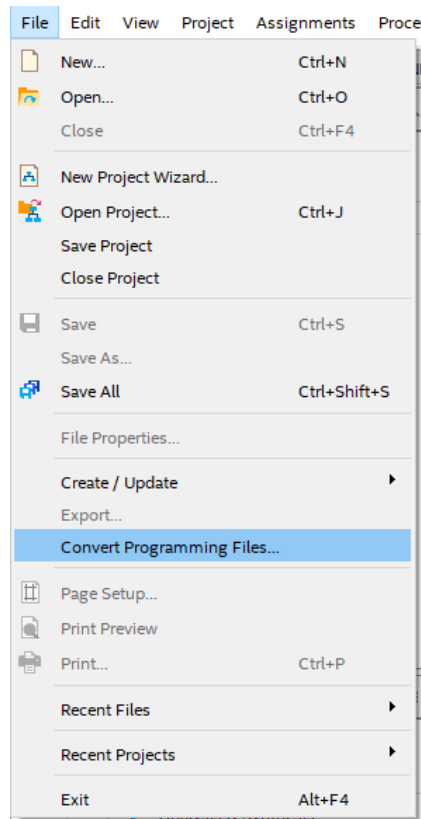
Flash programming procedure

- The following slides show how to create a jic file to program your flash using Quartus programmer.
- The example been created on Quartus 18.1
- The example requires a successful FOS and HEX files.

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Flash programming procedure

- 1- Go to File>> Convert Programming files

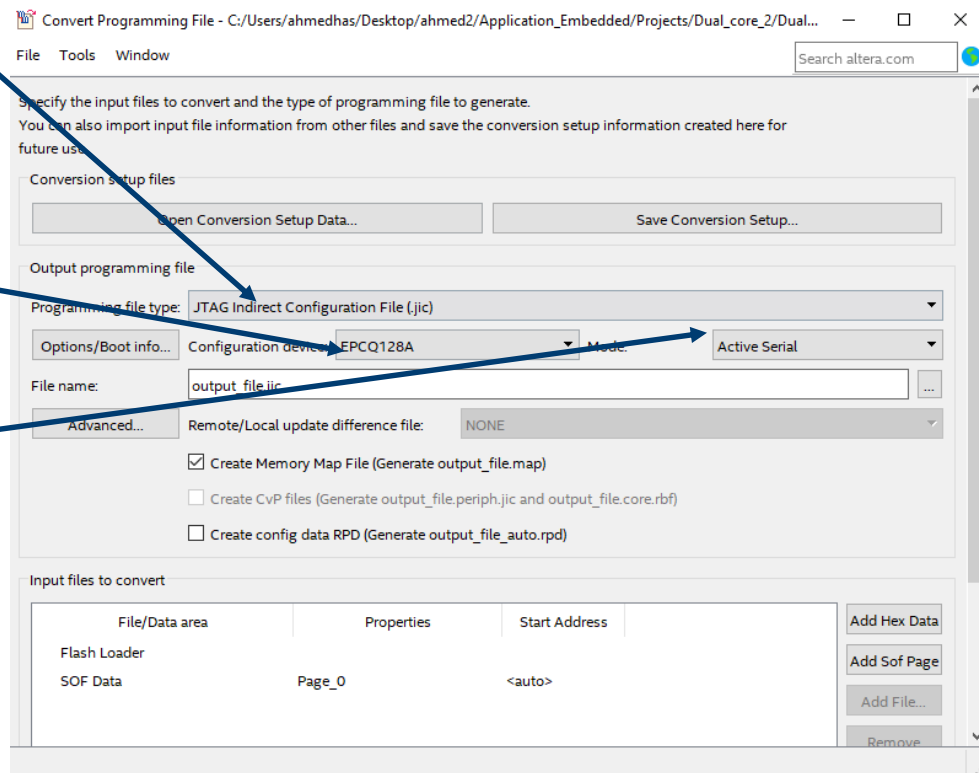


Flash programming procedure

- Select JTAG Indirect Configuration File (.jic)

Select your flash device.

- Select Active Serial mode.

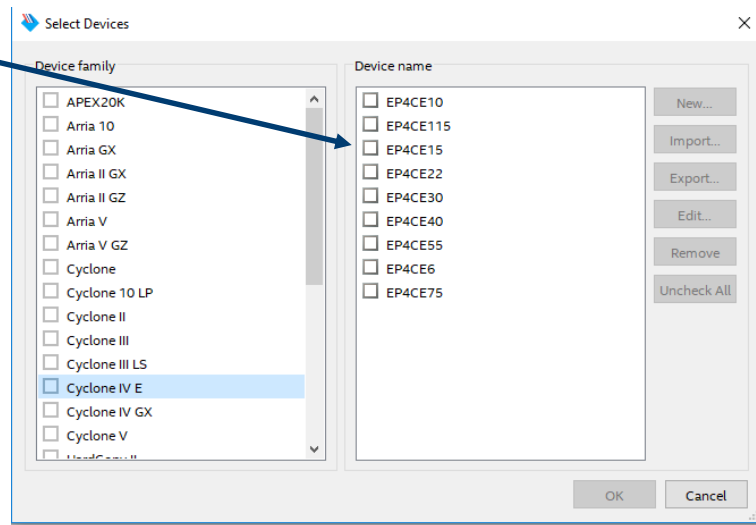
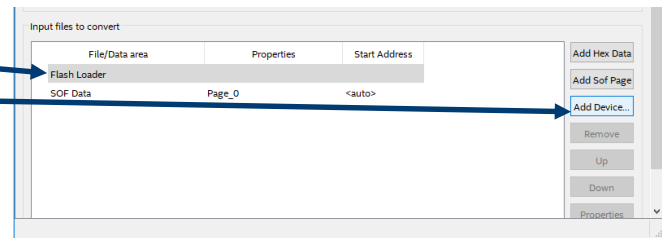


Flash programming procedure

- Select the flash loader page

- Press Add Device.

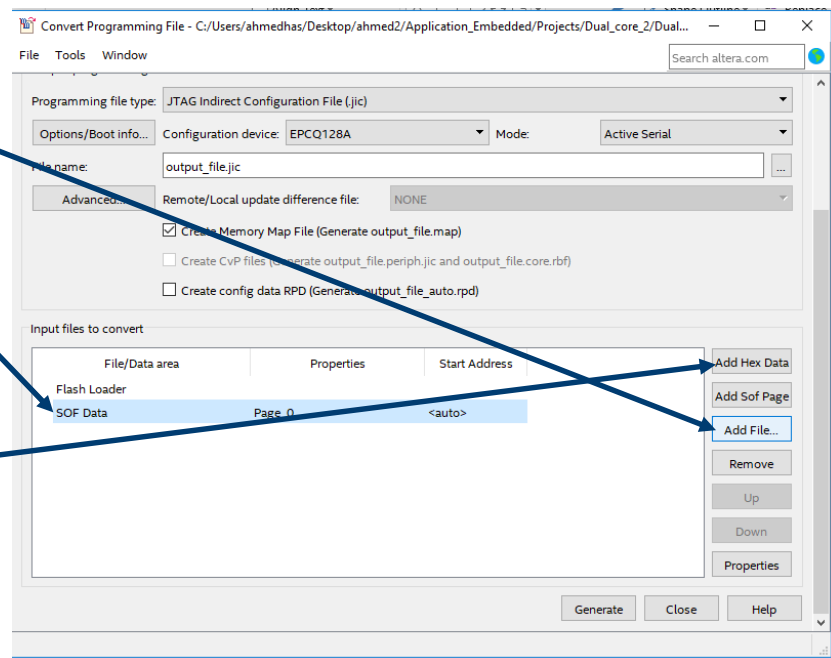
- Select your device.



Flash programming procedure

- Select the SOF Data page and Add the SOF file.

- Add HEX Data if you want to include it into the generated (.jic) file.



Flash programming procedure

- In the Quartus programmer, select Auto Detect after connecting your board.
- Right click the FPGA device>> Change file.
- Select your (.jic) file.

Hardware Setup... DE-SoC [USB-1]

Enable real-time ISP to allow background programming when available

File	Device	Checksum
<none>	SOCVHPS	00000000 <r
<none>	5CSEMA4	00000000 <r

Start

Stop

Auto Detect

Delete

Add File...

Change File...

Save File

Add Device...

Up

Down

TDI

TDO

SOCVHPS

5CSEMA4

Flash programming procedure

- The FPGA will auto detect the flash device based on the jic file loaded.

- Press Start to program the flash.

The screenshot shows the hardware setup window of the Intel programming software. The title bar reads "Hardware Setup... DE-SoC [USB-1]". There is a checkbox for "Enable real-time ISP to allow background programming when available" which is currently unchecked. On the left is a vertical toolbar with buttons: Start, Stop, Auto Detect, Delete, Add File..., Change File..., Save File, Add Device..., Up, and Down. The "Start" button is highlighted with a blue arrow pointing from the second bullet point in the text on the left. The main area contains a table of detected hardware:

File	Device	Checksum	Usercode
<none>	SOCVHPS	00000000	<none>
Factory default enhanc...	5CSEMA4	005BDA6A	005BDA6A
output_file.jic	EPCS128	C2630499	

Below the table is a hardware diagram showing the connection between three components: SOCVHPS, 5CSEMA4, and EPCS128. SOCVHPS is connected to 5CSEMA4 via a TDI (Test Data In) signal. 5CSEMA4 is connected to EPCS128. A TDO (Test Data Out) signal is shown exiting from the 5CSEMA4 component.

