



Flash programming procedure

Ahmed Hassan

Generating PFL.sof

Parallel Flash Loader example

In this section you will generate the PFL project to make the FPGA work as a bridge to the parallel flash, then program the flash with the HEX.pof file.

- Generate the HDL of a Parallel flash loader in Qsys.
- Connect it in the Top_Level in Quartus.
- Compile the project.
- Once compilation successful, open the Quartus Programmer.

Parallel Flash Loader II Intel FPGA IP

altera_parallel_flash_loader_2

General Flash Interface Setting

What operating mode will be used?: Flash Programming

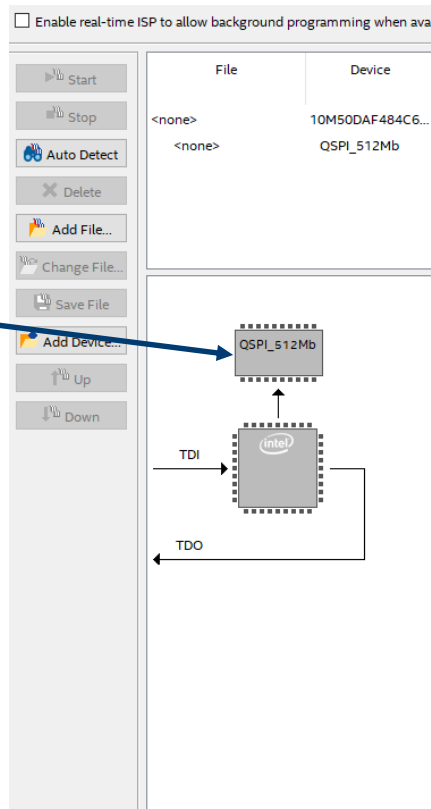
What is the targeted flash?:

- Quad SPI Flash
- CFI Parallel Flash
- Quad SPI Flash

Set flash bus pins to tri-state when not used

Parallel Flash Loader example

- In Quartus programmer, program the FPGA with the generated pfl.sof
- Press auto detect after a successful programming. (don't turn off the board power)
- The Quartus programmer will detect the parallel flash



Parallel Flash Loader example

- Right click the flash device>> Change file
- Select the generated HEX.pof file that carries the HEX file.
- After this step you can boot your NIOS II and it will find the HEX in place.
- Follow the following steps to boot NIOS II from a serial flash.

Enable real-time ISP to allow background programming when available

File	Device
<none>	10M50DAF484C6...
<none>	QSPI_512Mb

Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down

The diagram illustrates the hardware setup for the Parallel Flash Loader. It shows an Intel processor (represented by a square with the Intel logo) connected to a QSPI_512Mb flash device (represented by a square with a dotted border). The processor has two pins labeled TDI and TDO. The flash device is connected to the processor. A blue arrow points from the 'Add Device...' button in the software interface to the 'QSPI_512Mb' device in the diagram.

