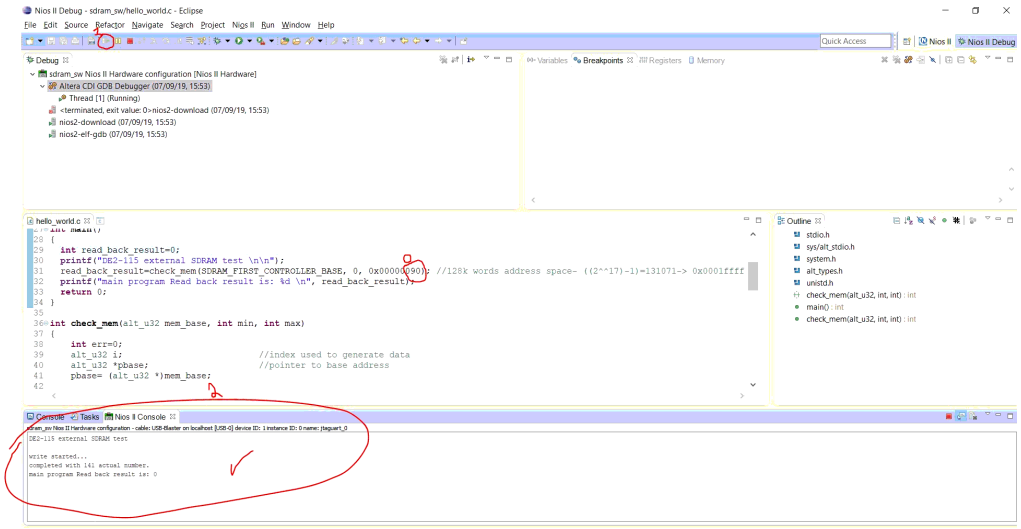
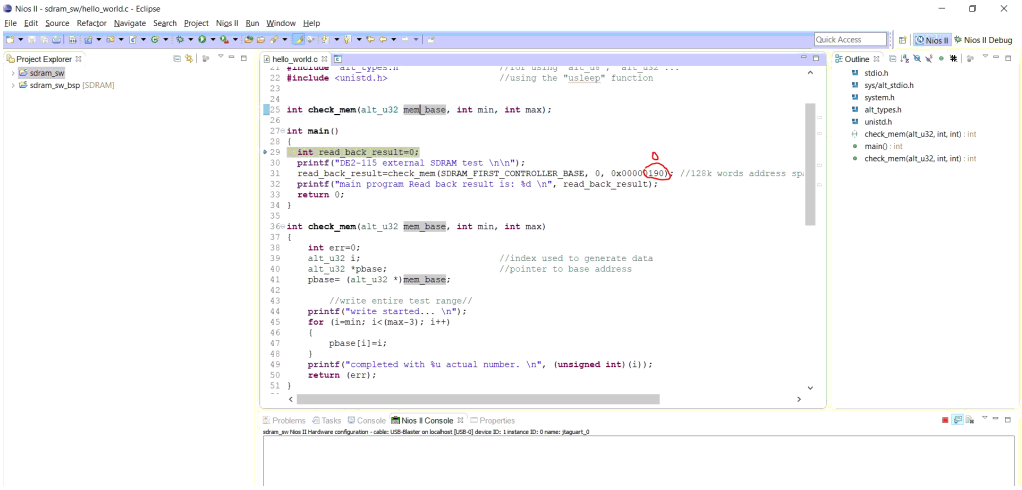
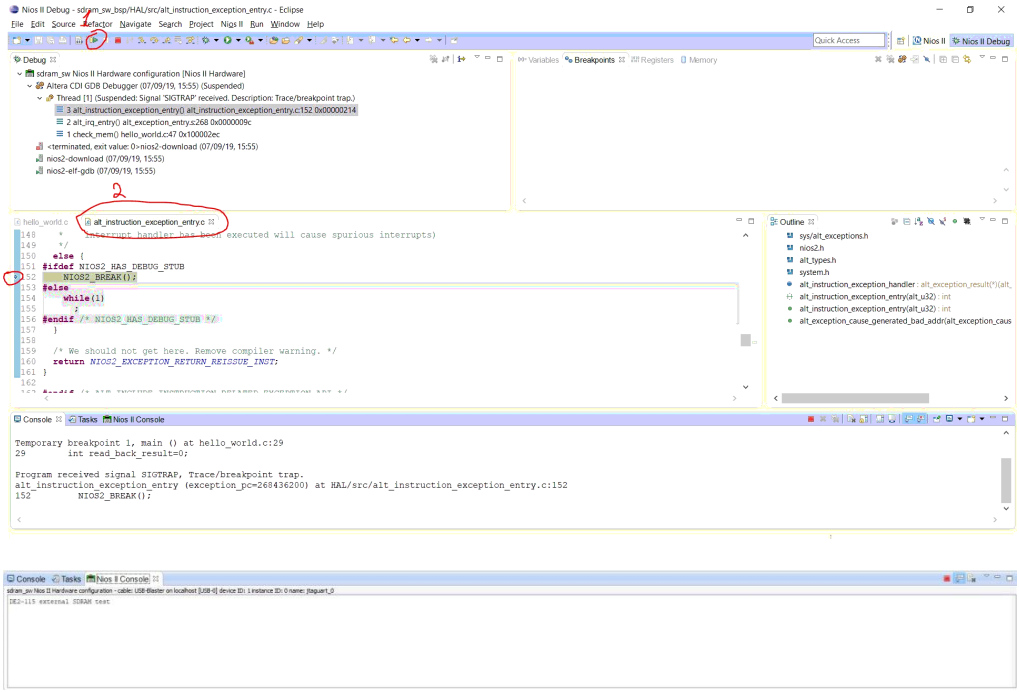
Attaché 1- writing successfully from 0 to max=0x90h (~144 cycles) of the SDRAM (massages is rightfully written on the "NIOS II Console"):

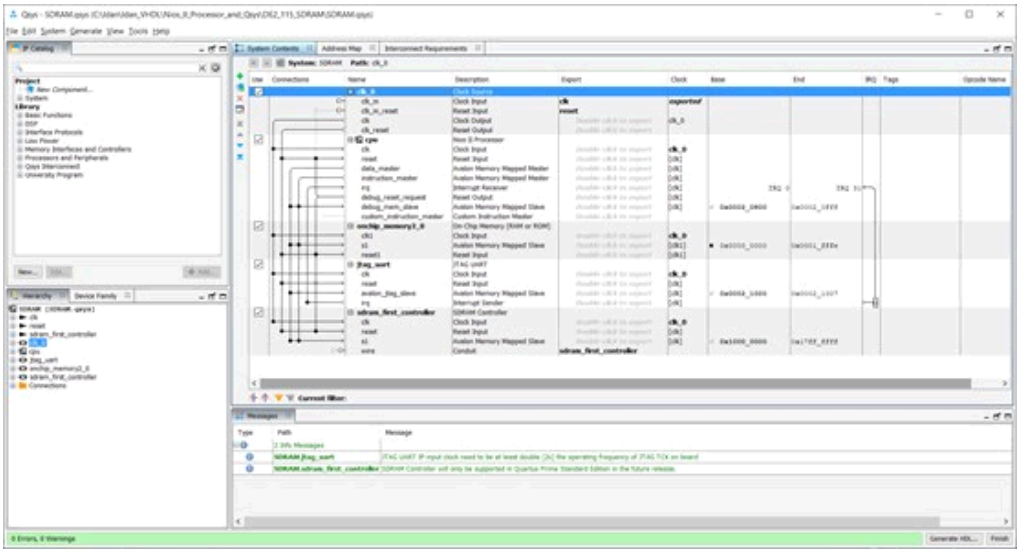


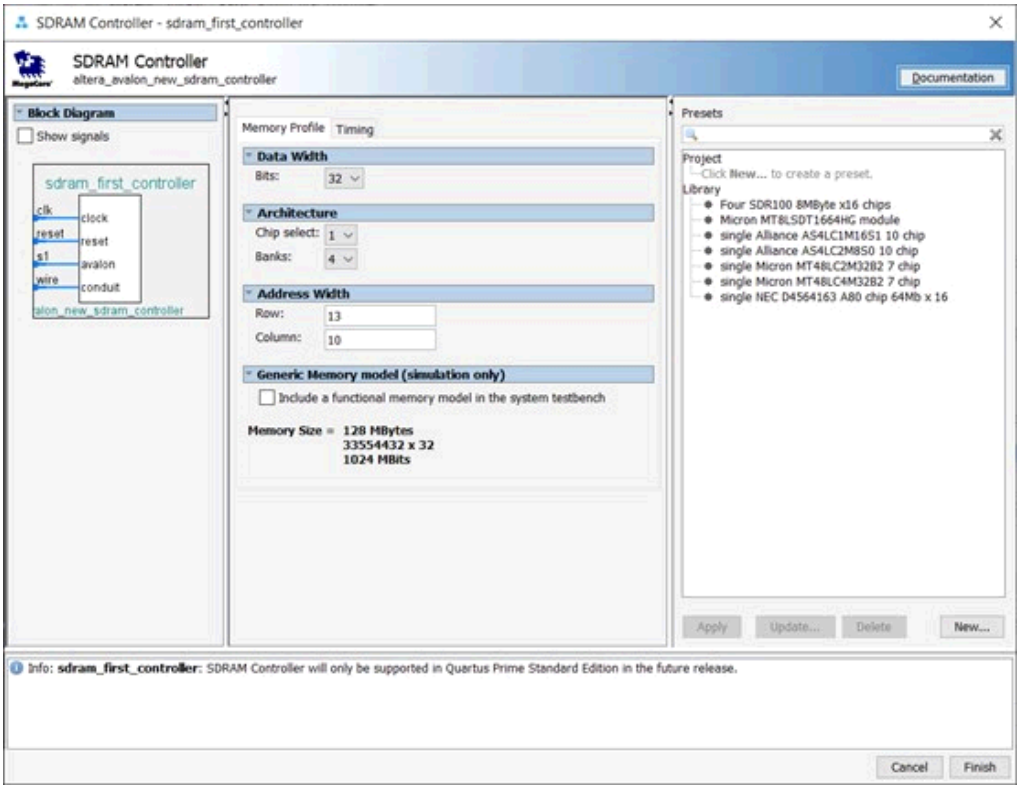
Attaché 2- writing unsuccessfully from 0 to max=0x190h (~400 cycles) of the SDRAM (massages stopped written on the "NIOS II Console"):

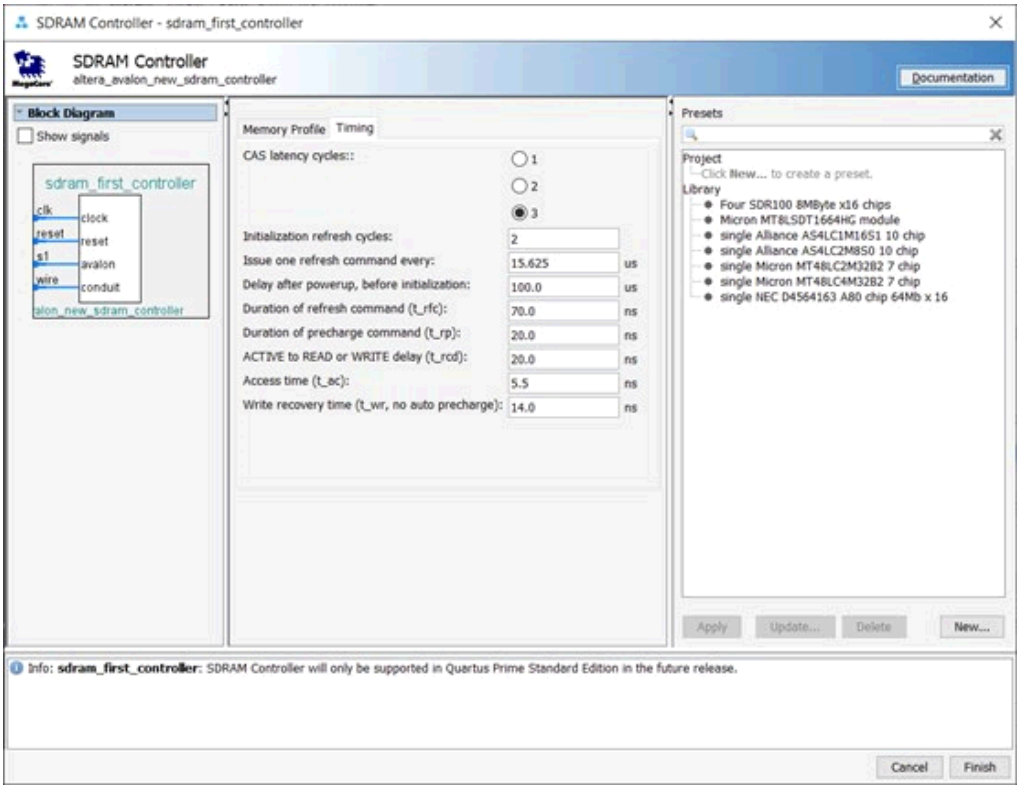




Attaché 3- General configuration (I have used two 50MHz PLL's: one for NIOS and one for external SDRAM (leading by -3.46 deg):






SDRAM Controller - sdram_first_controller
SDRAM Controller
altera_avalon_new_sdram_controller
Documentation
Block Diagram
Show signals
sdram_first_controller
clk
clock
reset
reset
s1
avalon
wire
conduit
alon_new_sdram_controller
Memory Profile
Timing
CAS latency cycles::
1
2
3
Initialization refresh cycles:
2
Issue one refresh command every:
15.625
us
Delay after powerup, before initialization:
100.0
us
Duration of refresh command (t_rfc):
70.0
ns
Duration of precharge command (t_rp):
20.0
ns
ACTIVE to READ or WRITE delay (t_rcd):
20.0
ns
Access time (t_ac):
5.5
ns
Write recovery time (t_wr, no auto precharge):
14.0
ns
Presets
Project
Click New... to create a preset.
Library
Four SDR100 8MByte x16 chips
Micron MT8LSDT1664HG module
single Alliance AS4LC1M16S1 10 chip
single Alliance AS4LC2M8S0 10 chip
single Micron MT48LC2M32B2 7 chip
single Micron MT48LC4M32B2 7 chip
single NEC D4564163 A80 chip 64Mb x 16
Apply
Update...
Delete
New...
Info: sdram_first_controller: SDRAM Controller will only be supported in Quartus Prime Standard Edition in the future release.
Cancel
Finish