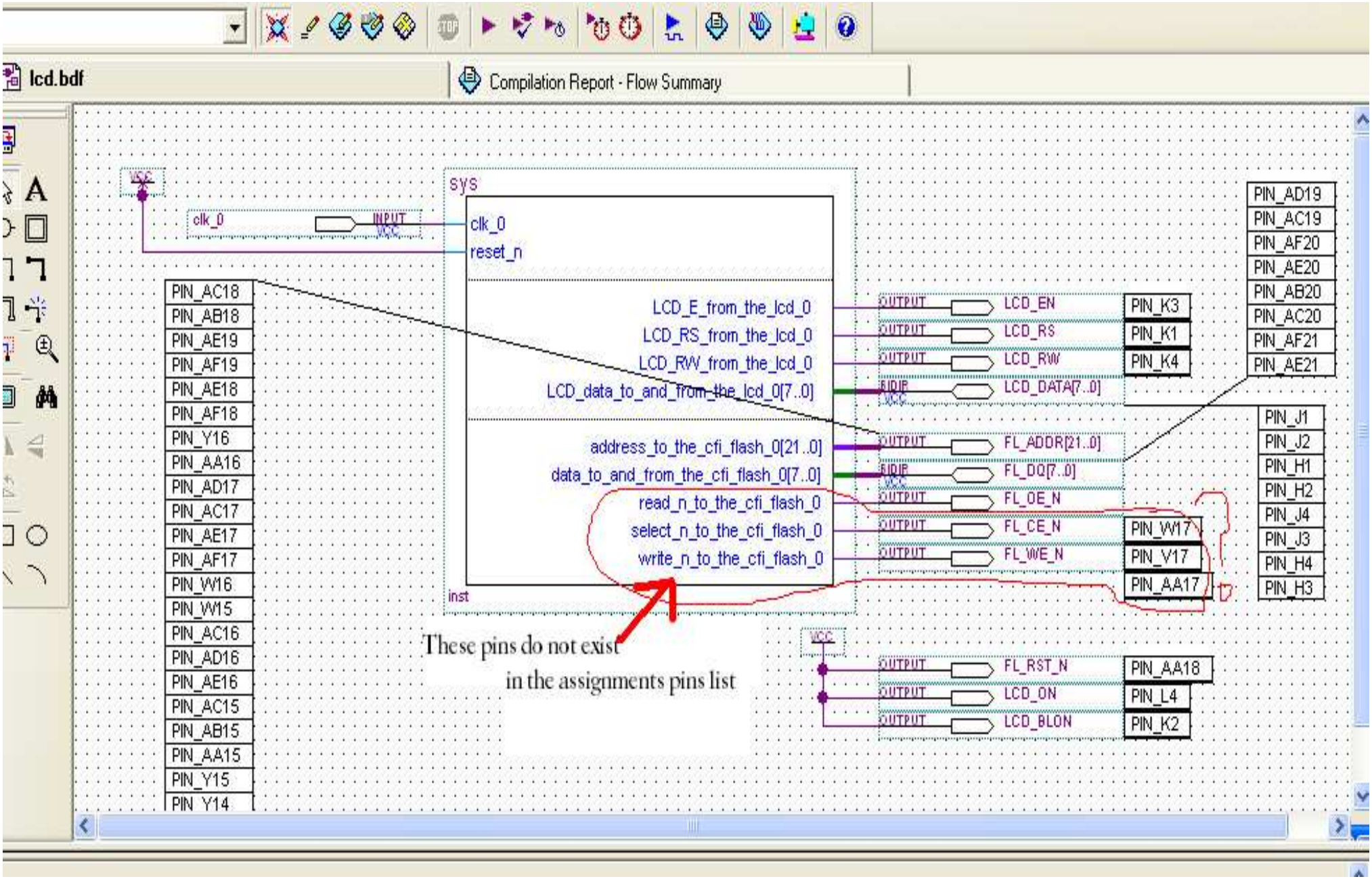
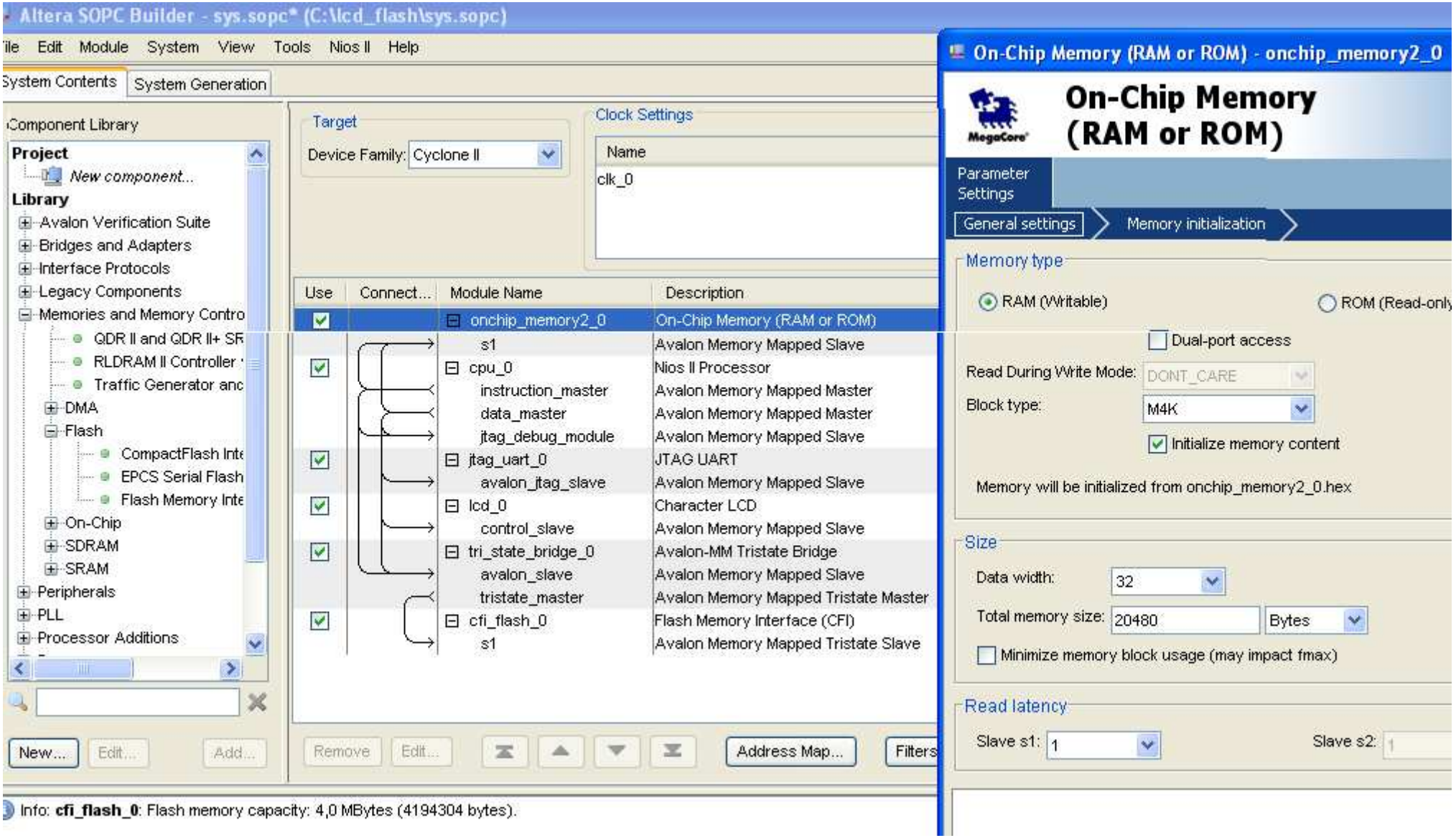
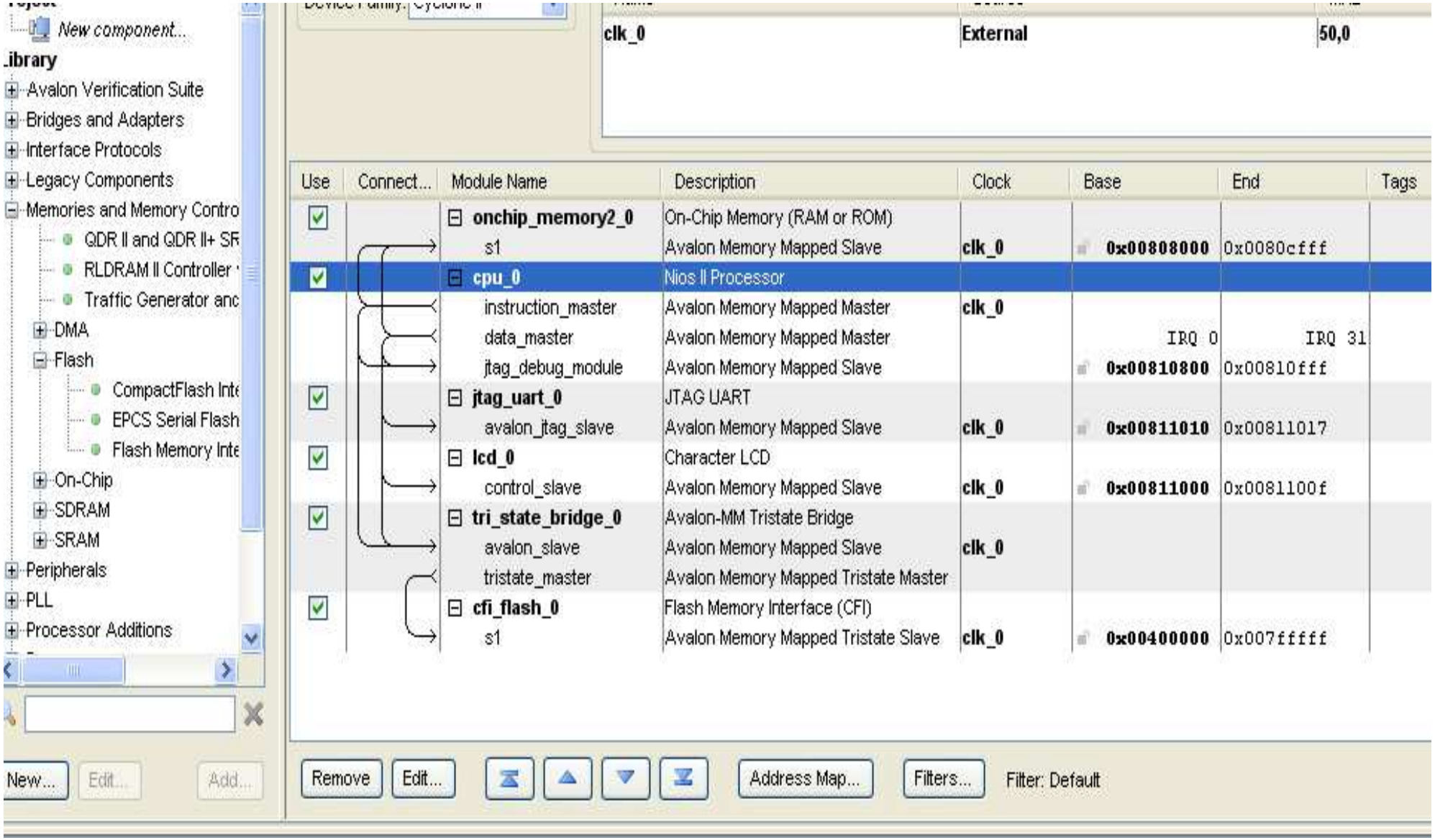

lcd.bdf
Compilation Report - Flow Summary
SYS
clk_0
reset_n
LCD_E_from_the_lcd_0
LCD_RS_from_the_lcd_0
LCD_RW_from_the_lcd_0
LCD_data_to_and_from_the_lcd_0[7..0]
address_to_the_cfi_flash_0[21..0]
data_to_and_from_the_cfi_flash_0[7..0]
read_n_to_the_cfi_flash_0
select_n_to_the_cfi_flash_0
write_n_to_the_cfi_flash_0
inst
LCD_EN
LCD_RS
LCD_RW
LCD_DATA[7..0]
FL_ADDR[21..0]
FL_DQ[7..0]
FL_OE_N
FL_CE_N
FL_WE_N
FL_RST_N
LCD_ON
LCD_BLON
PIN_K3
PIN_K1
PIN_K4
PIN_W17
PIN_V17
PIN_AA17
PIN_AA18
PIN_L4
PIN_K2
PIN_AC18
PIN_AB18
PIN_AE19
PIN_AF19
PIN_AE18
PIN_AF18
PIN_Y16
PIN_AA16
PIN_AD17
PIN_AC17
PIN_AE17
PIN_AF17
PIN_W16
PIN_W15
PIN_AC16
PIN_AD16
PIN_AE16
PIN_AC15
PIN_AB15
PIN_AA15
PIN_Y15
PIN_Y14
PIN_AD19
PIN_AC19
PIN_AF20
PIN_AE20
PIN_AB20
PIN_AC20
PIN_AF21
PIN_AE21
PIN_J1
PIN_J2
PIN_H1
PIN_H2
PIN_J4
PIN_J3
PIN_H4
PIN_H3
These pins do not exist
in the assignments pins list


Altera SOPC Builder - sys.sopc* (C:\lcd_flash\sys.sopc)
File Edit Module System View Tools Nios II Help
System Contents
System Generation
Component Library
Project
New component...
Library
Avalon Verification Suite
Bridges and Adapters
Interface Protocols
Legacy Components
Memories and Memory Contro
QDR II and QDR II+ SR
RLDRAM II Controller
Traffic Generator anc
DMA
Flash
CompactFlash Inte
EPCS Serial Flash
Flash Memory Inte
On-Chip
SDRAM
SRAM
Peripherals
PLL
Processor Additions
New...
Edit...
Add...
Target
Device Family: Cyclone II
Clock Settings
Name
clk_0
Use
Connect...
Module Name
Description
onchip_memory2_0
On-Chip Memory (RAM or ROM)
s1
Avalon Memory Mapped Slave
cpu_0
Nios II Processor
instruction_master
Avalon Memory Mapped Master
data_master
Avalon Memory Mapped Master
jtag_debug_module
Avalon Memory Mapped Slave
jtag_uart_0
JTAG UART
avalon_jtag_slave
Avalon Memory Mapped Slave
lcd_0
Character LCD
control_slave
Avalon Memory Mapped Slave
tri_state_bridge_0
Avalon-MM Tristate Bridge
avalon_slave
Avalon Memory Mapped Slave
tristate_master
Avalon Memory Mapped Tristate Master
cfi_flash_0
Flash Memory Interface (CFI)
s1
Avalon Memory Mapped Tristate Slave
Remove
Edit...
Address Map...
Filters
Info: cfi_flash_0: Flash memory capacity: 4,0 MBytes (4194304 bytes).
On-Chip Memory (RAM or ROM) - onchip_memory2_0
On-Chip Memory (RAM or ROM)
Parameter Settings
General settings
Memory initialization
Memory type
RAM (Writable)
ROM (Read-only
Dual-port access
Read During Write Mode: DONT_CARE
Block type: M4K
Initialize memory content
Memory will be initialized from onchip_memory2_0.hex
Size
Data width: 32
Total memory size: 20480 Bytes
Minimize memory block usage (may impact fmax)
Read latency
Slave s1: 1
Slave s2:


New component...
.ibrary
Avalon Verification Suite
Bridges and Adapters
Interface Protocols
Legacy Components
Memories and Memory Contro
QDR II and QDR II+ SR
RLDRAM II Controller
Traffic Generator and
DMA
Flash
CompactFlash Inte
EPCS Serial Flash
Flash Memory Inte
On-Chip
SDRAM
SRAM
Peripherals
PLL
Processor Additions
New...
Edit...
Add...
clk_0
External
50,0
Use
Connect...
Module Name
Description
Clock
Base
End
Tags
onchip_memory2_0
On-Chip Memory (RAM or ROM)
s1
Avalon Memory Mapped Slave
clk_0
0x00808000
0x0080cfff
cpu_0
Nios II Processor
instruction_master
Avalon Memory Mapped Master
clk_0
data_master
Avalon Memory Mapped Master
IRQ 0
IRQ 31
jtag_debug_module
Avalon Memory Mapped Slave
0x00810800
0x00810fff
jtag_uart_0
JTAG UART
avalon_jtag_slave
Avalon Memory Mapped Slave
clk_0
0x00811010
0x00811017
lcd_0
Character LCD
control_slave
Avalon Memory Mapped Slave
clk_0
0x00811000
0x0081100f
tri_state_bridge_0
Avalon-MM Tristate Bridge
avalon_slave
Avalon Memory Mapped Slave
clk_0
tristate_master
Avalon Memory Mapped Tristate Master
cfi_flash_0
Flash Memory Interface (CFI)
s1
Avalon Memory Mapped Tristate Slave
clk_0
0x00400000
0x007fffff
Remove
Edit...
Address Map...
Filters...
Filter: Default