Conversion Guide: Numonyx® Axcell™ P33 Flash Memory (128-Mbit, 64-Mbit) 130nm to 65nm SBC (Single Bit per Cell)

Application Note

Jul 2010

Contents

Revision History

Date of Revision	Revision	Description
Jul 2009	01	Initial Release
May 2010	02	Update 32-Word, 256-Word Buffer Program time, BEFP setup time, t_{DVWH} timing comments in Table 3, “Key AC Write Spec Comparison” on page 9. Update 70h usage in Table 6, “Command Bus Operations” on page 11. Update CFI with real performance in Table 9, “Value Changes” on page 14. Add the power loss recovery in Section 6.0, “Conversion Considerations” on page 15.
Jul 2010	03	Emphasize the legal and valid command usage.

1.0 Introduction

This application note describes the migration from the Numonyx® Axcell™ P33-130nm flash memory to the Numonyx® Axcell™ P33-65nm (SBC) flash memory.

Note: Unless otherwise indicated, throughout the rest of this document, the Numonyx® Axcell™ P33-130nm flash memory is referred to as the P33-130nm device and the Numonyx® Axcell™ P33-65nm (SBC) flash memory is referred to as the P33-65nm (SBC) device.

This document was written based on device information available at the time. Any changes in specifications to either device might not be reflected in this document. Refer to the appropriate documents or sales personnel for the current product information before finalizing any design.

2.0 Device Overview

The following sections provide a brief overview of the feature differences between the P33-130nm and the P33-65nm (SBC) devices.

2.1 P33-130nm Device

The P33-130nm device features 64-Mbit through 512-Mbit densities and AC/DC specifications for 52MHz operation. Other features include high performance synchronous-burst read, Buffered Enhanced Factory Programming (BEFP) with a 32-word buffer, and an expanded OTP register space. Packaging options include industry-standard Easy BGA and TSOP packages.

2.2 P33-65nm (SBC) Device

The P33-65nm device features 64-Mbit through 2-Gbit densities and AC/DC specifications for 52 MHz operation. This document covers specially 64-Mbit and 128-Mbit (SBC) product information. Other features include high performance synchronous-burst read, Buffer programming and Buffered Enhanced Factory Programming (BEFP) with a 256-word buffer, and an expanded OTP register space. The P33-65nm (SBC) device also features enhanced protection via a password access feature, which allows users to protect write access to the pre-defined blocks. Please contact the Numonyx Sales for further details concerning password access. Packaging options include industry-standard Easy BGA and TSOP packages.

2.3 P33-130nm and P33-65nm (SBC) Features Comparison

Table 1: P33-130nm and P33-65nm (SBC) Feature Comparison

Features / Specifications		P33-130nm	P33-65nm (SBC)
Available Densities (Monolithic)	64 Mbit	Yes	Yes
	128 Mbit	Yes	Yes
	256 Mbit	Yes	Note
Available Densities (Stack)	512 Mbit	Yes	Note
Performance	Speed	Easy BGA:52 MHz TSOP:40MHz	Easy BGA:52 MHz TSOP:40MHz
	Initial Access Time (Easy BGA)	85 ns	60 ns
	Initial Access Time (TSOP)	95 ns	70 ns
Block Architecture	Parameter Blocks	Four: 32-kByte	Four: 32-kByte
	Main Blocks	128-kByte	128-kByte
	16-bit data bus	Yes	Yes
Operating Voltage	Logic Core (V_{CC})	2.3 V to 3.6 V	2.3 V to 3.6 V
	I/O (V_{CCQ})	2.3 V to 3.6 V	2.3 V to 3.6 V
Features	OTP Register Space	128-bits + 2 Kbits	128-bits + 2 Kbits
	Flexible Block Locking	Yes	Yes
	Buffered Program	32-word buffer	256-word buffer
	Buffered Enhanced Factory Program	32-word buffer	256-word buffer
	Password Access	No	Yes
	Blank Check	No	Yes
Reliability	Operating Temperature	–40 °C to +85 °C	–40 °C to +85 °C
	Cycles	100,000	100,000

Note: This document doesn't cover 256-Mbit, 512-Mbit die information. Please refer to Numonyx local Sales for P33-65nm monolithic product detail.

3.0 Device Packaging and Ballout

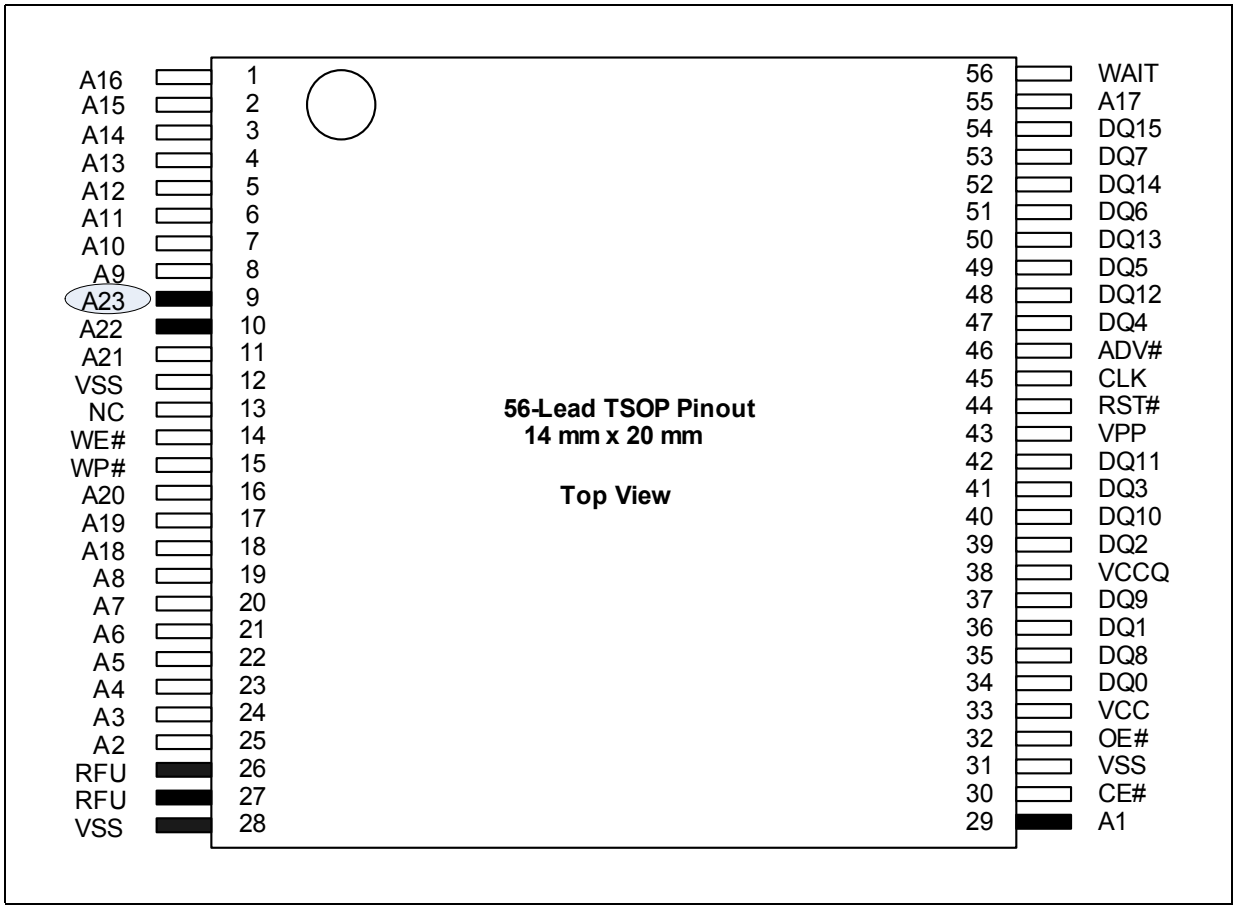
3.1 Easy BGA Ballout

The Easy BGA ballout is available and compatible for both P33-130nm and P33-65nm (SBC) products. Ball pitch of the Easy BGA ballout is 1.0 mm; the package has the same 8x 8 active-ball matrix.

3.2 TSOP Pinout

The TSOP Pinout is available and compatible for both P33-130nm and P33-65nm (SBC) products. Pin 13 on P33-130nm is connected to Vcc. For P33-65nm (SBC) this pin has no internal connection; it may be driven or left floated.

Figure 1: 56-Lead TSOP Pinout



Notes:
1. A1 is the least significant address bit.
2. A23 is valid for 128-Mbit densities; otherwise, it is a no connect (NC).
3. No Internal Connection on Pin 13; it may be driven or floated. For legacy 130nm designs, this pin can be tied to Vcc.

4.0 Hardware Design Considerations

The P33-130nm and P33-65nm (SBC) flash memory devices feature asymmetrically-blocked architecture, buffer programming, Buffered Enhanced Factory Programming, and synchronous-burst read mode. The following sections discuss hardware design considerations when converting from the P33-130nm device to the P33-65nm (SBC) device.

Note: Refer to the product datasheet for detailed list of all AC Read and Write/Erase specifications:

- Numonyx® Axcell™ P33-130nm Flash Memory Datasheet (314749)
- Numonyx® Axcell™ P33-65nm Flash Memory (SBC) Datasheet (208034)

4.1 AC Read Specifications

The below table lists the AC Read spec difference between P33-130nm and P33-65nm (SBC) devices. Asynchronous page size is enlarged up to 8 words.

Table 2: Key AC Read Spec Comparison

Features / Specifications		P33-130nm	P33-65nm(SBC)
Performance	Clock Frequency (Max)	Easy BGA:52MHz TSOP:40MHz	Easy BGA:52MHz TSOP:40MHz
	Asynchronous Access (t_{AVQV} t_{VLQV} t_{ELQV})	Easy BGA: 85 ns	Easy BGA: 60 ns
		TSOP: 95 ns	TSOP: 70ns
	Asynch Page Access time (t_{APA})	25 ns	25 ns
	Clock-to-Data Burst Access (t_{CHQV})(1)	17 ns	17 ns
	Burst Data Hold Time (t_{CHQX})(1)	3 ns	3ns
	Address and ADV# Setup Time (t_{AVCH}, t_{VLCH})(1)	9 ns	9 ns
	CE# Setup Time (t_{ELCH})(1)	9 ns	9 ns
	Rise/Fall Time ($t_{FCLK/LCLK}$)	3.0 ns	3.0 ns
	Clock High/Low Time ($t_{CH/CL}$)	5 ns	5ns
	Vcc power valid to RST# de-assertion (t_{VCCPH})	60 µs	60 µs
	Async Page Size	4 words	8 words
	Synchronous Burst Length (word)	4-, 8-, 16-, and Cont.	4-, 8-, 16- and Cont.
	Burst Suspend Mode	Yes	Yes

Note: These specs are valid only for Easy BGA package.

4.2 AC Write/Erase Specifications

The below table shows the difference between P33-130nm and P33-65nm (SBC). The P33-65nm (SBC) shows the compatible erase performance and the improved buffered programming performance.

Table 3: Key AC Write Spec Comparison

Features / Specifications		P33-130nm	P33-65nm (SBC)
Program Performance	Program Buffer Size	32Words	256Words
	Single Word Program Time (typ/max)	90/200µs	40/175µs
	Aligned 32-word Buffered Program Time (typ)	145KB/s	735KB/s
	Aligned 256-word Buffered Program Time (typ)	-	1.8MB/s
	BEFP Environment Requirement	25°C +/- 5°C 100 P/E cycles	30°C +/- 10°C 50 P/E cycles
	BEFP Time	188KB/s	3.2MB/s
	BEFP Setup	5µs	10µs
AC characteristics	t_{DVWH} (1)	50ns	50ns
Erase Performance	Erase Time - 16KW Param. Block (typ/max)	0.4/2.5s	0.4/2.5s
	Erase Time - 64KW Main Block (typ/max)	0.8/4.0	0.5/4.0s
	Program/Erase Suspend Latency (typ)	20µs	20µs
	Blank Check ($t_{BC/MB}$)	-	3.2ms
Note: This specification must be complied with by customer's writing timing. The result would be unpredictable if any violation to this timing specification.			

4.3 DC Current Specification

The P33-65nm (SBC) device consumes compatible power with the P33-130nm device during in standby mode.

Table 4: Key DC Current Spec Comparison

Features / Specifications		P33-130nm	P33-65nm (SBC)
DC Current Characteristics	Standby Current (typ/max)	70/195 µA (128Mb)	30/55 µA (128Mb)
	Continuous Burst Read Current (max)	28 mA (52MHz)	28 mA (52MHz)
	Program/Erase Current (typ/max)	35/50 mA	35/50 mA
	VPP Factory Program Current (max)	22 mA	10 mA

5.0 Flash Software Design Considerations

The following sections discuss software design considerations when converting from the P33-130nm device to the P33-65nm (SBC) device.

5.1 Device Identification

The P33-65nm (SBC) flash devices provide the same device identification codes as P33-130nm devices.

Table 5: P33 Device ID Codes

Code Type	Address Offset	Device Density	P33-130nm Codes		P33-65nm (SBC) Codes	
			Top	Bottom	Top	Bottom
Device Identification	0x01	64 Mbit	881D	8820	881D	8820
	0x01	128 Mbit	891E	8921	891E	8921

5.2 Read Configuration Register (RCR)

Read configurations for the P30-130nm and P30-65nm (SBC) devices are set using the Read Configuration Register (RCR). For example, to place the device in synchronous burst-read mode, you set the read mode bit in the RCR.

The P30-65nm (SBC) RCR configuration is same as P30-130nm.The differences are summarized in the table below.

5.3 Blank Check

Blank Check feature is enabled in P30-65nm product devices, which is used to confirm whether a main-array block is completely erased. A Blank Check operation is performed one block at a time, and cannot be used during Program Suspend or Erase Suspend.

To use Blank Check, issue the Blank Check setup command then the confirm command. The addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued. During a blank check operation, the Status Register indicates a busy status (SR.7 = 0). Upon completion, the Status Register indicates a ready status (SR.7 = 1).

5.4 Device Commands

The command set for the P33-65nm (SBC) and P33-130nm devices are fully compatible. However, the P33-65nm (SBC) device includes new features such as the blank check operation and the enhanced configuration operation.

Note: Some customer applications use illegal or invalid commands (like 0x00) accidentally or intentionally with the device. An illegal or invalid command will not change the device output mode on 130nm, such as if current state is Read Array or Read Query mode, illegal or invalid command will keep device at the same output mode, namely Read Array or Read Query. On the 65nm device, the output will change to Read Status Register mode.

After an illegal or invalid command, software may attempt to read the device. If the illegal command was intentional, software will expect to read Array or Query data on 130nm device, such as 0xFFFF in an unprogrammed location. On the 65nm device, software may not get the expected Array or Query data and instead the status register is read.

Please refer to the legal and valid commands/spec defined in the Datasheet, such as for read mode, issue 0xFF to Read Array mode, 0x90 to Read Signature, 0x98 to Read CFI/ OTP array mode.

Table 6: Command Bus Operations

Command		P33-130nm Code (Setup/Confirm)	P33-65nm (SBC) Code (Setup/Confirm)
Read Modes	Read Array	00FFh	00FFh
	Read Status Register	0070h	0070h
	Clear Status Register	0050h	0050h
	Read Device Information	0090h	0090h
	CFI Query	0098h	0098h
Program/Erase Operations	Word Program	0040h	0040h
	Buffered Program[(1)(2)(3)]	00E8h/00D0h	00E8h/00D0h
	Buffered Enhanced Factory Program	0080h/00D0h	0080h/00D0h
	Block Erase	0020h/00D0h	0020h/00D0h
	Program/Erase Suspend	00B0h	00B0h
	Program/Erase Resume	00D0h	00D0h
	Blank Check	N/A	00BCh/00D0h
Security	Lock Block	0060h/0001h	0060h/0001h
	Unlock Block	0060h/00D0h	0060h/00D0h
	Lock Down Block	0060h/002Fh	0060h/002Fh
	Password Access	N/A	Note 4
Registers	Program Read Configuration Register	0060h/0003h	0060h/0003h
	Program OTP Register	00C0h	00C0h

Notes:

1. The device defaults to output SR data after the Buffered Programming Setup Command (E8h) is issued. CE# or OE# must be toggled to update Status Register. Don't issue the Read SR command (70h), which would be interpreted by the internal state machine as Buffer Word Count.
2. During Buffered Program command (E8h) sequence, if a read of the Main Array Data needs to be performed during the loading of the program buffer, then a write to an address outside of current block will abort the Buffer Programming

Operation. Issuing the Read Array command (FFh) will put the device into Read Array mode. After Main Array read operation has been completed, the Buffer Program Operation must be restarted.

3. D0h is buffer program confirm command which should be issued at the corresponding block address that the buffer program setup command was issued.
4. Please ask the local representative to get the detail about the password security feature.

5.5 WAIT State Comparison

This section will compare the difference between the WAIT states on the P33-130nm and the P33-65nm (SBC).

5.5.1 WAIT State P33-65nm (SBC)

End of wordline (EOWL) WAIT states can result when the starting address of the burst operation is not aligned to a 8-word boundary; that is, A[3:1] of start address does not equal 0x0. Figure 2, "End of Wordline Timing Diagram" on page 12 illustrates the end of wordline WAIT state(s), which occur after the first 8-word boundary is reached. The number of data words and the number of WAIT states for both P33-130nm and P33-65nm (SBC) are summarized in Table 7, "End of Wordline Data and WAIT State Comparison" on page 12.

Figure 2: End of Wordline Timing Diagram

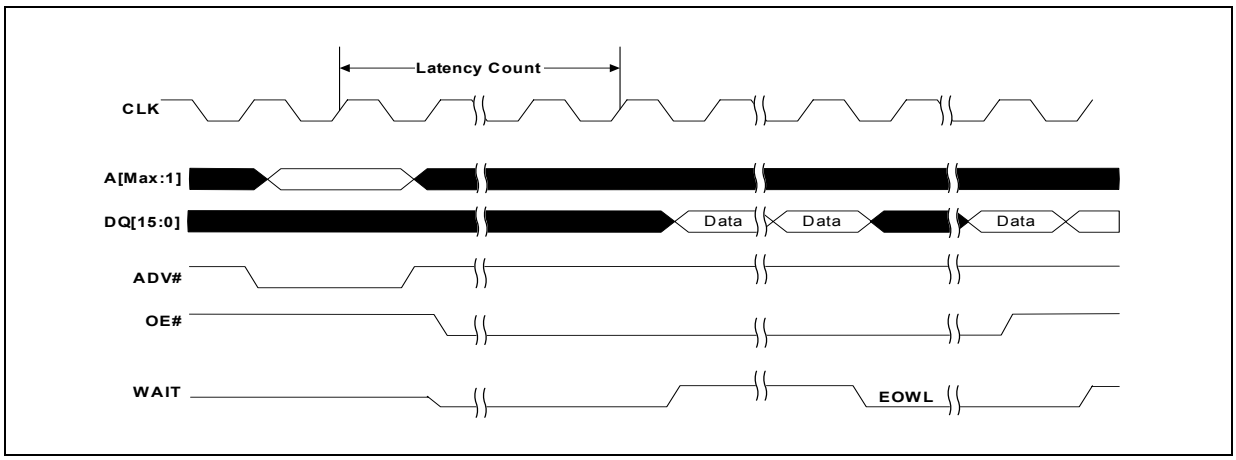


Table 7: End of Wordline Data and WAIT State Comparison

Latency Count	P33-130nm		P33-65nm (SBC)	
	Data States	WAIT States	Data States	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0 to 1	Not Supported	Not Supported
3	4	0 to 2	8	0 to 2
4	4	0 to 3	8	0 to 3
5	4	0 to 4	8	0 to 4
6	4	0 to 5	8	0 to 5
7	4	0 to 6	8	0 to 6

5.5.2 WAIT State P33-130nm

After encountering an EOWL situation, periodic WAIT states can occur in general as illustrated in Figure 3, "Periodic WAIT Timing Diagram" on page 13. Table 8, "Periodic Data and WAIT State Comparison" on page 13 shows that P33-130nm has periodic WAIT states, but P33-65nm (SBC) does not.

Figure 3: Periodic WAIT Timing Diagram

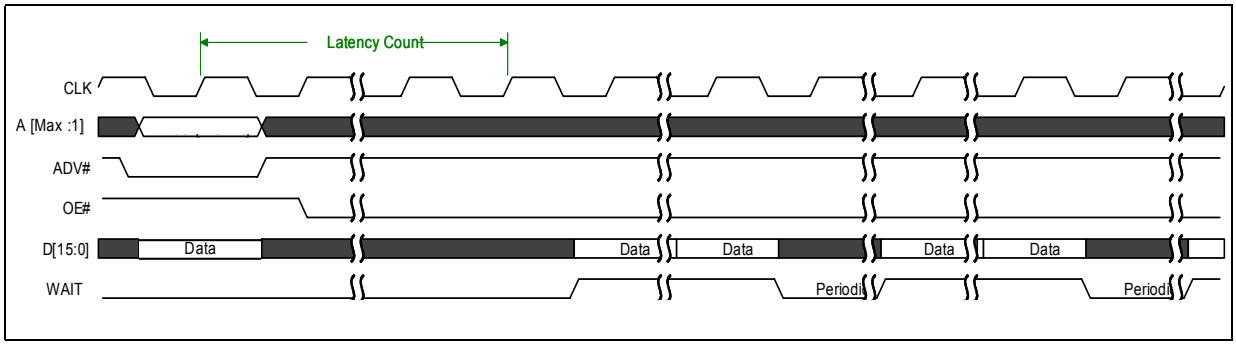


Table 8: Periodic Data and WAIT State Comparison

Latency Count	P33-130nm		P33-65nm	
	Data States	WAIT States	Data States	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0	Not Supported	Not Supported
3	4	0	8	0
4	4	0	8	0
5	4	1	8	0
6	4	2	8	0
7	4	3	8	0

5.6 CFI Differences

P33-65nm (SBC) has same CFI revision. During adoption of Numonyx or third party software, several differences must be taken into account. This section will describe the changes.

5.6.1 CFI revision

The CFI minor revision sorted in offset (P+4)h remains as "4".

CFI version 1.4 is supported in the software provided by Numonyx.

5.6.2 Time-out changes

All CFI time-out changes are listed in Table 9, "Value Changes" .

Table 9: Value Changes

Num	Difference	offset	130nm		65nm	
			Hex Code	Value	Hex Code	Value
1	"n" such that typical single word program time-out = 2^n µ-sec	1Fh	--08	256	--06	64
2	"n" such that typical max. buffer write time-out = 2^n µ-sec	20h	--09	512	--09	256
3	"n" such that typical block erase time-out = 2^n m-sec	21h	--0A	1s	--09	0.5s
5	"n" such that maximum word program time-out = 2^n times typical	23h	--01	512	--02	256
6	"n" such that maximum buffer write time-out = 2^n times typical	24h	--01	1024	--02	2048
7	"n" such that maximum number of bytes in write buffer = 2^n	2Ah	--06	64	--09	512
8	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	(P+1D)h	--03	8	--04	16

5.7 Performance Improvements in P33-65nm (SBC)

5.7.1 Write Performance

The write performance can be improved on P33-65nm (SBC) by using the 512 Byte/ 256 Word buffer. If buffered programming is being done using the 32 Byte buffer (similar to 130nm devices), no software changes need to be implemented.

To achieve maximum performance using the 512 Byte/256 Word buffer on 65nm devices, the following considerations apply during software modifications:

1. Use the Full 512 Byte/256 Word Buffer.

2. If 512 Byte/256 Word Buffer is being used, the programming addresses should be aligned in 256 word address boundaries (A[8:1]=0x00). For example: Start Programming address is 000000h and End Programming Address is 0000FFh.

3. If the addresses must be mis-aligned, the buffer programming range should not cross the 256 words boundary. The maximum buffer size depends on the Start programming address. For example: Start Programming Address is 000005h, the maximum buffer size would be 0000FAh (250 words), then the End programming Address is 0000FFh.

5.7.2 Read Performance

The Read performance can be improved by providing read page buffer up to 16 Bytes (P+1Dh).

6.0 Conversion Considerations

The P33-65nm (SBC) device includes a larger program buffer size to improve programming performance. Users should adjust their software and align the operation to take full advantage.

It is recommended that the user enable robust power loss recovery in software system, especially during the flash write operations. Please refer to the Application Note 309046 for detail information.

Order/Document Number	Document/Tool
314749	Numonyx® Axcell™ P33-130nm Flash Memory Datasheet
208034	Numonyx® Axcell™ P33-65nm Flash Memory (SBC) Datasheet
309046	Application Note: Power Loss Recovery for Nor Flash Memory

Note: Contact your local Numonyx or distribution sales office or visit Numonyx's World Wide Web home page at http://www.Numonyx.com for technical documentation, tools, and additional information.