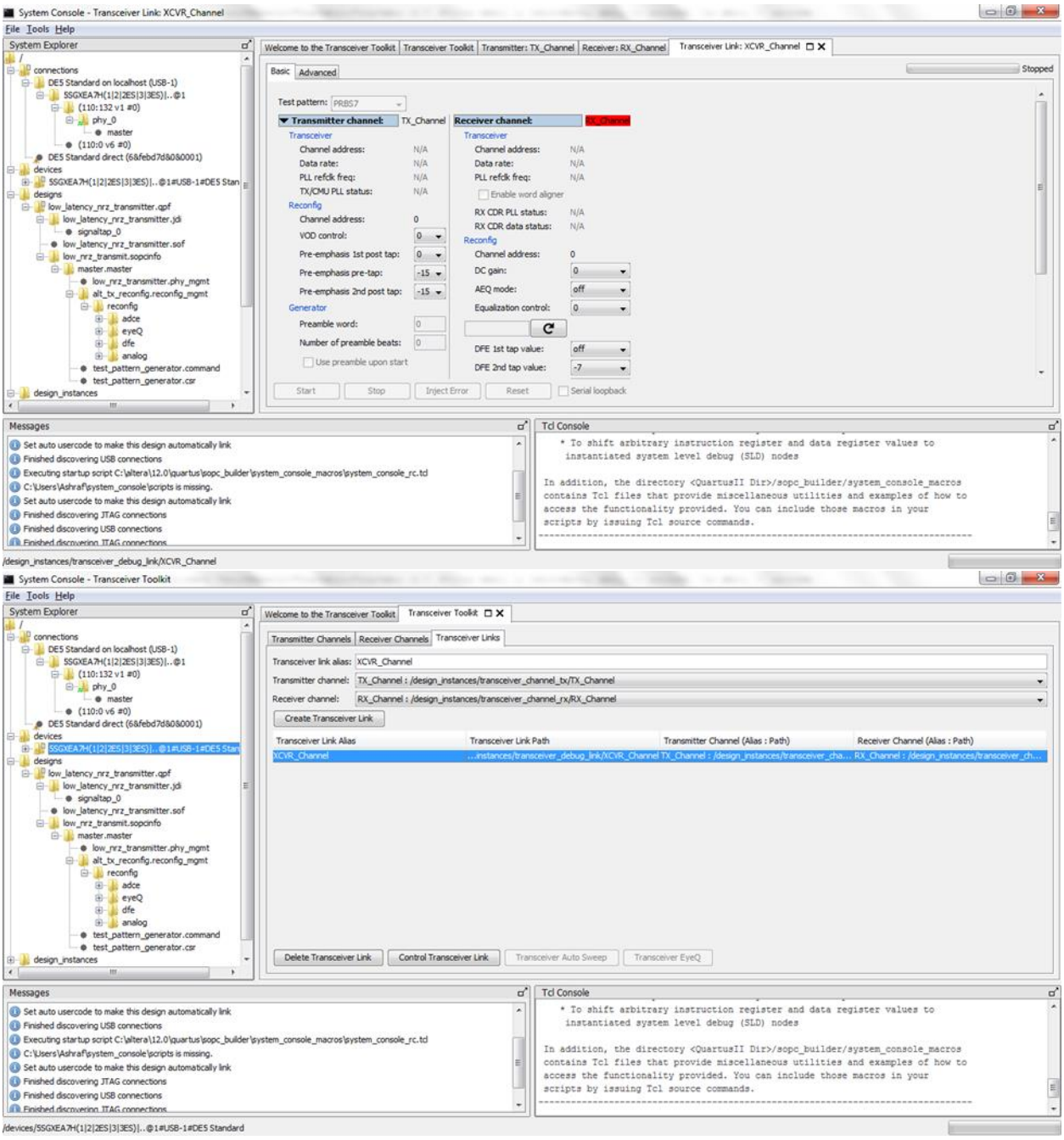
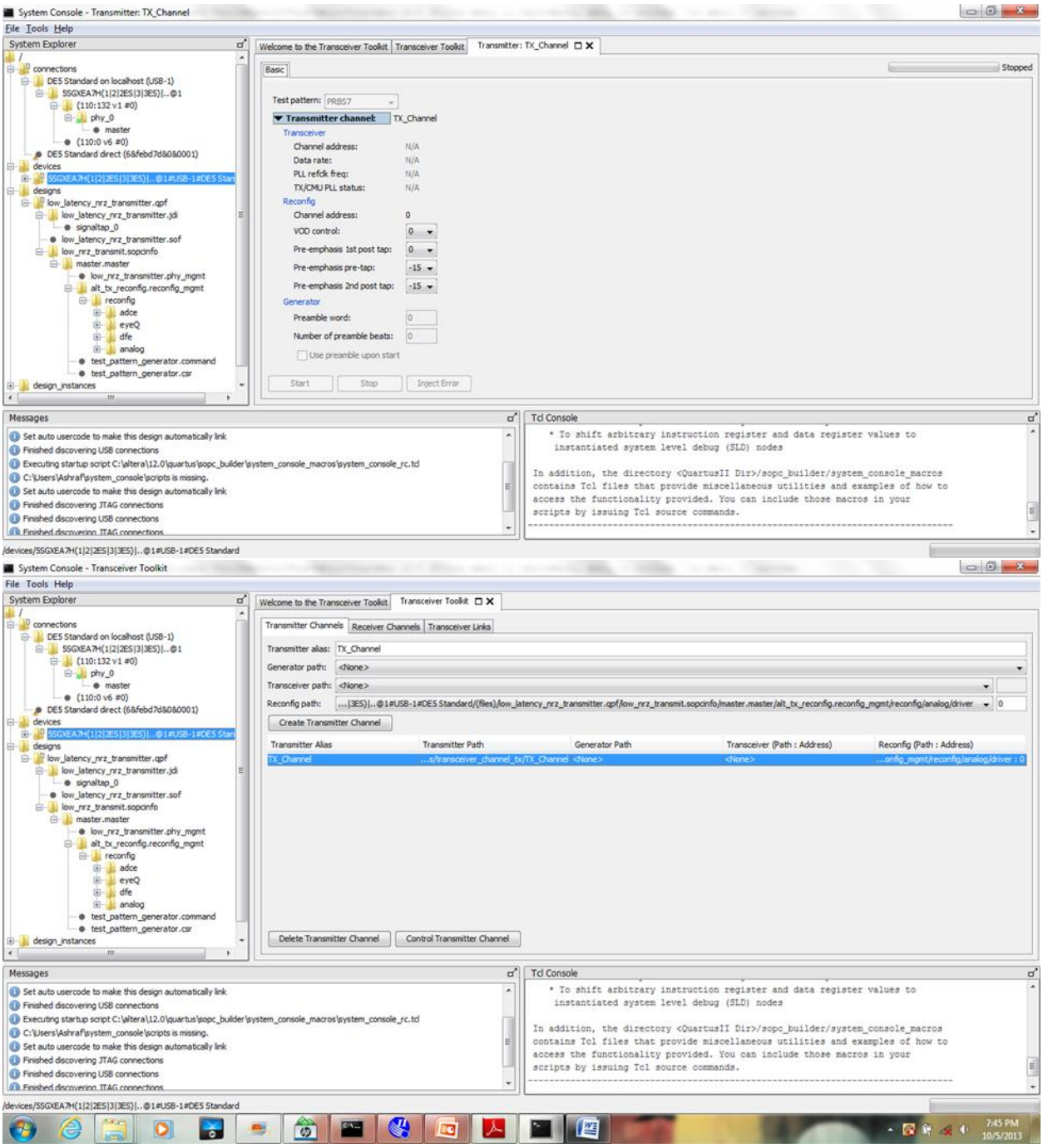
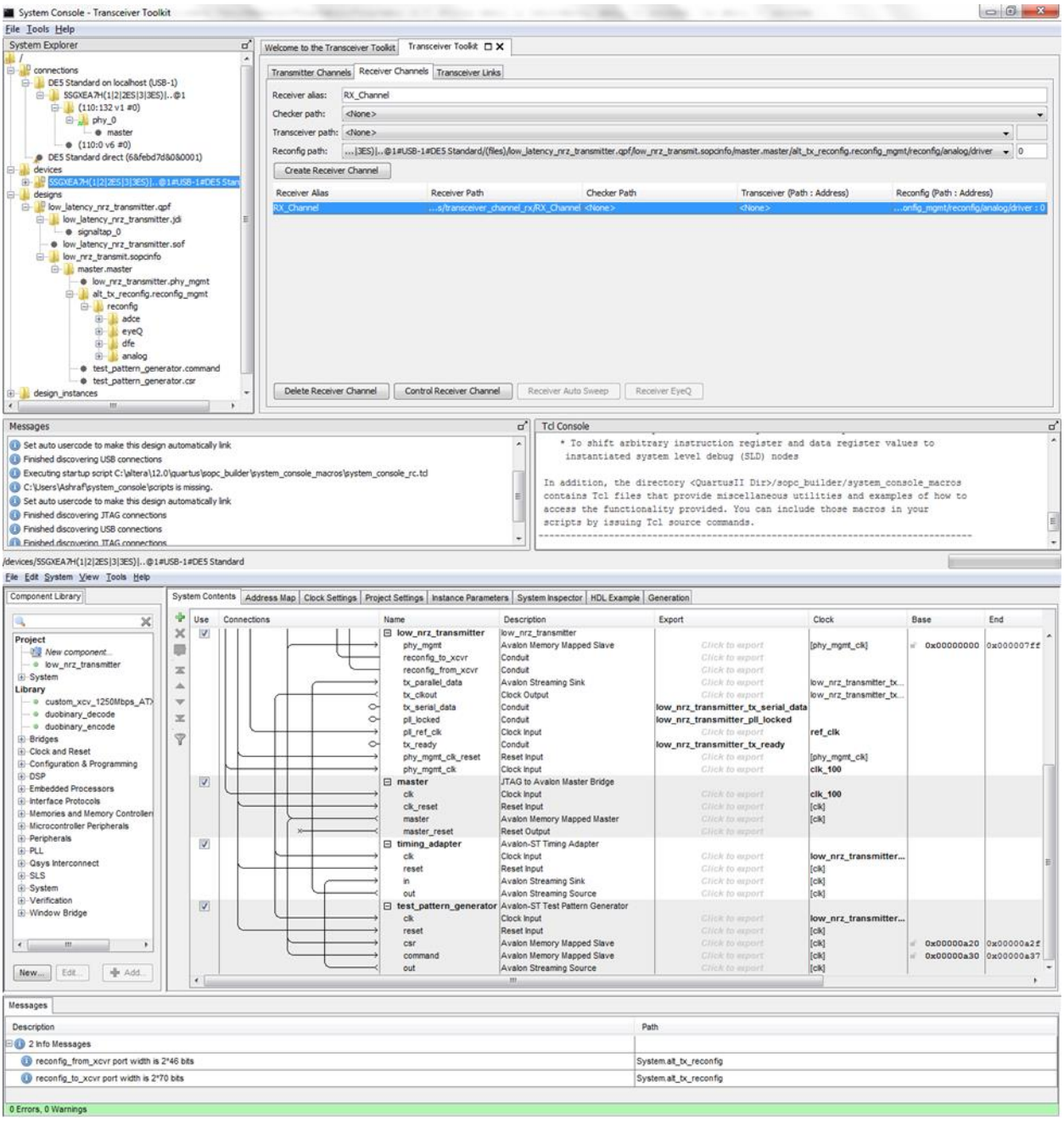
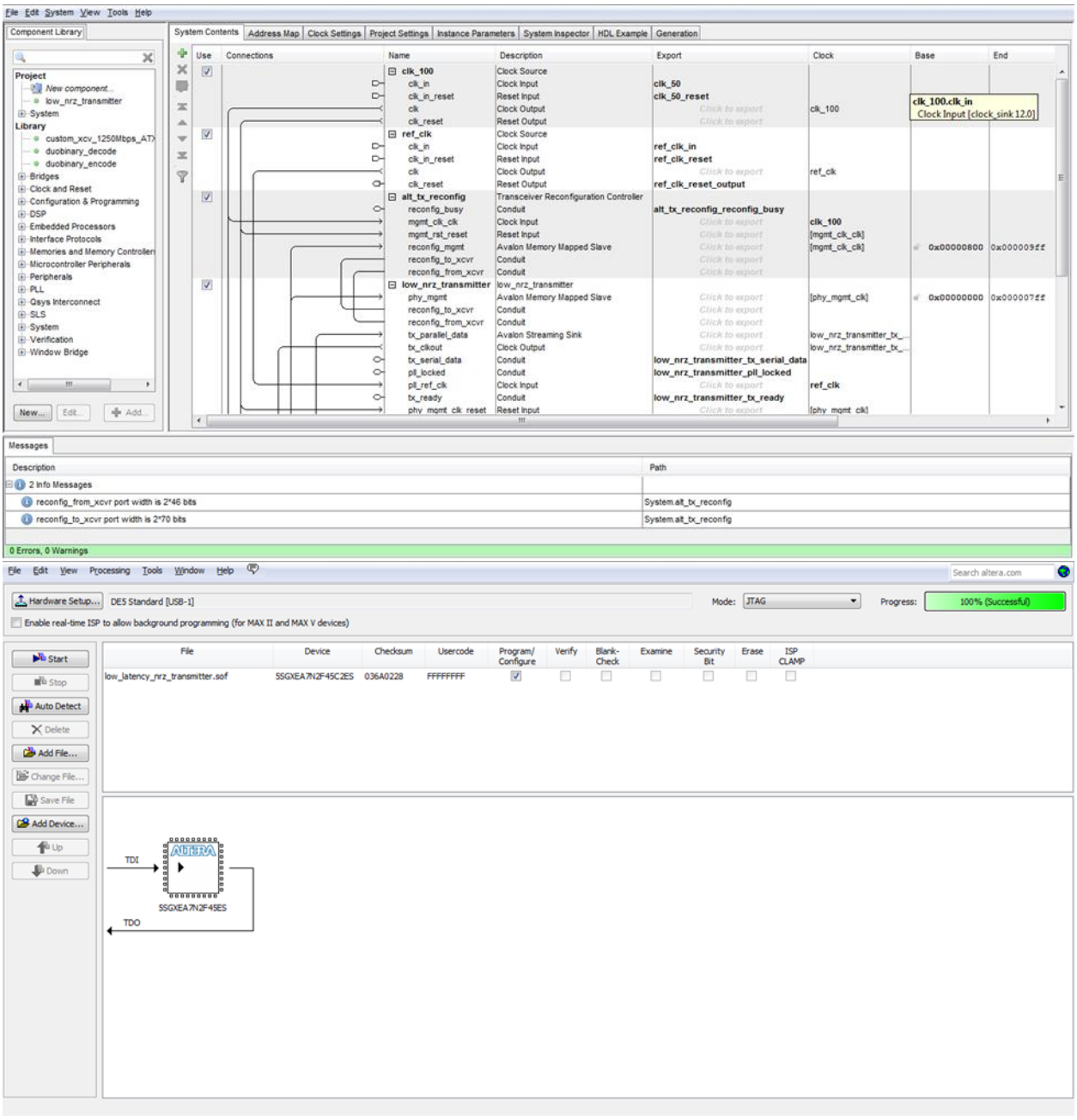
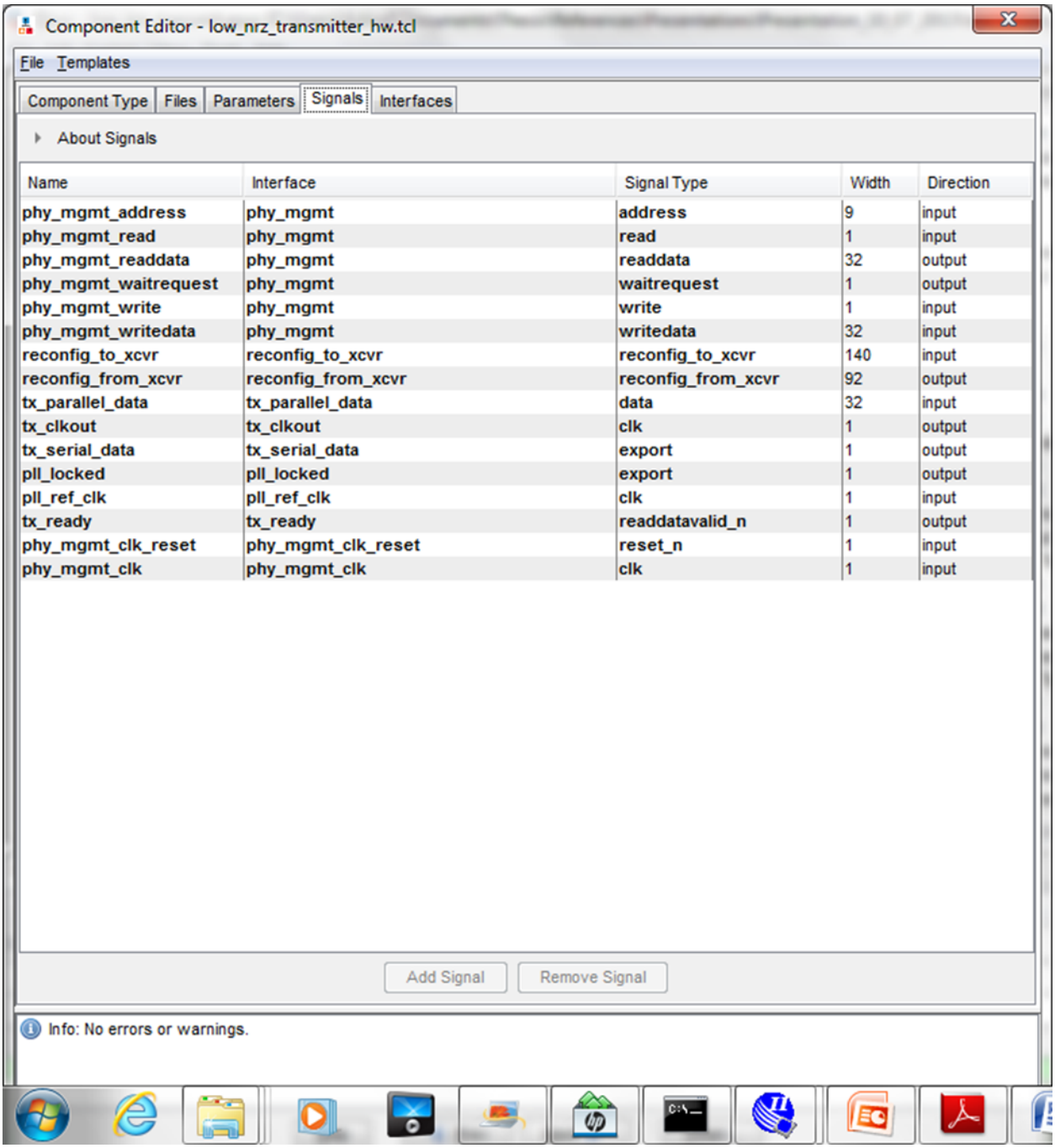
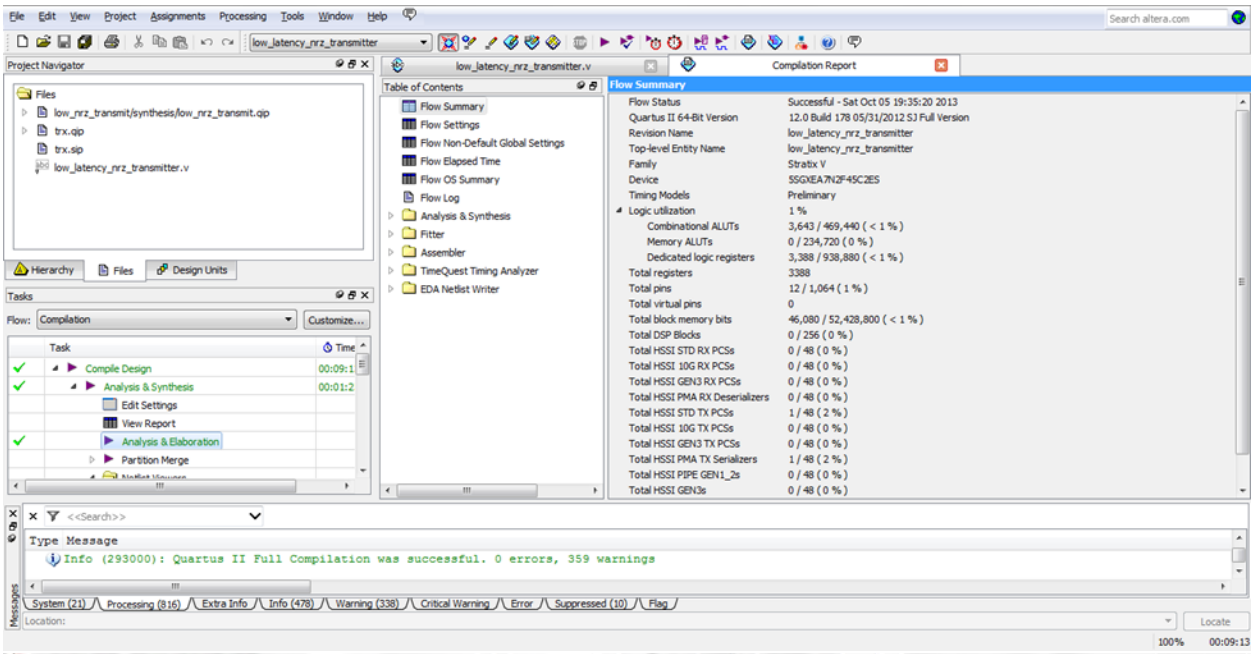

System Console - Transceiver Link: XCVR_Channel
File Tools Help
System Explorer
Welcome to the Transceiver Toolkit
Transceiver Toolkit
Transmitter: TX_Channel
Receiver: RX_Channel
Transceiver Link: XCVR_Channel
Basic
Advanced
Stopped
Test pattern:
PRBS7
Transmitter channel:
TX_Channel
Receiver channel:
RX_Channel
Transceiver
Channel address:
Data rate:
PLL refclk freq:
TX/CMU PLL status:
Reconfig
VOD control:
Pre-emphasis 1st post tap:
Pre-emphasis pre-tap:
Pre-emphasis 2nd post tap:
Generator
Preamble word:
Number of preamble beats:
Use preamble upon start
RX CDR PLL status:
RX CDR data status:
DC gain:
AEQ mode:
Equalization control:
DFE 1st tap value:
DFE 2nd tap value:
Start
Stop
Inject Error
Reset
Serial loopback
Messages
Set auto usercode to make this design automatically link
Finished discovering USB connections
Executing startup script C:\altera\12.0\quartus\sopc_builder\system_console_macros\system_console_rc.tcl
C:\Users\Ashraf\system_console\scripts is missing.
Finished discovering JTAG connections
Tcl Console
* To shift arbitrary instruction register and data register values to
instantiated system level debug (SLD) nodes
In addition, the directory <QuartusII Dir>/sopc_builder/system_console_macros
contains Tcl files that provide miscellaneous utilities and examples of how to
access the functionality provided. You can include those macros in your
scripts by issuing Tcl source commands.
/design_instances/transceiver_debug_link/XCVR_Channel
System Console - Transceiver Toolkit
File Tools Help
System Explorer
Welcome to the Transceiver Toolkit
Transceiver Toolkit
Transmitter Channels
Receiver Channels
Transceiver Links
Transceiver link alias:
XCVR_Channel
Transmitter channel:
TX_Channel : /design_instances/transceiver_channel_tx/TX_Channel
Receiver channel:
RX_Channel : /design_instances/transceiver_channel_rx/RX_Channel
Create Transceiver Link
Transceiver Link Alias
Transceiver Link Path
Transmitter Channel (Alias : Path)
Receiver Channel (Alias : Path)
XCVR_Channel
TX_Channel : /design_instances/transceiver_cha...
RX_Channel : /design_instances/transceiver_ch...
Delete Transceiver Link
Control Transceiver Link
Transceiver Auto Sweep
Transceiver EyeQ
Messages
Set auto usercode to make this design automatically link
Finished discovering USB connections
Executing startup script C:\altera\12.0\quartus\sopc_builder\system_console_macros\system_console_rc.tcl
C:\Users\Ashraf\system_console\scripts is missing.
Finished discovering JTAG connections
Tcl Console
* To shift arbitrary instruction register and data register values to
instantiated system level debug (SLD) nodes
In addition, the directory <QuartusII Dir>/sopc_builder/system_console_macros
contains Tcl files that provide miscellaneous utilities and examples of how to
access the functionality provided. You can include those macros in your
scripts by issuing Tcl source commands.
/devices/SSGXEA7H(1|2|2ES|3|3ES)..@1#USB-1#DE5 Standard

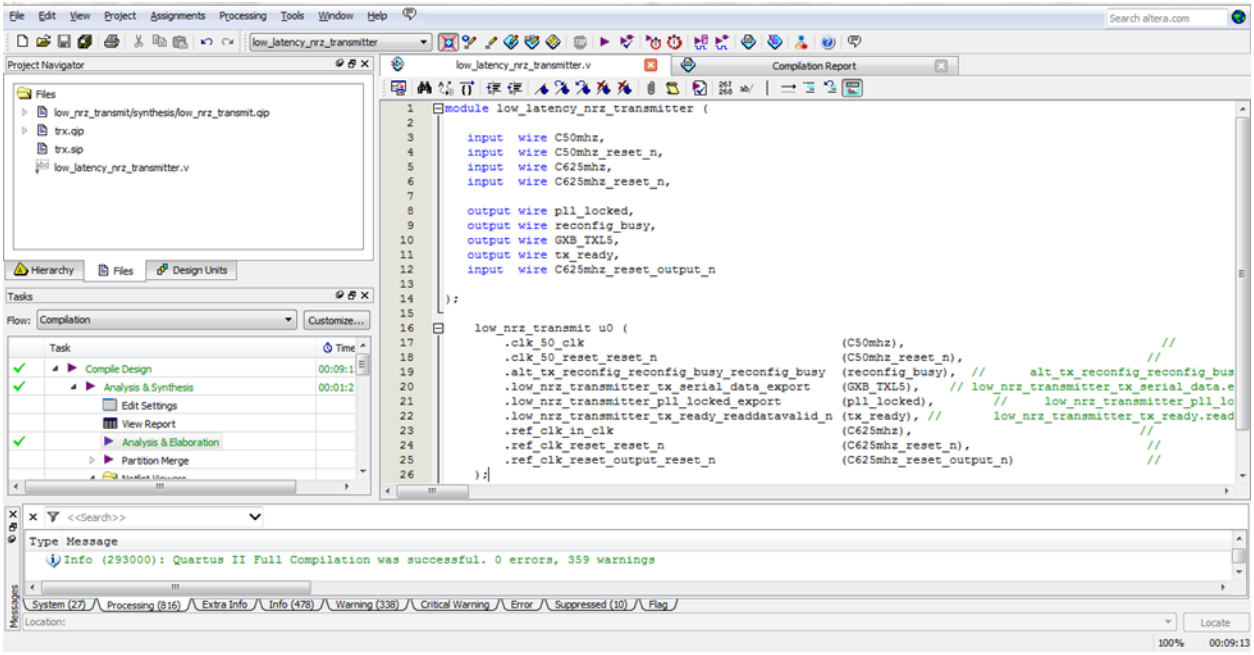

System Console - Transmitter: TX_Channel
File Tools Help
System Explorer
Welcome to the Transceiver Toolkit
Transceiver Toolkit
Transmitter: TX_Channel
Basic
Stopped
Test pattern:
PRBS7
Transmitter channel:
TX_Channel
Transceiver
Channel address:
Data rate:
PLL refclk freq:
TX/CMU PLL status:
Reconfig
Channel address:
VOD control:
Pre-emphasis 1st post tap:
Pre-emphasis pre-tap:
Pre-emphasis 2nd post tap:
Generator
Preamble word:
Number of preamble beats:
Use preamble upon start
Start
Stop
Inject Error
Messages
Set auto usercode to make this design automatically link
Finished discovering USB connections
Executing startup script C:\altera\12.0\quartus\sopc_builder\system_console_macros\system_console_rc.tcl
C:\Users\Ashraf\system_console\scripts is missing.
Set auto usercode to make this design automatically link
Finished discovering JTAG connections
Finished discovering USB connections
Tcl Console
* To shift arbitrary instruction register and data register values to
instantiated system level debug (SLD) nodes
In addition, the directory <QuartusII Dir>/sopc_builder/system_console_macros
contains Tcl files that provide miscellaneous utilities and examples of how to
access the functionality provided. You can include those macros in your
scripts by issuing Tcl source commands.
/devices/SSGXEA7H(1|2|2ES|3|3ES)|..@1#USB-1#DE5 Standard
System Console - Transceiver Toolkit
File Tools Help
System Explorer
Welcome to the Transceiver Toolkit
Transceiver Toolkit
Transmitter Channels
Receiver Channels
Transceiver Links
Transmitter alias:
TX_Channel
Generator path:
<None>
Transceiver path:
<None>
Reconfig path:
...|3ES)|..@1#USB-1#DE5 Standard/(files)/low_latency_nrz_transmitter.qpf/low_nrz_transmit.sopcinfo/master.master/alt_tx_reconfig.reconfig_mgmt/reconfig/analog/driver
Create Transmitter Channel
Transmitter Alias
Transmitter Path
Generator Path
Transceiver (Path : Address)
Reconfig (Path : Address)
TX_Channel
...s/transceiver_channel_tx/TX_Channel
<None>
<None>
...onfig_mgmt/reconfig/analog/driver : 0
Delete Transmitter Channel
Control Transmitter Channel
Messages
Set auto usercode to make this design automatically link
Finished discovering USB connections
Executing startup script C:\altera\12.0\quartus\sopc_builder\system_console_macros\system_console_rc.tcl
C:\Users\Ashraf\system_console\scripts is missing.
Set auto usercode to make this design automatically link
Finished discovering JTAG connections
Finished discovering USB connections
Tcl Console
* To shift arbitrary instruction register and data register values to
instantiated system level debug (SLD) nodes
In addition, the directory <QuartusII Dir>/sopc_builder/system_console_macros
contains Tcl files that provide miscellaneous utilities and examples of how to
access the functionality provided. You can include those macros in your
scripts by issuing Tcl source commands.
/devices/SSGXEA7H(1|2|2ES|3|3ES)|..@1#USB-1#DE5 Standard
7:45 PM
10/5/2013


System Console - Transceiver Toolkit
File Tools Help
System Explorer
Welcome to the Transceiver Toolkit
Transceiver Toolkit
Transmitter Channels
Receiver Channels
Transceiver Links
Receiver alias: RX_Channel
Checker path: <None>
Transceiver path: <None>
Reconfig path:
Create Receiver Channel
Receiver Alias
Receiver Path
Checker Path
Transceiver (Path : Address)
Reconfig (Path : Address)
RX_Channel
Delete Receiver Channel
Control Receiver Channel
Receiver Auto Sweep
Receiver EyeQ
Messages
Set auto usercode to make this design automatically link
Finished discovering USB connections
Executing startup script C:\altera\12.0\quartus\sopc_builder\system_console_macros\system_console_rc.tcl
C:\Users\Ashraf\system_console\scripts is missing.
Set auto usercode to make this design automatically link
Finished discovering JTAG connections
Finished discovering USB connections
Tcl Console
* To shift arbitrary instruction register and data register values to
instantiated system level debug (SLD) nodes
In addition, the directory <QuartusII Dir>/sopc_builder/system_console_macros
contains Tcl files that provide miscellaneous utilities and examples of how to
access the functionality provided. You can include those macros in your
scripts by issuing Tcl source commands.
/devices/SSGXEA7H(1|2|2ES|3|3ES)|..@1#USB-1#DE5 Standard
File Edit System View Tools Help
Component Library
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
End
low_nrz_transmitter
master
timing_adapter
test_pattern_generator
Messages
Description
Path
2 Info Messages
reconfig_from_xcvr port width is 2*46 bits
reconfig_to_xcvr port width is 2*70 bits
System.alt_tx_reconfig
0 Errors, 0 Warnings


File Edit System View Tools Help
Component Library
Project
New component...
low_nrz_transmitter
System
Library
custom_xcv_1250Mbps_AT
duobinary_decode
duobinary_encode
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Controller
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
SLS
System
Verification
Window Bridge
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
End
clk_100
Clock Source
clk_in
Clock Input
clk_50
clk_in_reset
Reset Input
clk_50_reset
clk
Clock Output
clk_100
clk_reset
Reset Output
clk_100.clk_in
Clock Input [clock_sink 12.0]
ref_clk
Clock Source
clk_in
Clock Input
ref_clk_in
clk_in_reset
Reset Input
ref_clk_reset
clk
Clock Output
ref_clk
clk_reset
Reset Output
ref_clk_reset_output
alt_tx_reconfig
Transceiver Reconfiguration Controller
reconfig_busy
Conduit
alt_tx_reconfig_reconfig_busy
mgmt_clk_clk
Clock Input
clk_100
mgmt_rst_reset
Reset Input
[mgmt_clk_clk]
reconfig_mgmt
Avalon Memory Mapped Slave
[mgmt_clk_clk]
0x00000800
0x000009ff
reconfig_to_xcvr
Conduit
reconfig_from_xcvr
Conduit
low_nrz_transmitter
low_nrz_transmitter
phy_mgmt
Avalon Memory Mapped Slave
[phy_mgmt_clk]
0x00000000
0x000007ff
reconfig_to_xcvr
Conduit
reconfig_from_xcvr
Conduit
tx_parallel_data
Avalon Streaming Sink
low_nrz_transmitter_tx_...
tx_clkout
Clock Output
low_nrz_transmitter_tx_...
tx_serial_data
Conduit
low_nrz_transmitter_tx_serial_data
pll_locked
Conduit
low_nrz_transmitter_pll_locked
pll_ref_clk
Clock Input
ref_clk
tx_ready
Conduit
low_nrz_transmitter_tx_ready
phy_mgmt_clk_reset
Reset Input
[phy_mgmt_clk]
Messages
Description
Path
2 Info Messages
reconfig_from_xcvr port width is 2*46 bits
System.alt_tx_reconfig
reconfig_to_xcvr port width is 2*70 bits
System.alt_tx_reconfig
0 Errors, 0 Warnings
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
DE5 Standard [USB-1]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
low_latency_nrz_transmitter.sof
5SGXEA7N2F45C2ES
036A0228
FFFFFFFF
TDI
TDO
5SGXEA7N2F45ES


Component Editor - low_nrz_transmitter_hw.tcl
File Templates
Component Type
Files
Parameters
Signals
Interfaces
About Signals
Name
Interface
Signal Type
Width
Direction
phy_mgmt_address
phy_mgmt
address
9
input
phy_mgmt_read
phy_mgmt
read
1
input
phy_mgmt_readdata
phy_mgmt
readdata
32
output
phy_mgmt_waitrequest
phy_mgmt
waitrequest
1
output
phy_mgmt_write
phy_mgmt
write
1
input
phy_mgmt_writedata
phy_mgmt
writedata
32
input
reconfig_to_xcvr
reconfig_to_xcvr
reconfig_to_xcvr
140
input
reconfig_from_xcvr
reconfig_from_xcvr
reconfig_from_xcvr
92
output
tx_parallel_data
tx_parallel_data
data
32
input
tx_clkout
tx_clkout
clk
1
output
tx_serial_data
tx_serial_data
export
1
output
pll_locked
pll_locked
export
1
output
pll_ref_clk
pll_ref_clk
clk
1
input
tx_ready
tx_ready
readdatavalid_n
1
output
phy_mgmt_clk_reset
phy_mgmt_clk_reset
reset_n
1
input
phy_mgmt_clk
phy_mgmt_clk
clk
1
input
Add Signal
Remove Signal
Info: No errors or warnings.


File Edit View Project Assignments Processing Tools Window Help
Search altera.com
low_latency_nrz_transmitter
Project Navigator
Files
low_nrz_transmit/synthesis/low_nrz_transmit.qip
trx.qip
trx.sip
low_latency_nrz_transmitter.v
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Time
Compile Design 00:09:1
Analysis & Synthesis 00:01:2
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
low_latency_nrz_transmitter.v
Compilation Report
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Sat Oct 05 19:35:20 2013
Quartus II 64-Bit Version 12.0 Build 178 05/31/2012 SJ Full Version
Revision Name low_latency_nrz_transmitter
Top-level Entity Name low_latency_nrz_transmitter
Family Stratix V
Device 5SGXEA7N2F45C2ES
Timing Models Preliminary
Logic utilization 1 %
Combinational ALUTs 3,643 / 469,440 (< 1 %)
Memory ALUTs 0 / 234,720 (0 %)
Dedicated logic registers 3,388 / 938,880 (< 1 %)
Total registers 3388
Total pins 12 / 1,064 (1 %)
Total virtual pins 0
Total block memory bits 46,080 / 52,428,800 (< 1 %)
Total DSP Blocks 0 / 256 (0 %)
Total HSSI STD RX PCSs 0 / 48 (0 %)
Total HSSI 10G RX PCSs 0 / 48 (0 %)
Total HSSI GEN3 RX PCSs 0 / 48 (0 %)
Total HSSI PMA RX Deserializers 0 / 48 (0 %)
Total HSSI STD TX PCSs 1 / 48 (2 %)
Total HSSI 10G TX PCSs 0 / 48 (0 %)
Total HSSI GEN3 TX PCSs 0 / 48 (0 %)
Total HSSI PMA TX Serializers 1 / 48 (2 %)
Total HSSI PIPE GEN1_2s 0 / 48 (0 %)
Total HSSI GEN3s 0 / 48 (0 %)
<<Search>>
Type Message
Info (293000): Quartus II Full Compilation was successful. 0 errors, 359 warnings
System (21) Processing (816) Extra Info Info (478) Warning (338) Critical Warning Error Suppressed (10) Flag
Location:
Locate
100%
00:09:13


File Edit View Project Assignments Processing Tools Window Help
Search altera.com
low_latency_nrz_transmitter
Project Navigator
Files
low_nrz_transmit/synthesis/low_nrz_transmit.qip
trx.qip
trx.sip
low_latency_nrz_transmitter.v
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Time
Compile Design 00:09:1
Analysis & Synthesis 00:01:2
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
low_latency_nrz_transmitter.v
Compilation Report
module low_latency_nrz_transmitter (
input wire C50mhz,
input wire C50mhz_reset_n,
input wire C625mhz,
input wire C625mhz_reset_n,
output wire pll_locked,
output wire reconfig_busy,
output wire GXB_TXL5,
output wire tx_ready,
input wire C625mhz_reset_output_n
);
low_nrz_transmit u0 (
.clk_50_clk (C50mhz), //
.clk_50_reset_reset_n (C50mhz_reset_n), //
.alt_tx_reconfig_reconfig_busy_reconfig_busy (reconfig_busy), // alt_tx_reconfig_reconfig_bus
.low_nrz_transmitter_tx_serial_data_export (GXB_TXL5), // low_nrz_transmitter_tx_serial_data.e
.low_nrz_transmitter_pll_locked_export (pll_locked), // low_nrz_transmitter_pll_lo
.low_nrz_transmitter_tx_ready_readdatavalid_n (tx_ready), // low_nrz_transmitter_tx_ready.read
.ref_clk_in_clk (C625mhz), //
.ref_clk_reset_reset_n (C625mhz_reset_n), //
.ref_clk_reset_output_reset_n (C625mhz_reset_output_n) //
);
<<Search>>
Type Message
Info (293000): Quartus II Full Compilation was successful. 0 errors, 359 warnings
System (27) Processing (816) Extra Info Info (478) Warning (338) Critical Warning Error Suppressed (10) Flag
Location:
Locate
100%
00:09:13