1.3 Power-on Timing

Figure 1 shows a diagram of the power-on timing for the TS4 board. The power-on sequence is;

- The user turns on the main power switch, which enables the chassis 12V power.
- The host CPU (PCIe root-complex) powers up, initializes, asserts the PCIe reset signal, waits 100ms, and then enumerates the PCIe bus (these tasks are typically implemented by firmware in the host CPU BIOS or bootloader).
- The peripheral board PCIe end-point has two implementation options;
  - An FPGA-based PCIe end-point (eg., Altera Cyclone IV GX [2]).
    The peripheral board powers up, the FPGA configures prior to PCIe reset deassertion, when reset deasserts, the PCIe end-point begins link training, and within 20ms is ready for PCIe accesses.
    The configuration time for a Cyclone IV GX EP4CGX15 configured via Fast Passive Parallel (FPP) mode using a 66MHz clock is; 3ms power-supply ramp + 9ms power-on-reset delay + 3,805,568-bits/66MHz = 70ms.
  - A processor-based PCIe end-point (eg., Freescale MPC8308 [18]).
    The peripheral board powers up, when reset deasserts, the PCIe end-point begins link training, and within 20ms is ready for PCIe accesses. If the processor software has not enabled the PCIe end-point by the time the host attempts a configuration space access, those accesses will receive a PCIe retry response. The end-point is allowed to issue retry responses for up to one second from the deassertion of PCIe reset.

The power-on timing in Figure 1 is specified in the following references;

- PCI Express Specification [11]:
  - A component must enter link training within 20ms of the deassertion of `PERST#` (p406 [11]).
  - System software must wait 100ms from the deassertion of `PERST#` before issuing configuration space accesses (p406 [11]).
  - System software must allow 1.0s before it can determine that configuration space accesses have failed (p406 [11]), i.e., an end-point can issue a PCIe retry for up to 1.0s.
  - T_{PVPERL} defines the time `PERST#` must remain active after power becomes valid. T_{PERST} defines the time `PERST#` must remain active when asserted. These timing parameters are platform specific (p407 [11]).
- CPCI-S.0 Specification [12]:
  - The system slot must drive PCIe reset low once the main 12V supply reaches 5V (p80 [12]).
  - $T_{\mathrm{RST}} > 1$ms (Table 13, p80 [12]). This parameter is the platform-specific T_{PERST} defined in the PCI Express specification.
- PCI Express Card Electromechanical (CEM) specification [10]
  - This specification discusses the implementation of desktop form-factor PCIe systems (also known as ATX or Advanced Technology eXtended motherboards). CPCI-S.0 power supplies are based on ATX power supplies, so the power supply discussion in this specification is relevant.
  - Deassertion of `PERST#` occurs $T_{\mathrm{PVPERL}} = 100$ms after power is stable (p22 [10]). Figure 1 is similar to Figure 2-10 on p23 [10].
  - The Intel ATX power supply design guide specifies 100ms $< T_{\mathrm{PVPERL}} <$ 500ms (see the T3 parameter in Figure 7 p25 and Table 15 p26 [7]).

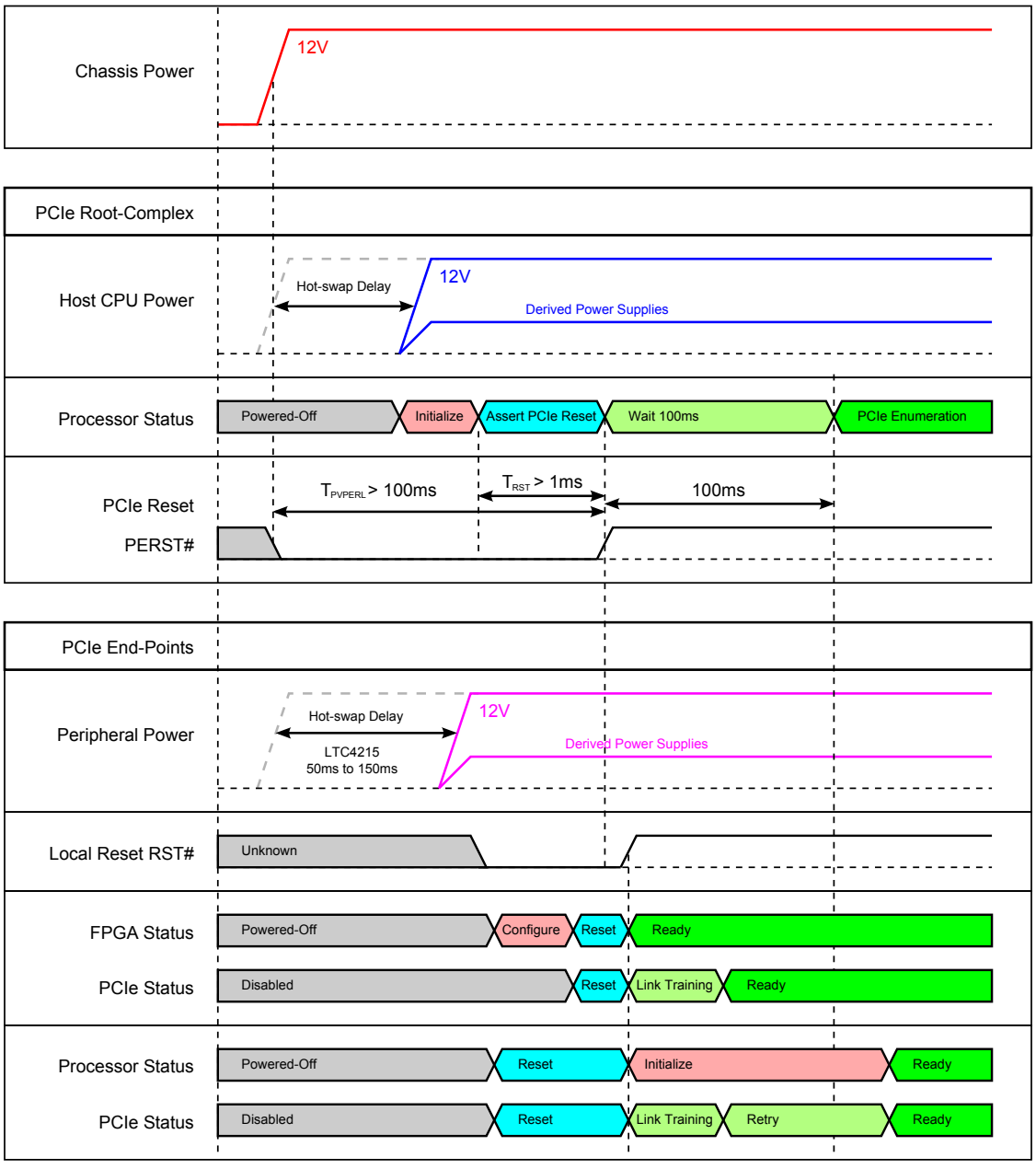

Figure 1: CPCI-S.0 power-on timing.

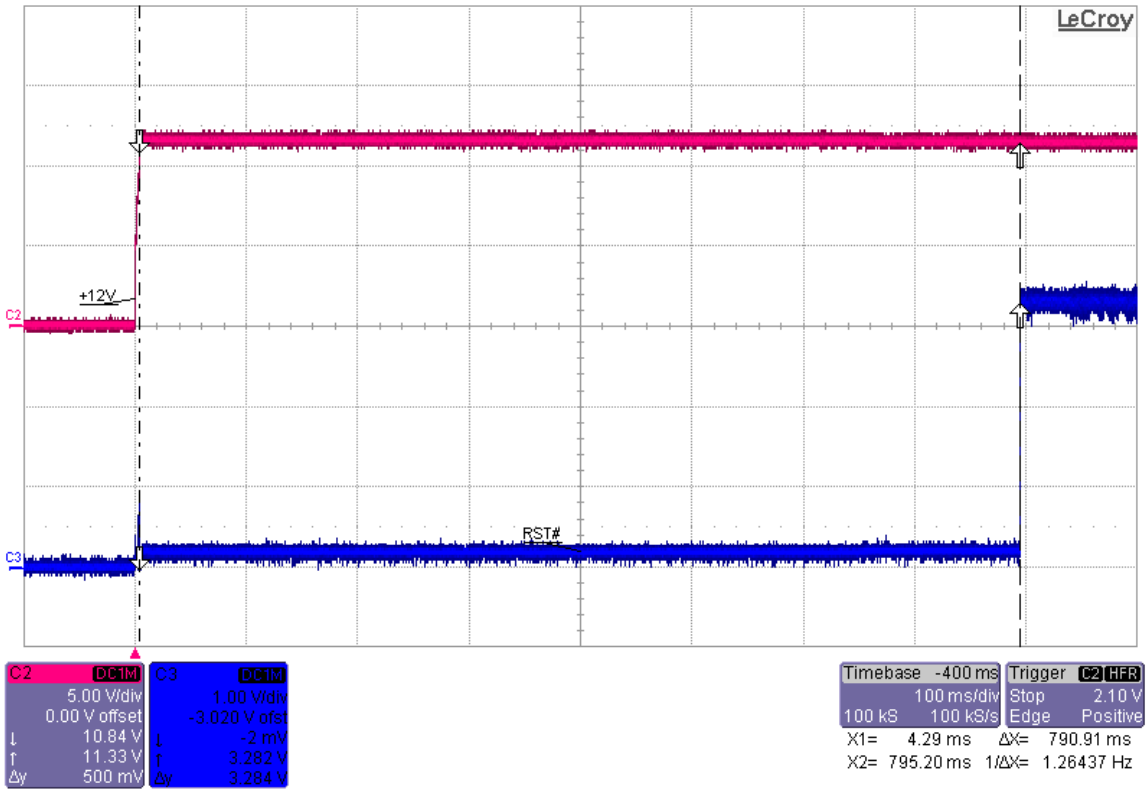

Figure 2: MEN G20 CPCI-S.0 host CPU board 12V to PCIe reset power-on timing.

Figure 2 shows the power-on timing of the MEN G20 CPCI-S.0 CPU (image courtesy of Stephen Cunha, MEN Microelectronics, 7/11/2012). PCIe reset deasserts approximately 800ms after the 12V supply is valid. This provides sufficient time for a PCIe end-point to be implemented using either an FPGA or processor.

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