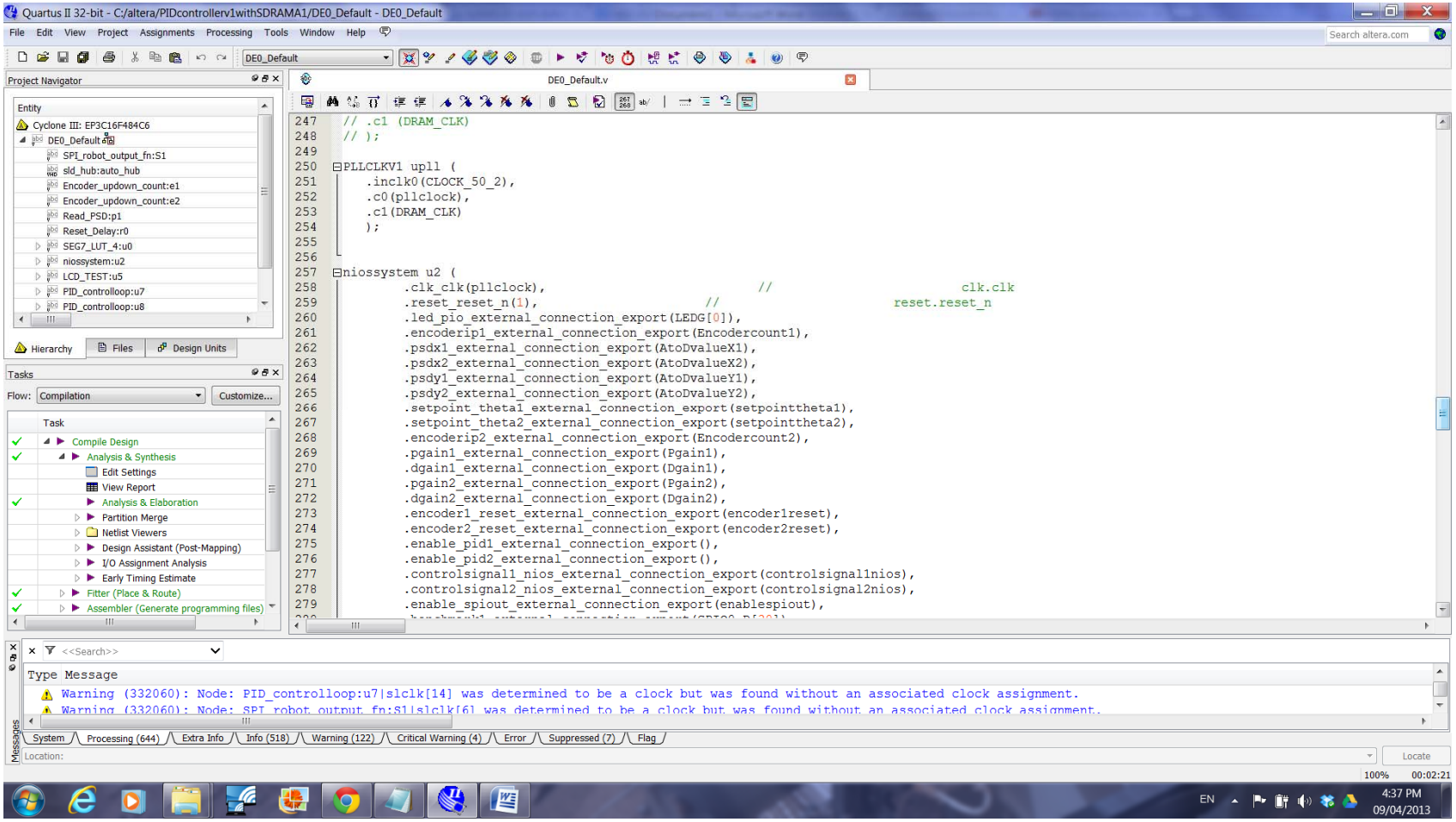
Quartus II 32-bit - C:/altera/PIDcontrollerv1withSDRAMA1/DE0_Default - DE0_Default
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
DE0_Default
Project Navigator
Entity
Cyclone III: EP3C16F484C6
DE0_Default
SPI_robot_output_fn:S1
sld_hub:auto_hub
Encoder_updown_count:e1
Encoder_updown_count:e2
Read_PSD:p1
Reset_Delay:r0
SEG7_LUT_4:u0
niossystem:u2
LCD_TEST:u5
PID_controlloop:u7
PID_controlloop:u8
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
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View Report
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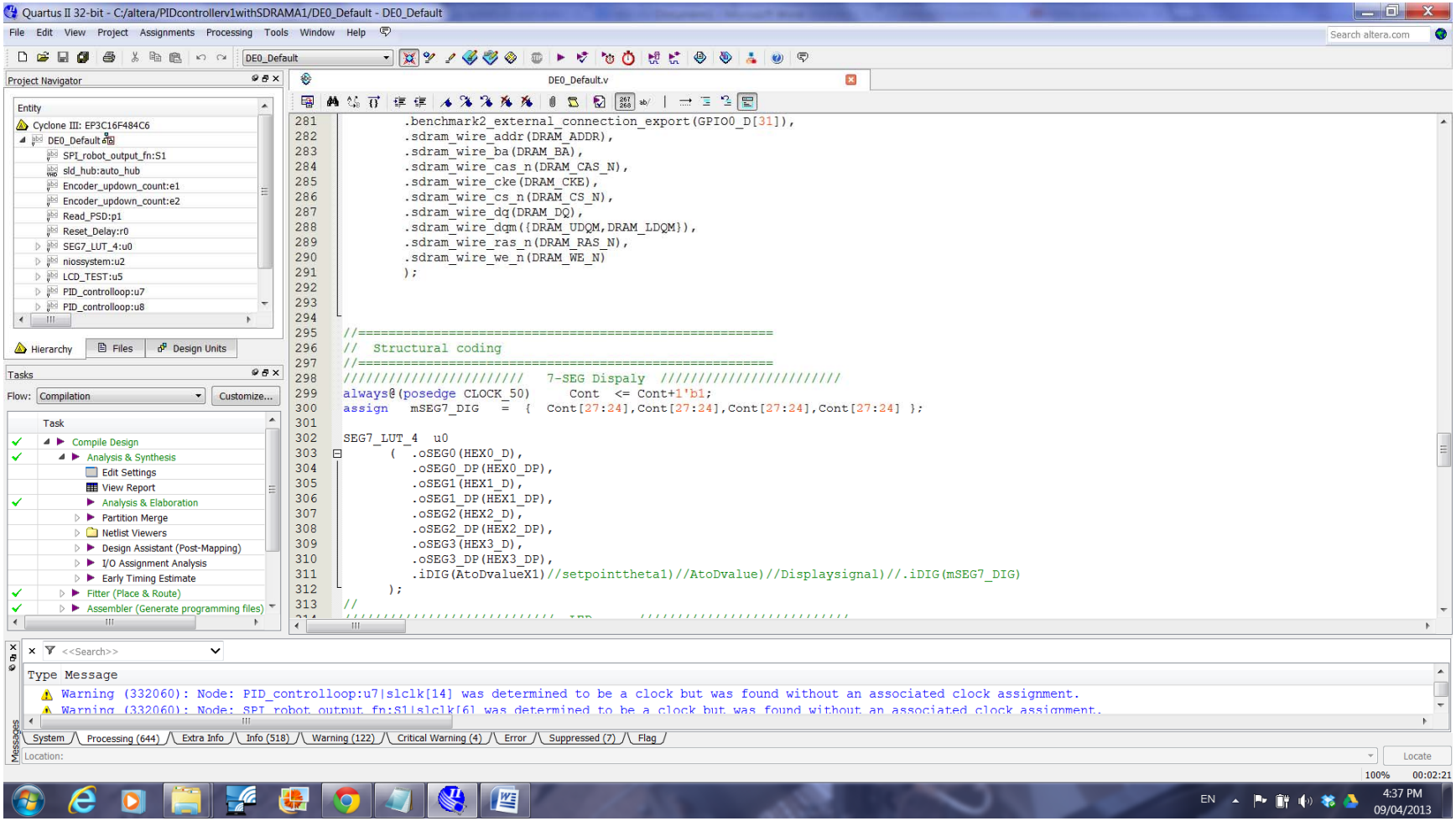
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapping)
I/O Assignment Analysis
Early Timing Estimate
Fitter (Place & Route)
Assembler (Generate programming files)
DE0_Default.v
247 // .c1 (DRAM_CLK)
248 //);
249
250 PLLCLKV1 upll (
251 .inclk0(CLOCK_50_2),
252 .c0(pllclock),
253 .c1(DRAM_CLK)
254);
255
256
257 niossystem u2 (
258 .clk_clk(pllclock), // clk.clk
259 .reset_reset_n(1), // reset.reset_n
260 .led_pio_external_connection_export(LEDG[0]),
261 .encoderip1_external_connection_export(Encodercount1),
262 .psdx1_external_connection_export(AtoDvalueX1),
263 .psdx2_external_connection_export(AtoDvalueX2),
264 .psdy1_external_connection_export(AtoDvalueY1),
265 .psdy2_external_connection_export(AtoDvalueY2),
266 .setpoint_theta1_external_connection_export(setpointtheta1),
267 .setpoint_theta2_external_connection_export(setpointtheta2),
268 .encoderip2_external_connection_export(Encodercount2),
269 .pgain1_external_connection_export(Pgain1),
270 .dgain1_external_connection_export(Dgain1),
271 .pgain2_external_connection_export(Pgain2),
272 .dgain2_external_connection_export(Dgain2),
273 .encoder1_reset_external_connection_export(encoder1reset),
274 .encoder2_reset_external_connection_export(encoder2reset),
275 .enable_pid1_external_connection_export(),
276 .enable_pid2_external_connection_export(),
277 .controlsignal1_nios_external_connection_export(controlsignal1nios),
278 .controlsignal2_nios_external_connection_export(controlsignal2nios),
279 .enable_spiout_external_connection_export(enablespiout),
<<Search>>
Type Message
Warning (332060): Node: PID_controlloop:u7|slclk[14] was determined to be a clock but was found without an associated clock assignment.
Warning (332060): Node: SPI_robot_output_fn:S1|slclk[6] was determined to be a clock but was found without an associated clock assignment.
Messages
System
Processing (644)
Extra Info
Info (518)
Warning (122)
Critical Warning (4)
Error
Suppressed (7)
Flag
Location:
Locate
100%
00:02:21
EN
4:37 PM
09/04/2013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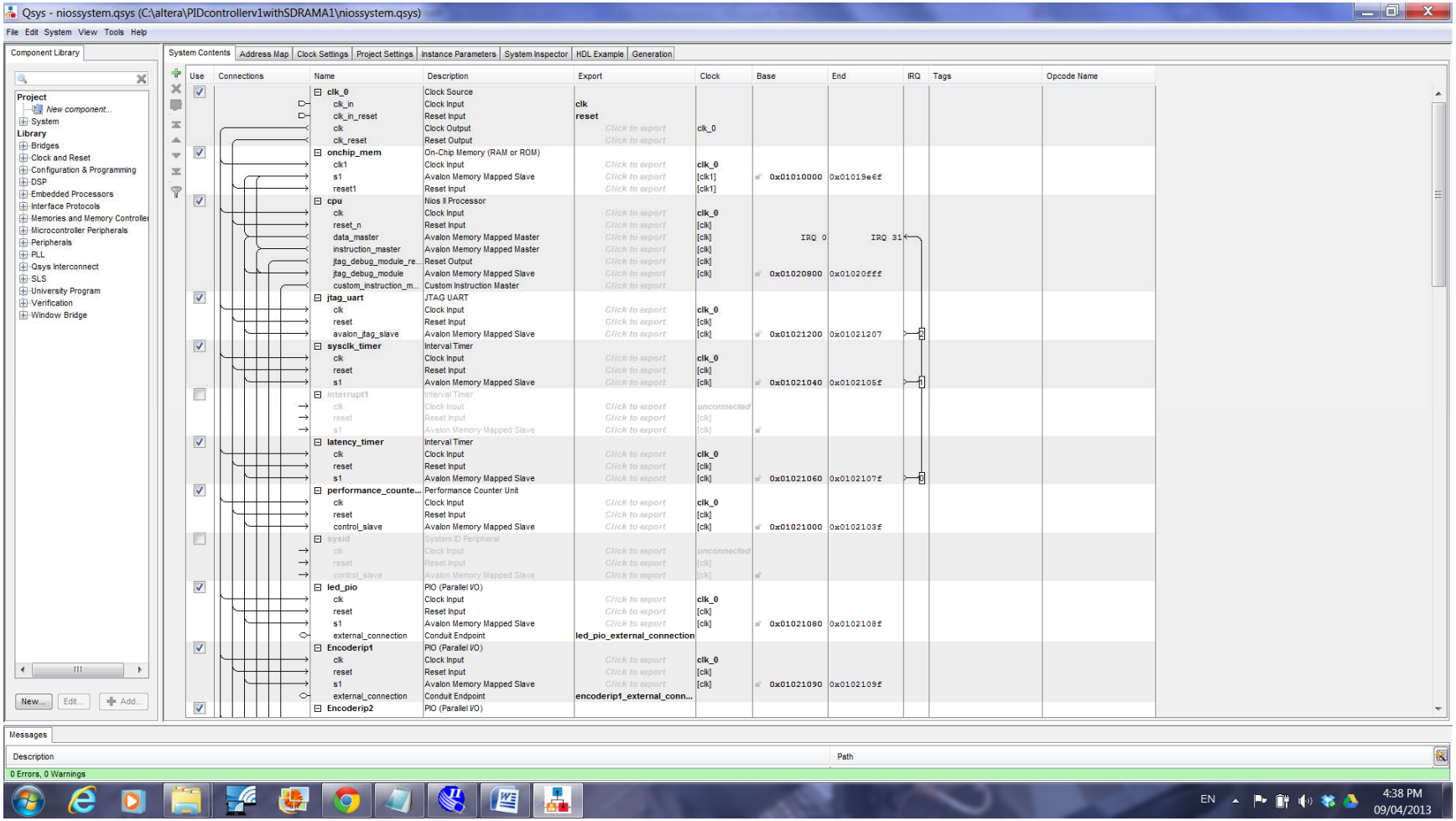
I/O Assignment Analysis
Early Timing Estimate
Fitter (Place & Route)
Assembler (Generate programming files)
DE0_Default.v
281 .benchmark2_external_connection_export(GPIO0_D[31]),
282 .sdram_wire_addr(DRAM_ADDR),
283 .sdram_wire_ba(DRAM_BA),
284 .sdram_wire_cas_n(DRAM_CAS_N),
285 .sdram_wire_cke(DRAM_CKE),
286 .sdram_wire_cs_n(DRAM_CS_N),
287 .sdram_wire_dq(DRAM_DQ),
288 .sdram_wire_dqm({DRAM_UDQM,DRAM_LDQM}),
289 .sdram_wire_ras_n(DRAM_RAS_N),
290 .sdram_wire_we_n(DRAM_WE_N)
291);
294
295 //===
296 // Structural coding
297 //===
298 ////////////////////// 7-SEG Dispaly //////////////////////
299 always@(posedge CLOCK_50) Cont <= Cont+1'b1;
300 assign mSEG7_DIG = { Cont[27:24],Cont[27:24],Cont[27:24],Cont[27:24] };
302 SEG7_LUT_4 u0
303 (.oSEG0(HEX0_D),
304 .oSEG0_DP(HEX0_DP),
305 .oSEG1(HEX1_D),
306 .oSEG1_DP(HEX1_DP),
307 .oSEG2(HEX2_D),
308 .oSEG2_DP(HEX2_DP),
309 .oSEG3(HEX3_D),
310 .oSEG3_DP(HEX3_DP),
311 .iDIG(AtoDvalueX1)//setpointtheta1)//AtoDvalue)//Displaysignal)//.iDIG(mSEG7_DIG)
312);
313 //
<<Search>>
Type Message
Warning (332060): Node: PID_controlloop:u7|slclk[14] was determined to be a clock but was found without an associated clock assignment.
Warning (332060): Node: SPI_robot_output_fn:S1|slclk[6] was determined to be a clock but was found without an associated clock assignment.
System Processing (644) Extra Info Info (518) Warning (122) Critical Warning (4) Error Suppressed (7) Flag
Location:
Locate
Messages
100% 00:02:21
EN
4:37 PM
09/04/2013


Qsys - niossystem.qsys (C:\altera\PIDcontrollerv1withSDRAMA1\niossystem.qsys)
File Edit System View Tools Help
Component Library
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New component...
System
Library
Bridges
Clock and Reset
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Microcontroller Peripherals
Peripherals
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Qsys Interconnect
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Verification
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Edit...
Add...
System Contents
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clk_0
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_0
clk_reset
Reset Output
onchip_mem
On-Chip Memory (RAM or ROM)
clk1
Clock Input
clk_0
s1
Avalon Memory Mapped Slave
[clk1]
0x01010000
0x01019e6f
reset1
Reset Input
[clk1]
cpu
Nios II Processor
clk
Clock Input
clk_0
reset_n
Reset Input
[clk]
data_master
Avalon Memory Mapped Master
[clk]
IRQ 0
IRQ 31
instruction_master
Avalon Memory Mapped Master
[clk]
jtag_debug_module_re...
Reset Output
[clk]
jtag_debug_module
Avalon Memory Mapped Slave
[clk]
0x01020800
0x01020fff
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
clk_0
reset
Reset Input
[clk]
avalon_jtag_slave
Avalon Memory Mapped Slave
[clk]
0x01021200
0x01021207
sysclk_timer
Interval Timer
clk
Clock Input
clk_0
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
[clk]
0x01021040
0x0102105f
interrupt1
Interval Timer
clk
Clock Input
unconnected
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
[clk]
latency_timer
Interval Timer
clk
Clock Input
clk_0
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
[clk]
0x01021060
0x0102107f
performance_counte...
Performance Counter Unit
clk
Clock Input
clk_0
reset
Reset Input
[clk]
control_slave
Avalon Memory Mapped Slave
[clk]
0x01021000
0x0102103f
sysid
System ID Peripheral
clk
Clock Input
unconnected
reset
Reset Input
[clk]
control_slave
Avalon Memory Mapped Slave
[clk]
led_pio
PIO (Parallel I/O)
clk
Clock Input
clk_0
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
[clk]
0x01021080
0x0102108f
external_connection
Conduit Endpoint
led_pio_external_connection
Encoderip1
PIO (Parallel I/O)
clk
Clock Input
clk_0
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
[clk]
0x01021090
0x0102109f
external_connection
Conduit Endpoint
encoderip1_external_conn...
Encoderip2
PIO (Parallel I/O)
Click to export
Messages
Description
Path
0 Errors, 0 Warnings
EN
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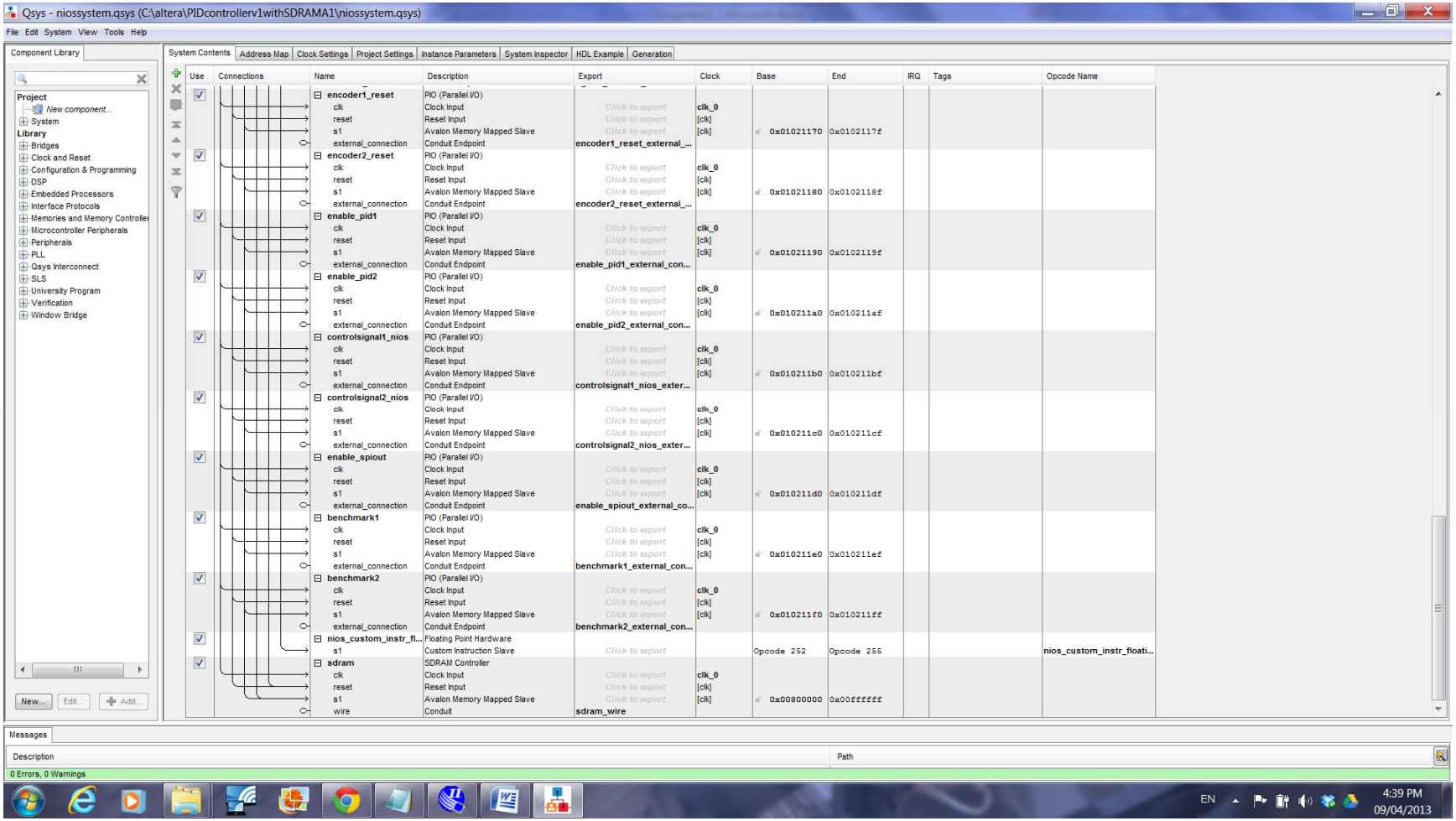
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Name
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Base
End
IRQ
Tags
Opcode Name
encoder1_reset
PIO (Parallel I/O)
clk
Clock Input
clk_0
reset
Reset Input
[clk]
s1
Avalon Memory Mapped Slave
0x01021170
0x0102117f
external_connection
Conduit Endpoint
encoder1_reset_external_...
encoder2_reset
PIO (Parallel I/O)
0x01021180
0x0102118f
encoder2_reset_external_...
enable_pid1
PIO (Parallel I/O)
0x01021190
0x0102119f
enable_pid1_external_con...
enable_pid2
PIO (Parallel I/O)
0x010211a0
0x010211af
enable_pid2_external_con...
controlsignal1_nios
PIO (Parallel I/O)
0x010211b0
0x010211bf
controlsignal1_nios_exter...
controlsignal2_nios
PIO (Parallel I/O)
0x010211c0
0x010211cf
controlsignal2_nios_exter...
enable_spiout
PIO (Parallel I/O)
0x010211d0
0x010211df
enable_spiout_external_co...
benchmark1
PIO (Parallel I/O)
0x010211e0
0x010211ef
benchmark1_external_con...
benchmark2
PIO (Parallel I/O)
0x010211f0
0x010211ff
benchmark2_external_con...
nios_custom_instr_fl...
Floating Point Hardware
s1
Custom Instruction Slave
Opcode 252
Opcode 255
nios_custom_instr_floati...
sdram
SDRAM Controller
0x00800000
0x00ffffff
wire
Conduit
sdram_wire
Click to export
Messages
Description
Path
0 Errors, 0 Warnings
EN
4:39 PM
09/04/2013