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A study on the low-cost digital spectrum analyzer design

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Abstract – **In a communication system having a limited bandwidth, it is very important to analyze the spectrum. The spectral analysis is performed by measuring the power of signal within a specific frequency band. A commercial spectrum analyzer is usually employed for instrument equipment and cannot be utilized for a communication auxiliary device because of its high cost. In this study, the low-cost digital spectrum analyzer is proposed and is implemented into FPGA chipsets, in which multiple filter banks are realized into a single FIR (Finite Impulse response) filter structure in order to reduce the size of the hardware. In order to decrease the complexity of the filter, it reduces sampling frequency by using the DDC (Digital Down Convertor). The proposed system is very useful for communication systems to increase the bandwidth efficiency with a low-cost and the high performance.**

Keywords- Digital spectrum analyser, FIR filter, Digital down convertor, CIC filter, Decimation.

I. INTRODUCTION

Recently, with the development of wireless communications, the demand of frequency has increased rapidly. In a communication with a limited bandwidth, it is very important to analyze spectrum in the frequency domain. By analyzing the spectrum which is a frequency component of a communication signal for analyzing performance of the communication system, it is possible to measure the characteristics of the communication signal. It represent that system is worked properly and information is transmitted accurately by measuring the communication signals. It is useful to know the characteristic of the communication signal such as interference between communication bands. Spectrum analysis is easy to analyze that it shows the spectrum of the signal component of the communication system optically. The methods of spectral analysis are sweep method which is analog method and Fourier Transform method which is digital method. Sweep method is based on the Super-Heterodyne technique [1]. It is able to do down conversion with PLL and while it transferred one by one the frequency of the PLL and determined RBW (Resolution Bandwidth) of fixed BPF (Band-Pass Filter), it gets past the spectrum in the RBW BPF. And it is method of reading the power in the log amplifier. The analog method is complicated to use a lot of power and expensive. Through a mathematical conversion process discrete input signal which is digitally sampled, by A/D (Analog/Digital) convertor, Fourier Transform is analyzed spectrum by FFT (Fast Fourier Transform) which is Radix-2 DIT (Decimation In Time) DFT (Discrete Fourier Transform) in the frequency domain [2-4]. With both the DSP (Digital Signal Processor) chipsets and embedded systems the methods of spectral analysis are increased the performance of spectral analysis dramatically, but they are raised the price correspondingly [5-10]. Digital spectrum analyzer with conventional FPGA (Field-Programmable Gate Array) chipsets are used a number of filters (Low-Pass Filter, Band-Pass Filter, RBW, and VBW) for analyzing signal. When it is implemented with the hardware, it is increased hardware complexity and area by the filter. Consequently, the size of FPGA has to be increase.

In this paper, it is implemented that digital spectrum analyzer can be analyzed from 5MHz to 10MHz band of the signal to 1MHz and 100KHz resolution in the sampling frequency of 40MHz. To reduce the complexity of the filters used in digital traditional spectrum analyzer, multiple filter banks are realized into a single FIR filter structure [11]. It is possible to reduce the area of hardware using the DDC multiple stages.

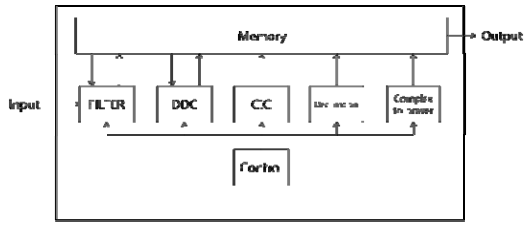
II. PROPOSED ARCHITECTURE

The method of spectral analysis can be divided into analog and digital system method. The analog method refers to a method to sweep the frequency based on the Super-Heterodyne technique. This method consumes the power of the computer. The cost of the analog parameter is high. The method of digital is a method of analyzing the spectrum using a mathematical transformation of digital discrete signal by A/D converter to time-domain with a Fourier Transform. With the FPGA chipsets which are lower cost than both systems using DSP chipsets and embedded systems, the existing spectrum analyzer of the digital systems are used a number of filters. As a result, it is used the FPGA of the big size.

In this paper, the proposed spectrum analyzer is implemented to share one filter with many filter with multistage filters and to use the DDC of the two stages in order to reduce sampling frequency.

The proposed digital spectrum analyzer measures the power of analyzed signal from 5MHz to 10MHz band of the signal to 1MHz and 100KHz resolution in the sampling frequency of 40MHz. Figure 1 shows a proposed total block diagram of digital spectrum analyzer.

Figure 1. Block diagram of the proposed digital spectrum analyzer.



The FILTER is module which pass any frequency band easily and the others with difficulty. It is implemented to allow function of low-pass, band-pass, and high-pass filter with the value of coefficient of the filter. The DDC moves to a lower frequency. It consists of sine/cosine look-up table for converting frequency and multiplier. In order to reduce the size of hardware, sine/cosine look-up table is implemented to look-up table which is 1/8 reduction with symmetry. The CIC (Cascaded Integrator Comb) filter has a regular structure, and does not require a multiplier and less memory. Since it is possible to switch the processing speed, it is suitable for the Decimation/Interpolation filter that requires low power consumption and high speed. The CIC filter consists of integrator part, decimation part, and comb filter part. Integrator part is formed by N integrators that are connected in series. Integrator part of the CIC filter has transfer function such as following:

$$H_I(z) = \left(\frac{1}{DM}\frac{1}{1-z^{-1}}\right)^N \quad (1)$$

M is the interpolation/decimation ratio, and D is the differential delay of the comb filter. By an up/down sampler between the integrator part and the comb filter part, comb filter part has transfer function such as following:

$$H_C(z) = (1 - z^{-DM})^N \quad (2)$$

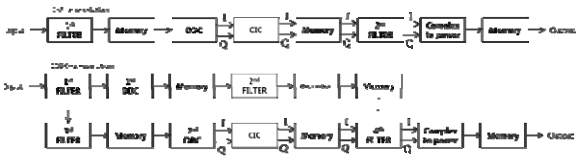
Thus, the whole of transfer function can be written as:

$$H(z) = \left(\frac{1}{DM}\frac{1-z^{-DM}}{1-z^{-1}}\right)^N \quad (3)$$

1/DM is the factor of scaling and to compensate the gain at DC. The DDC is module to lower frequency and consists of sine/cosine look-up table for converting frequency and multiplier. The sine/cosine look-up table is implemented to lower 8:1 than the original look-up table with symmetry between the signal of sine and cosine. It is reduced the size of hardware. As the CIC filter generate null at integer multiple of 1/M, it is possible to remove the factor of aliasing or image. The decimation lowers sampling frequency for reducing filter's complexity. Respectively, it is used to lower the 10:1 or 20:1 in the case of 1MHz resolution or 100KHz resolution. The complex to power module calculate the signal power by squaring the filtered signal. The control module is informed the start and end of spectrum analysis and controls process according to resolution.

The proposed digital spectrum analyzer is described data process according to resolution. Figure 2 shows data flow in the 1MHz resolution and 100KHz resolution.

Figure 2. Data flow of 1MHz resolution (Up) and 100KHz resolution (Down).



In the case of the 1MHz resolution, the 1st FILTER filters the input signal, with low-pass filter, at a time at 1MHz band. After the 1st FILTER, it is used to store data in memory due to data processing in series. The DDC makes the signal of real and image by multiplying the filtered data and the value of sine and cosine, respectively. The CIC filter removes the signal of image which is made by DDC and lowers sampling frequency in order to reduce the complexity of filter. Since the FILTER is recursive structure in hardware, the FILTER is implemented by the shared architecture for reducing the size of hardware. The 2nd FILTER filters exactly the signal to 1MHz for enhancing the accuracy of signal. By reducing sampling frequency, the complexity of filter is reduced. The complex to power module performs an I^2+Q^2 function on the complex data and store the calculated power data in memory. In the same way, it has to repeat the process of 5 times in order to analyze the power of signal, 1MHz at a time, from 5MHz to 10MHz band. The 100KHz resolution must be used 10 times better than the filter of 1MHz resolution. The filter which has the better resolution increases the complexity of the filter because of a number of the coefficient of the filter. In order to reduce the complexity of the filter, it is solved the complexity of the filter by using the lower sampling frequency than 1MHz resolution sampling frequency. In the case of 100KHz resolution, the 1st FILTER filters the input signal, with band-pass filter, 1MHz band at a time. After 1st FILTER, it doesn't store the filtered data in memory. Because 1st DDC utilize to move the frequency of the filtered signal with only the cosine look-up table in the case of 100KHz resolution. For using to share the filter, the down converted data is stored in memory. The 2nd FILTER removes the signal of image which is made by the DDC. Decimation lowers the sampling frequency in order to reduce the complexity of the filter. With the 3rd

FILTER, the processed data is stored in memory. It is the same way as 1MHz resolution data flow from the 3rd FILTER. 100KHz resolution After the same method, it has to repeat the process of 50 times in order to analyze the power of signal, 100KHz at a time, from 5MHz to 10MHz band.

In the case of 1MHz resolution, it is used to reduce the sampling frequency once because the resolution of filter is not high performance. Since the 100KHz resolution's filter need high resolution, it is used to reduce the sampling frequency two times. Also, as multiple filter banks are realized into a single FIR filter structure, the size of hardware can be reduced.

III. IMPLENETATION RESULTS

The proposed digital spectrum analyzer is implemented into FPGA chipsets. The FPGA is Kintex-7 XC7K70T in Xilinx's company. As shown in Figure 3, it is controlled hardware with UART architecture and performs to analyze a specific frequency band which is generated by signal generator. The signal is sent to the proposed digital spectrum FPGA board by a signal generator. The test signals are the specific bandwidth from 5MHz to 10MHz. The signal is analyzed in the proposed digital spectrum analyzer, and the analyzed power data of the target frequency band is shown by MFC (Microsoft Foundation Class Library) in PC (Personal Computer). It is possible to monitor the power data with graph.

Figure 3. Test environment of the proposed digital spectrum analyzer.

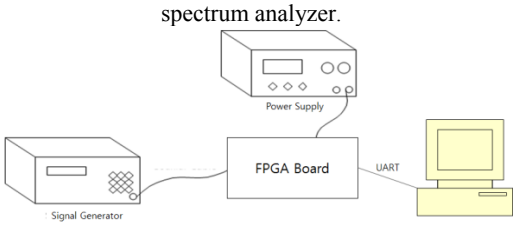


Figure 4 shows the PC-based software on the test. It is implemented with Visual MFC and can verify the function of the proposed digital spectrum analyzer. In a software program, it selects resolution and can start to analyze signal with the start button. The function of clock phase is to change clock phase by 0°, 90°, and 180°.

Figure 4. A software program for verification of the proposed digital spectrum analyzer

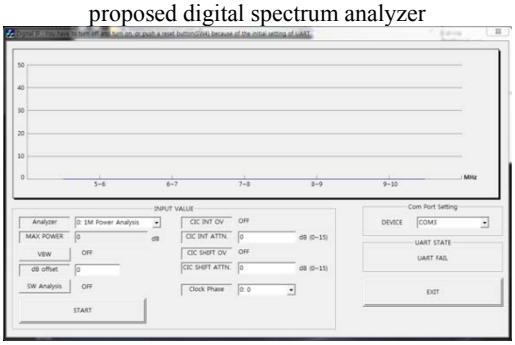


Figure 5 shows the evaluation results by the proposed digital spectrum analyzer with 1MHz resolution, graphically. It is the RF signal of 6.5MHz band which is generated by signal generator. The power of the analyzed RF signal of 6.5MHz band is the highest-power between 5MHz and 10MHz band. The value of max power is about -31dB.

Figure 5. 1MHz spectrum analysis result.

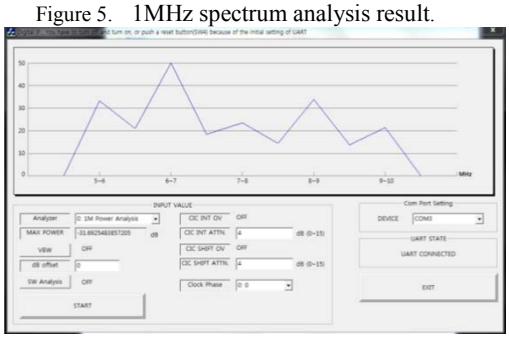
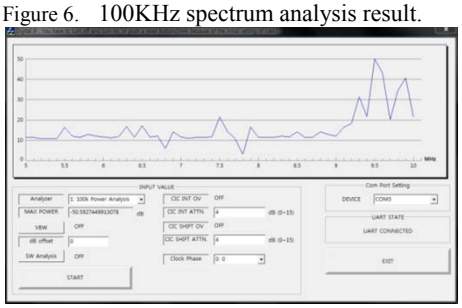


Figure 6 shows a analyzed result by the proposed digital spectrum analyzer with 100KHz resolution. It is the RF signal of 9.5MHz band which is generated by signal generator. The band which corresponds the maximum power is 9.5MHz band and the value is roughly -50dB.

Figure 6. 100KHz spectrum analysis result.



IV. CONCLUSIONS

In a communication system having a limited bandwidth, it was very important to analyze the spectrum. The methods of spectral analysis were sweep methods which were analog methods, Fourier Transform methods with both DSP chipsets and embedded systems, and methods which were implemented with FPGA chipsets. Analog methods are high power consumption. Fourier Transform methods are needed high speed FPGAs and increased the power consumption. Since method which was implemented with FPGA chipsets use a number of filters, the cost of FPGA was expensive.

In this proposed paper was the low-cost digital spectrum analyzer. In order to decrease the complexity of the filter, it reduced sampling frequency with the DDC. Also, multiple filter banks were realized into a single filter structure in order to reduce the size of the hardware. The proposed digital spectrum analyzer was useful for monitoring systems of the communication system with a limited bandwidth in which low-cost digital spectrum analyzers were suitable for low-cost implementation of system performance.

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