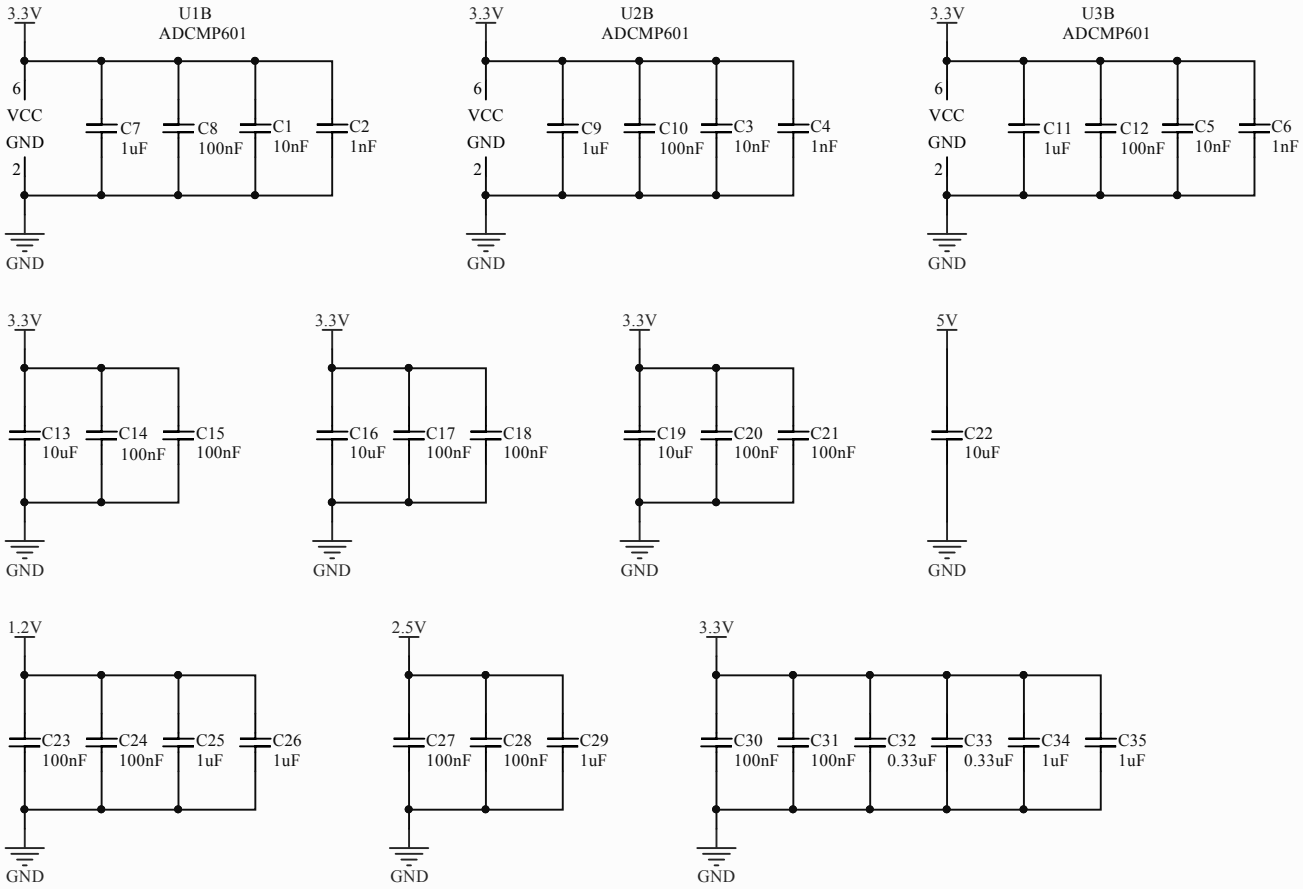
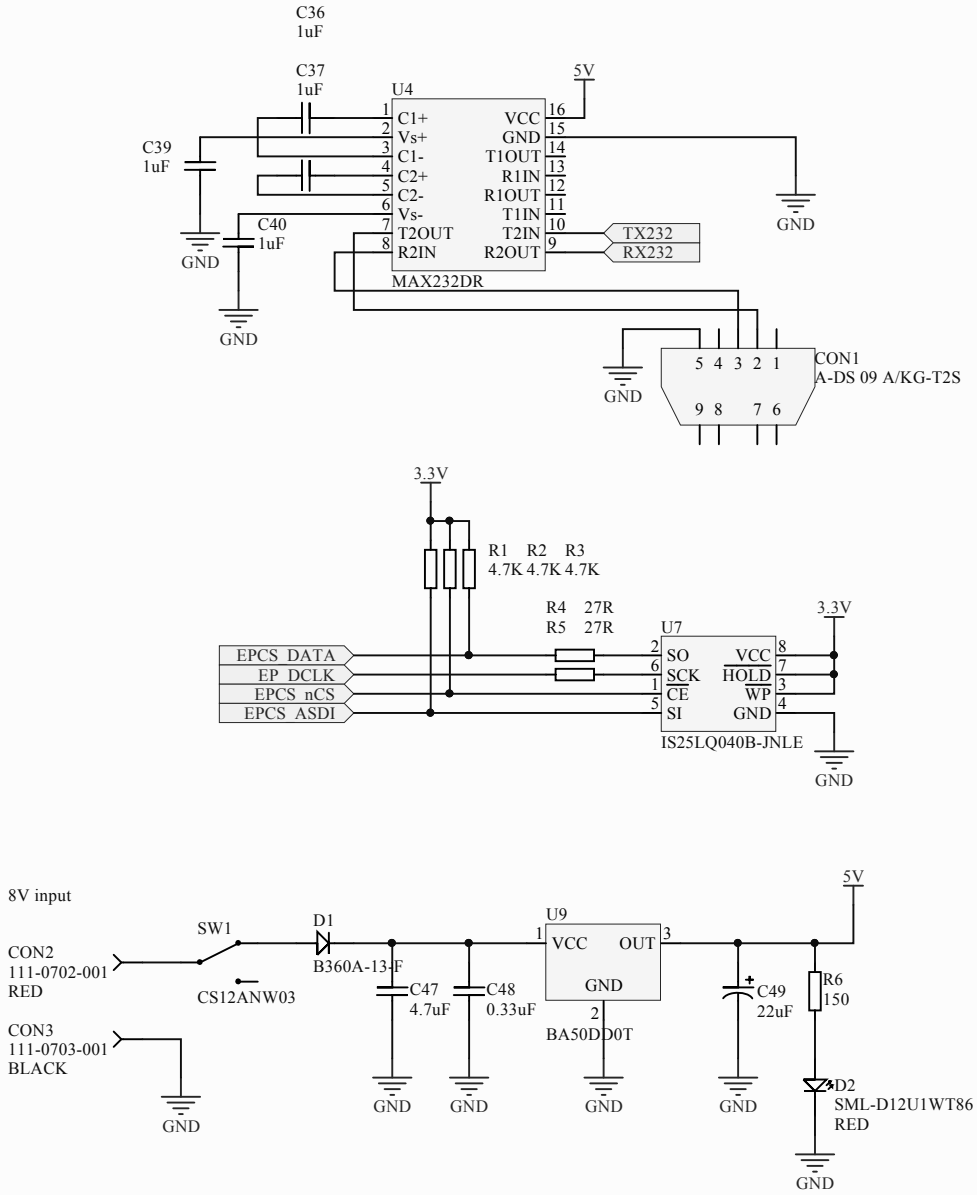
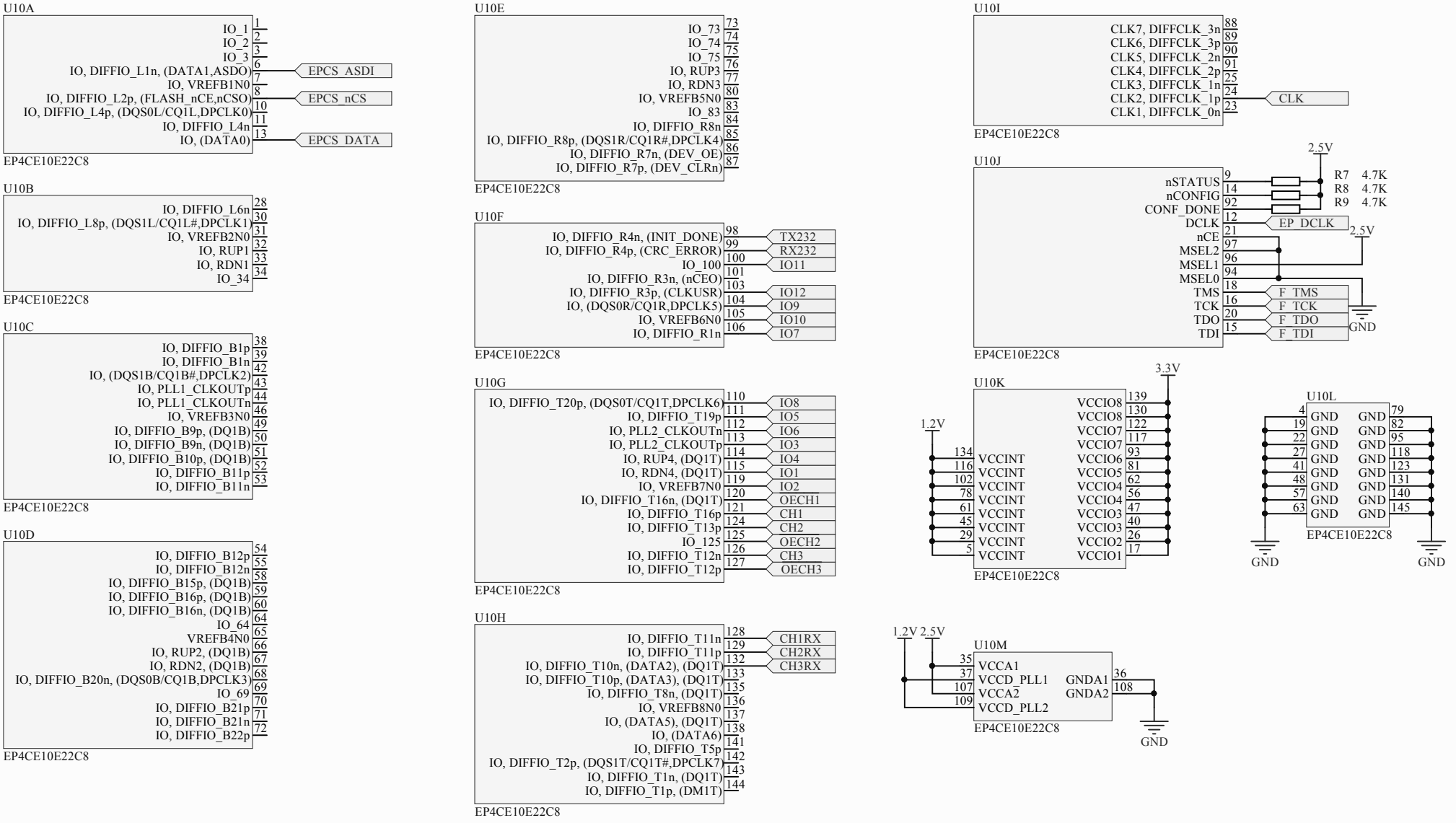


Title: Decoupling Capacitors		
Size: A4	Number:	Revision: v1.0
Date: 09/11/2019		Sheet 1 of 6
File: E:\Altium\..\Decoupling Capacitors.SchDoc		Drawn By:



Title	FPGA Peripherals	
Size: A4	Number:	Revision: v1.0
Date: 09/11/2019		Sheet 2 of 6
File: E:\Altium\..\FlashandClock.SchDoc		Drawn By:


U10A
IO_1 1
IO_2 2
IO_3 3
IO, DIFFIO_L1n, (DATA1,ASDO) 6
IO, VREFB1N0 7
IO, DIFFIO_L2p, (FLASH_nCE,nCSO) 8
IO, DIFFIO_L4p, (DQS0L/CQ1L,DPCLK0) 10
IO, DIFFIO_L4n 11
IO, (DATA0) 13
EPCS_ASDI
EPCS_nCS
EPCS_DATA
EP4CE10E22C8
U10B
IO, DIFFIO_L6n 28
IO, DIFFIO_L8p, (DQS1L/CQ1L#,DPCLK1) 30
IO, VREFB2N0 31
IO, RUP1 32
IO, RDN1 33
IO_34 34
EP4CE10E22C8
U10C
IO, DIFFIO_B1p 38
IO, DIFFIO_B1n 39
IO, (DQS1B/CQ1B#,DPCLK2) 42
IO, PLL1_CLKOUTp 43
IO, PLL1_CLKOUTn 44
IO, VREFB3N0 46
IO, DIFFIO_B9p, (DQ1B) 49
IO, DIFFIO_B9n, (DQ1B) 50
IO, DIFFIO_B10p, (DQ1B) 51
IO, DIFFIO_B11p 52
IO, DIFFIO_B11n 53
EP4CE10E22C8
U10D
IO, DIFFIO_B12p 54
IO, DIFFIO_B12n 55
IO, DIFFIO_B15p, (DQ1B) 58
IO, DIFFIO_B16p, (DQ1B) 59
IO, DIFFIO_B16n, (DQ1B) 60
IO_64 64
VREFB4N0 65
IO, RUP2, (DQ1B) 66
IO, RDN2, (DQ1B) 67
IO, DIFFIO_B20n, (DQS0B/CQ1B,DPCLK3) 68
IO_69 69
IO, DIFFIO_B21p 70
IO, DIFFIO_B21n 71
IO, DIFFIO_B22p 72
EP4CE10E22C8
U10E
IO_73 73
IO_74 74
IO_75 75
IO, RUP3 76
IO, RDN3 77
IO, VREFB5N0 80
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IO, DIFFIO_R8p, (DQS1R/CQ1R#,DPCLK4) 85
IO, DIFFIO_R7n, (DEV_OE) 86
IO, DIFFIO_R7p, (DEV_CLRn) 87
EP4CE10E22C8
U10F
IO, DIFFIO_R4n, (INIT_DONE) 98
IO, DIFFIO_R4p, (CRC_ERROR) 99
IO_100 100
IO, DIFFIO_R3n, (nCEO) 101
IO, DIFFIO_R3p, (CLKUSR) 103
IO, (DQS0R/CQ1R,DPCLK5) 104
IO, VREFB6N0 105
IO, DIFFIO_R1n 106
TX232
RX232
IO11
IO12
IO9
IO10
IO7
EP4CE10E22C8
U10G
IO, DIFFIO_T20p, (DQS0T/CQ1T,DPCLK6) 110
IO, DIFFIO_T19p 111
IO, PLL2_CLKOUTn 112
IO, PLL2_CLKOUTp 113
IO, RUP4, (DQ1T) 114
IO, RDN4, (DQ1T) 115
IO, VREFB7N0 119
IO, DIFFIO_T16n, (DQ1T) 120
IO, DIFFIO_T16p 121
IO, DIFFIO_T13p 124
IO_125 125
IO, DIFFIO_T12n 126
IO, DIFFIO_T12p 127
IO8
IO5
IO6
IO3
IO4
IO1
IO2
OECH1
CH1
CH2
OECH2
CH3
OECH3
EP4CE10E22C8
U10H
IO, DIFFIO_T11n 128
IO, DIFFIO_T11p 129
IO, DIFFIO_T10n, (DATA2), (DQ1T) 132
IO, DIFFIO_T10p, (DATA3), (DQ1T) 133
IO, DIFFIO_T8n, (DQ1T) 135
IO, VREFB8N0 136
IO, (DATA5), (DQ1T) 137
IO, (DATA6) 138
IO, DIFFIO_T5p 141
IO, DIFFIO_T2p, (DQS1T/CQ1T#,DPCLK7) 142
IO, DIFFIO_T1n, (DQ1T) 143
IO, DIFFIO_T1p, (DM1T) 144
CH1RX
CH2RX
CH3RX
EP4CE10E22C8
U10I
CLK7, DIFFCLK_3n 88
CLK6, DIFFCLK_3p 89
CLK5, DIFFCLK_2n 90
CLK4, DIFFCLK_2p 91
CLK3, DIFFCLK_1n 25
CLK2, DIFFCLK_1p 24
CLK1, DIFFCLK_0n 23
CLK
EP4CE10E22C8
U10J
2.5V
nSTATUS 9
nCONFIG 14
CONF_DONE 92
DCLK 12
nCE 21
MSEL2 97
MSEL1 96
MSEL0 94
TMS 18
TCK 16
TDO 20
TDI 15
R7 4.7K
R8 4.7K
R9 4.7K
EP_DCLK
F_TMS
F_TCK
F_TDO
F_TDI
GND
EP4CE10E22C8
U10K
3.3V
1.2V
VCCINT 134
VCCINT 116
VCCINT 102
VCCINT 78
VCCINT 61
VCCINT 45
VCCINT 29
VCCINT 5
VCCIO8 139
VCCIO8 130
VCCIO7 122
VCCIO7 117
VCCIO6 93
VCCIO5 81
VCCIO4 62
VCCIO4 56
VCCIO3 47
VCCIO3 40
VCCIO2 26
VCCIO1 17
EP4CE10E22C8
U10L
GND 4
GND 19
GND 22
GND 27
GND 41
GND 48
GND 57
GND 63
GND 79
GND 82
GND 95
GND 118
GND 123
GND 131
GND 140
GND 145
EP4CE10E22C8
GND
GND
U10M
1.2V
2.5V
VCCA1 35
VCCD_PLL1 37
VCCA2 107
VCCD_PLL2 109
GNDA1 36
GNDA2 108
EP4CE10E22C8
GND
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FPGA
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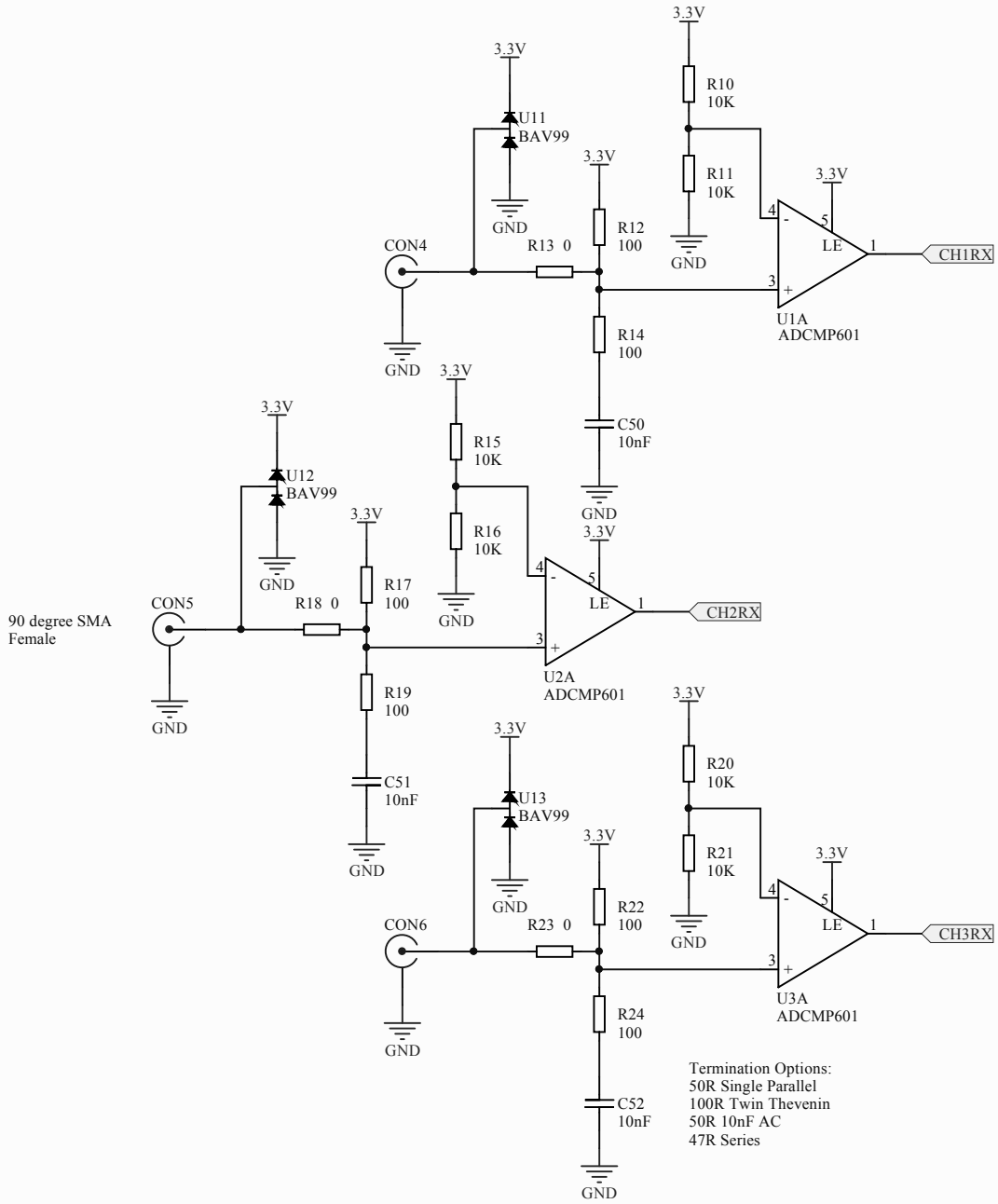
File: E:\Altium\..\FPGA.SchDoc
Drawn By:



Title: Front End Rx		
Size: A4	Number:	Revision: v1.0
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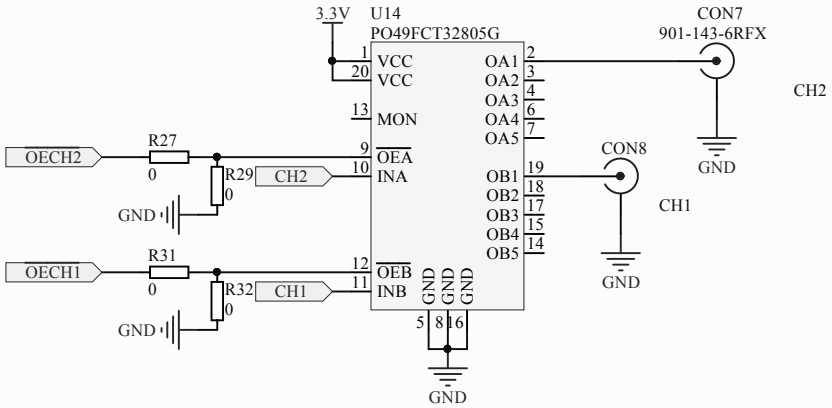
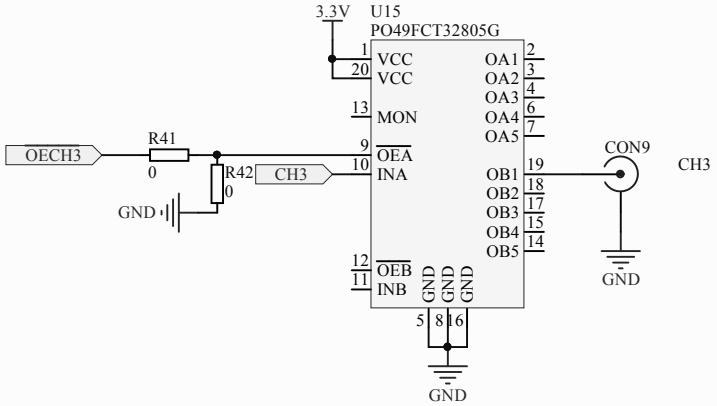
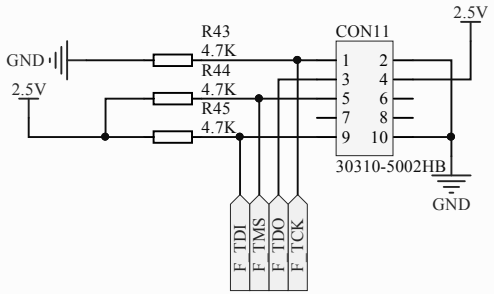
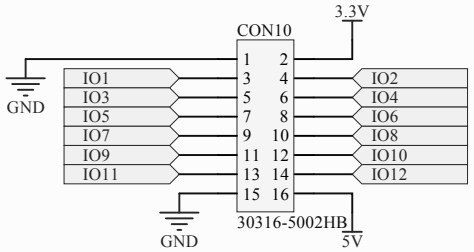
File: E:\Altium\..\Front End Rx.SchDoc		Drawn By:





Title: Front End Tx		
Size: A4	Number:	Revision: v1.0
Date: 09/11/2019		Sheet 5 of 6
File: E:\Altium\..\Front End Tx.SchDoc		Drawn By:





Title: Low Speed Interfaces		
Size: A4	Number:	Revision: v1.0
Date: 09/11/2019		Sheet 6 of 6
File: E:\Altium\..\Low Speed Interfaces.SchDoc		Drawn By: