FAILURE ANALYSIS REPORT FAR-JM0521-CIE

DATE:	APRIL-20-2021
MADE BY:	Jose Mejia
PROJECT:	Ciena Centauro
SERIAL ASSEMBLY 900:	M9553213
ASSY P/N 400:	LFNT134-5550-901RL005
SUSPECT COMPONENT:	FPGA
ASSY QTY:	1
FAIL TEST STATION:	CHAMBER
FAILURE DESCRIPCION:	pfpga_serdes_prbs_test

N/P SCI:	LFNL080-1763-001
SUPPLIER:	INTEL CORP
GENERIC:	5SGXMBBR2H40I2LNAC
SERIAL NUMBER:	CCAAR2037A
DATE CODE:	2037
COMPONENT DESCRIPTION:	FPGA, STRATIX V, 14.1 GBPS TX, MAINSTRM, 66 TX, HFLBGA, 1517 PINS, -40/100 C, SPD 2, LOW POWER SCRN

INTRODUCTION

The unit failed the ESS test, in hot cicles. The failure shows errors in FPGA 2.

```
SCRIPT2_46C_01:41:20> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
[31mPFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 7
```

ANALISIS

Lane 12 signals are checked, there is no difference in impedance measurement or diode mode.

Signal	Bad unit diode mode	Good unit diode mode
P1_INGR_D12_N	0.324V	0.324V
P1_INGR_D12_P	0.324V	0.324V
P1_EGR_D12_N	0.302V	0.303V
P1_EGR_D12_P	0.302V	0.302V

The flex cable is checked, there is no pin damage and there is continuity between the main board and WL3.

It proceeds to stress components involved with temperature, it is observed that by increasing the temperature in FPGA 2 the fault is reproduced.

SCRIPT1_29C_12:28:27> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
DIAGERR,UNKNOWN(31),pfpga_serdes_prbs_test: ,PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 2
PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 2
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!
pfpga_serdes_prbs_test : Failed.
Script Summary(commands.txt): 2 items run, 1 tests failed.
###################### Failed Commands ######################
>> pfpga_serdes_prbs_test * 0 * (+29C 12:28:27)
###

End script cycle 3: Failed.

##

SCRIPT1_29C_12:28:42> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
DIAGERR,UNKNOWN(31),pfpga_serdes_prbs_test: ,PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 8

PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 8
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!
pfpga_serdes_prbs_test : Failed.

Script Summary(commands.txt): 2 items run, 1 tests failed.
###################### Failed Commands ######################
>> pfpga_serdes_prbs_test * 0 * (+29C 12:28:42)
##

End script cycle 4: Failed.
##

SCRIPT1_28C_12:28:57> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
DIAGERR,UNKNOWN(31),pfpga_serdes_prbs_test: ,PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 2

PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test fails! Reason - Read Error Count 2
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!

pfpga_serdes_prbs_test : Failed.

When applying cold spray to FPGA 2 the errors are corrected and the unit passes.

SCRIPT1_29C_12:29:12> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!
pfpga_serdes_prbs_test : Passed.

Script Summary(commands.txt): 2 items run, 0 tests failed.
End script cycle 6: Passed.
##

SCRIPT1_29C_12:29:27> pfpga_serdes_prbs_test * 0 *

PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!
pfpga_serdes_prbs_test : Passed.

Script Summary(commands.txt): 2 items run, 0 tests failed.
End script cycle 7: Passed.

This validation is repeated 5 times with the same result

CONCLUSION

Based on the above, it is determined to replace FPGA U27 due to functional failure, U27 will be sent to the supplier.