FAILURE ANALYSIS REPORT

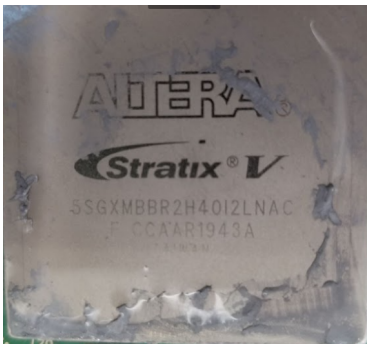
FAR-JR1321-CIENA

GENERAL DATA

DATE:	04-15-2021
MADE BY:	Jesus Rodriguez G
PROJECT:	Ciena Centauro
SERIAL ASSEMBLY 900:	**M9553213**
ASSY P/N 400:	**LFNT134-5550-901RL005**
SUSPECT COMPONENT:	U24
ASSY QTY:	2
FAIL TEST STATION:	ESS
FAILURE DESCRIPCION:	pfpga_serdes_prbs_test

N/P SCI:	LFNL080-1763-001
SUPPLIER:	INTEL CORP
GENERIC:	**5SGXMBBR2H40I2LNAC**
SERIAL NUMBER:	FCCAAR1943A-31
DATE CODE:	1943

COMPONENT DESCRIPTION: FPGA, STRATIX V, 14.1 GBPS TX, MAINSTRM, 66 TX, HFLBGA, 1517 PINS, -40/100 C, SPD 2, LOW POWER SCRN



INTRODUCTION

The unit has a fault in the ESS station thus showing the following failure mode.

```
    Fields)
1.  Comments
2.  Approved      MCS WS: 5.3.2.26
3.  ATEVersion    010
4.  TPVersion     001
5.  SWVersion     4.0.0.0_cl760394 (Updated on 2017-03-02 13:00:12 by cnbuilder on gaxvdiagbld01)
6.  ESS_Event     00:33:30 (2/12/2021 5:53 AM) chassis_functest.txt: 1 items run - 1 tests failed.#ESS_start.txt: 66 items run - 0 te
7.  Duration      04:41:06
8.  TimeToFailure 00:33:30 (2/12/2021 5:53 AM)
    FirstFailure
                  ------------------------------------------------------------------------
                  SN: M9553213
                  SLOT: 7
                  ESS: 39.85
                  Duration: 00:33:30 (2/12/2021 5:53 AM)
                  MSG: ,,,chassis_functest.txt: 1 items run, 1 tests failed.
                  □[0m#################### Failed Commands ####################
                  >> exec_script /diags/scripts/commonfunctest.txt FE_DELAY=10 MP_DELAY=5 BE_DELAY=10 (+44C 05:54:16)
                  ##########################################################


                  ################ Failed Command Summary ################
                  >> exec_script /diags/scripts/commonfunctest.txt FE_DELAY=10 MP_DELAY=5 BE_DELAY=10 (1 failure)
                  1: +44C 05:54:16
                  >> pfpga_serdes_prbs_test * 0 * (1 failure)
                  1: +44C 06:01:53
                  >> port_xco4_prbs_test * (1 failure)
                  1: +44C 06:03:31
                  ##########################################################


                  OSLM2 CLIDE 4.0.0.0_cl760394 (Updated on 2017-03-02 13:00:12 by cnbuilder on gaxvdiagbld01)
                  Start time: Fri 02/12/21 05:54:16
                  End time: Fri 02/12/21 06:04:05
                  Elapsed time: 589.415627 seconds
                  □[31mexec_script : FAILED
9.                □[0m
                  □[2K
                  OSLM2_7> ,,,ESS_start.txt: 66 items run, 0 tests failed.

                  OSLM2 CLIDE 4.0.0.0_cl760394 (Updated on 2017-03-02 13:00:12 by cnbuilder on gaxvdiagbld01)
                  Start time: Fri 02/12/21 06:04:34
                  End time: Fri 02/12/21 06:07:35
                  Elapsed time: 180.789666 seconds
                  exec_script : PASSED
```

ANALYSIS

The unit has failed in link 1, when performing the subtest of pfpga_serdes_prbs_test

```
PFPGA 2 (DIAG):

PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!

ESC[31mPFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test fails! Reason - Read Error Count 2

ESC[0mPFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test success!
```

This test is communication between the OCLD and the FPGAs, measurements are made of the links to rule out a possible high impedance or, failing that, an incorrect repair, as can be seen in table 1, the component does not present high impedance or bad repair.

	Bad unit	Good unit
Signal	Diode Mode	
PFPGA_CFG_DATA<0>	0.400V	0.402V
PFPGA_CFG_DATA<1>	0.397	0.400V
PFPGA_CFG_DATA<2>	0.397V	0.400V
PFPGA_CFG_DATA<3>	0.400V	0.402V
PFPGA_CFG_DATA<4>	0.400V	0.402V
PFPGA_CFG_DATA<5>	0.398V	0.400V
PFPGA_CFG_DATA<6>	0.400V	0.403V
PFPGA_CFG_DATA<7>	0.399V	0.402V
PFPGA_CFG_DATA<8>	0.397V	0.399V
PFPGA_CFG_DATA<9>	0.397V	0.400V
PFPGA_CFG_DATA<10>	0.400V	0.403V
PFPGA_CFG_DATA<11>	0.397V	0.400V
PFPGA_CFG_DATA<12>	0.398V	0.401V
PFPGA_CFG_DATA<13>	0.397V	0.400V
PFPGA_CFG_DATA<14>	0.400V	0.403V
PFPGA_CFG_DATA<15>	0.398V	0.400V

Table 1.-measurements

The unit has not a difference in impedances compared to a good unit, it is decided to enter the unit into LTMA stressing the component, thus being able to replicate the failure mode.This can be seen in image 1 and in image 2 it can be seen that when applying silijet in component U27, the problem is solved, it is decided to have the component changed as a functional failure.

```
PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
DIAGERR,UNKNOWN(31),pfpga_serdes_prbs_test: ,PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test fails! Reason - Read Error Count 2

PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test fails! Reason - Read Error Count 2
PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
```

Image 1.- Component exposed to high temperature

```
PFPGA 2 (DIAG):
PFPGA 2 (DIAG) LANE 0: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 1: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 2: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 3: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 4: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 5: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 6: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 7: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 8: TFI 6 PRBS test success!
PFPGA 2 (DIAG) LANE 9: TFI 6 PRBS test success!
pfpga_serdes_prbs_test : PASSED
```

Image 2.- component stressed with cold once it was exposed to high temperature

CONCLUSION

By only presenting the failure when the unit is stressed with hot. we can deduce that it is a functional failure on the part of the component U27. BGAs will be made available to SUPPLIER.