1 QPS 17.1

Failures occur on Read DMA (but not on write DMA). There are two issues:

1.1 Suboptimal Avalon Master Behavior.

The PCIe/DMA core has an Avalon-MM master interface, which connects to local memory; the local memory is the destination memory for Read DMA operations.

Data is transferred to the local memory via a series of burst write transactions. The bus with is 16 bytes (128 bits), and the burst length is 8 words.

The master behavior is odd. The write command is asserted (with address, data, burst length, byte enables) until wait_req is negated. Then write is negated for two clocks, then asserted again, with new values for the address and burst length (address is incremented by 0x10, burst length is decremented by 1). This continues until all eight words of the burst have been transferred.

The master interface lacks a burst_begin signal; as a result, this looks like a sequence of 8 bursts of length 8, 7, 6, 5, 4, 3, 2, and 1 words, but in reality only 8 words are transferred

1.2 Address Corruption

After the first burst write transaction of the Read DMA transfer, the remaining burst write transactions have a corrupted address value:

The corrupted address is an output from the Avalon-MM master on the PCIe/DMA core; I traced the source all the way back to the read_dma_mover. It appears that **cpl_tag**[7:0] (which is selected from input **RxFifoDataq_i**) takes on an illegal value, which corrupts the output of the 2-dimensional array **tag_address_reg**. The output of tag_address_reg is the input to an accumulator, which increments the address according to the data width; The address is thus perpetually corrupted.

2 QPS 19.1

We have encountered problems with the simulation model of the PCIe/DMA core with older versions of Quartus in the past (specifically, QPP 17.1). So I have built a new design/sim database for use with QPS 19.1.

The problem here is more fundamental. I generated a testbench with root port model, but the simulator fails to load the design because two modules are missing:

```
# ** Error: (vsim-3033) Instantiation of 'altpcietb_bfm_driver_avmm' failed. The design
unit was not found.
#    Time: 0 ns  Iteration: 0  Region:
/pcie_idma_tb/RP/g_bfm_top_rp/altpcietb_bfm_top_rp/genblk1 File:
../quartus/pcie_dma_ep/testbench/pcie_dma_ep_tb/simulation/submodules/altpcietb_bfm_top_r
p.v Line: 509
```
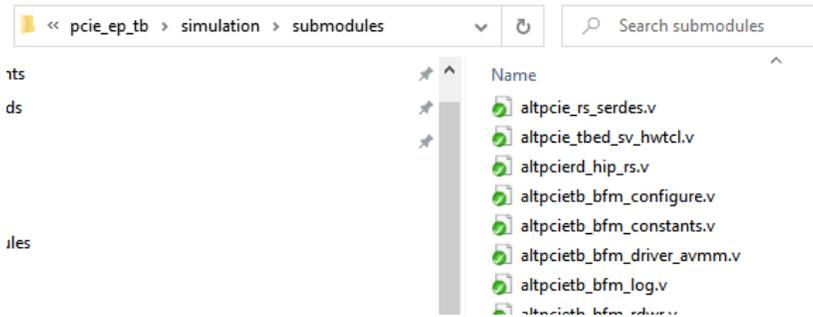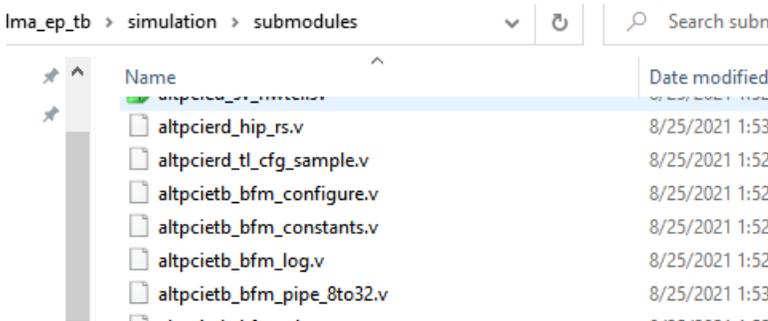
```
# ** Error: (vsim-3033) Instantiation of 'altpcietb_bfm_rp_top_x8_pipen1b' failed. The
design unit was not found.
#    Time: 0 ns  Iteration: 0  Region:
/pcie_idma_tb/RP/g_bfm_top_rp/altpcietb_bfm_top_rp/g_bfm/genblk1 File:
../quartus/pcie_dma_ep/testbench/pcie_dma_ep_tb/simulation/submodules/altpcietb_bfm_top_r
p.v Line: 871
```

altpcietb_bfm_driver_avmm is readily found in databases produced by older versions of QPS (17.1, for example):

But is not produced by QPS 19.1:

The other missing module, **altpcietb_bfm_rp_top_x8_pipen1b**, is likewise missing from the database: