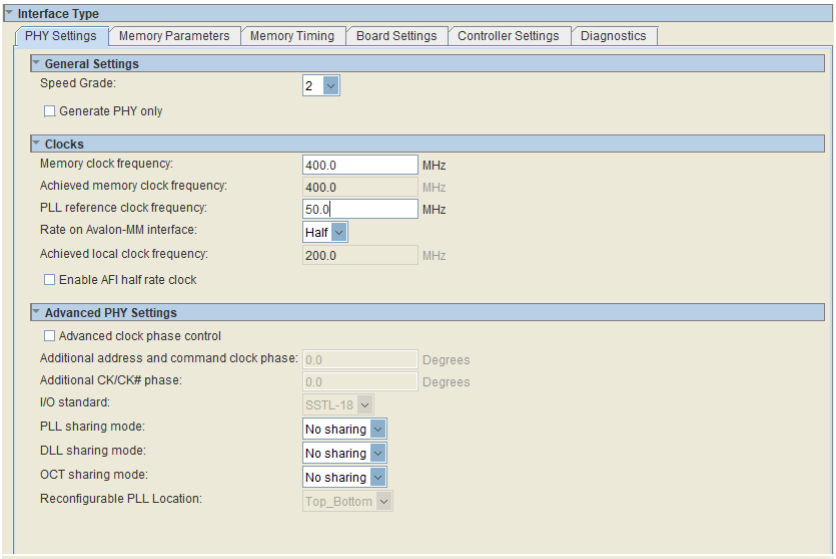
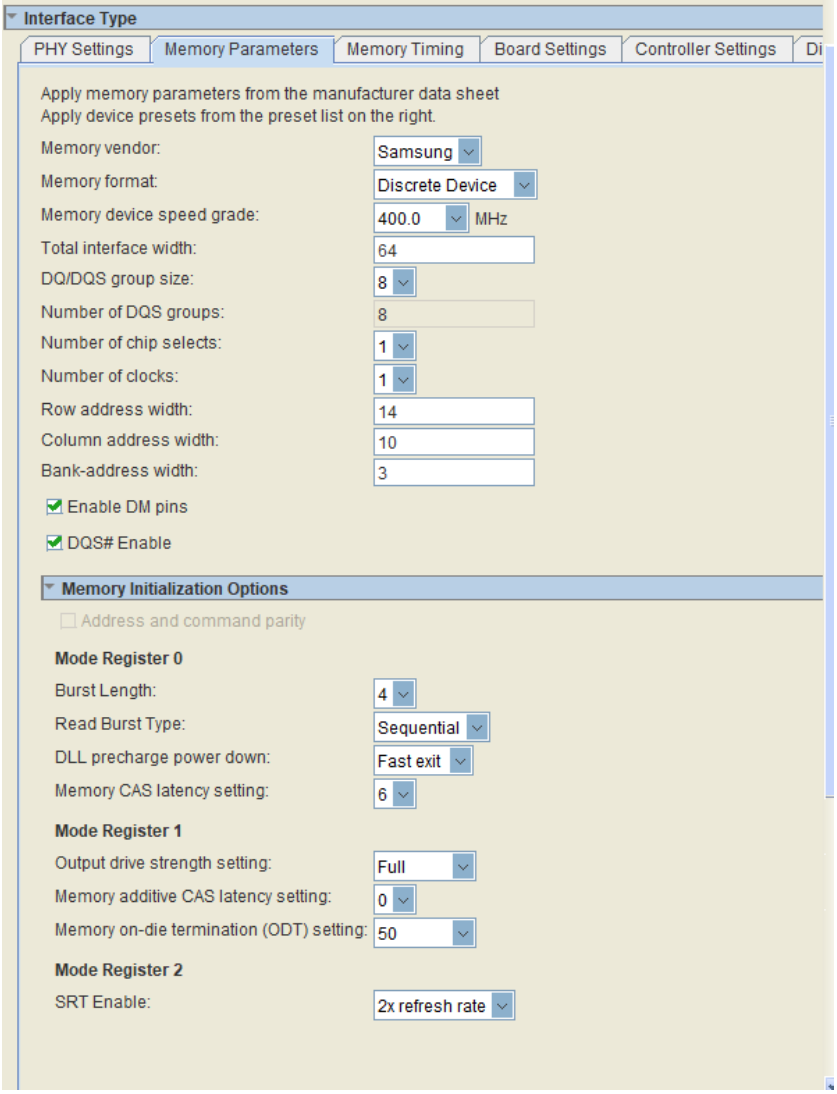
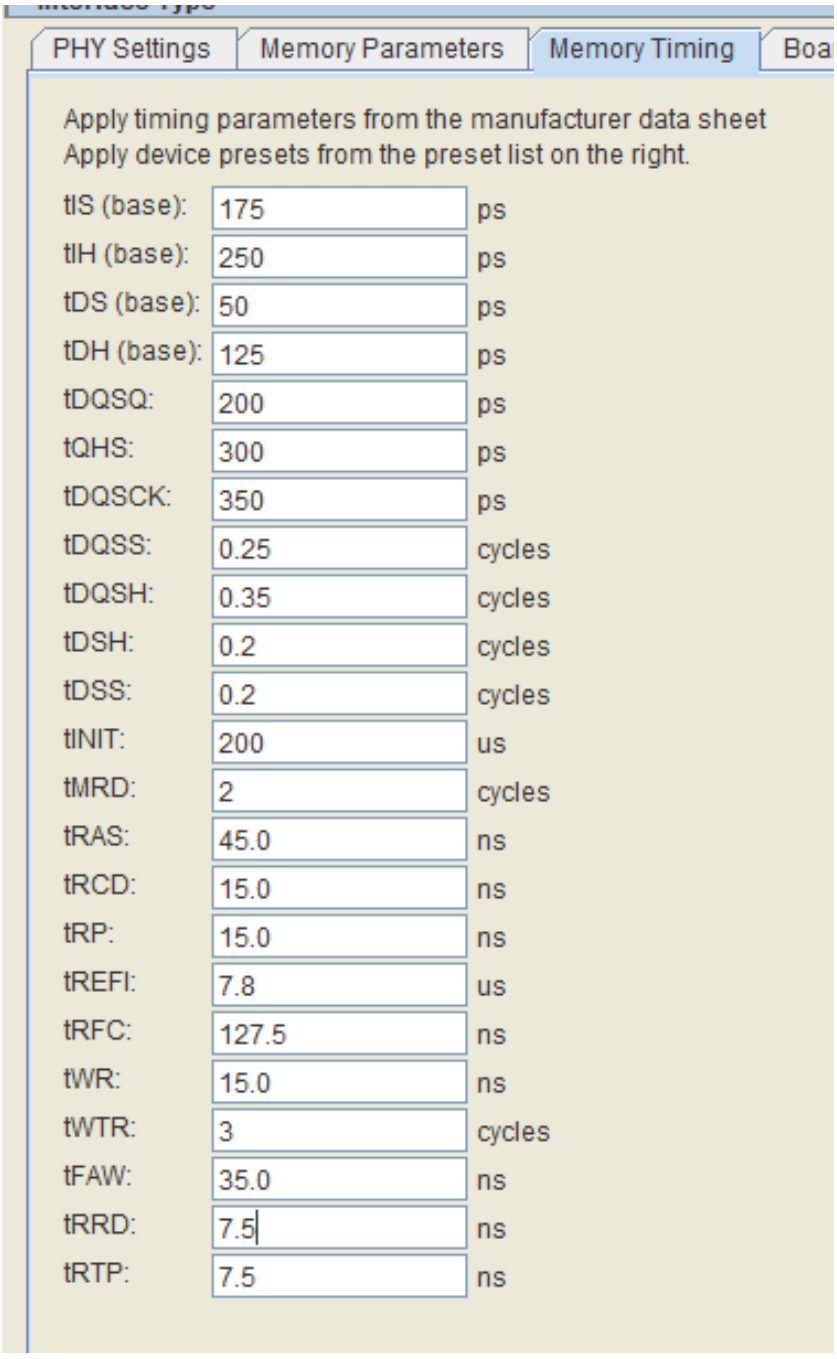
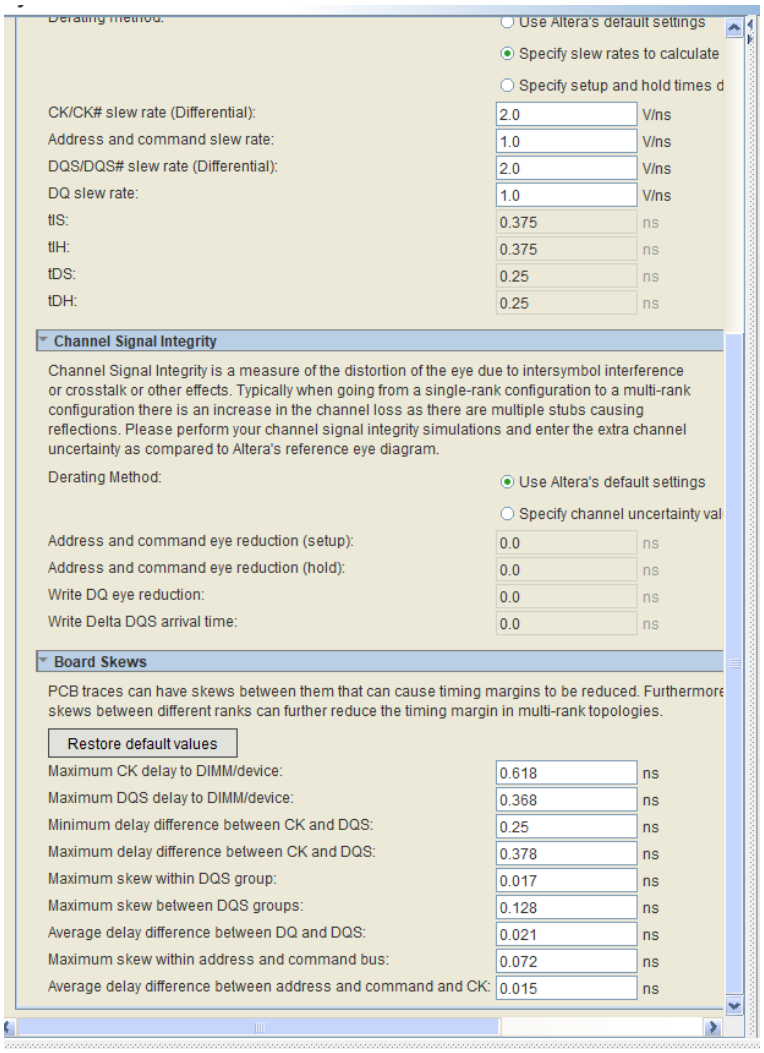
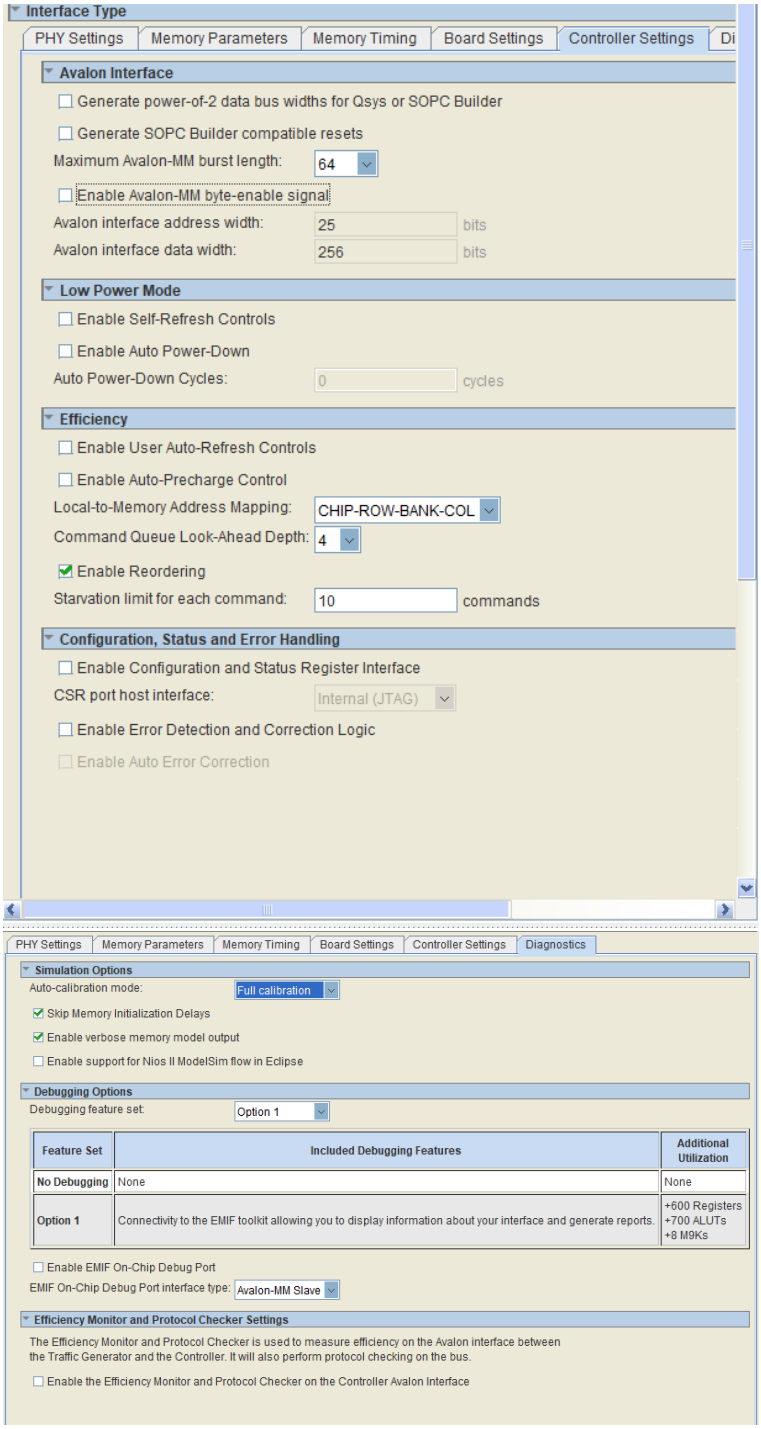

Interface Type
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Controller Settings
Diagnostics
General Settings
Speed Grade:
2
Generate PHY only
Clocks
Memory clock frequency:
400.0
MHz
Achieved memory clock frequency:
400.0
MHz
PLL reference clock frequency:
50.0
MHz
Rate on Avalon-MM interface:
Half
Achieved local clock frequency:
200.0
MHz
Enable AFI half rate clock
Advanced PHY Settings
Advanced clock phase control
Additional address and command clock phase:
0.0
Degrees
Additional CK/CK# phase:
0.0
Degrees
I/O standard:
SSTL-18
PLL sharing mode:
No sharing
DLL sharing mode:
No sharing
OCT sharing mode:
No sharing
Reconfigurable PLL Location:
Top_Bottom


Interface Type
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Controller Settings
Apply memory parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
Memory vendor:
Samsung
Memory format:
Discrete Device
Memory device speed grade:
400.0
MHz
Total interface width:
64
DQ/DQS group size:
8
Number of DQS groups:
8
Number of chip selects:
1
Number of clocks:
1
Row address width:
14
Column address width:
10
Bank-address width:
3
Enable DM pins
DQS# Enable
Memory Initialization Options
Address and command parity
Mode Register 0
Burst Length:
4
Read Burst Type:
Sequential
DLL precharge power down:
Fast exit
Memory CAS latency setting:
6
Mode Register 1
Output drive strength setting:
Full
Memory additive CAS latency setting:
0
Memory on-die termination (ODT) setting:
50
Mode Register 2
SRT Enable:
2x refresh rate


PHY Settings
Memory Parameters
Memory Timing
Boa
Apply timing parameters from the manufacturer data sheet
Apply device presets from the preset list on the right.
tIS (base): 175 ps
tIH (base): 250 ps
tDS (base): 50 ps
tDH (base): 125 ps
tDQSQ: 200 ps
tQHS: 300 ps
tDQSCK: 350 ps
tDQSS: 0.25 cycles
tDQSH: 0.35 cycles
tDSH: 0.2 cycles
tDSS: 0.2 cycles
tINIT: 200 us
tMRD: 2 cycles
tRAS: 45.0 ns
tRCD: 15.0 ns
tRP: 15.0 ns
tREFI: 7.8 us
tRFC: 127.5 ns
tWR: 15.0 ns
tWTR: 3 cycles
tFAW: 35.0 ns
tRRD: 7.5 ns
tRTP: 7.5 ns


Derating method:
Use Altera's default settings
Specify slew rates to calculate
Specify setup and hold times d
CK/CK# slew rate (Differential): 2.0 V/ns
Address and command slew rate: 1.0 V/ns
DQS/DQS# slew rate (Differential): 2.0 V/ns
DQ slew rate: 1.0 V/ns
tIS: 0.375 ns
tIH: 0.375 ns
tDS: 0.25 ns
tDH: 0.25 ns
Channel Signal Integrity
Channel Signal Integrity is a measure of the distortion of the eye due to intersymbol interference or crosstalk or other effects. Typically when going from a single-rank configuration to a multi-rank configuration there is an increase in the channel loss as there are multiple stubs causing reflections. Please perform your channel signal integrity simulations and enter the extra channel uncertainty as compared to Altera's reference eye diagram.
Derating Method:
Use Altera's default settings
Specify channel uncertainty val
Address and command eye reduction (setup): 0.0 ns
Address and command eye reduction (hold): 0.0 ns
Write DQ eye reduction: 0.0 ns
Write Delta DQS arrival time: 0.0 ns
Board Skews
PCB traces can have skews between them that can cause timing margins to be reduced. Furthermore skews between different ranks can further reduce the timing margin in multi-rank topologies.
Restore default values
Maximum CK delay to DIMM/device: 0.618 ns
Maximum DQS delay to DIMM/device: 0.368 ns
Minimum delay difference between CK and DQS: 0.25 ns
Maximum delay difference between CK and DQS: 0.378 ns
Maximum skew within DQS group: 0.017 ns
Maximum skew between DQS groups: 0.128 ns
Average delay difference between DQ and DQS: 0.021 ns
Maximum skew within address and command bus: 0.072 ns
Average delay difference between address and command and CK: 0.015 ns


Interface Type
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Controller Settings
Di
Avalon Interface
Generate power-of-2 data bus widths for Qsys or SOPC Builder
Generate SOPC Builder compatible resets
Maximum Avalon-MM burst length:
64
Enable Avalon-MM byte-enable signal
Avalon interface address width:
25
bits
Avalon interface data width:
256
bits
Low Power Mode
Enable Self-Refresh Controls
Enable Auto Power-Down
Auto Power-Down Cycles:
0
cycles
Efficiency
Enable User Auto-Refresh Controls
Enable Auto-Precharge Control
Local-to-Memory Address Mapping:
CHIP-ROW-BANK-COL
Command Queue Look-Ahead Depth:
4
Enable Reordering
Starvation limit for each command:
10
commands
Configuration, Status and Error Handling
Enable Configuration and Status Register Interface
CSR port host interface:
Internal (JTAG)
Enable Error Detection and Correction Logic
Enable Auto Error Correction
PHY Settings
Memory Parameters
Memory Timing
Board Settings
Controller Settings
Diagnostics
Simulation Options
Auto-calibration mode:
Full calibration
Skip Memory Initialization Delays
Enable verbose memory model output
Enable support for Nios II ModelSim flow in Eclipse
Debugging Options
Debugging feature set:
Option 1
Feature Set
Included Debugging Features
Additional Utilization
No Debugging
None
None
Option 1
Connectivity to the EMIF toolkit allowing you to display information about your interface and generate reports.
+600 Registers
+700 ALUTs
+8 M9Ks
Enable EMIF On-Chip Debug Port
EMIF On-Chip Debug Port interface type:
Avalon-MM Slave
Efficiency Monitor and Protocol Checker Settings
The Efficiency Monitor and Protocol Checker is used to measure efficiency on the Avalon interface between the Traffic Generator and the Controller. It will also perform protocol checking on the bus.
Enable the Efficiency Monitor and Protocol Checker on the Controller Avalon Interface