How to calculate the fractional divider value when using the Altera PLL megafunction

Introduction

This document will describe how the Quartus® II software calculates the PLL Fractional Divison parameter, when using the Altera PLL megafunction in fractional mode.

1. Setup

Screenshots are taken from Quartus II software version 12.0 SP2.

2. PLL Fractional Divison Calculation Example

Let's take the following example. Input frequency of the PLL, Fin = 50 MHz. and the output Frequency, Fout = 107.142857 MHz

If you just enter these into the Altera PLL megafunction (Fractional Mode) and compile a design containing this PLL, the Quartus II Fitter Report will show a PLL Usage Summary as shown in Figure 1 below.

PLL Usage Summary

1	top_0002:top_inst|altera_pll:altera_pll_i|altera_str...ll:stratixv_pll|altera_stratixv_pll_base:fpll_0|fpll	
1	-- PLL Type	Fractional PLL
2	-- PLL Location	FRACTIONALPLL_X0_Y46_N0
3	-- PLL Feedback clock type	Global Clock
4	-- PLL Bandwidth	Auto
5	-- Reference Clock Frequency	50.0 MHz
6	-- PLL VCO Frequency	428.571426 MHz
7	-- PLL Operation Mode	Normal
8	-- PLL Freq Min Lock	50.000000 MHz
9	-- PLL Freq Max Lock	75.833333 MHz
10	-- PLL Enable	On
11	-- PLL Fractional Division	9586980 / 16777216
12	-- M Counter	8
13	-- N Counter	1
14	-- VCO Phase Shift Step	291 ps
15	-- Post VCO Scale	2
16	-- PLL Refclk Select	
1	-- PLL Refclk Select Location	PLLREFCLKSELECT_X0_Y52_N0
2	-- PLL Reference Clock Input 0 source	clk_3
3	-- PLL Reference Clock Input 1 source	clk_3
4	-- ADJPLLIN source	N/A
5	-- CORECLKIN source	N/A
6	-- IQTXRXCLKIN source	N/A
7	-- PLLIQCLKIN source	N/A
8	-- RXIQCLKIN source	N/A
9	-- CLKIN(0) source	N/A
10	-- CLKIN(1) source	N/A
11	-- CLKIN(2) source	N/A
12	-- CLKIN(3) source	refclk~input
17	-- PLL Output Counter	
1	-- top_0002:top_inst|altera_pll:altera_pll_i|a...ixv_pll:stratixv_pll|counter[0].output_counter	
1	-- Output Clock Frequency	107.142856 MHz
2	-- Output Clock Location	PLLOUTPUTCOUNTER_X0_Y51_N1
3	-- C Counter Odd Divider Even Duty Enable	Off
4	-- Duty Cycle	50.0000
5	-- Phase Shift	0.000000 degrees
6	-- C Counter	4
7	-- C Counter PH Mux PRST	0
8	-- C Counter PRST	1
2		

Figure 1. PLL Usage Summary

Note that Quartus II reports a PLL Fractional Divison value.

This is how it is calculated:

Recall that the VCO frequency (Fvco) of the PLL is calculated as follows :

FVco = Fin * M/N, where M is composed of an integer and a fraction, in a frational PLL.

For the example above, N=1 so, M = Fvco/Fin = 428.571426/50 = 8.57142852

The integer part of M = 8, whilst the fractional part = 0.57142852 = Fa/Fb

Fa = 0.57142852 * [2^Fractional Carry Out] = 9586979.709
= 9586980
= PLL Fractional Division Value

Note that in these examples the Fractional Carry Out = 24.

3. Entering a PLL Fractional Divison Value into the megafunction

Now, if you wanted to enter this value (or another fractional value) into the Altera PLL megafunction, do the following:

- Check “Enable physical output clock parameters”
- Work out the Fractional Divison value required as shown in the calculation previously
- Enter this value (along with the M, N values) into the megafunction, as shown in Figure 2

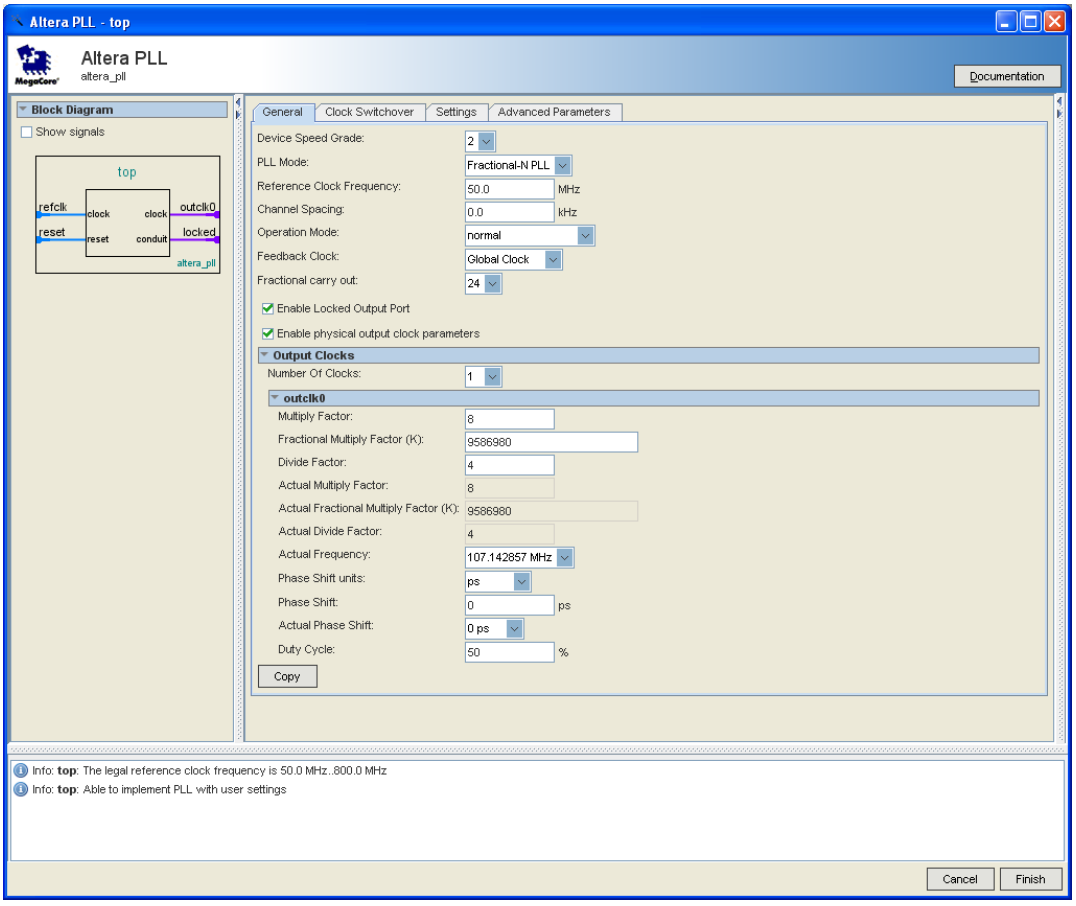

Figure 2. Altera PLL megafunction GUI

5. Conclusion

This document provides an example on how the Quartus II software calculates and reports the PLL Fractional Division Value of a fractional PLL, based on the user parameters entered into Altera PLL.

megafunction, and also how the user can enter their own value, using the “Enable Physical Output Parameters” option in the megafunction GUI

6. Revision History

Revision	Changes Made	Date
V1.0	Initial release.	August 2012