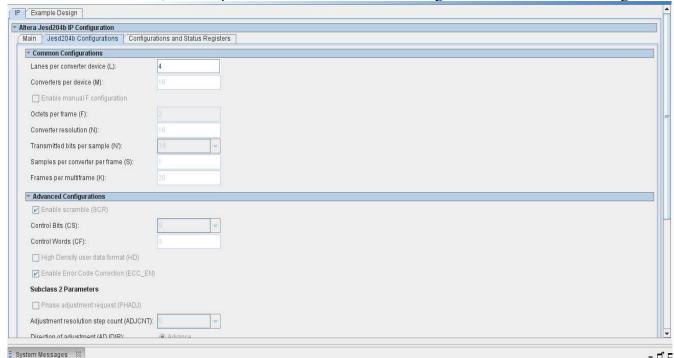
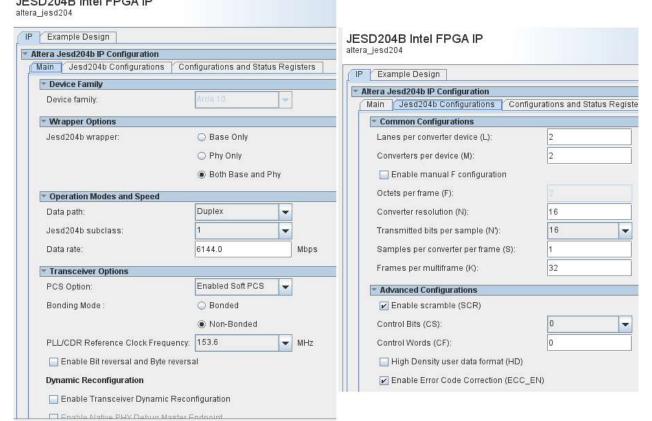
Questions about JESD204B Intel FPGA IP.

1. after I click save, then all parameters in the Jesd204b Configurations menu can't be changed.



2. the Octets per frame(F) will be forced to 2, if I select Phy Only in the main menu. Here are the steps I modify the parameters.

1. choose any presets for jesd 204_0 in the library. For example LMF = 222, 6.144Gbps JESD204B Intel FPGA IP



2. now I edit the parameters as following and I click save. The LMF = 4 16 8 which I target.

era Jesd204b IP Configuration			JESD2U4B INTEL FPGA IP		
ain Jesd204b Configurations Co	nfigurations and Status	Registers	altera_jesd204		
Device Family			IP Example Design		
Device family:	Arria 10	*	Altera Jesd204b IP Configuration		
Wrapper Options			Main Jesd204b Configurations Confi	gurations and Status Register	
Jesd204b wrapper:	Base Only		▼ Common Configurations		
	O Phy Only		Lanes per converter device (L):	4	
	Both Base and Phy	2 10	Converters per device (M):	16	
	Dour base and i my	0	Enable manual F configuration	,	
Operation Modes and Speed	D. 1		Octets per frame (F):		
Data path:	Duplex		Converter resolution (N):	16	
Jesd204b subclass:	1	<u>×</u>	Transmitted bits per sample (N'):		
Data rate:	6144.0	Mbps		16	
Transceiver Options			Samples per converter per frame (S):	1	
PCS Option:	Enabled Soft PCS	-	Frames per multiframe (K):	20	
Bonding Mode :	○ Bonded		 Advanced Configurations 		
	Non-Bonded				
PLL/CDR Reference Clock Frequency:		▼ MHz	Control Bits (CS):	0	
	1	WILL.	Control Words (CF):	0	
Enable Bit reversal and Byte revers	di		☐ High Density user data format (HD)	1	
Dynamic Reconfiguration					
			✓ Enable Error Code Correction (ECC	ction (ECC EN)	

3. if in the main menu, if I change Wrapper Options from Bothe Base and Phy to Phy Only. Once I click save, the the LMF will be forced to 4, 16, 2. I don't see why this could happen. Is there anything I missed here? Why Phy only wrapper options has to use F = 2?

ESD204B Intel FPGA IP era_jesd204 IP Example Design			IP Example Design Attera Jesd204b IP Configuration		
			Main Jesd204b Configurations Configurations and Status Register		
Altera Jesd204b IP Configuration			 Common Configurations 		
	onfigurations and Status	Registers	Lanes per converter device (L):	4	
Device Family			Converters per device (M):	16	
Device family:	Arria 10		Enable manual F configuration		
▼ Wrapper Options			Octets per frame (F):		
Jesd204b wrapper:	Base Only	7	Converter resolution (N):	16	
	Phy Only		Transmitted bits per sample (N'):	15 +	
	Both Base and Phy		Samples per converter per frame (S):	1	
▼ Operation Modes and Speed			Frames per multiframe (K):		
Data path:	Receiver		* Advanced Configurations		
Jesd204b subclass:	5	~	☑ Enable scramble (SCR)		
Data rate:	6144.0	Mbps	Control Bits (CS):	0	
▼ Transceiver Options			Control Words (CF):	0	
PCS Option:	Enabled Soft PCS		High Density user data format (HD)		
PLL/CDR Reference Clock Frequenc	y: 153.6	▼ MHz	☑ Enable Error Code Correction (ECC	EN)	
Enable Bit reversal and Byte reve	rsal				