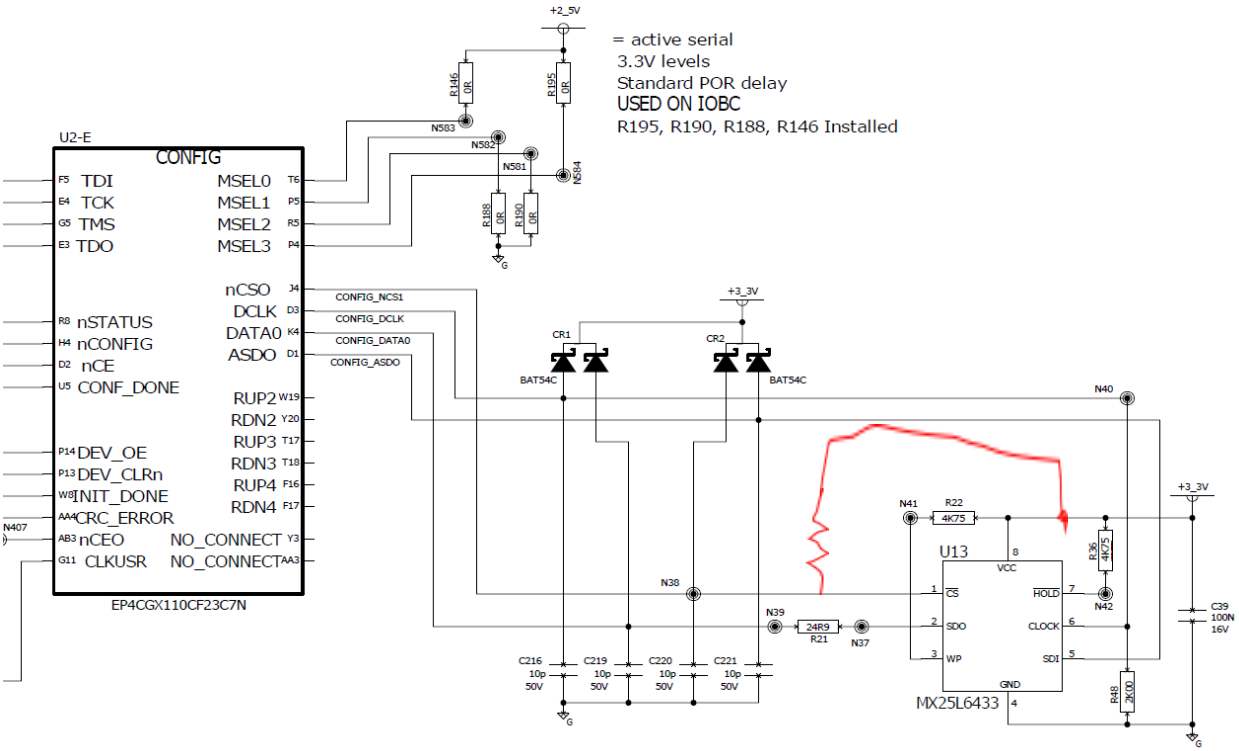
Hi.

I have a few questions regarding an issue I see with AS configuration for the Cyclone IV GX.

We have the SCD connected to the Cyclone IV as shown in this picture (without the red resistor that I drew).

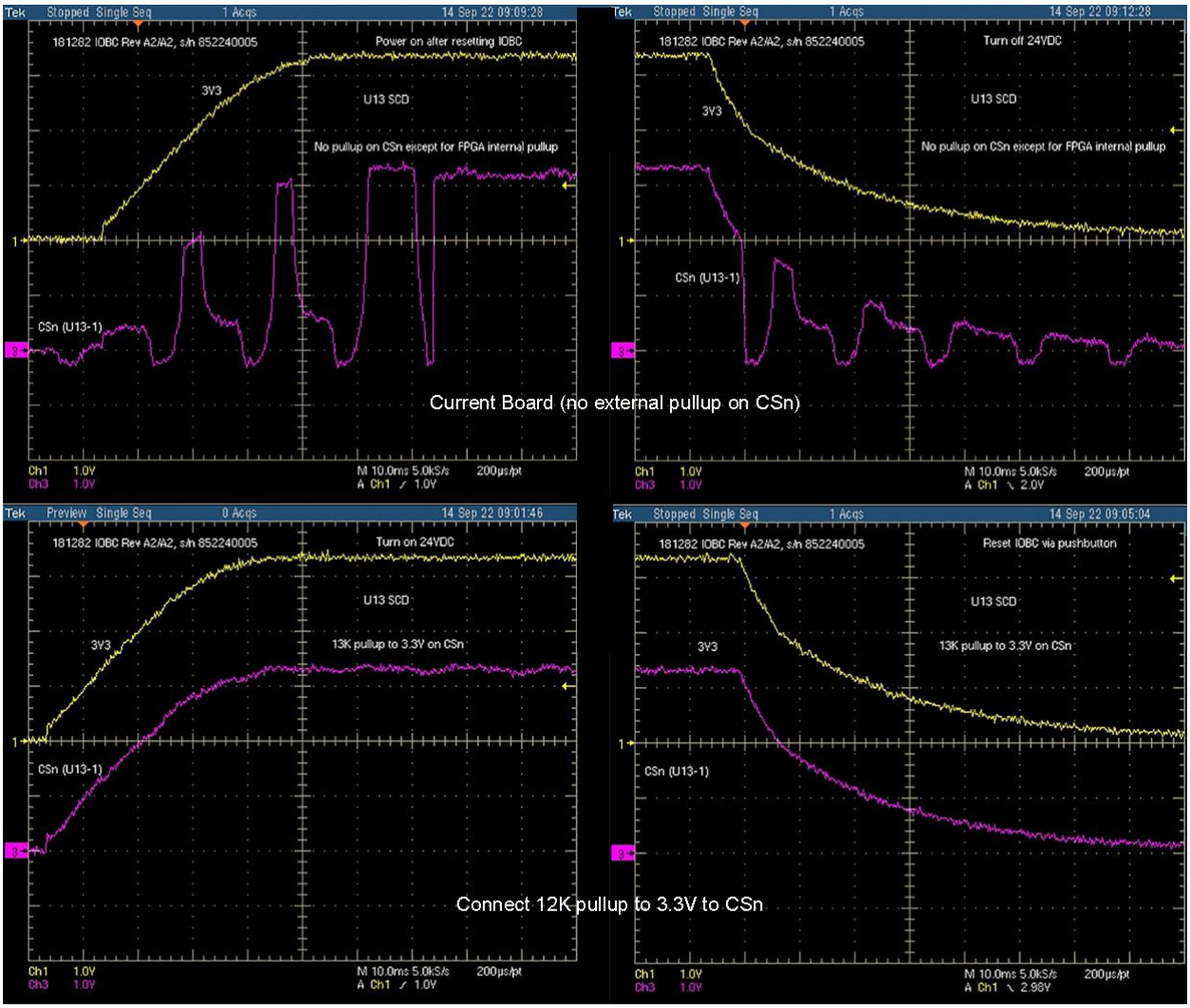


Everything works fine up to about 55C. Above that temperature, when the board is reset configuration fails at least one time. When the configuration fails, our watch dog timer resets the board and configuration is retried. Sometimes, that works and sometimes it fails a couple of other times before the FPGA is successfully loaded. We drive nCONFIG with the board's reset signal.

I troubleshot the problem and determined that the problem was caused by FPGA's nCSO signal going on and off multiple times at power up and at power down. See the scope picture, below. The datasheet for the configuration device clearly says that it's CSn input must be kept inactive as Vdd (3_3V) ramps up. Since the FPGA's datasheet says that it has an always-active internal pullup, I expected that would keep nCSO at the same level as Vdd as power ramped up or down. However, as you can see in the picture, it does not do anything like that. I fixed our problem by adding an external pullup resistor (shown in red) to the signal. With the resistor, FPGA configuration does not fail even at high temperatures.

Why do I need to do add the resistor? Is this particular FPGA chip broken? Is there some Quartus project setting that we need to make?

Are any other FPGA outputs also susceptible to this behavior? If so, we have a problem because we frequently depend on the FPGA's internal pullups to keep signals from floating.



Another question concerns the allowable capacitive load on the FPGA's SCD interface signals. The data book says that the load on DCLK cannot exceed 15pF and the loads on the other three signals cannot exceed 30pF. However, the data book also shows a protection circuit that has 10pF caps to ground. That is an appreciable part of the allowable load, especially for DCLK. The data sheet shows this circuit being used when a programming cable is also attached to the circuit. We put it on our board even though we do not connect the programmer there. Do you recommend that we remove the circuit even though configuration seems to be working now?

I also have a question about the frequency for DCLK. The data book says that for the 40MHz internal oscillator, DCLK will be 20MHz minimum, 30MHz typical, and 40MJHz maximum. At room temperature, I measure it at just under 16MHz.

My last question concerns the 2K pull down resistor shown on DCLK. We put that on the board to prevent any glitches on the clock as the chips powered up. I do not hink it does any harm. But, I am wondering if we need it.

Hi.

I saw the same failure at 60C on another board. I do not have scope pictures at 60C of that board but the external symptoms were exactly the same at the first board.

I brought board #2 back to my bench and scoped the signals at room temperature. A scope capture of nCSO as 3V3 rises is shown below. I added a 10K pullup to nCSO and now nCSO rises in sync with 3V3 as shown in the pictures in my previous email. I will run board #2 at temperature on Monday.