Using Selectable I/O Standards in APEX 20KE, APEX 20KC & MAX 7000B Devices

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Introduction

High-performance, low-voltage I/O standards have been introduced to keep pace with increasing clock speeds, higher data rates, and new low-voltage devices. These I/O standards are used to interface with memory, microprocessors, backplanes, and peripheral devices. Designers who want to use these new standards with programmable logic need flexible, high-performance, multi-standard I/O buffers.

Altera's revolutionary APEX™ 20KE and APEX 20KC devices offer the highest density, highest performance programmable logic solution with the necessary I/O standards for the communication and computer industries. Altera® MAX® 7000B devices are the product-term leader in I/O standard support: MAX 7000B devices are the only macrocell-based devices to support GTL+, 2.5-V SSTL-2, and 3.3-V SSTL-3.

With the new programmable I/O standards supported by APEX 20KE and MAX 7000B devices, a single device can simultaneously support multiple I/O standards, as well as interface with high-speed, low-voltage memory buses and backplanes. These I/O standards include LVDS, which supports data rates up to 840 megabits per second (Mbps). Embedding I/O standard support in programmable logic devices (PLDs) simplifies board design. Dedicated circuitry like LVDS transceivers is integrated into PLDs, saving board space, reducing pin usage, and improving performance.

This application note provides guidelines for designing with selectable I/O standards in Altera devices and covers the following topics:

- Overview of I/O standards and applications
- APEX 20KE, APEX 20KC and MAX 7000B I/O standard support
- Operating conditions
- Board termination schemes
- APEX 20K family I/O standard software support

Overview of I/O Standards & Applications

The ability for PLDs to support industry I/O standards gives customers a quick time-to-market design solution. This section provides an overview of typical applications for the selectable I/O standards supported by Altera devices. The specifications for each I/O standard are listed in this section.

LVTTL

The LVTTL standard is a single-ended, general-purpose standard for 3.3-V applications. The LVTTL interface is defined by JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. The LVTTL output buffer is a push-pull driver. This standard requires the output buffer to drive to 2.4 V (minimum V_{OH} = 2.4 V). It does not require the use of input reference voltages or termination. APEX 20K, APEX 20KE, and MAX 7000B devices are compliant with this standard. The maximum recommended input voltage for APEX and MAX 7000B devices is 4.1 V, which exceeds the 3.9-V requirement of this specification.

LVCMOS

The LVCMOS standard is defined in JEDEC Standard JESD 8-A, *Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits*. LVCMOS is a single-ended general-purpose standard also used for 3.3-V applications. The input buffer requirements are the same as the LVTTL requirements, and the output buffer is required to drive to the rail (minimum $V_{OH} = V_{CCIO} - 0.2$ V). This standard requires a 3.3-V I/O supply voltage (V_{CCIO}), but not the use of input reference voltages or termination. APEX 20K, APEX 20KE, APEX 20KC and MAX 7000B devices are compliant with the LVCMOS standard.

2.5 V

The 2.5-V I/O standard is documented by JEDEC Standard JESD 8-5, *2.5 V ± 0.2 V (Normal Range) and 1.7 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*. This standard is similar to LVCMOS but is used for 2.5-V power supply levels. APEX 20K, APEX 20KE, APEX 20KC and MAX 7000B devices are compliant with this standard, which requires a 2.5-V V_{CCIO}, but not the use of input reference voltages or termination.

1.8 V

The 1.8-V I/O standard is documented by JEDEC Standard JESD 8-7, *1.8 V ± 0.15 V (Normal Range) and 1.2 V to 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*. This standard is similar to LVCMOS but is used for 1.8-V power supply levels and reduced input and output thresholds. APEX 20K, APEX 20KE, APEX 20KC and MAX 7000B devices are compliant with this standard, which requires a 1.8-V V_{CCIO}, but not the use of input reference voltages or termination.

3.3-V PCI

APEX 20K, APEX 20KE and APEX 20KC devices are compliant with ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation. At 3.3 V, the PCI standard supports up to 64-bit bus width operation at 33 or 66 MHz. This standard uses LVTTL-type input and output buffers and requires a 3.3-V V_{CCIO}, but not the use of input reference voltages or termination. MAX 7000B devices are compliant with all aspects of this standard except that they do not offer clamps to V_{CCIO}.

PCI-X

The PCI-X standard is an enhanced version of the PCI standard that can support higher average bandwidth and has more stringent requirements. The APEX 20KE and APEX 20KC I/O drivers meet the requirements for PCI-X. In the Quartus II™ software, set the buffer setting to PCI to support PCI-X requirements, including the overshoot clamp. A future version of the Quartus II software will include the ability to choose PCI-X as an I/O standard.

LVDS

The LVDS I/O standard is used for very high-performance, low-power-consumption data transfer. Two key industry standards define LVDS: IEEE 1596.3 SCI-LVDS and ANSI/TIA/EIA-644. Both standards have similar key features, but the IEEE standard supports a maximum data transfer of 250 Mbps. APEX 20KE devices are designed to meet the ANSI/TIA/EIA-644 requirements at up to 840 Mbps. The LVDS standard requires a 3.3-V V_{CCIO} and a 100-Ω termination resistor between the two traces at the input buffer. No input reference voltage is required.

For more information on LVDS, see the Altera web site at **http://www.altera.com**.

LVPECL

The LVPECL standard is a differential I/O standard that is similar to LVDS. APEX 20KE devices can support LVPECL I/O standard by using the I/O pins in LVDS mode with an external resistor network.

GTL+

The GTL+ standard is a high-speed bus standard first used by Intel Corporation for interfacing with the Pentium Pro processor and is often used for processor interfacing or communication across a backplane. GTL+ is a voltage-referenced standard requiring a 1.0-V input reference voltage (V_{REF}) and board termination voltage (V_{TT}) of 1.5 V. The GTL+ standard is an open-drain standard that requires a minimum V_{CCIO} supply voltage of 3.0 V. APEX 20KE and MAX 7000B devices are compliant with this standard.

SSTL-2 Class I & II

The SSTL-2 standard, specified by JEDEC Standard JESD 8-9, *Stub-Series Terminated Logic for 2.5 Volts (SSTL-2)*, is a voltage-referenced standard requiring a 1.25-V V_{REF}, a 2.5-V V_{CCIO}, and a 1.25-V V_{TT}. SSTL-2 is used for high-speed SDRAM interfaces. APEX 20KE, APEX 20KC and MAX 7000B devices are compliant with this standard.

SSTL-3 Class I & II

The SSTL-3 standard, specified by JEDEC Standard JESD 8-8, *Stub-Series Terminated Logic for 3.3 Volts (SSTL-3)*, is a voltage-referenced standard requiring a 1.5-V V_{REF}, a 3.3-V V_{CCIO}, and a 1.5-V V_{TT}. SSTL-3 is used for high-speed SDRAM interfaces. APEX 20KE, APEX 20KC and MAX 7000B devices are compliant with this standard.

HSTL Class I

The HSTL standard, specified by JEDEC Standard JESD 8-6, *High-Speed Transceiver Logic (HSTL)*, is a 1.5 V output buffer supply voltage based interface standard for digital integrated circuits. HSTL is a voltage-referenced standard requiring a 0.75-V V_{REF}, a 1.5-V V_{CCIO}, and a 0.75-V V_{TT}. APEX 20KE and APEX 20KC devices support HSTL Class I operation with a V_{CCIO} voltage of 1.8 V. APEX 20KE and APEX 20KC devices drive compliant V_{OH} and V_{OL} levels with V_{CCIO} at 1.8 V.

AGP

The AGP standard is specified by the *Advanced Graphics Port Interface Specification Revision 2.0* introduced by Intel Corporation for graphics applications. AGP is a voltage-referenced standard requiring a 1.32-V V_{REF} and a 3.3-V V_{CCIO}. AGP does not require termination. APEX 20KE and APEX 20KC devices support the AGP interface.

CTT

The CTT standard is specified by JEDEC Standard JESD 8-4, *Center-Tap-Terminated (CTT) Low-Level, High-Speed Interface Standard for Digital Integrated Circuits*. CTT is a voltage-referenced standard requiring a 1.5-V V_{REF}, a 3.3-V V_{CCIO}, and a 1.5-V V_{TT}. The CTT standard is a superset of LVTTL and LVCMOS. CTT receivers are compatible with LVCMOS and LVTTL standards. CTT drivers, when unterminated, are compatible with the AC and DC specifications for LVCMOS and LVTTL.

APEX 20KE & MAX 7000B I/O Standards Support

The APEX 20KE I/O blocks support 16 I/O standards and are the only PLDs in the industry with LVDS. MAX 7000B devices provide support for GTL+, SSTL-2, and SSTL-3, a unique feature among product-term-based PLDs.

The programmable input/output element (IOE) blocks in both APEX 20KE and MAX 7000B devices have individual power supplies with separate I/O supply voltage (`VCCIO`) pins for each I/O block. The V_{CCIO} supply supports 3.3-V, 2.5-V, and 1.8-V levels.

APEX 20KE & MAX 7000B I/O Standards

The APEX 20KE and MAX 7000B I/O buffers meet the voltage, drive strength, and AC characteristics necessary to comply with the I/O standards listed in Table 1.

Table 1. APEX 20KE & MAX 7000B Supported I/O Standards

I/O Standard	Device		Type	Input Reference Voltage (V_{REF}) (V) *(1)*	Output Supply Voltage (V_{CCIO}) (V) *(1)*	Board Termination Voltage (V_{TT}) (V) *(1)*
	APEX 20KE	MAX 7000B				
LVTTL	✓	✓	Single-ended	N/A	3.3	N/A
LVCMOS	✓	✓	Single-ended	N/A	3.3	N/A
2.5 V	✓	✓	Single-ended	N/A	2.5	N/A
1.8 V	✓	✓	Single-ended	N/A	1.8	N/A
PCI	✓	✓ *(2)*	Single-ended	N/A	3.3	N/A
PCI-X	✓		Single-ended	N/A	3.3	N/A
LVDS	✓		Differential	N/A	N/A	N/A
LVPECL	✓		Differential	N/A	3.3	N/A
GTL+	✓	✓	Voltage-referenced	1.0	N/A	1.5
SSTL-2 Class I and II	✓	✓	Voltage-referenced	1.25	2.5	1.25
SSTL-3 Class I and II	✓	✓	Voltage-referenced	1.5	3.3	1.5
HSTL Class I	✓		Voltage-referenced	0.75	1.8 *(3)*	0.75
AGP	✓		Voltage-referenced	1.32	3.3	N/A
CTT	✓		Voltage-referenced	1.5	3.3	1.5

Notes:
(1) The values shown for V_{REF}, V_{CCIO}, and V_{TT} are typical values.
(2) MAX 7000B devices do not have the PCI diode clamp to V_{CCIO}. These devices comply with all other 64-bit/66-MHz 3.3-V PCI specifications.
(3) APEX 20KE devices drive HSTL-compliant signal levels with V_{CCIO} corrected to a 1.8-V supply.

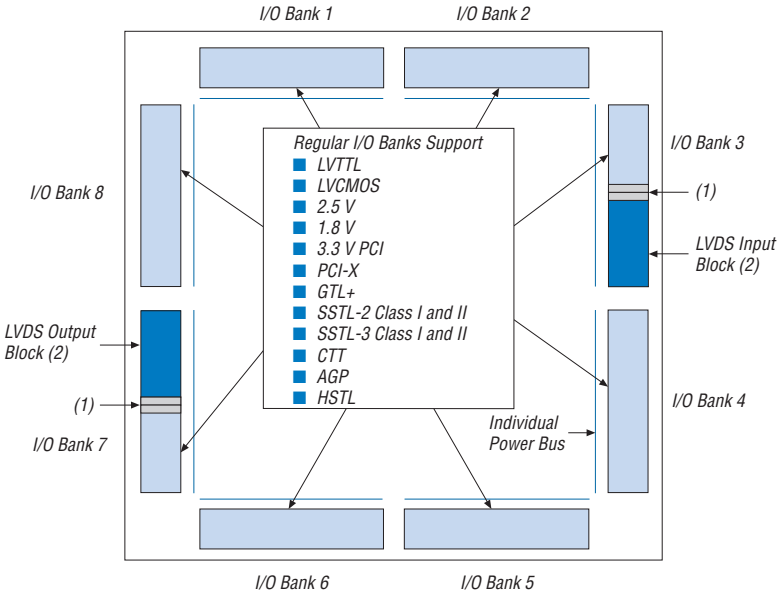
Each I/O standard has different V_{REF}, V_{TT}, and V_{CCIO} requirements. For more information, refer to "Board Termination Schemes" on page 14.

APEX 20KE I/O Standards

The I/O banks in the APEX 20KE devices support 16 I/O standards and are the first programmable logic devices (PLDs) in the industry with dedicated LVDS circuitry. APEX 20KE devices in BGA and FineLine BGA™ packages have eight programmable I/O banks and two LVDS I/O blocks (one transmitter block and one receiver block) within two of the I/O banks. The programmable input/output element (IOE) banks in APEX 20KE devices have individual power planes with separate I/O supply voltage (VCCIO) pins for each I/O bank. The V_{CCIO} supply supports 3.3-V, 2.5-V, and 1.8-V levels.

APEX 20KE devices in FineLine BGA packages have eight programmable I/O blocks and two LVDS I/O blocks. Figure 1 shows the representation of the I/O blocks. For APEX 20KE designs that do not use LVDS, the LVDS I/O blocks can be used for any other standard.

Figure 1. APEX 20KE I/O Blocks



Note:

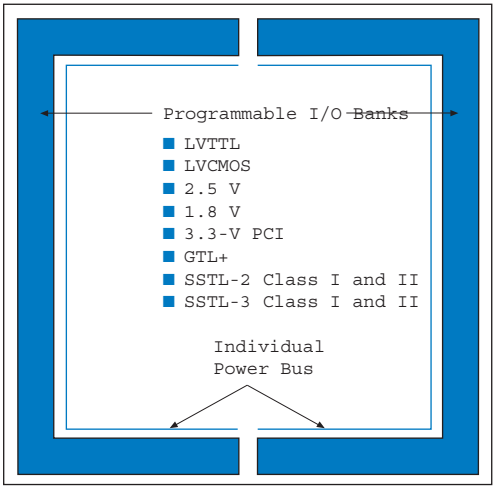
(1) For more information on placing I/O pins in LVDS blocks, refer to the "Guidelines for Using LVDS Blocks" section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

MAX 7000B I/O Standards

Each MAX 7000B device has two programmable I/O blocks. Each I/O block can be configured independently to utilize any of the I/O standards supported by MAX 7000B devices. Additionally, you can use I/O standards with common V_{CCIO} voltages simultaneously within a single block. Each programmable I/O block has its own power supply with separate VCCIO pins and support for 3.3-V, 2.5-V, and 1.8-V voltage levels. Figure 2 shows a representation of the MAX 7000B programmable I/O blocks.

Figure 2. MAX 7000B I/O Banks *Notes (1), (2), (3)*



Notes:
(1) Any input pin can be referenced to one of the two available V_{REF} levels.
(2) MAX 7000B devices have two VREF pins that can be referenced by any I/O pin in both I/O blocks.
(3) The output drivers are dependent on V_{CCIO}. The VCCIO pins for each I/O block can be powered to a different voltage.

Operating Conditions

Tables 2 through 17 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only. APEX 20KE and MAX 7000B devices may exceed these specifications. Consult individual device data sheets for details.

Table 2. LVTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–5	10	µA
V_{OH}	High-level output voltage	I_{OH} = –4 mA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		0.4	V

Table 3. LVCMOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0 V I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0 V I_{OL} = 0.1 mA		0.2	V

Table 4. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OH} = 1 mA		0.4	V
		I_{OH} = 2 mA		0.7	V

Table 5. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage			0.35 × V_{CCIO}	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.45	V

Table 6. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 7. 3.3-V PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
I_{IL}	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10.0		10.0	µA
V_{OH}	High-level output voltage	I_{out} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{out} = 1500 µA			$0.1 \times V_{CCIO}$	V
L_{pin}	Pin Inductance				15.0	nH

Table 8. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		450	mV
ý V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ý V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX devices)		90	100	110	Ω

Table 9. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA			0.65	V

Table 10. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA			V_{TT} – 0.57	V

Table 11. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA			V_{TT} – 0.76	V

Table 12. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O Supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{TT} – 0.6	V

Table 13. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O Supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA			V_{TT} – 0.8	V

Table 14. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O Supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V

Table 15. LVPECL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output Supply Voltage	3.135	3.3	3.465	V
V_{IL}	Low-level input voltage	1300		1700	mV
V_{IH}	High-level input voltage	2100		2600	mV
V_{OL}	Low-level output voltage	1450		1650	mV
V_{OH}	High-level output voltage	2275		2420	mV
V_{ID}	Input Voltage Differential	400	600	950	mV
V_{OD}	Output Voltage Differential	625	800	950	mV
t_r, t_f	Rise/Fall Time (20 to 80%)	85		325	ps
t_{DSKEW}	Differential Skew			25	ps
t_O	Output Load		150		Ω
R_L	Receiver differential input resistor		100		Ω

Table 16. 3.3-V AGP I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1500 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 17. CTT I/O Specifications

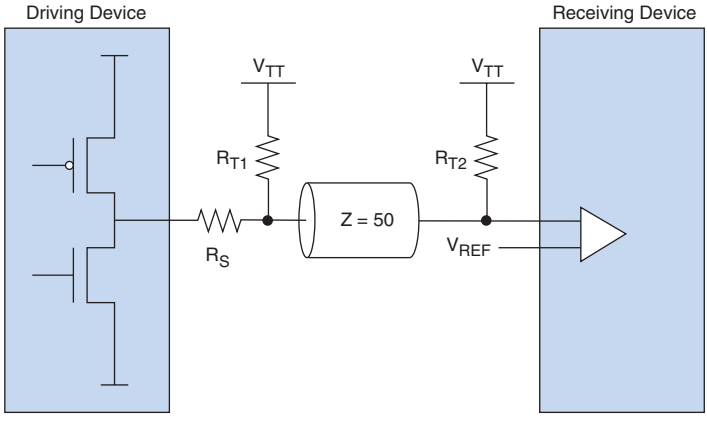
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(1)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND õ V_{OUT} õ V_{CCIO}	–10		10	µA

Note:
(1) V_{REF} specifies center point of switching range.

Board Termination Schemes

The various I/O standards supported by APEX 20KE and MAX 7000B devices require specific termination schemes to achieve their high speeds. Each I/O standard has an individual termination scheme. The diagram in Figure 3 shows the series and parallel termination resistors that are used with the I/O standards.

Figure 3. Board Termination Diagram



The LVDS I/O standard requires a termination resistor between the signals at the receiving device as shown in Figure 4. The termination resistor should match the differential load impedance of the bus ranging from 90 to 110 Ω, but typically 100 Ω.

Figure 4. LVDS Board Termination at the Receiver

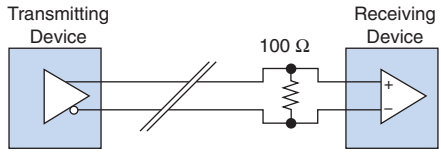


Table 18 shows the board termination values and reference voltages that each APEX 20KE I/O standard uses.

Table 18. Board Termination Values

I/O Standard	Output Driver	R_S (Ω)	R_{T1} (Ω)	R_{T2} (Ω)	V_{REF} (V)	V_{TT} (V)
GTL+	Open-drain	–	50	50	1.0	1.5
SSTL-2 Class I	Push-pull	25	–	50	1.25	1.25
SSTL-2 Class II	Push-pull	25	50	50	1.25	1.25
SSTL-3 Class I	Push-pull	25	–	50	1.5	1.5
SSTL-3 Class II	Push-pull	25	50	50	1.5	1.5
HSTL Class I	Push-pull	–	–	50	0.75	0.75
AGP	Push-pull	–	–	–	1.32	–
CTT	Push-pull	–	–	50	1.5	1.5

MAX 7000B Software Support

Software Support for MAX 7000B Devices

Selectable I/O standards are programmable on a per pin basis for both APEX 20KE and MAX 7000B devices. APEX 20KE devices have a total of 10 I/O blocks, including two LVDS blocks. The LVDS I/O blocks can also be used for any of the other I/O standards when not used for LVDS. MAX 7000B devices have two I/O blocks; I/O standards supported by MAX 7000B devices are shown in Table 1 on page 6. The Quartus™ II and MAX+PLUS® II software tools define the I/O standard used for each I/O block.

Software support for MAX 7000B devices selectable I/O standards is provided in the MAX+PLUS II software version 9.4 and higher. This document explains the Quartus II software's support for selectable I/O standards. For information on how the MAX+PLUS II software supports these standards, contact Altera Applications.

APEX 20K Family I/O Standard Software Support

This section shows how to implement and view the selectable I/O standards for the APEX 20K family in the Quartus II software and gives placement and assignment guidelines. The following topics will be discussed:

- **Device and Pin Options** dialog box
- **Pin Assignments** dialog box
- Representation of I/O banks and I/O standards in the floorplan editor
- Automatic placement & verification of selectable I/O standards with the Quartus II software
- Guidelines for selectable I/O standards
- I/O and VREF pin placement guidelines

Device & Pin Options Dialog Box

The **Voltage** tab in the **Device & Pin Options** dialog box (**Compiler Settings** dialog box) contains a **Default I/O Standard** drop-down menu, which is used to set the default I/O standard for a device. All I/O pins without a specific I/O standard assignment will default to the I/O standard specified in this drop-down menu. The drop-down menu has the following options for APEX 20KE devices:

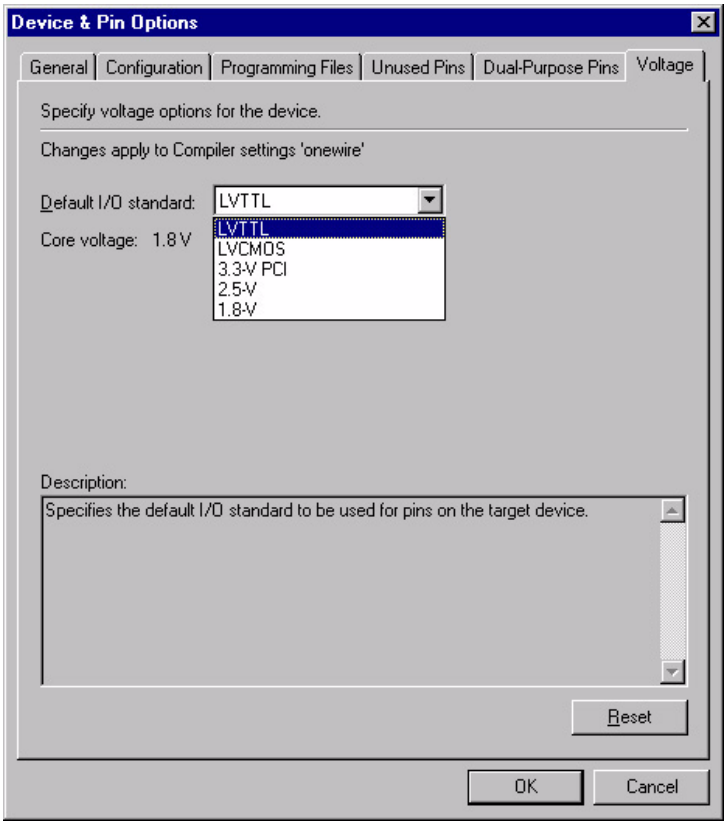
- LVTTL (default setting)
- LVCMOS
- 2.5 V
- 1.8 V
- PCI
- PCI-X (supported in a future version of the Quartus II software)
- LVDS
- LVPECL (supported in a future version of the Quartus II software)
- GTL+
- SSTL-2 Class I & II
- SSTL-3 Class I & II
- HSTL Class I (supported in a future version)
- AGP
- CTT

The options available for APEX 20K devices in the drop-down menu are as follows:

- LVTTL
- LVCMOS (default setting)
- 3.3-V PCI
- 2.5 V
- 1.8 V

Figure 5 shows the **Device & Pin Options** dialog box (**Compiler Settings** dialog box) when targeting an APEX 20KE device.

Figure 5. Device & Pin Options Dialog Box for APEX 20KE Devices



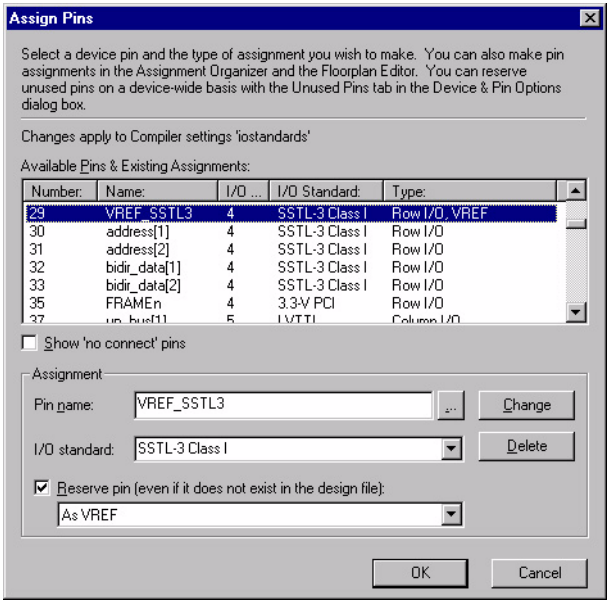
Pin Assignments Dialog Box

In the **Pin Assignments** dialog box, designers can make pin assignments, specify I/O standards, V_{REF} assignments, and view the settings made to each pin.

Figure 6 shows the **Pin Assignments** dialog box. The Number column corresponds with the pin number on the specified package. The Name column contains the user-specified pin name in the design. There are two relevant columns to note: I/O Bank and I/O Standard. The Type column in the **Available Pins & Existing Assignments** list box displays the following pin types: Row I/O, Column I/O, V_{REF}, Reserved, and dual-purpose pin names. The list box is sortable on any column by clicking on the column heading.

There are drop-down menus for making I/O standard and reserved pin assignments on a pin-by-pin basis. V_{REF} pins are assigned the same way as reserved pins. To select the I/O standard for I/O and V_{REF} pins, choose an I/O standard from the **I/O standard** drop-down menu. To assign a pin to be a V_{REF}, enter a pin name (reserve pin names are not declared in the design file), check the **Reserve pin** box, and select reserve as V_{REF} from the drop-down menu.

Figure 6. Pin Assignments Dialog Box



Follow the steps below to make pin assignments, designate I/O standard types, and reserve pins. Designers should reserve I/O pins that may be needed in the future.

1. If you have not already done so, open or create the project that you want to modify.
2. Choose **Compiler Settings** (Processing menu).
3. Click the **Chips & Devices** tab.
4. Select the target device in the **Available devices** list.
5. Click **Assign Pins**.
6. In the **Pin Assignments** dialog box, to show the pins for which you cannot assign a node name in the **Available pins & existing assignments** list, select **Show no connect pins.**
7. In the **Available pins & existing assignments** list, select the pin number for the pin to which you want to assign, change, or delete a node name assignment.
8. To delete the node name assignment from the pin, under **Assignment,** click **Delete**.
9. To assign a new node name to the pin, or change the existing node name assignment for the pin, under **Assignment**, type a node name in the **Pin name** box or Copy the node name to the **Pin Assignments** dialog box with the Node Finder.
10. If you added or changed the node name assignment for the pin and you want to assign an **I/O Standard** to the pin, under **Assignment**, select a standard from the **I/O Standard** list.
11. If you added or changed the node name assignment or I/O standard and you want to reserve the pin for future use, under **Assignment**, turn on **Reserve pin (even if it does not exist in the design file),** and select **As input tri-stated**, **As output driving ground**, **As output driving an unspecified signal**, or **As VREF** from the list.
12. To save a new assignment and add the assignment to the **Available pins & existing assignments** list, under **Assignment**, click **Add**.
13. To save the changed assignment and add the assignment to the **Available pins & existing assignments** list, under **Assignment**, click **Change**.
14. Repeat steps 7 to 13 for each additional assignment you want to make, change, or delete.
15. Click **OK**.

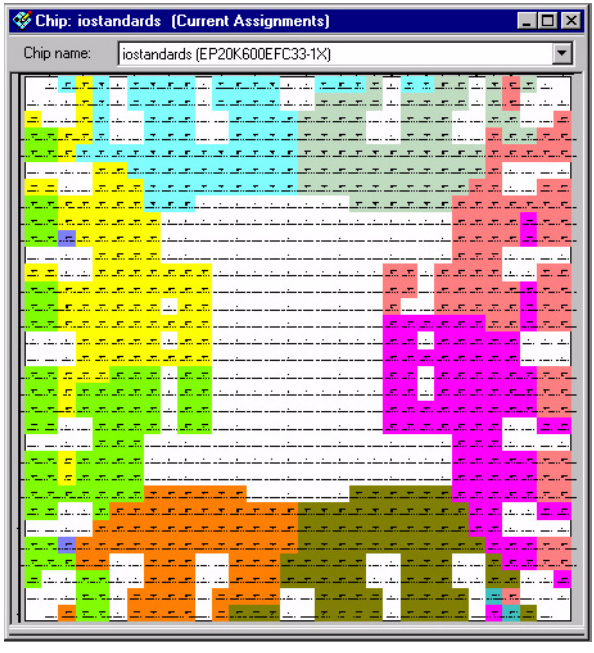
Representation of I/O Banks & Standards in the Floorplan Editor

The Floorplan Editor supports many features in APEX 20KE devices, including multiple I/O standards, PLLs, and the LVDS transmitter and receiver block.

The Floorplan Editor shows membership in I/O banks by using a unique background fill color around each pin for each I/O bank. In addition, the bank number is shown. The Floorplan editor has two package views (Package Top and Package Bottom) and three internal views (Interior MegaLAB™, Interior LABs and Interior Cells). In the package views the I/O bank number is labeled above the pin for pin-grid array (PGA) and BGA packages, or on the inside of the device for quad flat pack (QFP) packages. In the interior views, the I/O is outside the package as a background around the pin name.

Only I/O and `VCCIO` pins have the colored background; `GNDINT`, `GNDIO`, and `VCCINT` pins do not, as they are not specific to a particular I/O bank. Figure 7 shows the coloring in the Floorplan Editor for the EP20K600E device (1,020-pin FineLine BGA device package) in package view.

Figure 7. Package View with Show I/O Banks On



Under the View pull-down menu in the Floorplan Editor, the **Show I/O Banks** option controls and displays the I/O bank colors. This command also turns on the display of both the I/O bank colors and bank numbers in the three interior views.

The Floorplan Editor **Color Legend**, located under the View pull-down menu, has an entry for each I/O bank color, as shown in Figure 8. The output clock and feedback pins for PLL1 and PLL2 reside in I/O Bank 9 and I/O Bank 10 and can support any of the I/O standards supported for APEX 20KE devices.

Figure 8. Pin Color Legend Window for the Floorplan Editor

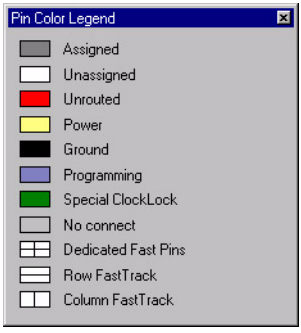


Figure 9 shows a portion of the package view of two EP20K100E device I/O Banks of a 240-pin plastic quad flat pack (PQFP) package in the Floorplan Editor.

In the PQFP packages, the eight I/O banks have been merged into 4 merged I/O banks. The VCCIO planes on merged I/O banks are internally connected in the PQFP packages. The naming convention for merged I/O banks lists the real I/O bank that the pin belongs to, and then lists the I/O bank with which it shares VCCIO. The I/O bank and Bank6 (Bank7) share the VCCIO with Bank7 (and Bank6), but has a different V_{REF} bus. This allows Bank6 (and Bank7) to be used for one voltage-referenced I/O standard and Bank7 (and Bank6) for another because they have separate V_{REF} buses, as long as those two standards use the same VCC level. For example, Bank6 (and Bank7) can implement GTL+ while Bank7 (and Bank6) implements SSTL-3 Class I.

Figure 9. Top View of the 240-Pin PQFP Package

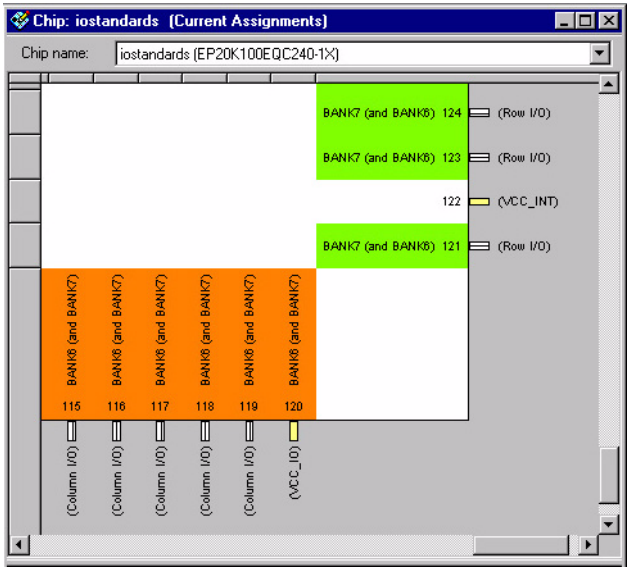
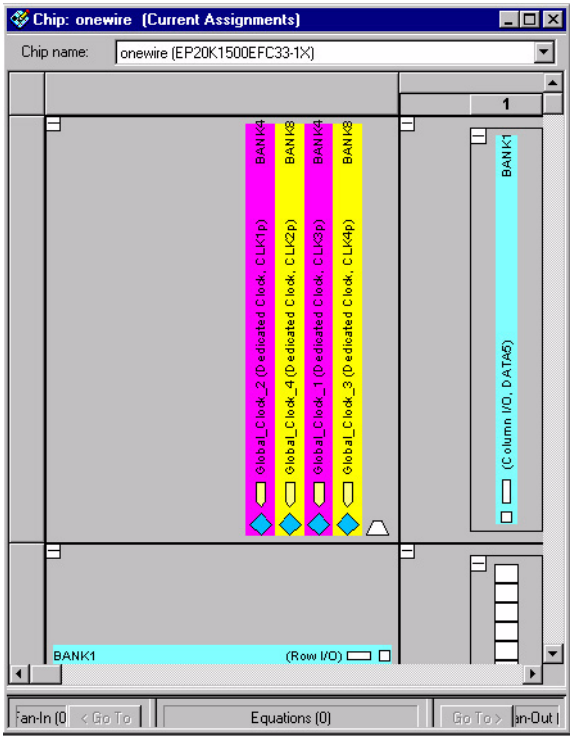


Figure 10 shows the internal cells view of the APEX 20KE device's PLL support. The diamond next to the dedicated clocks indicates that the PLL is used.

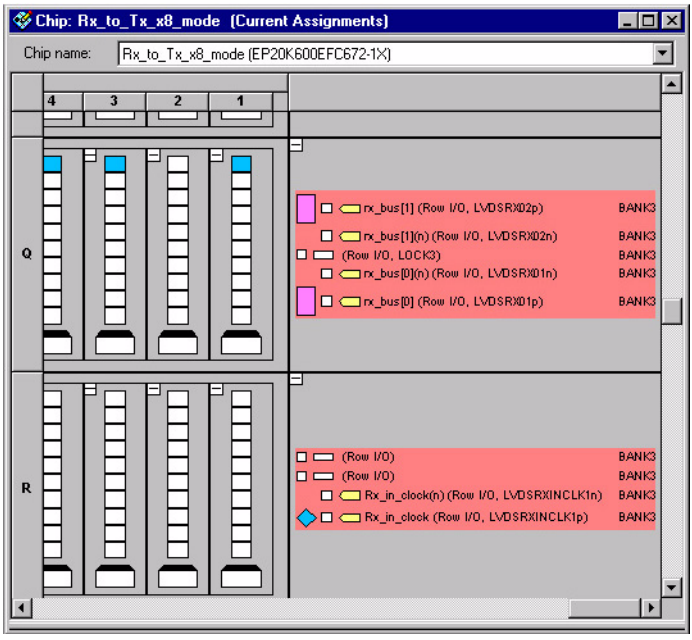
Figure 10. View of Internal Cells in Floorplan Editor



The dedicated clock pins (CLK1p, CLK2p, CLK3p, CLK4p) support LVDS and have optional dual-purpose negative polarity pins associated with them. The PLL feedback pins (CLKLK_FB1p, CLKLK_FB2p) and the PLL output pins (CLKLK_OUT1p, CLKLK_OUT2p) also support LVDS following the same convention as the dedicated clock pins.

Figure 11 shows the LVDS receiver in the Floorplan Editor. The receiver data channel, represented by LVDSRX01p and LVDSRX01n, feeds the dedicated serial-to-parallel converter. The LVDS clock (LVDSRXINCLK1p, LVDSINCLK1n) clocks the serial-to-parallel converter. The serial-to-parallel converter is shown by the filled rectangle adjacent to the IOE register associated with each positive polarity LVDS data and clock pin.

Figure 11. Internal Cells View of LVDS Receiver



Guidelines for Selectable I/O Standards

The following guidelines should be used when designing for the selectable I/O standards in APEX 20KE devices. The guidelines define which standards are compatible based on input, output, and bidirectional types within an I/O bank.

- No two input pins can be placed in the same I/O bank if their I/O standards require a different V_{REF} voltage. However, non-voltage-referenced standards can coexist with voltage-referenced standards; e.g., one bank can support GTL+ and LVTTL. For PQFP packages, the two merged I/O banks still support separate V_{REF} inputs for each bank. For example, if Bank1 and Bank8 are merged together, bank 1 can support GTL+ while Bank8 can support SSTL-3.

- No two push-pull standard output pins can be placed in the same I/O bank if they require a different VCCIO voltage level. All output pins have the same VCCIO level for merged I/O banks in the PQFP packages. GTL+ is an open-drain I/O standard and therefore can be assigned to I/O banks with a 2.5-V or 3.3-V VCCIO level.

- The clamp diode affects input tolerance. When the PCI clamp diode is turned on, an I/O pin is clamped to VCCIO. For example, a 2.5-V VCCIO bank without the clamp diode is tolerant to 3.3-V inputs. However, when the clamp is turned on, the 2.5-V VCCIO bank is not 3.3-V tolerant. An LVTTL input that does not have its clamp diode turned on can be placed in a bank that has a 2.5-V VCCIO level.

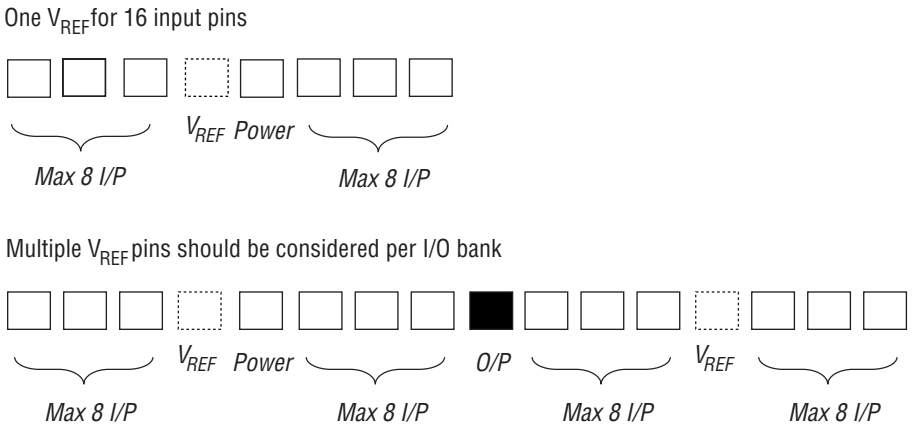
- Bidirectional pins have to satisfy both input and output guidelines.

- All output drivers between two GNDIO pins should not sink more current than 273 mA in total. Pins using the 1.8-V standard are not current limited. The current requirement for I/O standards with 3.3-V and 2.5-V VCCIO levels are defined as follows:

  - For VCCIO = 3.3 V,
    [(# of GTL+ × 36) + (# of LVTTL × I_{LVTTL}) + (# of PCI × 1.5) + (# of LVCMOS × I_{LVCMOS}) + (# of SSTL-3 class I × 8) + (SSTL-3 class II × 16) + (# of LVDS × 4.5) + (# of AGP × 1.5) + (# of CTT × 8)] mA ð 273 mA
  - Where I_{LVTTL} (4-mA default value) and I_{LVCMOS} (0.1 mA default value) are the current sink on the LVTTL and LVCMOS pins, respectively. If your system requires higher I_{CC} for LVTTL or LVCMOS pins (for example, due to termination) then adjust the equation accordingly.
  - For VCCIO = 2.5 V,
    ((# of 2.5V × 2) + (# of SSTL-2 class I × 7.6) + (# of SSTL-2 class II × 15.2) mA ð 273 mA
  - In practice, this rule applies only to SSTL-2 Class II, SSTL-3 Class II, GTL+, and LVCMOS and LVTTL pins which can sink more than 14 mA per output pin. For other standards, every pin can be used without violating this requirement.
  - The *APEX 20K Programmable Logic Device Family Data Sheet* shows the relationship of I/O pins to GNDIO pins to enable correct pin placement. This is also shown in the Quartus II software's Floorplan Editor and in Quartus II Help.

- When placing VREF pins, follow these guidelines. Output pins that can switch while an input is using a VREF have to be placed a distance of two pads away from the VREF pin, or a distance of one pad away from the VREF pin if the pad between them is a power (VCC or GND) pad. Figure 12 shows both cases. Multiple VREF pins may be used in an I/O bank of the same standards. Further VREF guidelines are discussed in the "I/O & VREF Placement Guidelines" on page 27.

Figure 12. Examples of V_{REF} Placement



Automatic Placement & Verification of Selectable I/O Standards With Quartus II Software

The Quartus II software verifies correct placement of all I/O and V_{REF} pins, following the same rules outlined in the "Guidelines for Selectable I/O Standards" on page 24.

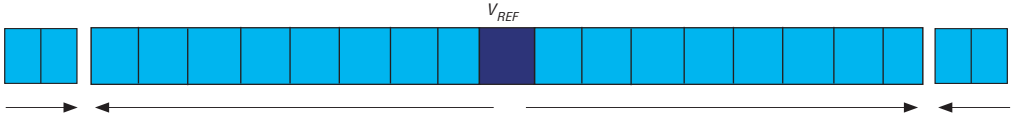
- Designers must assign VREF pins for all voltage-referenced I/O pins. The Quartus software automatically places I/O pins of different VREF standards without pin assignments in separate I/O banks.
- The Quartus software verifies that no two voltage-referenced I/O pins requiring different VREF or LVDS pin levels are placed in one bank.
- The Quartus software ensures that an I/O pin requiring a VREF pin is no more than 16 pins from a VREF pin. All 16 voltage-referenced I/O pins may be placed on only one side of the VREF pin or staggered on both sides of the VREF pin.
- The Quartus II software reports an error message if the current limitation is exceeded between GNDIO pins. It uses the equations documented in the "Guidelines for Selectable I/O Standards" on page 24.
- The Quartus II software ensures that no more than 16 voltage referenced I/O standard pins are using a single VREF.

- The Quartus II software does not allow you to place an output pin within two pins of a VREF if a power pin does not separate them. To view pad orientation, use the Show Pads view in the Floorplan Editor.
- The Quartus II software will reserve the unused LVDS channels in the LVDS transmitter and receiver blocks when any of the LVDS channels are being used. It will also reserve the two I/O pins adjacent to the LVDS blocks that share a VCCIO pin with the LVDS blocks.
- The Quartus II software will not allow placement of non-LVDS output pins in or within two I/O pins (with a common VCCIO pin) of the LVDS blocks.

I/O & V_{REF} Placement Guidelines

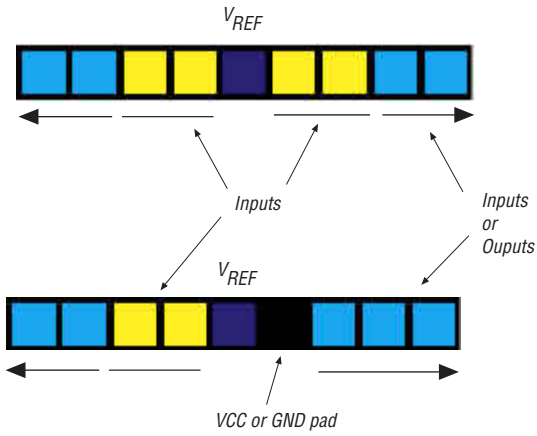
This section discusses VREF and I/O pin placement guidelines when designing with I/O buses. Each VREF pin can support up to eight voltage-referenced input pins on each side, or 16 input pins in total, as shown in Figure 13. The Quartus II software will give an error message if a voltage-referenced input pin is placed more than 16 pads from a VREF pin.

Figure 13. Each V_{REF} Can Support 16 Input Pins



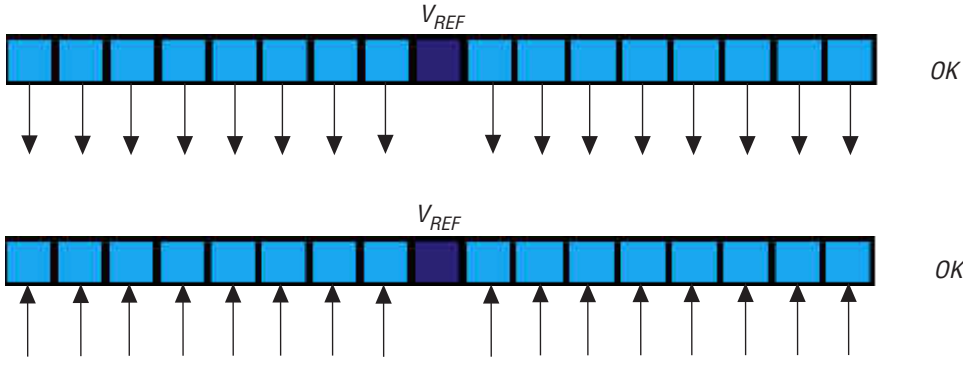
Output pins should be placed two or more pins away from VREF pins, except when the VREF is next to a power pin. In that case the power pin isolates the VREF pin from the switching output. Output pins can be placed on the other side of the power pin, as shown in Figure 14.

Figure 14. VREF Pin Placement Guidelines



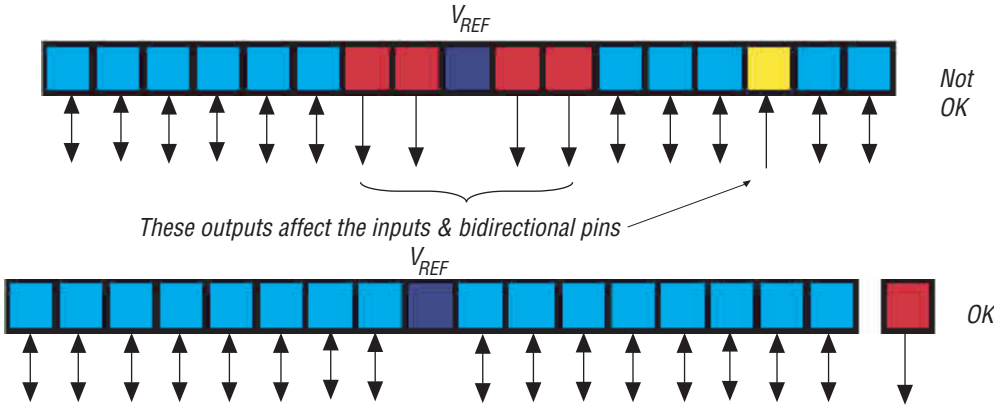
Voltage-referenced bidirectional buses that share a single tri-state control signal can be placed around the VREF pin, as shown in Figure 15. This works because the bus is only operating in one direction at a time. When the bidirectional pins are driving out, no inputs are using the VREF pin. When the bidirectional pins are accepting input signals, there are no output pins that would interfere with the input pins' ability to use the V_{REF} level.

Figure 15. Placement of Bidirectional Buses with Single OE Control



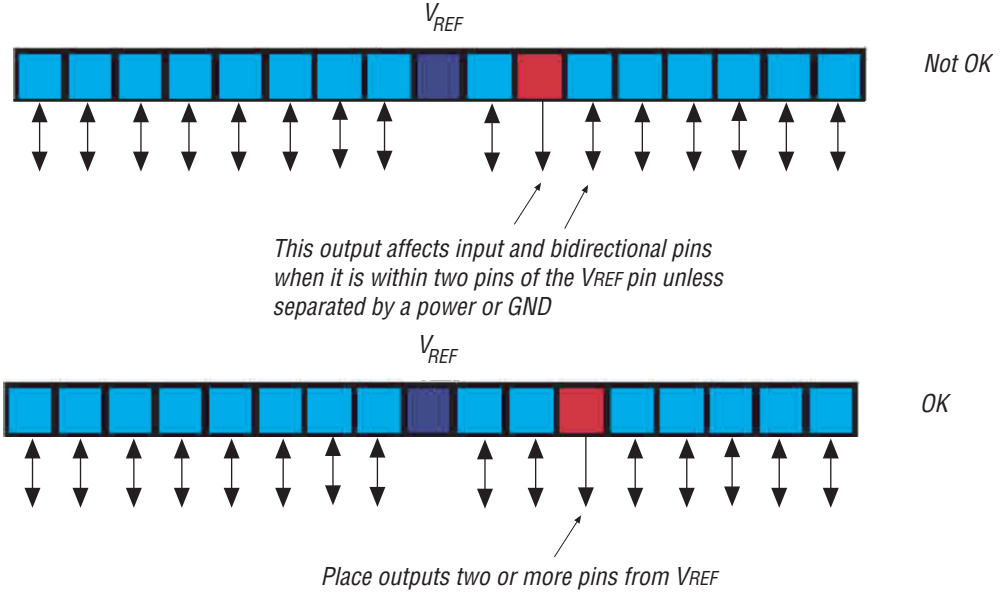
Output pins can be placed outside the bus without affecting the use of VREF in the bidirectional bus, as shown in Figure 16. Furthermore, an unrelated output pin may be placed within a voltage-referenced bidirectional bus if the output pin is more than two pads from the VREF pin or separated by a power pin.

Figure 16. Placement of Output Pins Outside the Bidirectional Buses



Output pins can also be placed inside the bus if they are more than two pins away from the VREF pin, as shown in Figure 17.

Figure 17. Output Pin Placement in a Bidirectional Bus



Conclusion

The advanced programmable I/O features and standards simplify board design by minimizing the number of devices used to interface with memory, microprocessors, and backplanes. The APEX 20KE devices, which are 64-bit, 66-MHz PCI compliant, support 16 programmable I/O standards, allowing customization for a wide variety of applications. Input, output, and bidirectional pins of different I/O standards can be intermixed with I/O banks by following the guidelines in this document. APEX 20KE devices also offer increased I/O performance with new standards and features like LVDS (840 Mbps data transfer).

References

- *Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits*, JESD8-A, Electronic Industries Association, June 1994.
- *Stub-Series Terminated Logic for 3.3 Volts (SSTL-3)*, EIA/JESD8-8, Electronic Industries Association, August 1996.
- *Stub-Series Terminated Logic for 2.5 Volts (SSTL-2)*, EIA/JESD8-9, Electronic Industries Association, September 1998.
- *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunication Industry Association/Electronic Industries Association.
- *2.5 V ±0.2 V (Normal Range) and 1.7 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*, EIA/JESD8-5, Electronic Industries Association, October 1995.
- *1.8 V ±0.15 V (Normal Range) and 1.2 V to 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit*, EIA/JESD8-7, Electronic Industries Association, February 1997.
- ***PCI Local Bus Specification, Revision 2.2***, PCI Special Interest Group, December 1998.

Revision History

The information contained in *Application Note 117 (Using Selectable I/OStandards in APEX 20KE, APEX 20KC & MAX 7000B Devices)* version 2.2 supersedes information published in previous versions.

Version 2.2

Application Note 117 (Using Selectable I/OStandards in APEX 20KE, APEX 20KC & MAX 7000B Devices) version 2.2 contains the folllowing change:

- Updated Figure 7.
- Updated *Note (1)* to Figure 7.

Version 2.1

Application Note 117 (Using Selectable I/OStandards in APEX 20KE, APEX 20KC & MAX 7000B Devices) version 2.1 contains the folllowing change: The title has been changed throughout the document.

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