Reduced Gigabit Media Independent Interface (RGMII)

4/1/2002
Version 2.0

Reduced Pin-count Interface
For
Gigabit Ethernet Physical Layer Devices

Revision Level	Date	Revision Description
1.0	June 1, 2000	Released for public review and comment
1.1	August 1, 2000	a) Modified RXERR and TXERR coding to reduce transitions and power in normal conditions. b) Removed CRS_COL pin and incorporated coding alternative for half duplex implementation. c) Found and corrected some inconsistencies in which clock was specified for timing. PHY generated signals are based on RXC and MAC generated signals are based on TXC. Specified that RXC is derived from TXC to eliminate need for FIFOs in the MAC. d) Modified timing diagram to incorporate PC board load conditions. e) Removed references to SMII due to broad concerns about IP exclusivity and added specification for 10/100 MII operation. f) Modified Intellectual Property statement to address incorporation of IP from multiple sources. g) Modified document formatting.
1.2	Sept 11, 2000	a) Changed TD[4]/TXEN_TXERR signal name to TX_CTL b) Changed RD[4]/RXEN_RXERR signal name to RX_CTL c) Removed 100ps jitter requirement from TXC d) Changed RXC derivation to received data stream e) Clarified Table 1 description of TX_CTL and RX_CTL logical functions f) Required CRS assertion/deassertion to be synchronous for all speeds. g) Returned timing numbers to absolute from percentages. h) Relaxed 10/100 Duty cycle requirements to 40/60 i) Added verbage to allow clock cycle stretching during speed changes and receive data and clock acquistion. j) Modified Table 4 to incorporate optional in-band signaling of link status, speed, and duplex. k) Slight wording change on IP statements to limit scope and indemnify.
1.2a	Sept 22, 2000	a) Clarified 3.4.2 statement to eliminate suggestion that in-band status was only required for half-duplex. b) Modified Table 2 to from "Clock to Data skew" to "Data to Clock skew" to clarify the fact that clock is delayed relative to data. c) Modified section 4.0 to clarify that MDIO/MDC are also operating at 2.5v CMOS levels.
1.3	Dec 10, 2000	a) Clarified RX_CTL and TX_CTL functionality by modifying Figure 4 and adding Figure 5 and Figure 6. b) Modified Table 3 to include the value of FF as reserved when TX_CTL=0,1. c) Reduced TskewR in Table 2 to a value of 2.6ns maximum for Gigabit operation and relaxed it in note #1 for 10/100 operation. d) Put maximum delay in note #1 of Table 2 of 2ns to ensure minimum setup time for subsequent edges.
2.0	April 1, 2002	a) Changed I/O specification to HSTL Class 1 per JESD 8-6 and removed table 5. b) Changed timing specification to allow transmitter to integrate delay previously allocated to PC layout; modified figure 2, added figure 3, and modified table 2 to address these changes.

1.0 Purpose

The RGMII is intended to be an alternative to the IEEE802.3u MII, the IEEE802.3z GMII and the TBI. The principle objective is to reduce the number of pins required to interconnect the MAC and the PHY from a maximum of 28 pins (TBI) to 12 pins in a cost effective and technology independent manner. In order to accomplish this objective, the data paths and all associated control signals will be reduced and control signals will be multiplexed together and both edges of the clock will be used. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100 operation, the clocks will operate at 2.5MHz or 25MHz respectively.

2.0 System Diagram

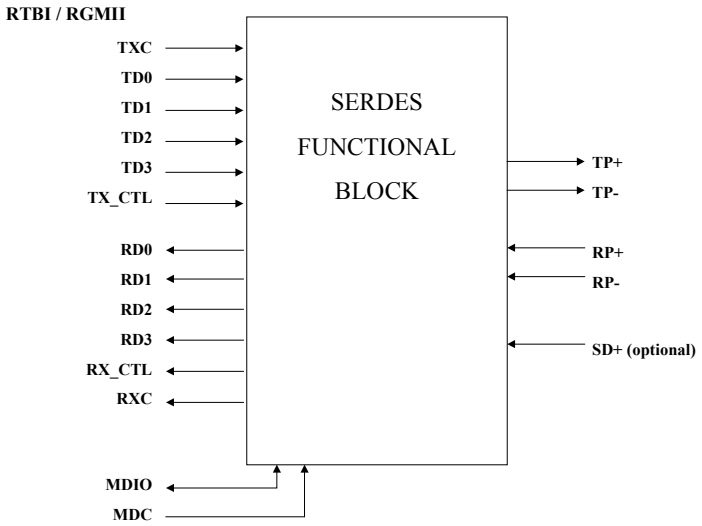

FIGURE 1 (System Diagram)

3.0 Signal Definitions

The RGMII will share four data path signals with the Reduced Ten Bit Interface (RTBI) and share control functionality with the fifth data signal. With the inclusion of the MDIO/MDC serial management signals, the RTBI will not require independent control signals like LK_REF, BYTE_EN, etc. Register assignment of SERDES control bits is left to the implementer.

Signal Name	RTBI	RGMII	Description
TXC	**MAC**	**MAC**	The transmit reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm depending on speed.
TD[3:0]	**PCS**	**MAC**	In RTBI mode, contains bits 3:0 on ↑ of TXC and bits 8:5 on ↓ of TXC. In RGMII mode, bits 3:0 on ↑ of TXC, bits7:4 on ↓ of TXC
TX_CTL	**PCS**	**MAC**	In RTBI mode, contains the fifth bit on ↑ of TXC and tenth bit on ↓ of TXC. In RGMII mode, TXEN on ↑ of TXC, and a logical derivative of TXEN and TXERR on ↓ of TXC as described in section 3.4
RXC	**PHY**	**PHY**	The continuous receive reference clock will be 125Mhz, 25Mhz, or 2.5Mhz +- 50ppm. and shall be derived from the received data stream
RD[3:0]	**PHY**	**PHY**	In RTBI mode, contains bits 3:0 on ↑ of RXC and bits 8:5 on ↓ of RXC. In RGMII mode, bits 3:0 on ↑ of RXC, bits7:4 on ↓ of RXC
RX_CTL	**PHY**	**PHY**	In RTBI mode, contains the fifth bit on ↑ of RXC and tenth bit on ↓ of RXC. In RGMII mode, RXDV on ↑ of RXC, and a derivative of RXDV and RXERR on ↓ of RXC as described in section 3.4

TABLE 1 (Signal Definitions)

3.1 Signal Logic Conventions

All signals shall be conveyed with positive logic except as specified differently. For descriptive purposes, a signal shall be at a logic "high" when it is at a valid voltage level greater than V_{OH_MIN}, and logic "low" when it is at a valid voltage level less than V_{OL_MAX}.

3.2 Multiplexing of Data and Control

Multiplexing of data and control information is done by taking advantage of both edges of the reference clocks and sending the lower 4 bits on the ↑ edge and the upper 4 bits on the ↓ edge. Control signals can be multiplexed into a single clock cycle using the same technique.

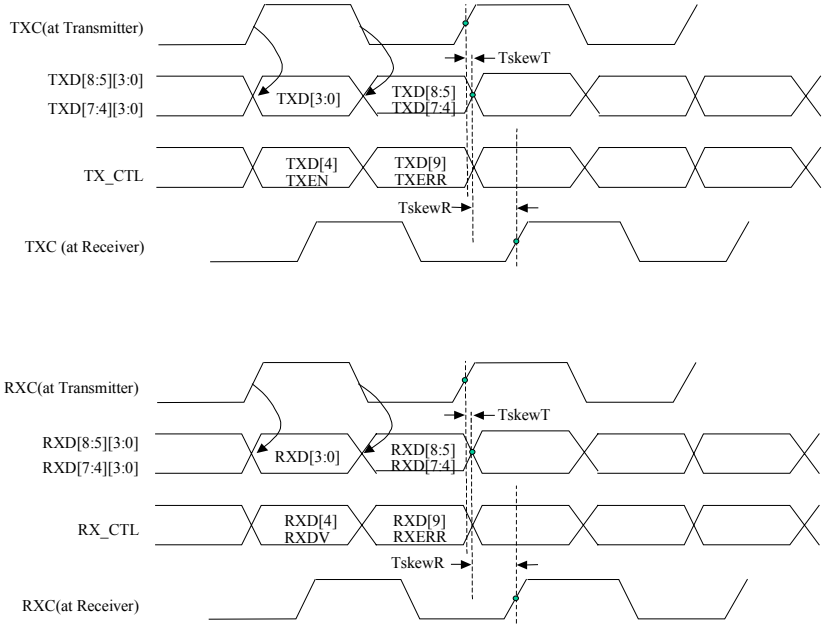

FIGURE 2 (Multiplexing & Timing Diagram - Original RGMII)

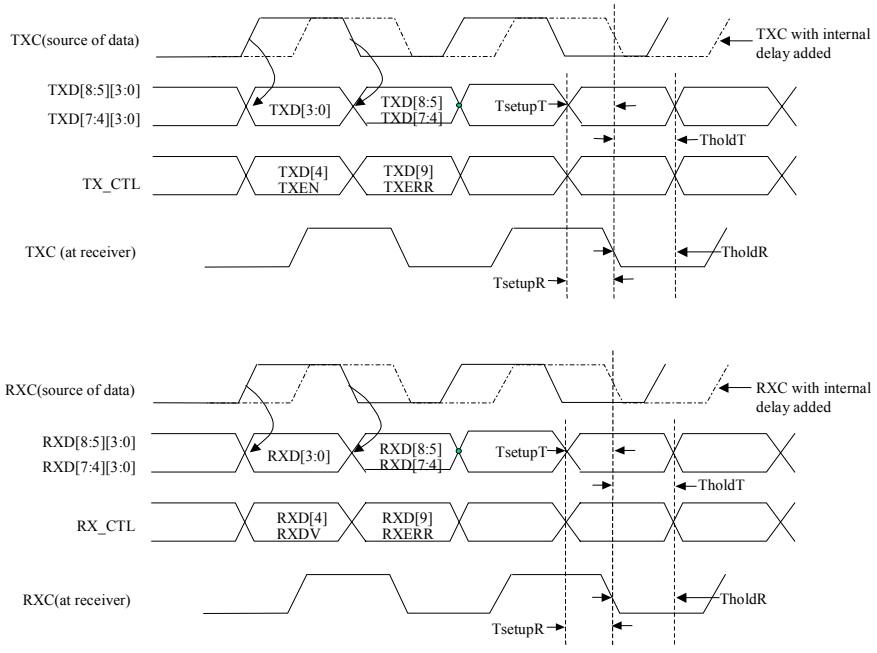

FIGURE 3 (Multiplexing & Timing Diagram – RGMII-ID)

3.3 Timing Specifics (Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2)

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation. This approach is being used to provide tighter control of skew. Duty Cycle values are defined in percentages of the nominal clock period so to make this table speed independent.

Symbol	Parameter	Min	Typical	Max	Units
TskewT	Data to Clock output Skew (at Transmitter) *note 1	-500	0	500	ps
TskewR	Data to Clock input Skew (at Receiver) *note 1	1	1.8	2.6	ns
TsetupT	Data to Clock output Setup (at Transmitter – integrated delay) *note 4	1.2	2.0		ns
TholdT	Clock to Data output Hold (at Transmitter – integrated delay) *note 4	1.2	2.0		ns
TsetupR	Data to Clock input setup Setup (at Receiver – integrated delay) *note 4	1.0	2.0		ns
TholdR	Data to Clock input setup Setup (at Receiver – integrated delay) *note 4	1.0	2.0		ns
Tcyc	Clock Cycle Duration *note 2	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit *note 3	45	50	55	%
Duty_T	Duty Cycle for 10/100T *note 3	40	50	60	%
Tr / Tf	Rise / Fall Time (20-80%)			.75	ns

note 1: For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. For 10/100 the Max value is unspecified.

note 2: For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.

note 3: Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Note 4: TsetupT / TholdT allows implementation of a delay on TXC or RXC inside the transmitter. Devices which implement internal delay shall be referred to as **RGMII-ID**. Devices may offer an option to operate with/without internal delay and still remain compliant with this spec.

TABLE 2

3.4 TXERR and RXERR Coding

To reduce power of this interface, TXERR and RXERR, will be encoded in a manner that minimizes transitions during normal network operation. This is done by the following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

TXERR <= GMII_TX_ER (XOR) GMII_TX_EN
RXERR <= GMII_RX_ER (XOR) GMII_RX_DV

When receiving a valid frame with no errors, RXDV=true is generated as a logic high on the ↑ edge of RXC and RXERR=false is generated as a logic high the ↓ edge of RXC. When no frame is being received, RXDV=false is generated as a logic low on the ↑ edge of RXC and RXERR=false is generated as a logic low on the ↓ edge of RXC.

When receiving a valid frame with errors, RXDV=true is generated as logic high on the ↑ edge of RXC and RXERR=true is generated as a logic low on the ↓ edge of RXC.

TXERR is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of TXC and during the period between frames where no errors are to be indicated, the signal stays low for both edges.

TX_CTL	GMII_TX_EN	GMII_TX_ER	TXD[7:0]	Description	PLS_DATA.request parameter
0,0	0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0,1	0	1	00 through 0E	Reserved —	
0,1	0	1	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	10 through 1E	Reserved —	
0,1	0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0,1	0	1	20 through FF	Reserved —	
1,1	1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1,0	1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD[7:0] column are in hexadecimal

TABLE 3 (Allowable Encoding of TXD, TXERR and TXEN)

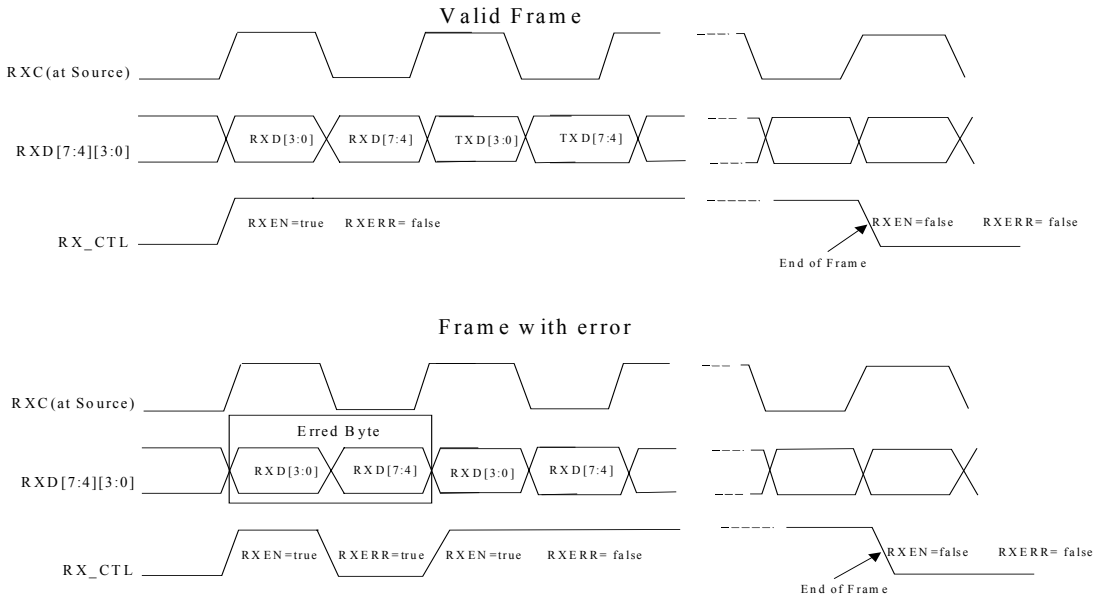

FIGURE 4

RX_CTL	GMII_RX_DV	GMII_RX_ER		RXD[7:0]	Description	PLS_DATA.indicate or PHY_ status parameter
0,0	0	0	#	xxx1 or xxx0	Normal inter-frame	Indicates link status 0=down, 1=up
0,0	0	0	#	x00x or x01x x10x or x11x	Normal inter-frame	Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved
0,0	0	0	#	1xxx or 0xxx	Normal inter-frame	Indicates duplex status 0=half-duplex, 1=full duplex
0,1	0	1	*	00	Reserved	—
0,1	0	1	*	01through 0D	Reserved	—
0,1	0	1	*	0E	False Carrier indication	False Carrier Present
0,1	0	1	*	0F	Carrier Extend	EXTEND (eight bits)
0,1	0	1	*	10 through 1E	Reserved	—
0,1	0	1	*	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0,1	0	1	*	20 through FE	Reserved	—
0,1	0	1	*	FF	Carrier Sense	PLS_Carrier.Indicate
1,1	1	0	*	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1,0	1	1	*	00 through FF	Data reception error	ZERO, ONE(eight bits)

* NOTE— (Required Function) Values in RXD[7:0] column are in hexadecimal.

\# NOTE— (Optional) Values in RXD[7:0] column are in binary; nibbles are repeated on ↑ edge and ↓ edge.

TABLE 4 (Allowable Encoding of RXD, RXDV and RXERR)

3.4.1 In-Band Status (Optional)

In order to ease detection of the link status, speed and duplex mode of the PHY, inter-frame signals will be placed onto the RXD[3:0] signals as indicated in table 4. The status of the PHY shall be indicated whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, or False Carrier are not present. When link status is down, PHY speed and duplex are defined by the PHY's internal setting.

3.4.2 In-Band Status (Required)

CRS is indicated by the case where RXDV is true, or the case where RXDV is false, RXERR is true, and a value of FF exists on the RXD[7:0] bits simultaneously or in the case where a Carrier Extend, Carrier Extend Error or False Carrier are occurring as defined in Table 4. Carrier Extend and Carrier Extend Error are applicable to Gigabit speeds only.

Collision is determined at the MAC by the assertion of TXEN being true while either CRS or RXDV are true. The PHY will not assert CRS as a result of TXEN being true.

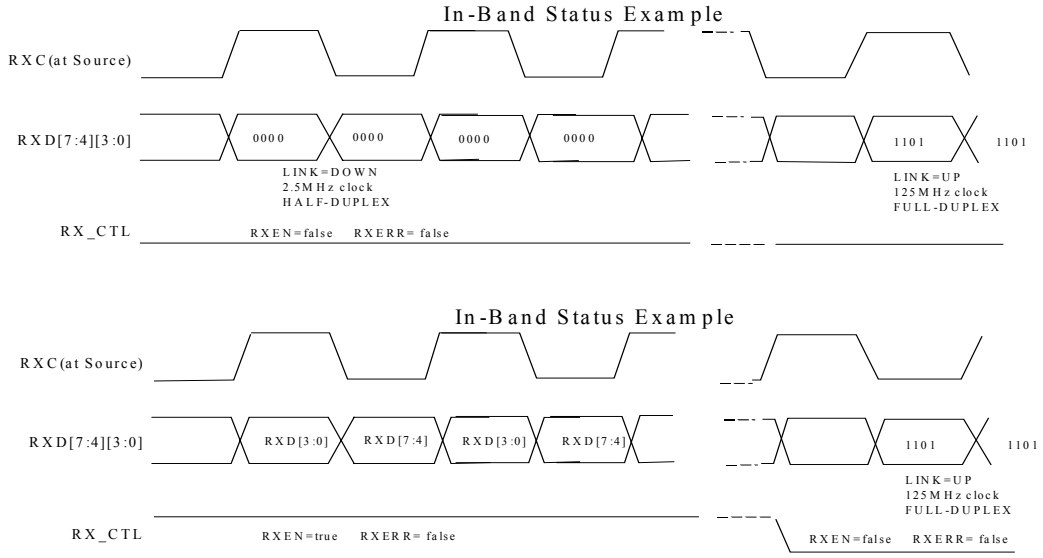

FIGURE 5

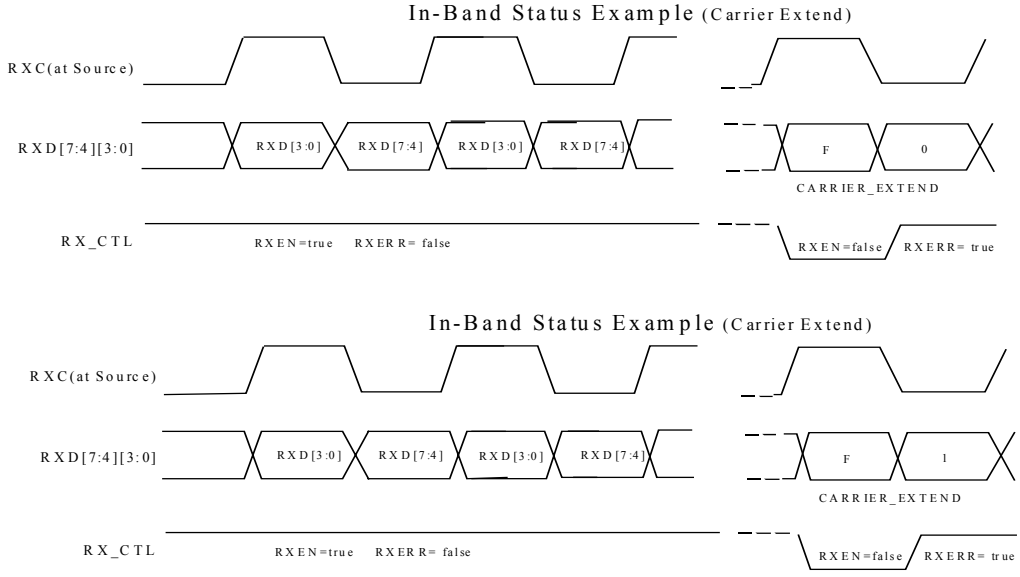

FIGURE 6

4.0 Electrical Characteristics

The RGMII and RTBI signals (including MDIO/MDC) will be based upon 1.5v HSTL interface voltages as defined by JEDEC EIA/JESD8-6. Please refer to that specification for details on the Class 1 drivers and receivers.

5.0 10/100 Functionality

This interface can be used to implement the 10/100 Mbps Ethernet Media Independent Interface (MII) by reducing the clock rate to 25MHz for 100Mbps operation and 2.5MHz for 10Mbps. The TXC will always be generated by the MAC and RXC will be generated by the PHY. During packet reception, the RXC may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data-synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks are allowed during speed transitions.

This interface will operate at 10 and 100Mbps speeds exactly the same way it does at Gigabit speed with the exception that the data may be duplicated on the ↓ edge of the appropriate clock.

The MAC will hold TX_CTL low until it has ensured that it is operating at the same speed as the PHY.

6.0 Mode Selection

The decision about which mode of operation this interface will use is left to the implementers. It may be done with hard-wired pins, or through register bits that are controlled by software.

7.0 Hewlett Packard Intellectual Property

The Hewlett-Packard Company has released its proprietary rights to information contained in this document for the express purpose of implementation of this specification to encourage others to adopt this interface as an industry standard. Any company wishing to use this specification may do so if they will in turn relinquish their proprietary rights to information contained or referenced herein. Any questions concerning this release should be directed to the Director of Intellectual Property, Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA.

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7.2 Disclaimer

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