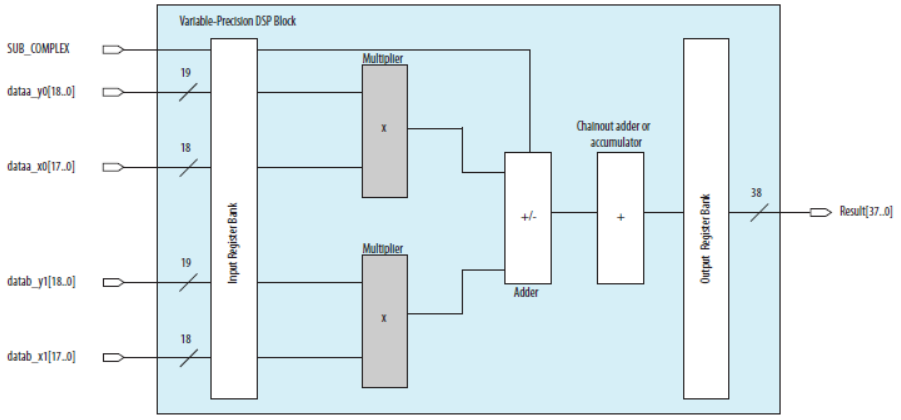
Hi all,

I am optimizing a filter that was made in a Cyclone V device. The current filter uses two DSP blocks for two multiplications; according to the Cyclone V device handbook, it should be possible to fit two independent multipliers in one DSP block. I tried to implement the multipliers by using the 'Multiply adder' intel FPGA which uses the 'altera_mult_add' module from the 'altera_lm' library. Unfortunately, it seems to implement the two multipliers in 'Multiplier Adder mode', this mode is shown in the figure below.

Multiplier Adder Sum Mode

Figure 3-11: One Sum of Two 18 x 19 Multipliers with One Variable Precision DSP Block for Cyclone V Devices



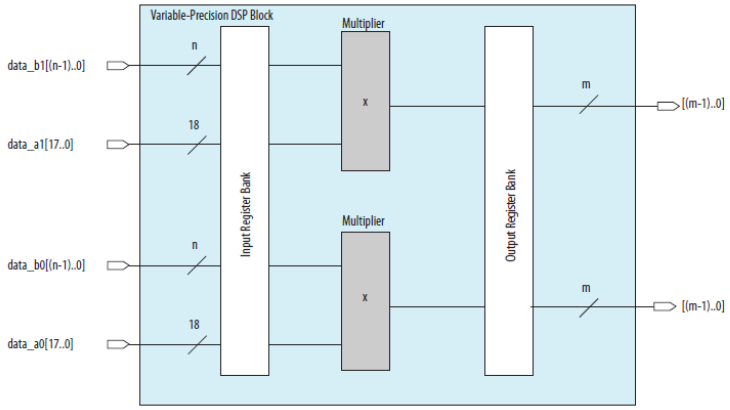
I would like to implement the two multipliers independently. However, I can't figure out how I can bypass the adder from the DSP block as shown in the next figure.

18 x 18 or 18 x 19 Independent Multiplier

Figure 3-5: Two 18 x 18 or 18 x 19 Independent Multiplier Mode per Variable Precision DSP Block for Cyclone V Devices

In this figure, the variables are defined as follows:

- n = 19 and m = 37 for 18 x 19 mode
- n = 18 and m = 36 for 18 x 18 mode



I would be very thankful if someone can give me a solution to this problem, I am working with the Intel FPGA lite 18.1 software.

Kind regards,

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