altera
An Intel Company

Date:
05/27/24

Addressed To:
Emma Jackson,
Renishaw PLC,
New Mills, Wotton-Under-Edge, GL12 8JR,
United Kingdom.

Dear Emma:

This letter is intended to clarify the memory types contained within the Cyclone® III FPGA devices, such as part number **EP3C40F484C8N**, and their level of volatility.

- **Logic Elements (LEs)**: These are the smallest units of logic in the Cyclone® III device family architecture. They are compact and provide advanced features with efficient usage. Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic. They are volatile, and their contents are completely erased when the power to the device is removed.
- **User logic (LAB)**: Logic array blocks (LABs) contain groups of LEs. The user logic is implemented using look-up-table memory blocks. This memory is volatile and the contents are completely erased when the power to the device is removed.
- **Device configuration memory**: This memory is on the die and holds the configuration bitstream that represents the user's design. This memory is volatile, and its contents are completely erased when the power to the device is removed.
- **User embedded memory (M9K)**: This memory addresses the on-chip memory needs of Cyclone® III device family designs. The embedded memory structure consists of columns of M9K memory blocks that can be configured to provide various memory functions. This memory is volatile, and its contents are completely erased when the power to the device is removed.
- **User registers**: These registers are on the die and are an optional resource available to the user for the user's design. They are volatile, and their contents are completely erased when the power to the device is removed.

Should you have additional questions or require more information, please do not hesitate to contact us.

Sincerely,

Alex Fong
Altera Product Marketing
Accelerating Innovators.

Address:
101 Innovation Dr
San Jose, CA 95134

Email:
yim.hui.fong@intel.com