EL302

DIGITAL INTEGRATED CIRCUITS

DESIGN PROJECT#3

CMOS Edge Triggered D flip-flip with

asynchronous SET and RESET

TOLGA DİNÇ

9303

1. INTRODUCTION

1.1. Design Specifications: In this project we are required to perform the schematic and layout design of a CMOS positive (rising) edge triggered master-slave type D flip-flop with a low-asserted asynchronous set and reset using AMS 0.35 μm CMOS technology according to the following criteria:

- Clock signal parameters: trise = tfall = 100 ps, duty cycle = 50 % and fclk(min) = 1 GHz.
- Output load 50 fF.
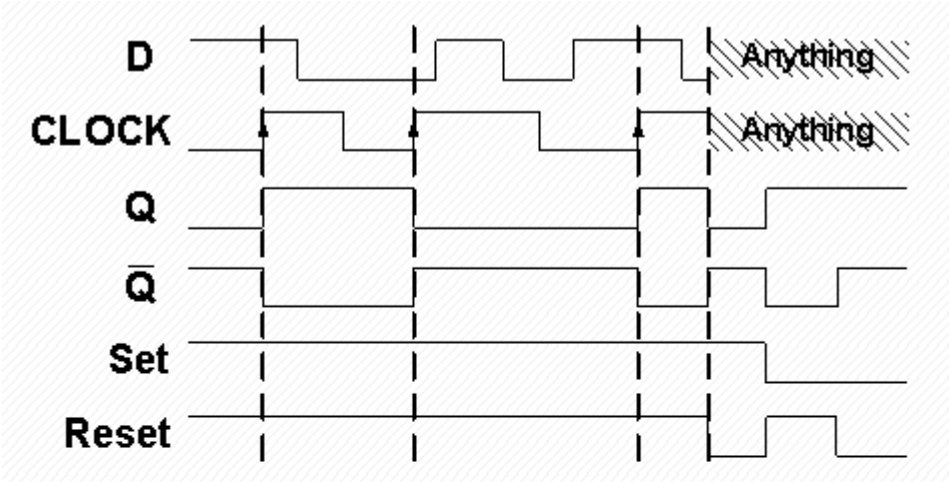- Standard cell layout.

1.2. Basics of Flip-Flops:

Flip-flops are synchronous bistable regenerative device which operate as memory elements to store one bit of information. Also, flip-flops can be referred as non-transparent(edge-triggered) components of sequential systems which are designed to prevent uncontrolled oscillation of output of transparent memory components(latches).They are mostly used as basic building blocks of counters, registers, and memories.

Basic flip-flops are composed of two cascaded latch stages that are activated with opposite clock levels. These configuration is called as master-slave flip-flop. Operation of commonly used D master-slave flip-flop which will be implemented in this assignment can be depicted as follow:

- Master is activated when the clock is low: In this phase, first stage follows the D input while second stage holds its previous value.
- When there is a clock transition from 0 to 1, first latch(master) stops sampling D input and stores the D value just before clock transition. During this time, second latch is transparent and thus output of master latch is transferred to output of slave latch.
- When there is a clock transition from 1 to 0, first stage starts sampling and second stage is non-transparent again.

The circuit depicted above is a positive edge-triggered D flip-flop since it samples the input at the rising edge of the clock(timing diagram and truth table of a D flip flop with low

asserted Set and Reset is shown in Fig.1). Also, as seen, master and slave stages are decoupled from each other so that inputs are never reflected directly to the outputs.

SET	RESET	D	CK	Q	Q̄
0	1	-	-	1	0
1	0	-	-	0	1
0	0	-	-	1	1
1	1	1	⌐	1	0
1	1	0	⌐	0	1

Figure 1: Timing Diagram of a Positive-Edge-Triggered D Flip-flop with low asserted Set and Reset and D Flip-flop Truth-Table.

1.3. D-Flip-Flop Topologies

A simple D Flip-Flop can be built by cascading two D latches as shown in Fig2. However, as seen in logic diagram, this implementation requires 4 AND2 gates and 4 NOR2 gates as well as 2 inverters. Therefore, layout of Dflip-flop purely made of CMOS gates covers relatively big chip area. This drawback leads us to search for other topologies with small area consumption rather than topologies consist of purely CMOS gates.
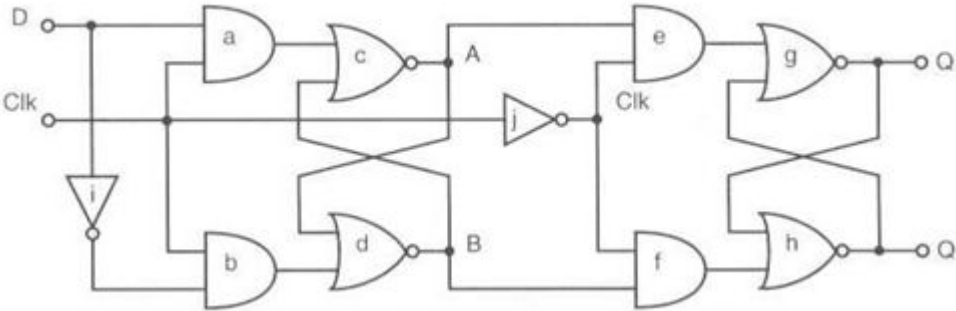

Figure 2: Logic Diagram of a master-slave D flip-flop

As it known, implementation of CMOS transmission gates in digital circuit design, results in compact circuit structures which usually require smaller number of transistors than standart CMOS implementations. Therefore, it would be reasonable to research for topologies which include transmission gates to control signal flow. One topology for D flip flop using transmission gates is shown in Fig.3.
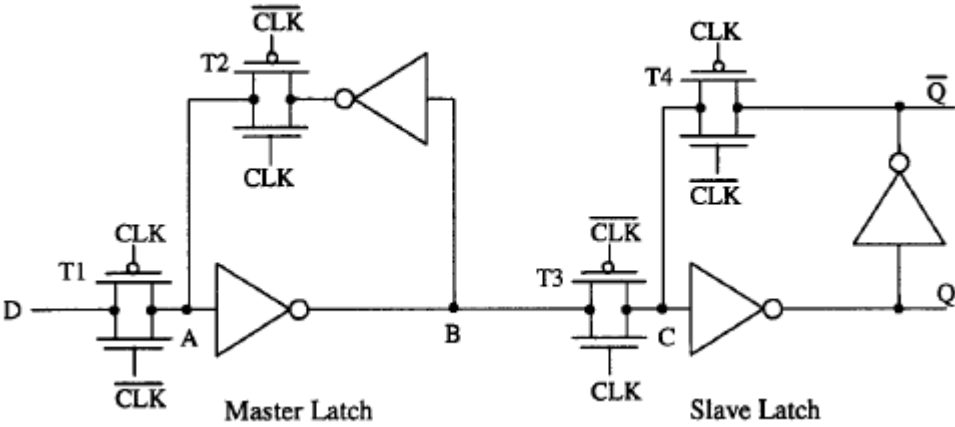

Figure 3:Implementation of positive-edge triggered D flip flop using transmission gates.

In the configuration shown in Fig.3, when the CLK is low, the logic value at D is setting at node A and invert of D is on node B. Transmission gates T2 and T3 are off. The data on node C is available on the output of the FF and is the result of the previous leading edge transition of the CLK input pulse. When CLK goes high, T1 and T4 turn off, while T2 and T3 turn on and the data on node is C is transferred, with the appropriate inversion to the outputs. In order to add set and reset feature to D flip-flop shown in Fig.3, inverters can be replaced by NOR2 or NAND2 gates with appropriate inputs. D flip flop with low asserted set and reset using NOR2 gates are shown in Fig.4.
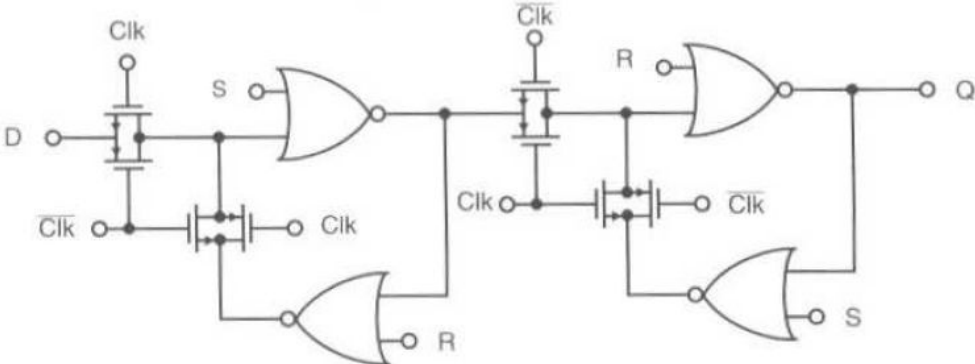

Figure 4:Master-slave D flip-flop using NOR2 and transmission gates

Low to high and high to low propogation delay of NOR2 gate built in previous assignment was worse than the propogation delays of NAND2 gate. Also NOR2 gate was more compact compared to NAND2 gate although total area covered by each was equal. Therefore routing in D flip flop using NOR2 gates is more complicated and propogation delay is expected to be worse than D flip flop using NAND2 gates. Hence, it is reasonable to chose topology with NAND2 shown in Fig5 in order to implement.
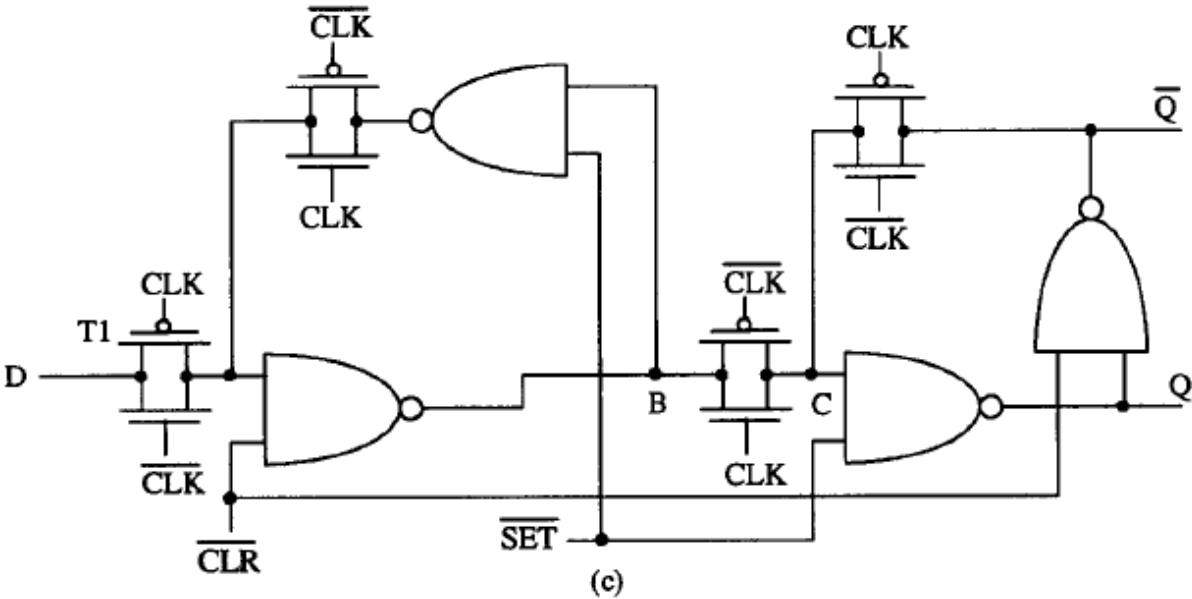

Figure 5: Positive edge triggered D flip flop with low asserted set and clear (using NAND2 gates).

Another topology for D flip flop with asynchronous set and reset is shown in Fig.6. This topology suggested as one of the best topologies in order to add standard cell library by K.Martin. However as seen in Fig.6, it requires more transistors than the topology with NAND2 gates. Also its layout design process is a bit complicated since we are required to connect body of D transistor into input of inverter.
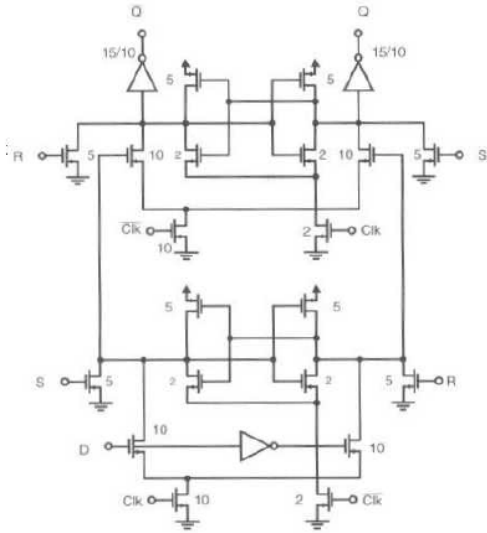

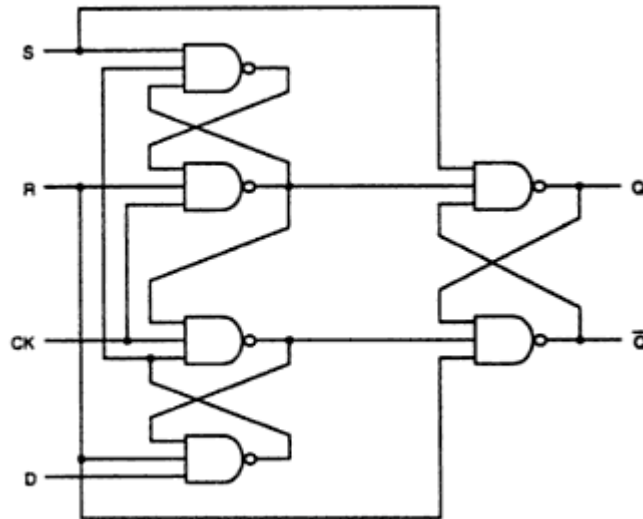Figure 6: Inverter based D flip flop with asynchronous set and reset.

Figure 7:NAN3 based positive edge triggered D flip-flop circuit.

Another implementation of edge-triggered D flip-flop is shown in Fig.7, which consists of six NAND3 gates. Area covered by this topology is larger than all topologies represented so far since it requires 36 transistors.

2. SCHEMATIC AND LAYOUT DESIGN

2.1.Schematic View and Layout

The circuit shown in Fig.5, positive edge triggered D flip flop using NAND2 gates and transmission gates, is built. The NAND2 gate built in previous lab assignment will be used in this circuit. This topology is chosen since propagation delay of NAND2 gates were better than NOR2 gates in previous lab and also routing is relatively simple compared to other topologies. Also it covers relatively small area than some of the topologies shown (eg, circuit in Fig7). Schematic of D flip flop based on the topology shown in Fig5, is shown in Fig8. Widths of pmos transistors in transmission gates are arranged as 2.7um so that their size equal with the pmos transistors used to build NAND2 gate in previous lab. Similarly widths of nmos transistors chosen to be equal with dimensions in NAND2 so that Wn=3.05um.
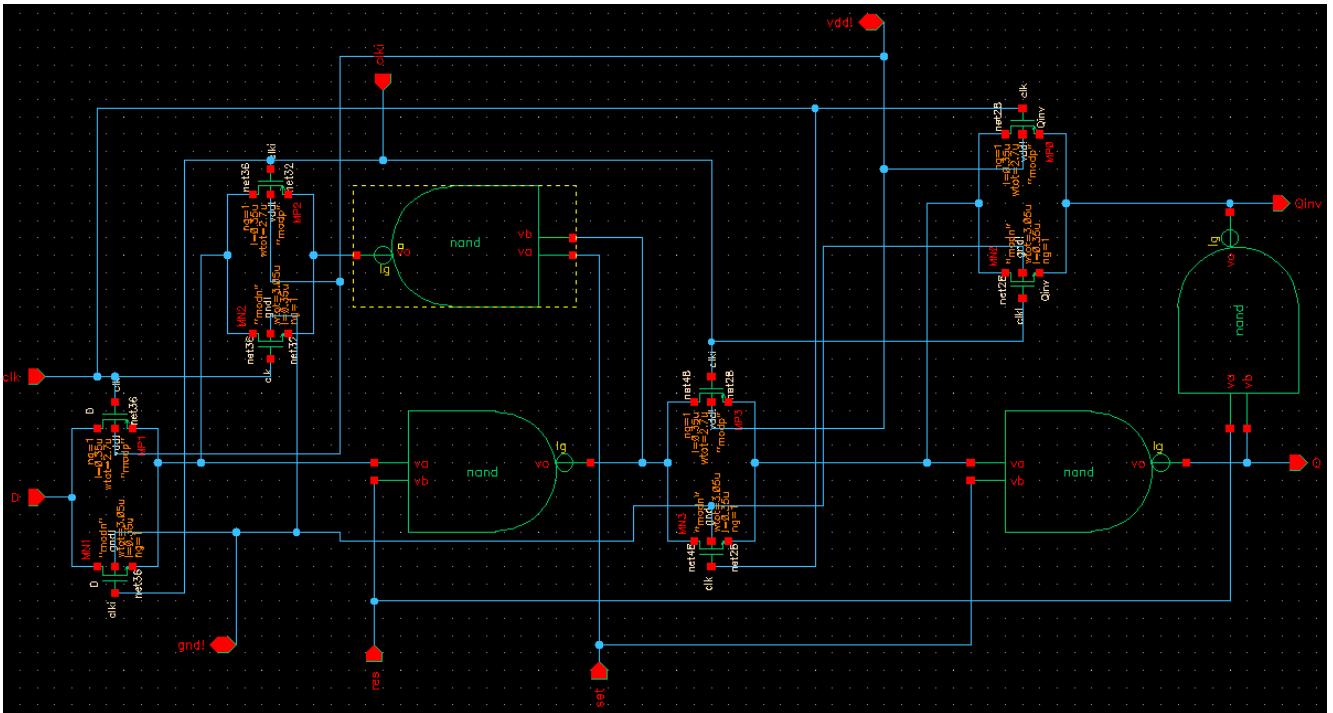
Figure 8: The Schematic view of positive edge triggered D flip flop with low asserted set and reset
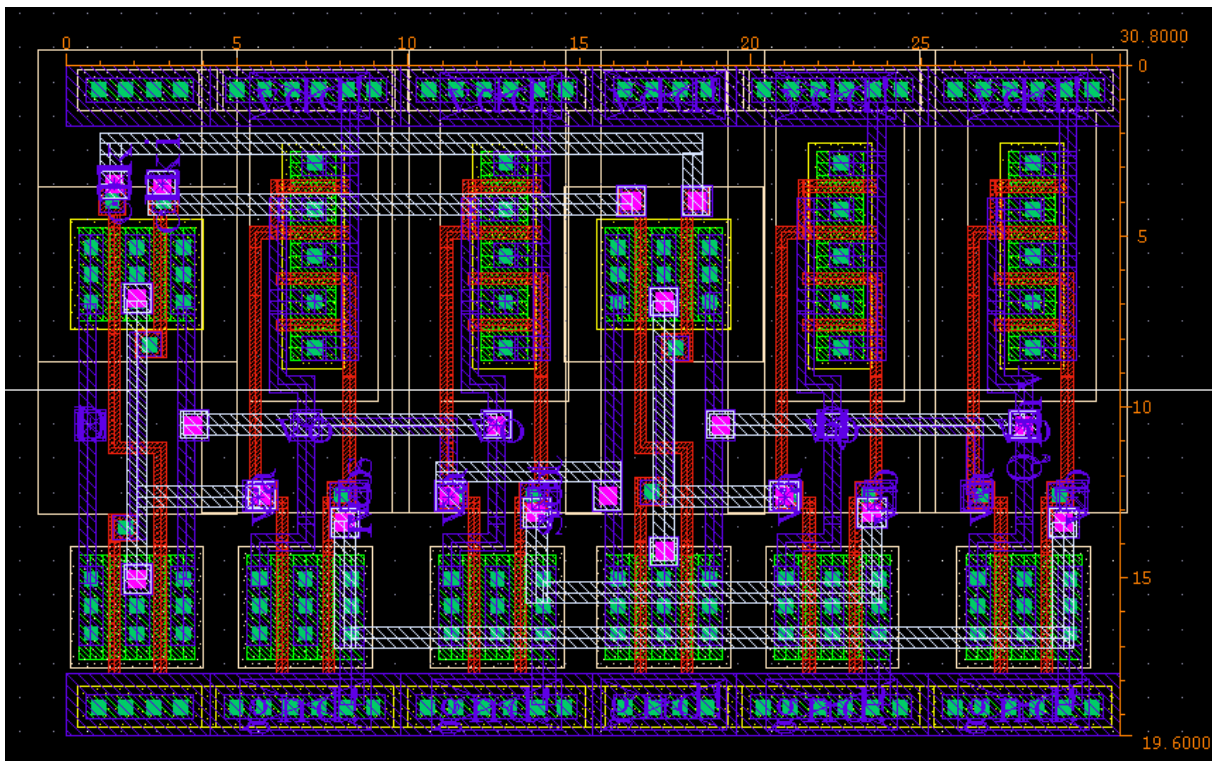

Figure 9: Layout of positive edge triggered D flip flop with low asserted set and reset.

As seen in Fig.9, source and drain sharing method between neighbor transmission gates are

utilized in order to decrease the area covered by circuit. However, it complicated the routing

of interconnections so that using of met2 lines was inevitable. Area covered by circuit is 30.8x19.6 $um^2=603um^2$.
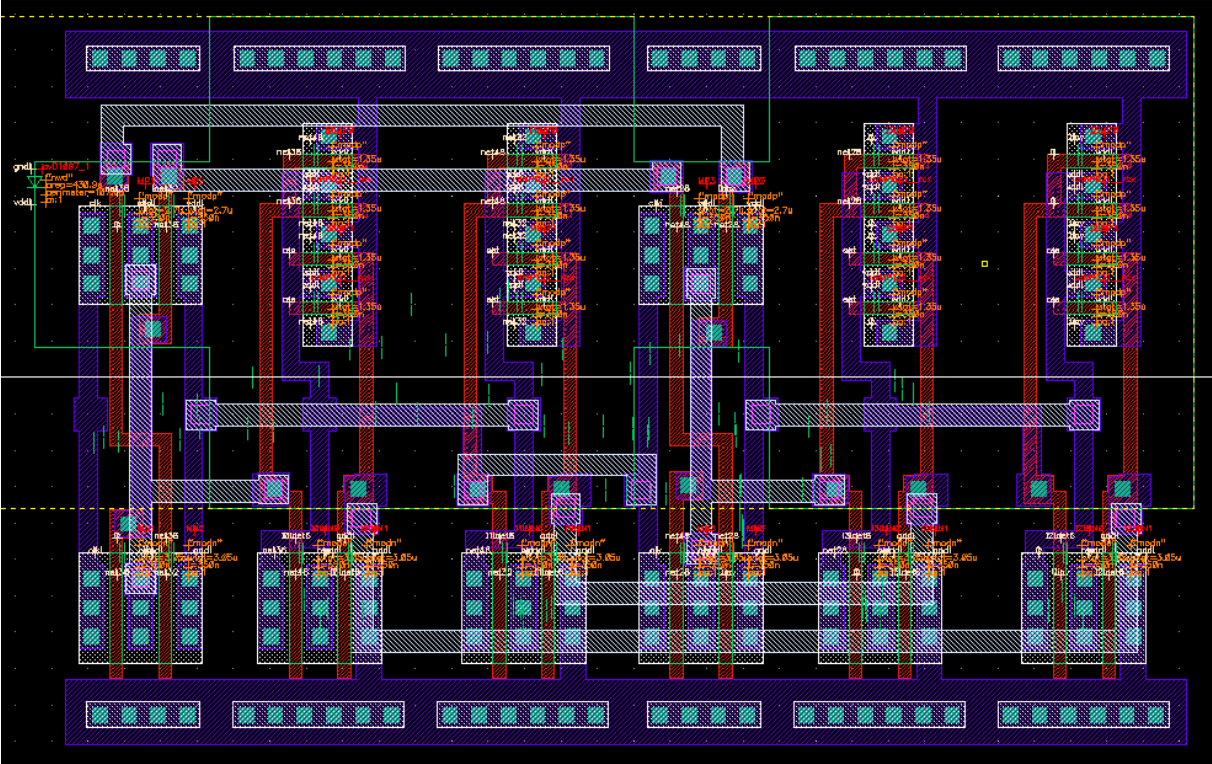

Figure 10: Extracted view of layout of D flips flop

As seen in Fig.10, extracted view of layout involves some parasitic capacitances mainly located around intersections between met1, met2 and poly interconnects. 81 parasitic capacitances formed and value of most of them is in atto scales. Larges parasitic capacitance is 3.696fF. We expect a variaton in dynamic response of D flip flop because of these parasitic capacitances.
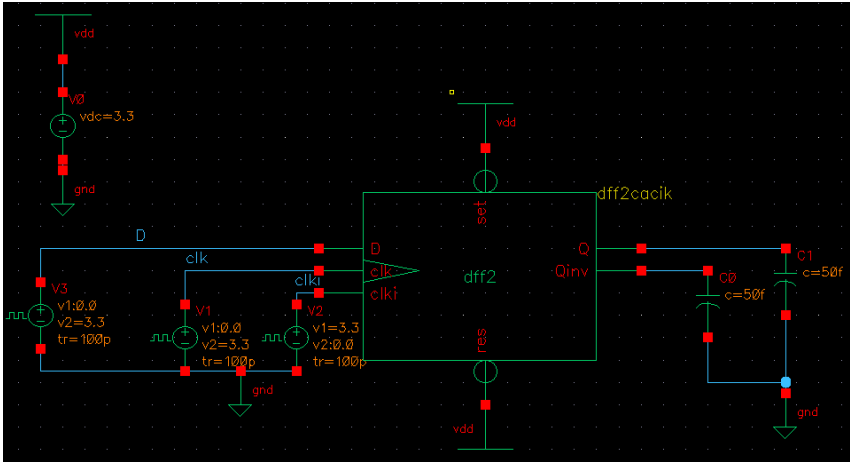

Figure 11: Symbol of D flip-flop with low asserted set and reset

Circuit used for simulation is shown in Fig.11. In the figure asynchronous set and reset signals is set to VDD level so that transmission of D input to Q output can be tracked. In order to reset flip flop we need to connect reset to ground while set is connected to VDD. Similarly in order to set flip flop, Set input should be in gnd level whereas reset input is connected to VDD. Therefore, we can connect pulse signals with different phases to set and reset inputs in order to observe whether set and reset works or not.

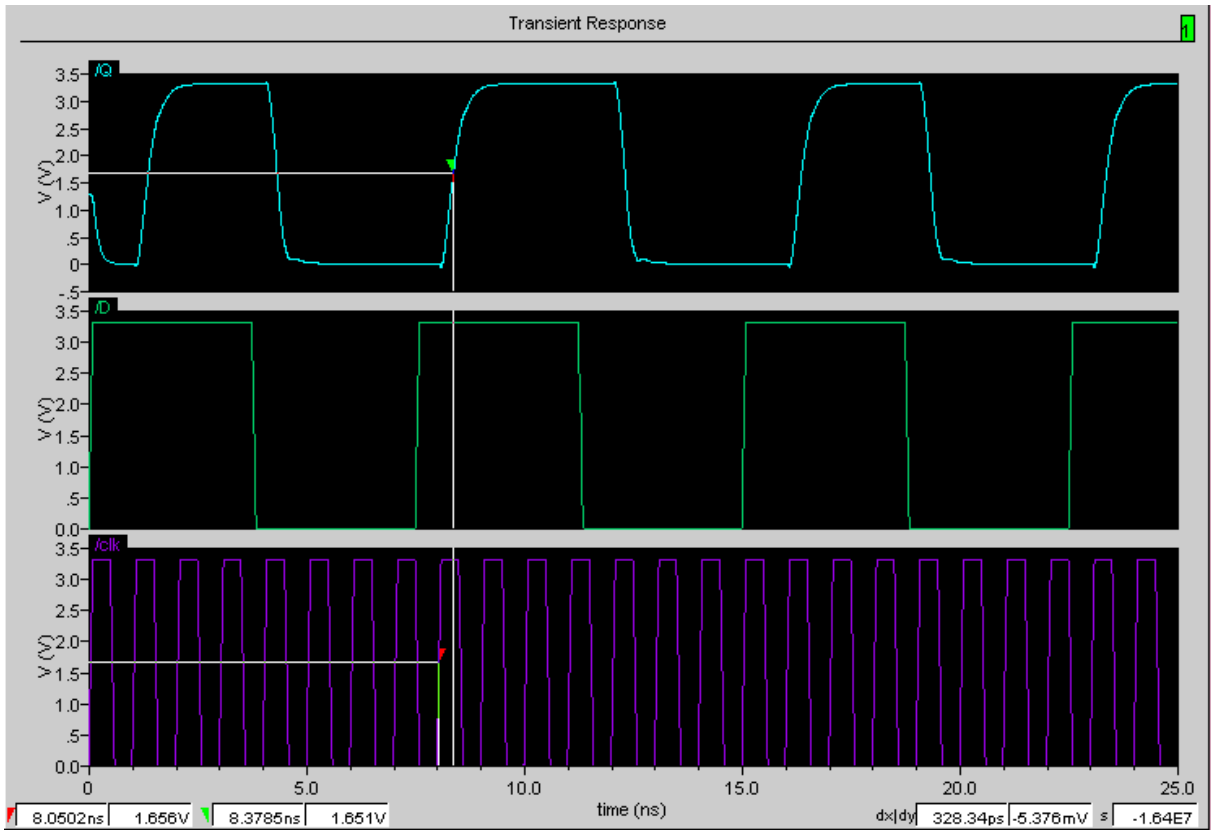## 2.2. Simulation Results in Schematic Level

Figure 12: Low-to-High Time Delay of D flip-flop.

As seen in Fig.12, low to high propagation delay of D flip flop in schematic level is 328.34ps. In order to measure it, pulse signal with 7.5ns period is applied to D input of flip flop so that D input and clock signal out of phase (don't start to rise or fall at the same time). Also during this measurement both of set and reset connected to VDD.

Figure 13: High-to-low Time Delay of D flip-flop.
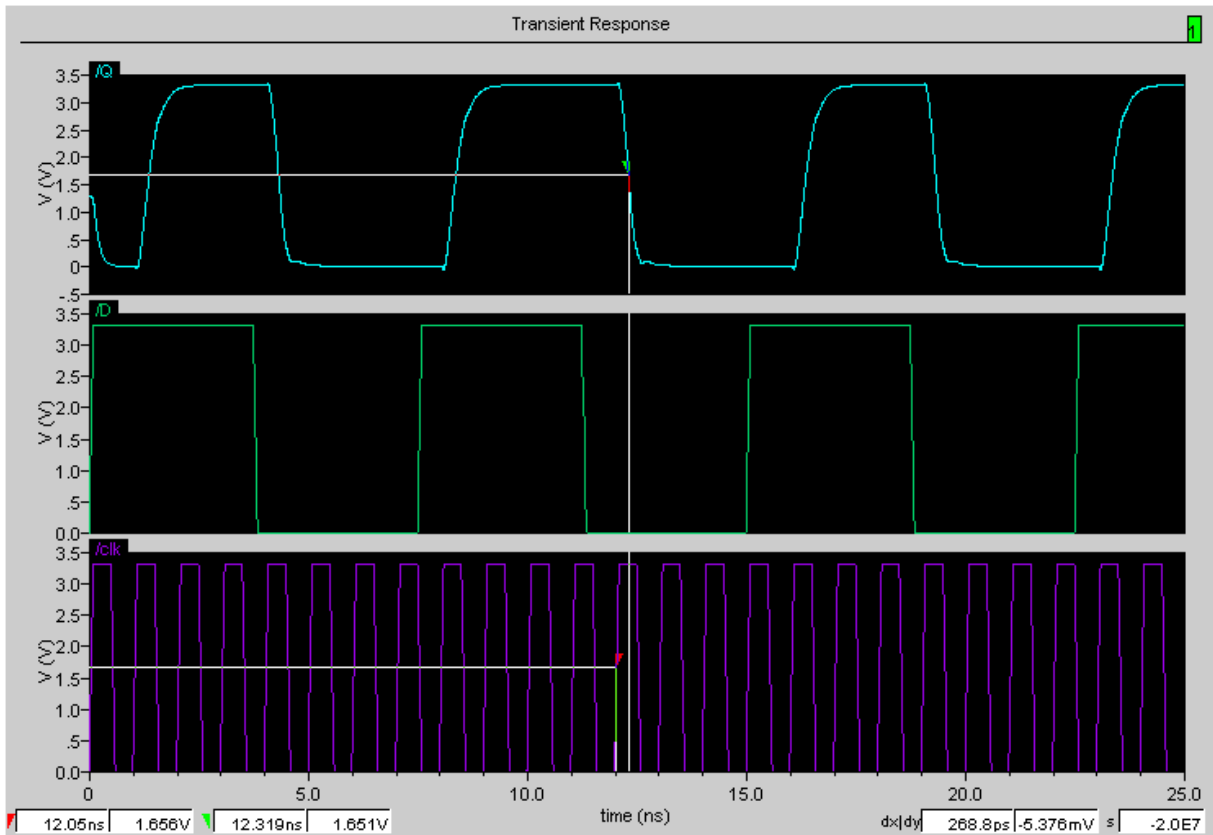
As shown in Fig. 13, high-to-low propagation delay of D flip flop is 268.8ps which is better than low-to-high propagation delay.

Figure 14: Rise time of the output of D flip-flop.
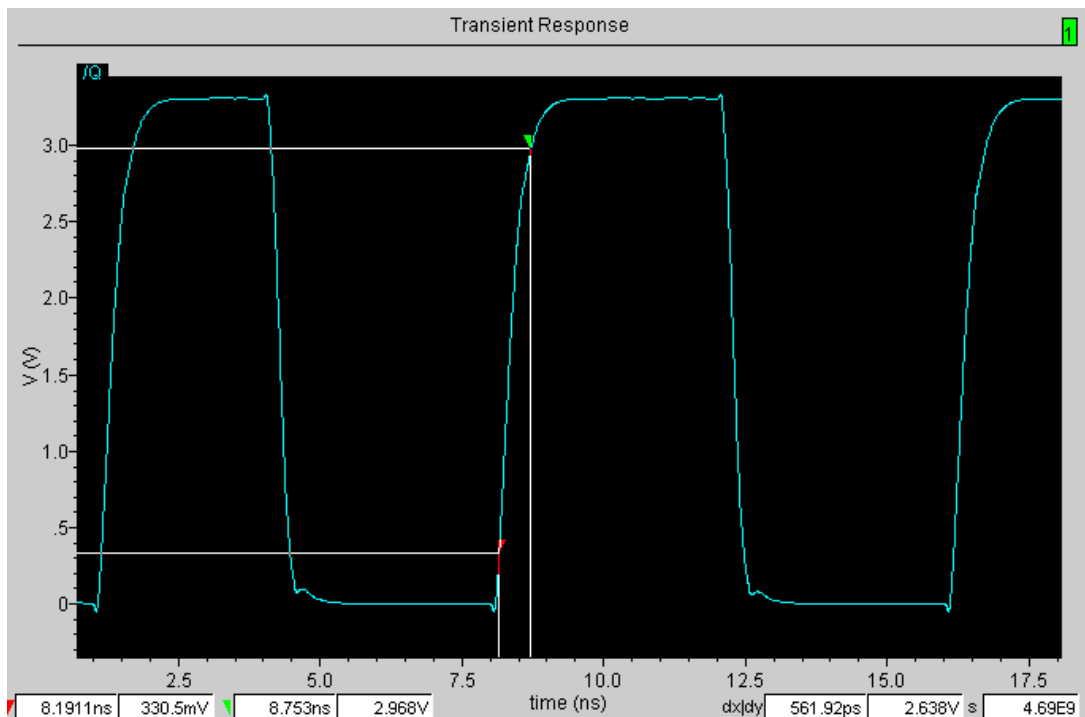
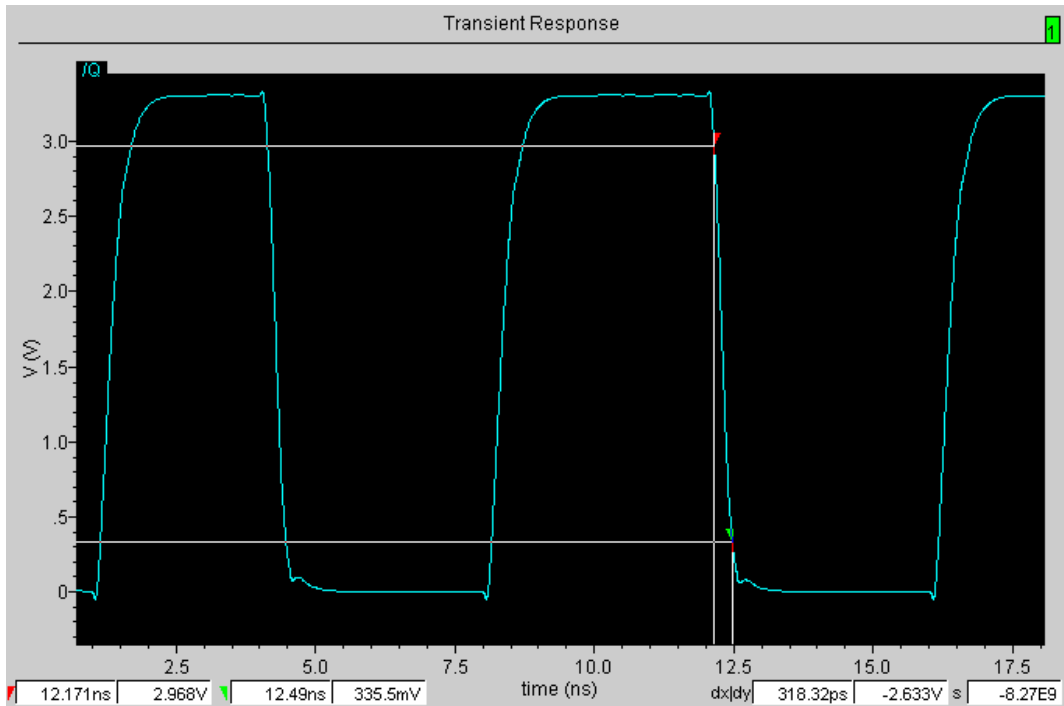As shown in Fig.14, rise time of output is 561.92ps.

Figure 15: Fall time of the output of D flip-flop.

As shown in Fig.15, fall time of output is 318.32ps which is better than rise time of output. The rise time can be defined as the time required for the output voltage to rise from V10% level to V90% level. Similarly, fall time is defined as the time required for output voltage to drop from V90% level to V10% level. V%10=330mV , V%90=2.97V. Measurements in Fig 14 and 15 is done according to this fact.

Circuit used to observe functionality of SET and RESET inputs is as below.
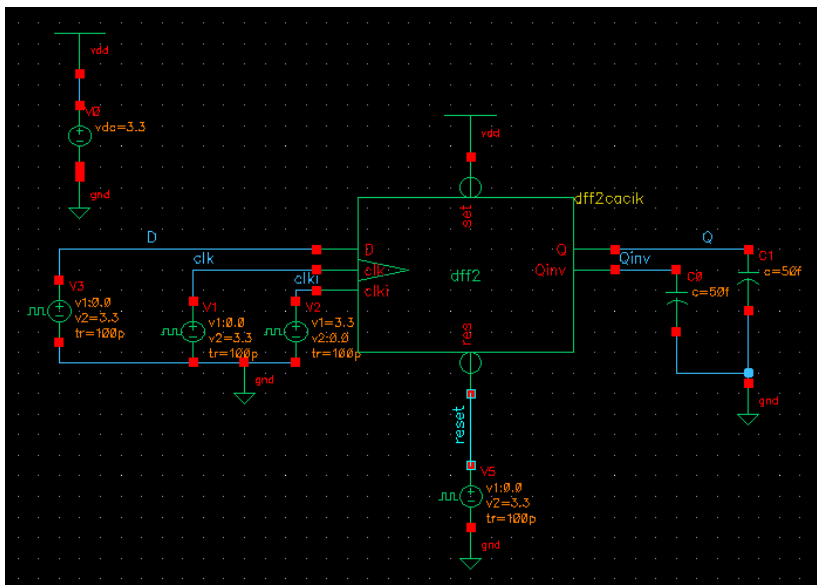

Figure 16: Circuit used to examine functionality of set and reset inputs.

As seen, Set input connected to VDD while a pulse signal is given to reset input in order to examine reset functionality.
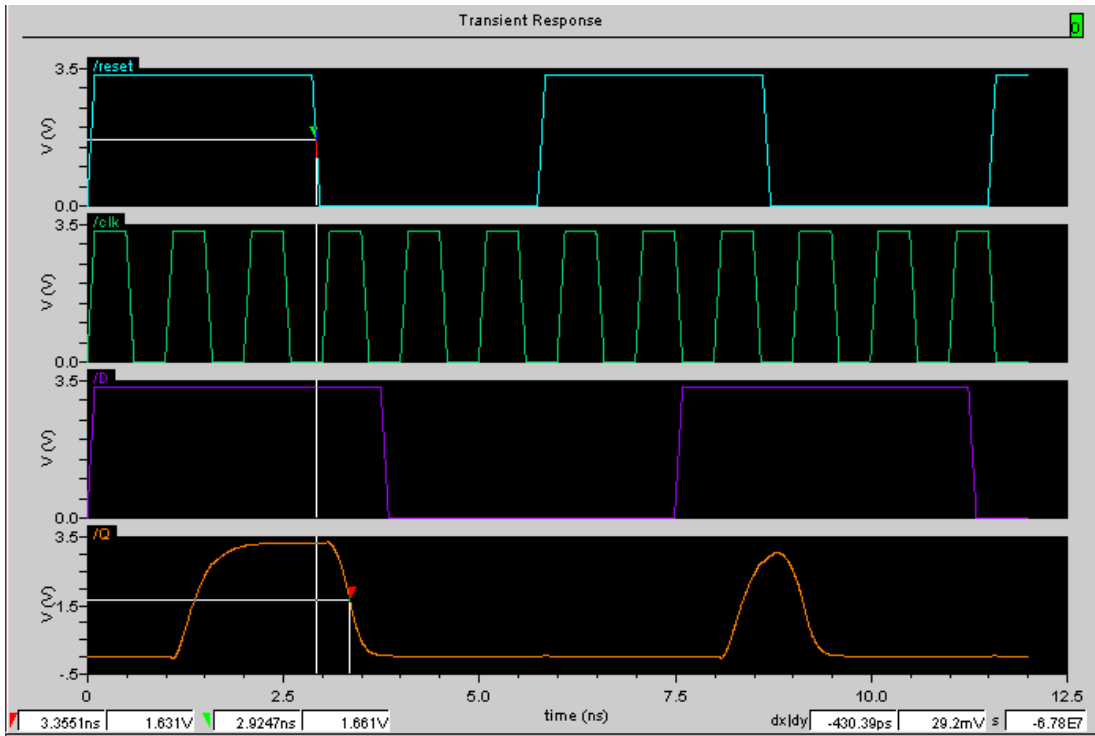
Figure 17: Functionality of Reset input.

As seen in Fig17, reset inputs functions properly: when reset input becomes low, output Q of flip flop starts to drop from VDD to 0 as independent of clock level. However, this transition is not instant and there is delay between reset signal and output. The asynchronous Reset delay is around 430ps as seen in graph.
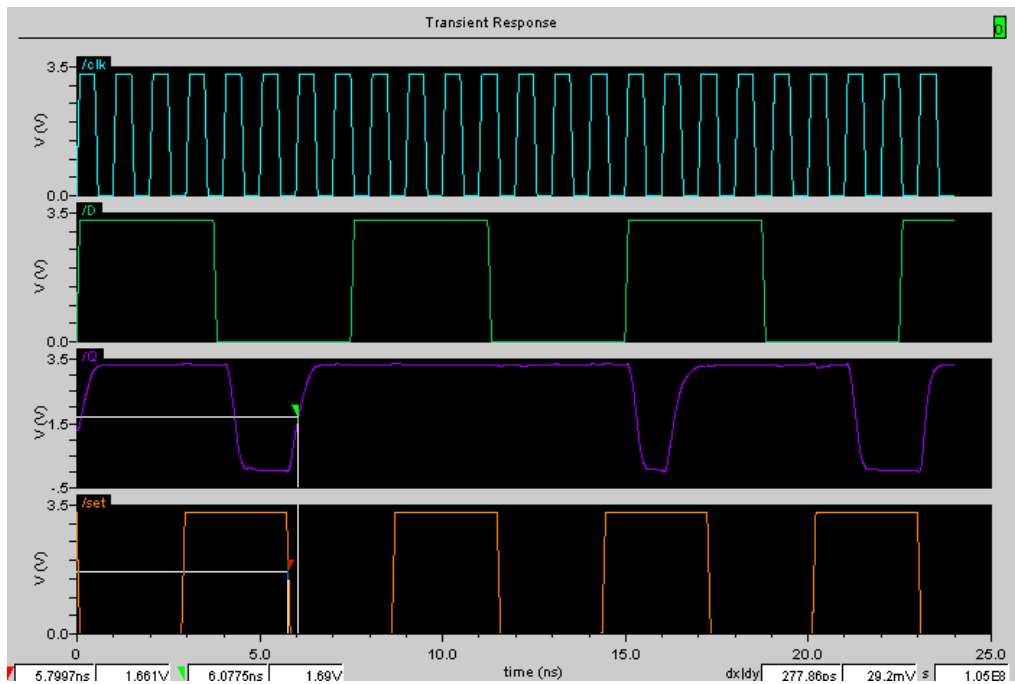

Figure 17: Functionality of Set input.

As seen in Fig17, similar to reset input, set input functions properly too: when set input becomes low, output Q of flip flop starts to rise from 0 to VDD as independent of clock level. The asynchronous Set delay is around 277.8ps. This value is reasonable since it is so close to propagation delay of NAND2 measured in previous lab. As seen in Fig.5, output Q can be set to 1 with propagation of set signal through a NAND2 gate.
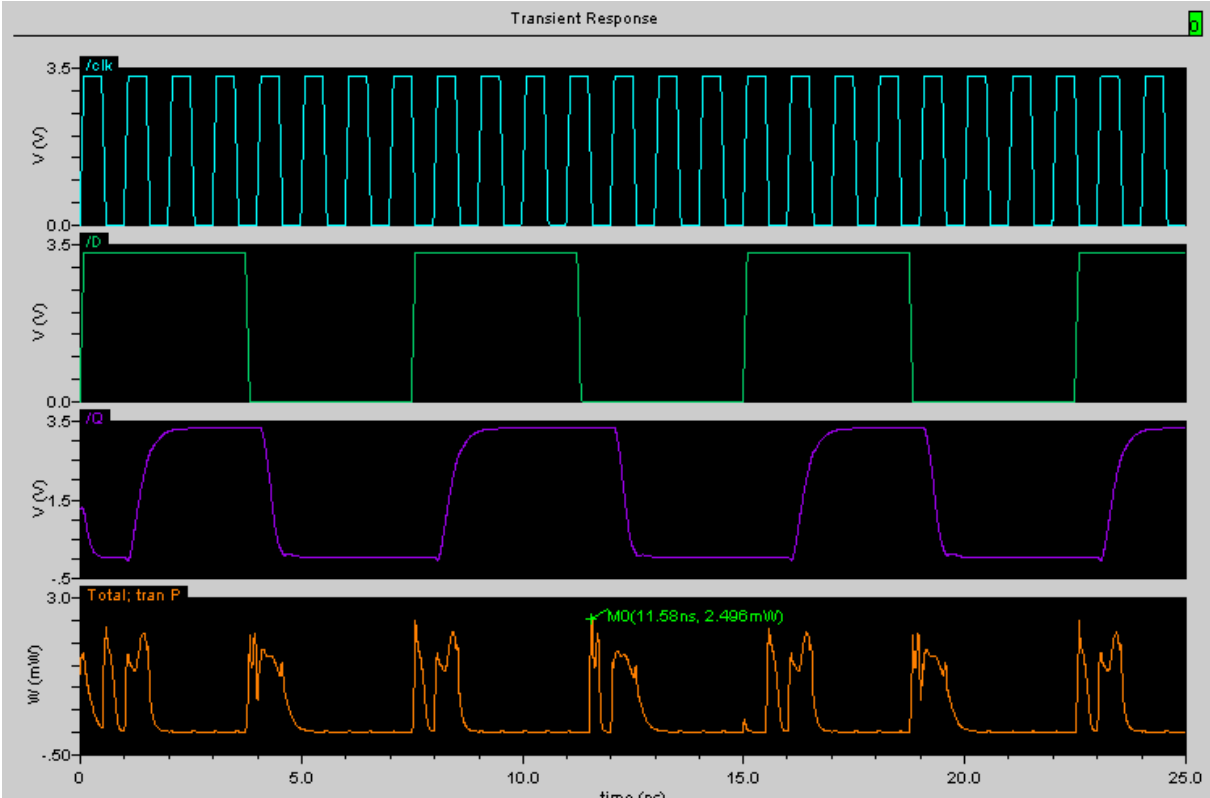

Figure 18: Total power dissipation of D flip flop.

As seen in Fig.18, most of the power is dissipated when output makes a transition at clock edges. Maximum instantaneous power dissipation is 2.496mW and root mean square of total power dissipated is 0.8mW.

Rise and fall time of output can be decreased to around 130ps by using 2 cascaded inverter at the Q and Q invert outputs as shown in Fig.19. However, by doing this, circuit's area will

increase by 4x Inverter Area (4x4.2x19.6um^2). Also, if we add this inverters propogation delay of flip flop will increase because of propagation delays of inverters.
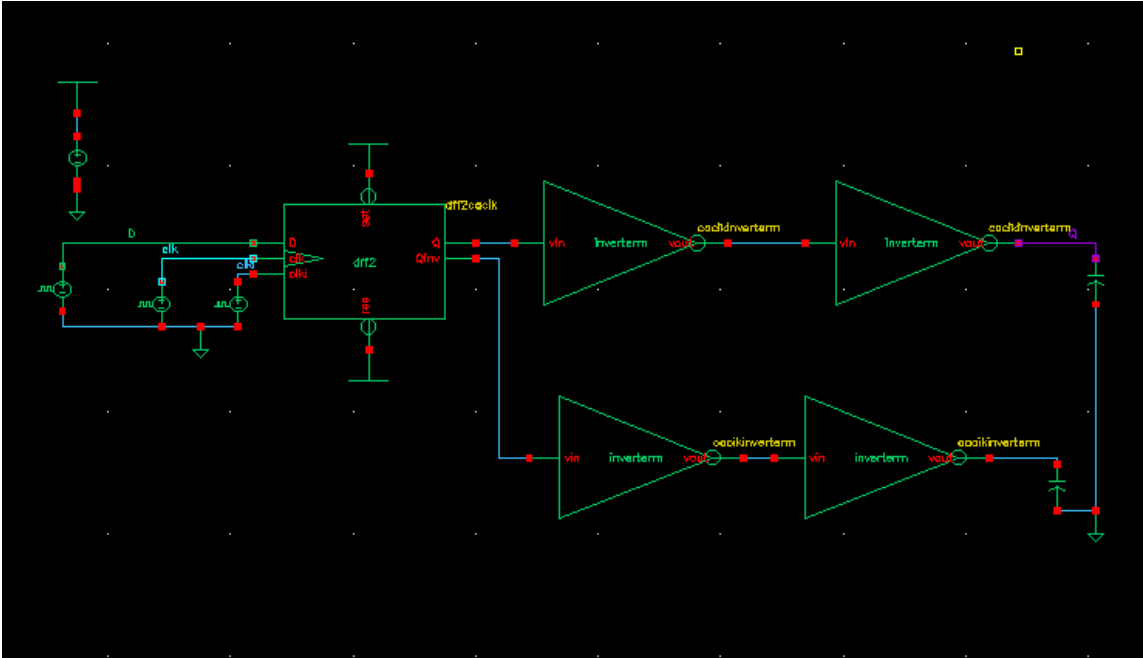

Figure 19: D flip flop design with additional inverters at output stage to decrease fall and rise times.

In addition, power dissipation of circuit shown in Fig.19 is around 8.5mw, which is nearly10times of previous value. The drawbacks of this circuit will be more than improvements. Another way to improve performance of D flip flop would be design new NAND2 gates with greater driving strengths and better propagation delays. However this would require designing each component in our standard cell library again in order to get components with same Ntube legth. Therefore I decided on continuing to layout process with D flip flop without inverters at output stage although its rise and fall times are a bit high.

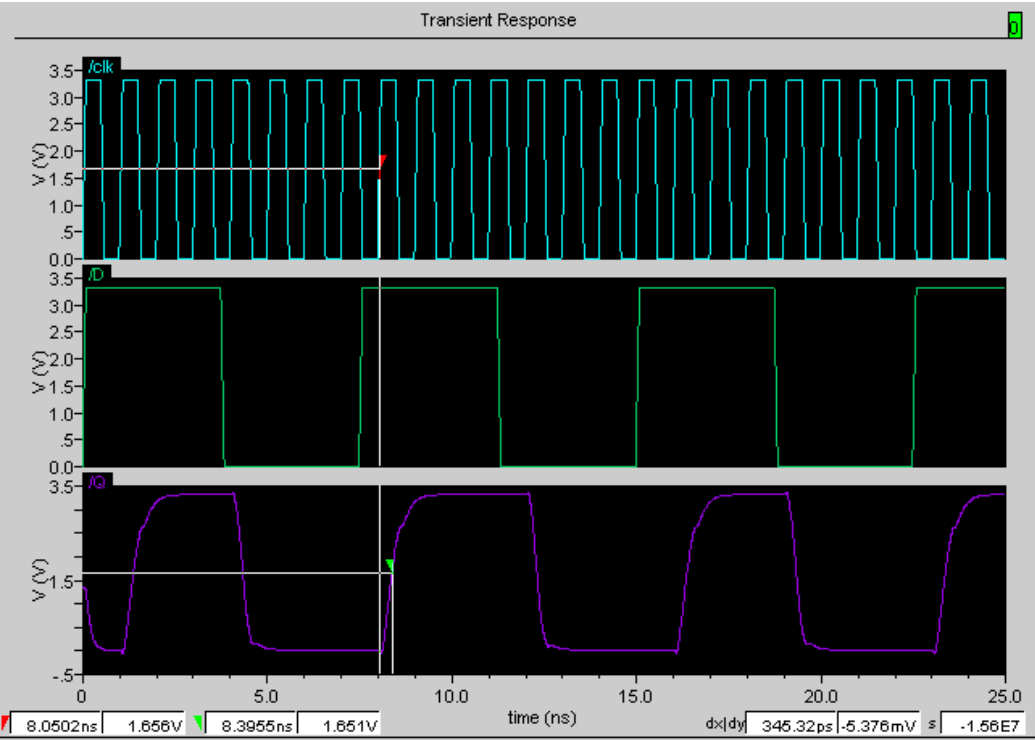## 2.3. Post Layout Simulation Results

Figure 20: Low-to-High Time Delay of D flip-flop in post layout.

As seen in Fig.20, low to high propagation delay of D flip flop in post layout is 345.32ps. Low to high propagation delay increased by 17ps in postlayout due to parasitic capacitances formed around intersection of between met1, met2 or poly interconnections.
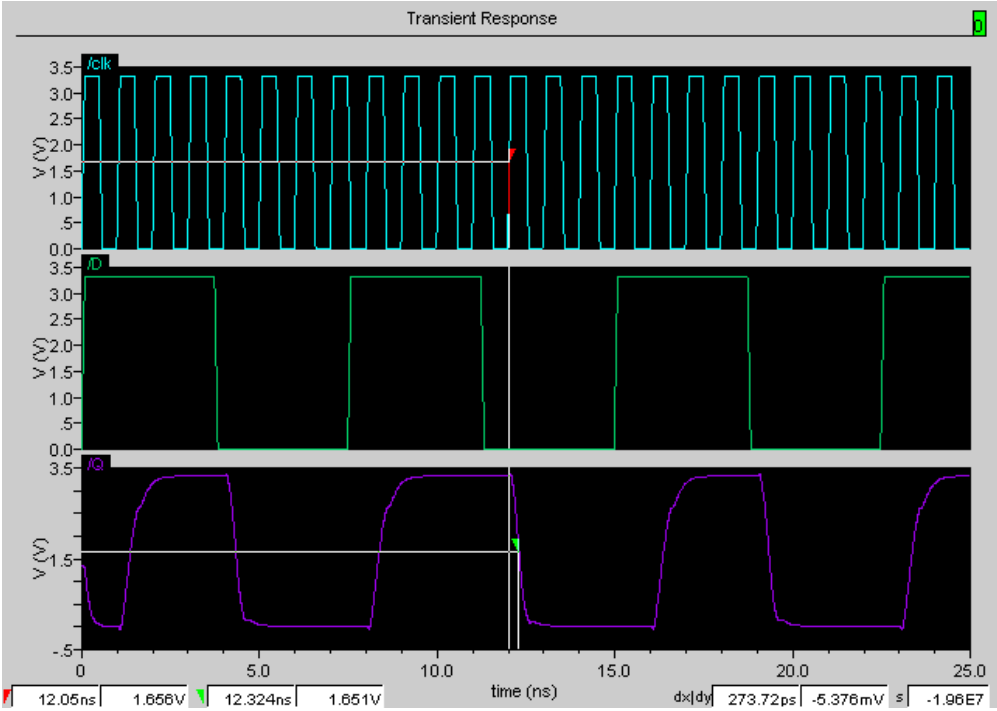

Figure 21: High-to-low Time Delay of D flip-flop in post layout.

As shown in Fig. 21, high-to-low propagation delay of D flip flop is 273.72ps. High to low propagation delay in post layout is bigger than schematic by 5ps due to effect of extracted capacitances.
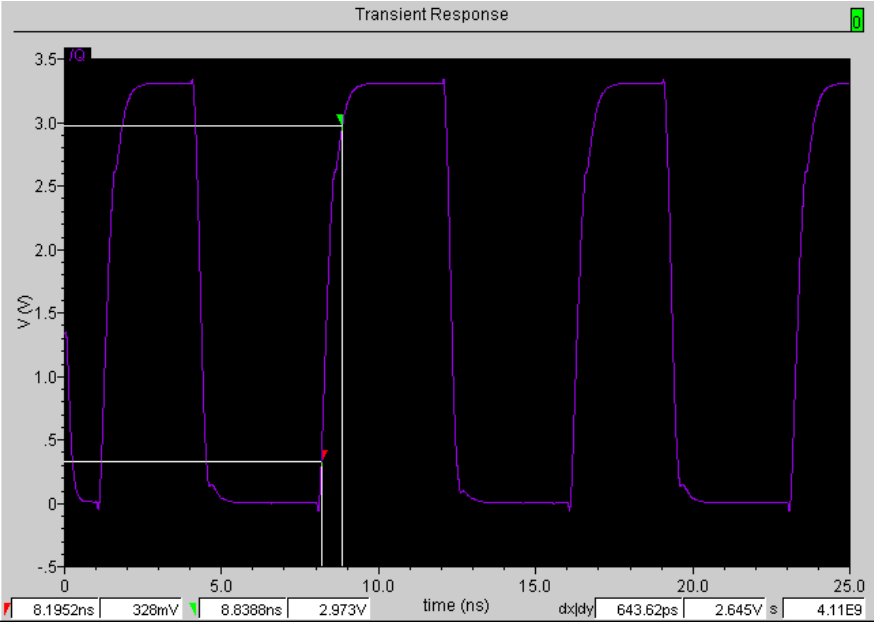

Figure 22: Rise time of the output of D flip-flop in post layout.

As shown in Fig.22, rise time of output is 643.62ps in post layout. This value is 82ps bigger than the value in schematic level simulations. Total capacitance is increased by effect of parasitic capacitances thus rise time of flip flop which is closely related to total capacitance need to be charged up increased.
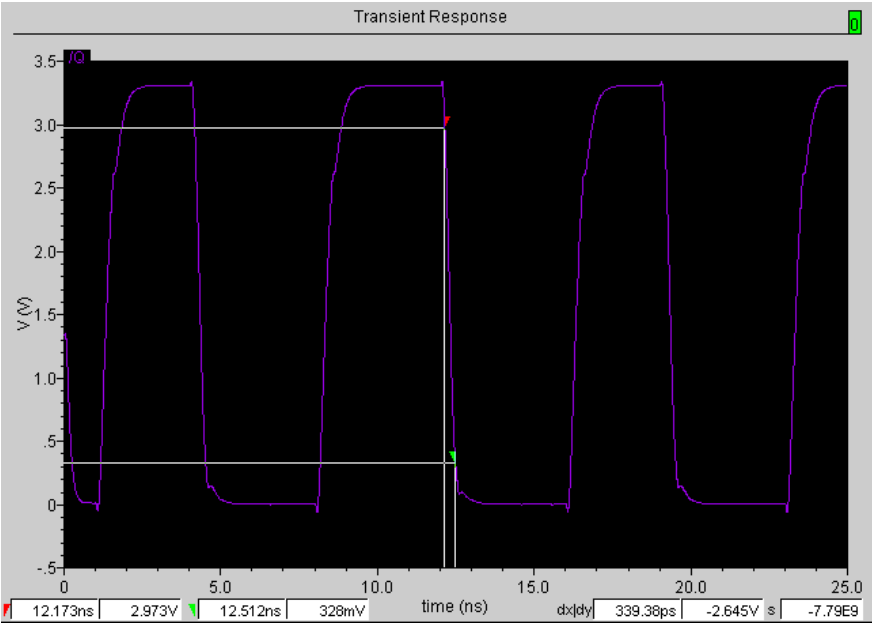

Figure 22: Fall time of the output of D flip-flop in post layout.

As shown in Fig.22, fall time of output is 339.38ps in post layout. This value is 21ps bigger than the value in schematic level simulations due to role of parasitic capacitances. Discrepancy between layout and schematic's fall times is lower than rise time's deviation.
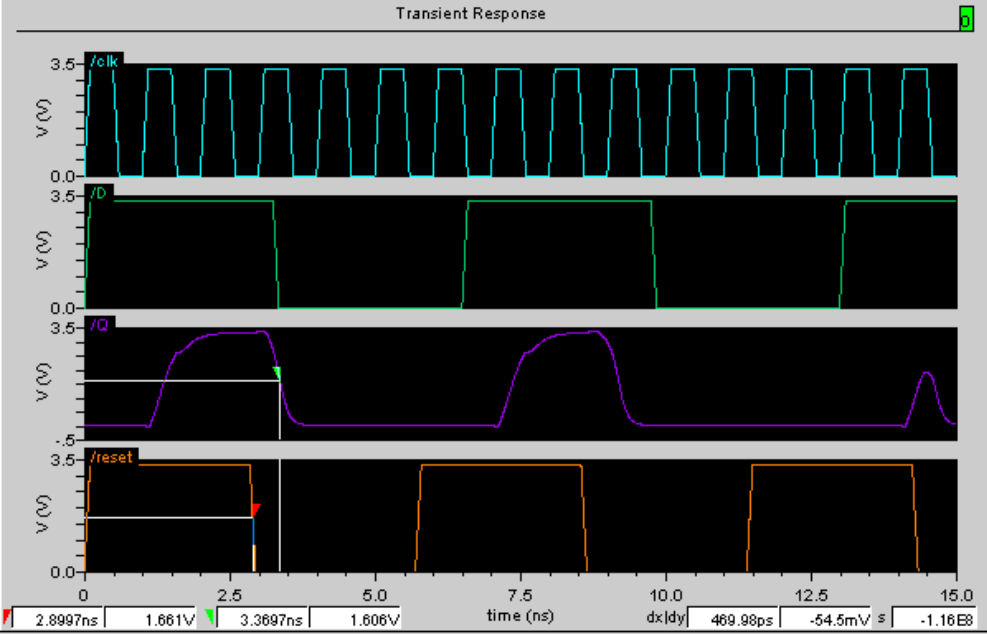

Figure 23: Functionality of Reset input in post layout.

The asynchronous Reset delay increased to around 470ps in post layout as seen in Fig23.
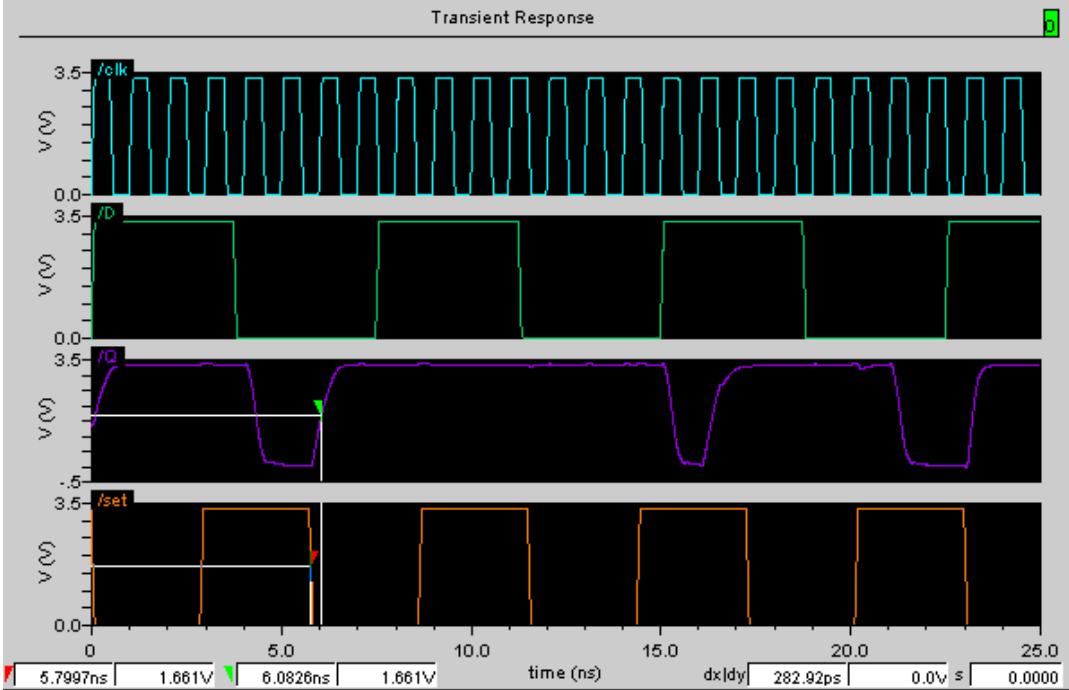

Figure 24: Figure 23: Functionality of Set input in post layout.

The asynchronous Reset delay increased to 282.92ps in post layout. Deviation between schematic value and post layout value is 5.12ps.
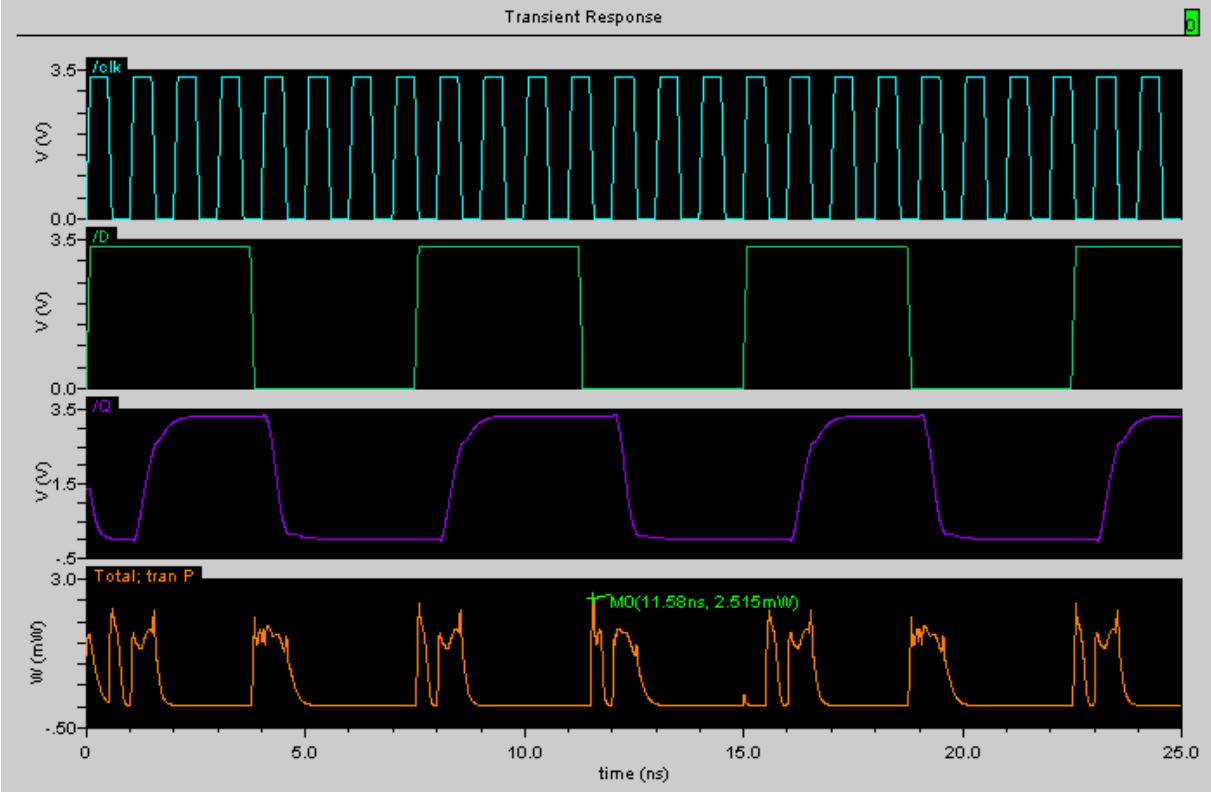

Figure 18: Total power dissipation of D flip flop in post layout.

As seen in Fig.18, most of the power is dissipated when output makes a transition at clock edges. Maximum instantaneous power dissipation is 2.515mW in post layout and root mean square of total power dissipated is 0.818mW.

3. CONCLUSION

	τ_{PHL}	τ_{PLH}	Rise Time	Fall Time	Power Dissipation(rms)
Schematic	**268.8ps**	**328.34ps**	**561.92ps**	**318.32ps**	**0.8mW**
Layout	**273.72ps**	**345.32**	**643.62ps**	**339.38ps**	**0.818mW**

In conclusion we managed to build a positive edge triggered D flip flop with low asserted set and reset inputs that works properly at 1GHz clock frequency. Rise and fall times of built flip flop can be improved by adding 2 cascade inverters to strengthen flip flop to drive 50fF capacitances better. However tradeoff of doing so is increased power dissipation and propagation delay. Another way to improve our flip flop is redesigning NAND2 gates with better rise time and propagation delays.