Birzeit University - Faculty of Information Technology
Computer Systems Engineering Department - ENCS234
Digital Systems - 1^{st} semester - 2012/13

HDL Project
Due: January 5, 2013

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We would like to design a 2-decade up/down BCD counter in HDL language using behavioral description. Since the counter is a 2-decade one, it is thus able to count from `00` to `99` and then back to `00`.

The counter has the following input control signals:

1. `Load` signal to load inputs in parallel.
2. `Up` signal so that the counter can count upwards.
3. `Down` signal so that the counter can count downwards

Note that the order of precedence for the 3 control signals defined above is `Load`, `Up` and `Down`.

To do

You are required to build a Quartus project in groups of 3 students per group and that responds to the above specifications. In case you need sequential elements in your design, you should choose *JK* flip-flops.

In addition to building the Quartus project, you need to write down one report for each group that includes the following items:

A. State diagram.

B. Design.

C. Verilog code.

D. Simulation results showing timing diagrams.

You should also create a test bench and test your design by executing and verifying the following sequence:

- `Up` signal is 1, `Load` and `Down` signals are both 0.
- `Down` signal is 1, `Load` and `Up` signals are both 0.
- `Down`, `Load` and `Up` signals are all 1.
- `Down`, `Load` and `Up` signals are all 0.

Your inputs and outputs should be defined as follows:

- I_3, I_2, I_1, I_0 are input signals for decade 1, I_7, I_6, I_5, I_4 are input signals for decade 2.
- `Load`, `Up`, `Down` are input control signals.
- A_3, A_2, A_1, A_0 are output signals of decade 1 and A_7, A_6, A_5, A_4 are output signals of decade 2.