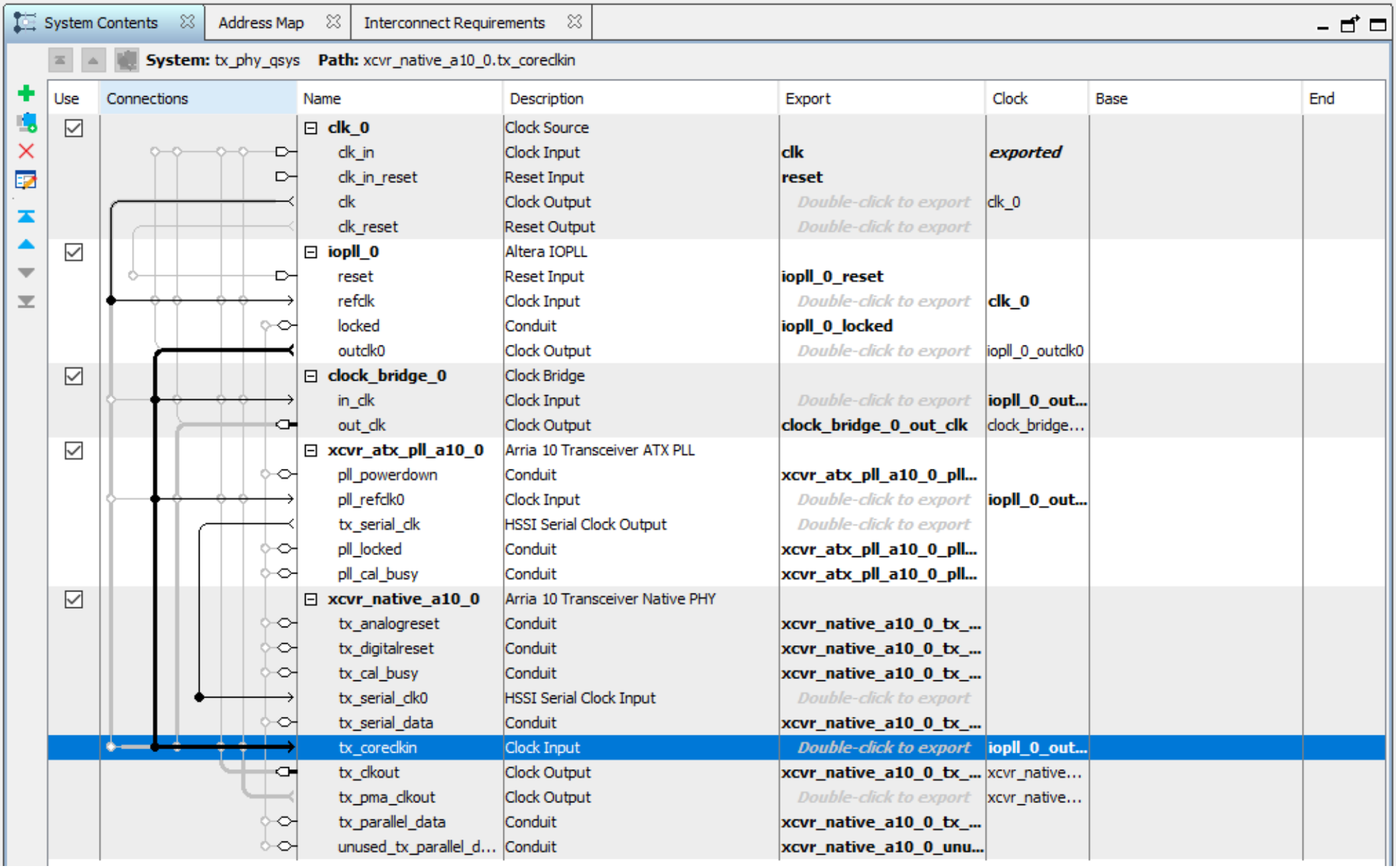
System Contents
Address Map
Interconnect Requirements
System: tx_phy_qsys Path: xcvr_native_a10_0.tx_coreclkin
Use
Connections
Name
Description
Export
Clock
Base
End
clk_0
Clock Source
clk_in
Clock Input
clk
exported
clk_in_reset
Reset Input
reset
clk
Clock Output
Double-click to export
clk_0
clk_reset
Reset Output
Double-click to export
iopll_0
Altera IOPLL
reset
Reset Input
iopll_0_reset
refclk
Clock Input
Double-click to export
clk_0
locked
Conduit
iopll_0_locked
outclk0
Clock Output
Double-click to export
iopll_0_outclk0
clock_bridge_0
Clock Bridge
in_clk
Clock Input
Double-click to export
iopll_0_out...
out_clk
Clock Output
clock_bridge_0_out_clk
clock_bridge...
xcvr_atx_pll_a10_0
Arria 10 Transceiver ATX PLL
pll_powerdown
Conduit
xcvr_atx_pll_a10_0_pll...
pll_refclk0
Clock Input
Double-click to export
iopll_0_out...
tx_serial_clk
HSSI Serial Clock Output
Double-click to export
pll_locked
Conduit
xcvr_atx_pll_a10_0_pll...
pll_cal_busy
Conduit
xcvr_atx_pll_a10_0_pll...
xcvr_native_a10_0
Arria 10 Transceiver Native PHY
tx_analogreset
Conduit
xcvr_native_a10_0_tx_...
tx_digitalreset
Conduit
xcvr_native_a10_0_tx_...
tx_cal_busy
Conduit
xcvr_native_a10_0_tx_...
tx_serial_clk0
HSSI Serial Clock Input
Double-click to export
tx_serial_data
Conduit
xcvr_native_a10_0_tx_...
tx_coreclkin
Clock Input
Double-click to export
iopll_0_out...
tx_clkout
Clock Output
xcvr_native_a10_0_tx_...
xcvr_native...
tx_pma_clkout
Clock Output
Double-click to export
xcvr_native...
tx_parallel_data
Conduit
xcvr_native_a10_0_tx_...
unused_tx_parallel_d...
Conduit
xcvr_native_a10_0_unu...