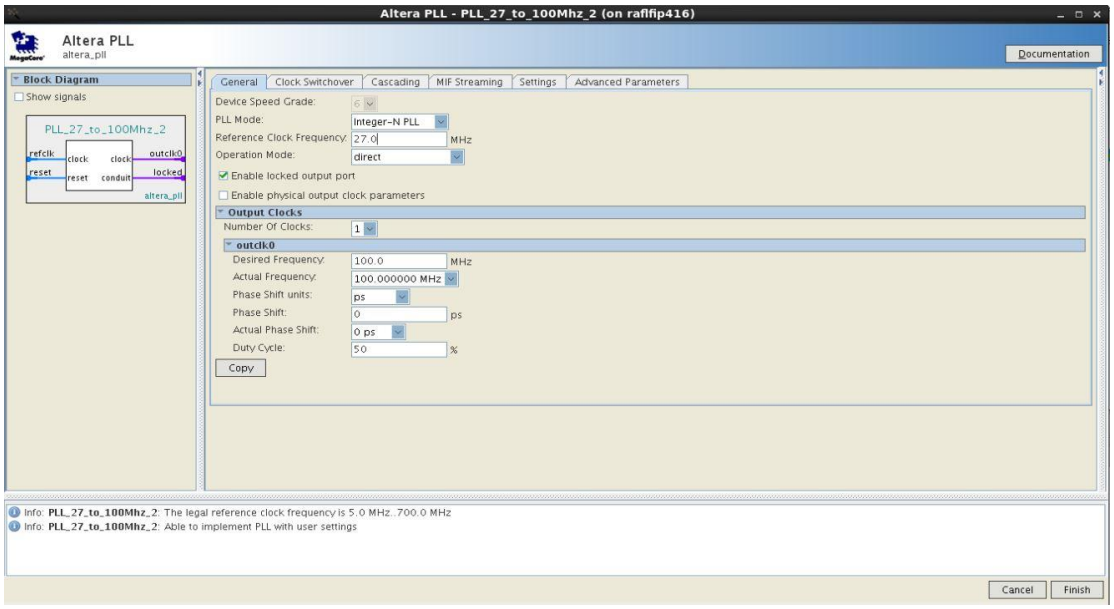
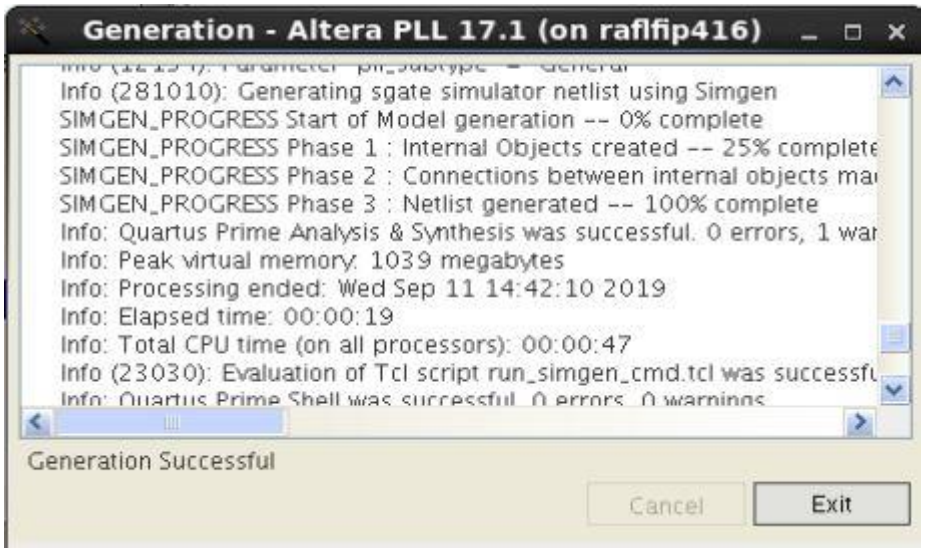
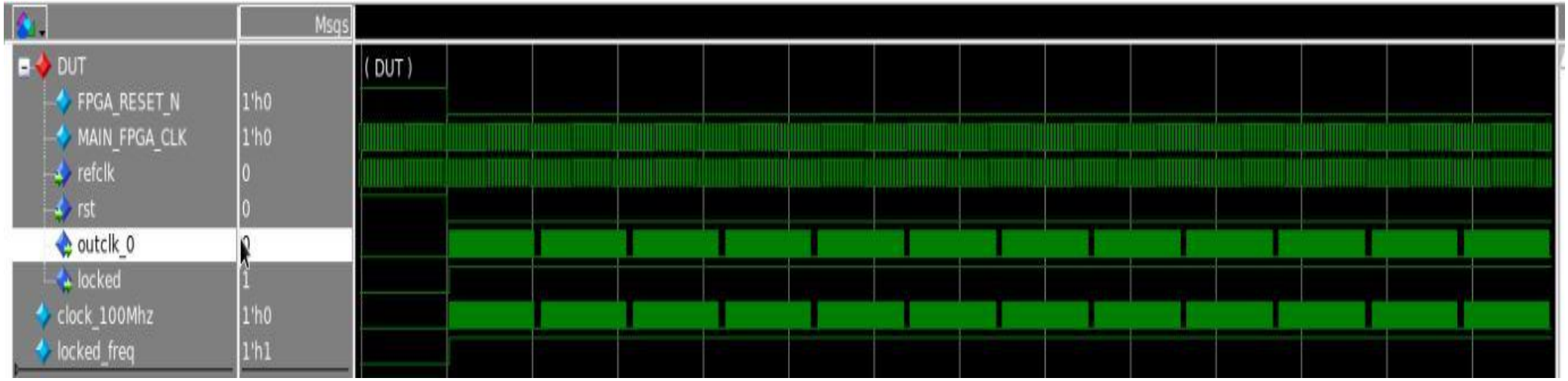
Pic No.1: **PLL setting**



Pic No.2:



Pic No.3**: the simulation of the PLL 27Mhz to 100Mhz**



The VHO FILE

```
IP Functional Simulation Model--
VERSION_BEGIN 17.1 cbx_mgl 2017:10:19:06:38:12:SJ cbx_simgen --
2017:10:19:05:46:40:SJ  VERSION_END


.Copyright (C) 2017  Intel Corporation. All rights reserved --
Your use of Intel Corporation's design tools, logic functions --
and other software and tools, and its AMPP partner logic --
functions, and any output files from any of the foregoing --
including device programming or simulation files), and any) --
associated documentation or information are expressly subject --
to the terms and conditions of the Intel Program License --
,Subscription Agreement, the Intel Quartus Prime License Agreement --
the Intel FPGA IP License Agreement, or other applicable license --
agreement, including, without limitation, that your use is for --
the sole purpose of programming logic devices manufactured by --
Intel and sold by Intel or its authorized distributors.  Please --
.refer to the applicable agreement for further details --

You may only use these simulation model output files for simulation --
purposes and expressly not for synthesis or any other purposes (in which --
.(event Intel disclaims all warranties of any kind --


synopsys translate_off--

;LIBRARY altera_lnsim
;USE altera_lnsim.altera_lnsim_components.all

synthesis_resources = altera_pll 1--
;LIBRARY ieee
;USE ieee.std_logic_1164.all

ENTITY  PLL_27_to_100Mhz_2 IS
PORT
)
;OUT  STD_LOGIC          : locked
;OUT  STD_LOGIC          :          outclk_0
;IN  STD_LOGIC          :   refclk
IN  STD_LOGIC          :       rst
;(
;END PLL_27_to_100Mhz_2

ARCHITECTURE RTL OF PLL_27_to_100Mhz_2 IS

;ATTRIBUTE synthesis_clearbox : natural
;ATTRIBUTE synthesis_clearbox OF RTL : ARCHITECTURE IS 1
;STD_LOGIC          :        SIGNAL  wire_gnd
: SIGNAL  wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_locked
;STD_LOGIC
```

```
: SIGNAL  wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_outclk
;(STD_LOGIC_VECTOR (0 DOWNTO 0
BEGIN

;'wire_gnd <= '0
;locked <= wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_locked
;(outclk_0 <= wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_outclk(0
pll_27_to_100mhz_2_altera_pll_altera_pll_i_639 :  altera_pll
) GENERIC MAP
,"c_cnt_bypass_en0 => "false
,"c_cnt_bypass_en1 => "false
,"c_cnt_bypass_en10 => "false
,"c_cnt_bypass_en11 => "false
,"c_cnt_bypass_en12 => "false
,"c_cnt_bypass_en13 => "false
,"c_cnt_bypass_en14 => "false
,"c_cnt_bypass_en15 => "false
,"c_cnt_bypass_en16 => "false
,"c_cnt_bypass_en17 => "false
,"c_cnt_bypass_en2 => "false
,"c_cnt_bypass_en3 => "false
,"c_cnt_bypass_en4 => "false
,"c_cnt_bypass_en5 => "false
,"c_cnt_bypass_en6 => "false
,"c_cnt_bypass_en7 => "false
,"c_cnt_bypass_en8 => "false
,"c_cnt_bypass_en9 => "false
,c_cnt_hi_div0 => 1
,c_cnt_hi_div1 => 1
,c_cnt_hi_div10 => 1
,c_cnt_hi_div11 => 1
,c_cnt_hi_div12 => 1
,c_cnt_hi_div13 => 1
,c_cnt_hi_div14 => 1
,c_cnt_hi_div15 => 1
,c_cnt_hi_div16 => 1
,c_cnt_hi_div17 => 1
,c_cnt_hi_div2 => 1
,c_cnt_hi_div3 => 1
,c_cnt_hi_div4 => 1
,c_cnt_hi_div5 => 1
,c_cnt_hi_div6 => 1
,c_cnt_hi_div7 => 1
,c_cnt_hi_div8 => 1
,c_cnt_hi_div9 => 1
,"c_cnt_in_src0 => "ph_mux_clk
,"c_cnt_in_src1 => "ph_mux_clk
,"c_cnt_in_src10 => "ph_mux_clk
,"c_cnt_in_src11 => "ph_mux_clk
,"c_cnt_in_src12 => "ph_mux_clk
,"c_cnt_in_src13 => "ph_mux_clk
,"c_cnt_in_src14 => "ph_mux_clk
```

,"c_cnt_in_src15 => "ph_mux_clk
,"c_cnt_in_src16 => "ph_mux_clk
,"c_cnt_in_src17 => "ph_mux_clk
,"c_cnt_in_src2 => "ph_mux_clk
,"c_cnt_in_src3 => "ph_mux_clk
,"c_cnt_in_src4 => "ph_mux_clk
,"c_cnt_in_src5 => "ph_mux_clk
,"c_cnt_in_src6 => "ph_mux_clk
,"c_cnt_in_src7 => "ph_mux_clk
,"c_cnt_in_src8 => "ph_mux_clk
,"c_cnt_in_src9 => "ph_mux_clk
,c_cnt_lo_div0 => 1
,c_cnt_lo_div1 => 1
,c_cnt_lo_div10 => 1
,c_cnt_lo_div11 => 1
,c_cnt_lo_div12 => 1
,c_cnt_lo_div13 => 1
,c_cnt_lo_div14 => 1
,c_cnt_lo_div15 => 1
,c_cnt_lo_div16 => 1
,c_cnt_lo_div17 => 1
,c_cnt_lo_div2 => 1
,c_cnt_lo_div3 => 1
,c_cnt_lo_div4 => 1
,c_cnt_lo_div5 => 1
,c_cnt_lo_div6 => 1
,c_cnt_lo_div7 => 1
,c_cnt_lo_div8 => 1
,c_cnt_lo_div9 => 1
,"c_cnt_odd_div_duty_en0 => "false
,"c_cnt_odd_div_duty_en1 => "false
,"c_cnt_odd_div_duty_en10 => "false
,"c_cnt_odd_div_duty_en11 => "false
,"c_cnt_odd_div_duty_en12 => "false
,"c_cnt_odd_div_duty_en13 => "false
,"c_cnt_odd_div_duty_en14 => "false
,"c_cnt_odd_div_duty_en15 => "false
,"c_cnt_odd_div_duty_en16 => "false
,"c_cnt_odd_div_duty_en17 => "false
,"c_cnt_odd_div_duty_en2 => "false
,"c_cnt_odd_div_duty_en3 => "false
,"c_cnt_odd_div_duty_en4 => "false
,"c_cnt_odd_div_duty_en5 => "false
,"c_cnt_odd_div_duty_en6 => "false
,"c_cnt_odd_div_duty_en7 => "false
,"c_cnt_odd_div_duty_en8 => "false
,"c_cnt_odd_div_duty_en9 => "false
,c_cnt_ph_mux_prst0 => 0
,c_cnt_ph_mux_prst1 => 0
,c_cnt_ph_mux_prst10 => 0
,c_cnt_ph_mux_prst11 => 0

```
,c_cnt_ph_mux_prst12 => 0
,c_cnt_ph_mux_prst13 => 0
,c_cnt_ph_mux_prst14 => 0
,c_cnt_ph_mux_prst15 => 0
,c_cnt_ph_mux_prst16 => 0
,c_cnt_ph_mux_prst17 => 0
,c_cnt_ph_mux_prst2 => 0
,c_cnt_ph_mux_prst3 => 0
,c_cnt_ph_mux_prst4 => 0
,c_cnt_ph_mux_prst5 => 0
,c_cnt_ph_mux_prst6 => 0
,c_cnt_ph_mux_prst7 => 0
,c_cnt_ph_mux_prst8 => 0
,c_cnt_ph_mux_prst9 => 0
,c_cnt_prst0 => 1
,c_cnt_prst1 => 1
,c_cnt_prst10 => 1
,c_cnt_prst11 => 1
,c_cnt_prst12 => 1
,c_cnt_prst13 => 1
,c_cnt_prst14 => 1
,c_cnt_prst15 => 1
,c_cnt_prst16 => 1
,c_cnt_prst17 => 1
,c_cnt_prst2 => 1
,c_cnt_prst3 => 1
,c_cnt_prst4 => 1
,c_cnt_prst5 => 1
,c_cnt_prst6 => 1
,c_cnt_prst7 => 1
,c_cnt_prst8 => 1
,c_cnt_prst9 => 1
,"clock_name_0 => "UNUSED
,"clock_name_1 => "UNUSED
,"clock_name_2 => "UNUSED
,"clock_name_3 => "UNUSED
,"clock_name_4 => "UNUSED
,"clock_name_5 => "UNUSED
,"clock_name_6 => "UNUSED
,"clock_name_7 => "UNUSED
,"clock_name_8 => "UNUSED
,"clock_name_global_0 => "false
,"clock_name_global_1 => "false
,"clock_name_global_2 => "false
,"clock_name_global_3 => "false
,"clock_name_global_4 => "false
,"clock_name_global_5 => "false
,"clock_name_global_6 => "false
,"clock_name_global_7 => "false
,"clock_name_global_8 => "false
,data_rate => 0
```

```
,deserialization_factor => 4
,duty_cycle0 => 50
,duty_cycle1 => 50
,duty_cycle10 => 50
,duty_cycle11 => 50
,duty_cycle12 => 50
,duty_cycle13 => 50
,duty_cycle14 => 50
,duty_cycle15 => 50
,duty_cycle16 => 50
,duty_cycle17 => 50
,duty_cycle2 => 50
,duty_cycle3 => 50
,duty_cycle4 => 50
,duty_cycle5 => 50
,duty_cycle6 => 50
,duty_cycle7 => 50
,duty_cycle8 => 50
,duty_cycle9 => 50
,"fractional_vco_multiplier => "false
,"m_cnt_bypass_en => "false
,m_cnt_hi_div => 1
,m_cnt_lo_div => 1
,"m_cnt_odd_div_duty_en => "false
,"mimic_fbclk_type => "gclk
,"n_cnt_bypass_en => "false
,n_cnt_hi_div => 1
,n_cnt_lo_div => 1
,"n_cnt_odd_div_duty_en => "false
,number_of_clocks => 1
,"operation_mode => "direct
,"output_clock_frequency0 => "100.000000 MHz
,"output_clock_frequency1 => "0 MHz
,"output_clock_frequency10 => "0 MHz
,"output_clock_frequency11 => "0 MHz
,"output_clock_frequency12 => "0 MHz
,"output_clock_frequency13 => "0 MHz
,"output_clock_frequency14 => "0 MHz
,"output_clock_frequency15 => "0 MHz
,"output_clock_frequency16 => "0 MHz
,"output_clock_frequency17 => "0 MHz
,"output_clock_frequency2 => "0 MHz
,"output_clock_frequency3 => "0 MHz
,"output_clock_frequency4 => "0 MHz
,"output_clock_frequency5 => "0 MHz
,"output_clock_frequency6 => "0 MHz
,"output_clock_frequency7 => "0 MHz
,"output_clock_frequency8 => "0 MHz
,"output_clock_frequency9 => "0 MHz
,"phase_shift0 => "0 ps
,"phase_shift1 => "0 ps
```

```
,"phase_shift10 => "0 ps
,"phase_shift11 => "0 ps
,"phase_shift12 => "0 ps
,"phase_shift13 => "0 ps
,"phase_shift14 => "0 ps
,"phase_shift15 => "0 ps
,"phase_shift16 => "0 ps
,"phase_shift17 => "0 ps
,"phase_shift2 => "0 ps
,"phase_shift3 => "0 ps
,"phase_shift4 => "0 ps
,"phase_shift5 => "0 ps
,"phase_shift6 => "0 ps
,"phase_shift7 => "0 ps
,"phase_shift8 => "0 ps
,"phase_shift9 => "0 ps
,"pll_auto_clk_sw_en => "false
,"pll_bw_sel => "low
,pll_bwctrl => 0
,"pll_clk_loss_sw_en => "false
,pll_clk_sw_dly => 0
,"pll_clkin_0_src => "clk_0
,"pll_clkin_1_src => "clk_0
,pll_cp_current => 0
,"pll_dsm_out_sel => "1st_order
,"pll_extclk_0_cnt_src => "pll_extclk_cnt_src_vss
,"pll_extclk_1_cnt_src => "pll_extclk_cnt_src_vss
,"pll_fbclk_mux_1 => "glb
,"pll_fbclk_mux_2 => "fb_1
,pll_fractional_cout => 24
,pll_fractional_division => 1
,"pll_m_cnt_in_src => "ph_mux_clk
,"pll_manu_clk_sw_en => "false
,"pll_output_clk_frequency => "0 MHz
,"pll_slf_rst => "false
,"pll_subtype => "General
,"pll_type => "General
,pll_vco_div => 1
,pll_vcoph_div => 1
,"refclk1_frequency => "0 MHz
,"reference_clock_frequency => "27.0 MHz
sim_additional_refclk_cycles_to_lock => 0
(
) PORT MAP
,fbclk => wire_gnd
,locked => wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_locked
,outclk => wire_pll_27_to_100mhz_2_altera_pll_altera_pll_i_639_outclk
,refclk => refclk
rst => rst
;(

END RTL; --PLL_27_to_100Mhz_2
```

synopsys translate_on--
VALID FILE--

The VHD file:

```
megafunction wizard: %Altera PLL v17.1% --
GENERATION: XML --
PLL_27_to_100Mhz_2.vhd --

Generated using ACDS version 17.1 590 --

;library IEEE
;use IEEE.std_logic_1164.all
;use IEEE.numeric_std.all

entity PLL_27_to_100Mhz_2 is
) port
refclk   : in  std_logic := '0'; --  refclk.clk
rst      : in  std_logic := '0'; --   reset.reset
outclk_0 : out std_logic;       -- outclk0.clk
locked   : out std_logic        --  locked.export
;(
;end entity PLL_27_to_100Mhz_2

architecture rtl of PLL_27_to_100Mhz_2 is
component PLL_27_to_100Mhz_2_0002 is
) port
refclk   : in  std_logic := 'X'; -- clk
rst      : in  std_logic := 'X'; -- reset
outclk_0 : out std_logic;       -- clk
locked   : out std_logic        -- export
;(
;end component PLL_27_to_100Mhz_2_0002

begin

pll_27_to_100mhz_2_inst : component PLL_27_to_100Mhz_2_0002
) port map
refclk   => refclk,   --  refclk.clk
rst      => rst,      --   reset.reset
outclk_0 => outclk_0, -- outclk0.clk
locked   => locked    --  locked.export
;(

end architecture rtl; -- of PLL_27_to_100Mhz_2
<?"Retrieval info: <?xml version="1.0 --
--!>--
Generated by Altera MegaWizard Launcher Utility version 1.0         --
************************************************************         --
!THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE         --
************************************************************         --
Copyright (C) 1991-2019 Altera Corporation         --
,(Any megafunction design, and related net list (encrypted or decrypted         --
support information, device programming or simulation file, and any other         --
associated documentation or information provided by Altera or a partner         --
```

under Altera's Megafunction Partnership Program may be used only to --
program PLD devices (but not masked PLD devices) from Altera. Any other --
use of such megafunction design, net list, support information, device --
programming or simulation file, or any other related documentation or --
information is prohibited for any other purpose, including, but not --
limited to modification, reverse engineering, de-compiling, or use with --
any other silicon devices, unless such use is explicitly licensed under --
a separate agreement with Altera or a megafunction partner. Title to --
,the intellectual property, including patents, copyrights, trademarks --
,trade secrets, or maskworks, embodied in any such megafunction design --
net list, support information, device programming or simulation file, or --
any other related documentation or information provided by Altera or a --
megafunction partner, remains with Altera, the megafunction partner, or --
their respective licensors. No other licenses, including any licenses --
.needed under any third party's intellectual property, are provided herein --
<----
< "Retrieval info: <instance entity-name="altera_pll" version="17.1 --
</ "<generic name="debug_print_output" value="false Retrieval info: --
</ "<generic name="debug_use_rbc_taf_method" value="false Retrieval info: --
</ "<generic name="device_family" value="Cyclone V Retrieval info: --
</ "<generic name="device" value="5CEBA2F17A7 Retrieval info: --
</ "<generic name="gui_device_speed_grade" value="1 Retrieval info: --
</ "<generic name="gui_pll_mode" value="Integer-N PLL Retrieval info: --
</ "<generic name="gui_reference_clock_frequency" value="27.0 Retrieval info: --
</ "<generic name="gui_channel_spacing" value="0.0 Retrieval info: --
</ "<generic name="gui_operation_mode" value="direct Retrieval info: --
</ "<generic name="gui_feedback_clock" value="Global Clock Retrieval info: --
</ "<generic name="gui_fractional_cout" value="32 Retrieval info: --
</ "<generic name="gui_dsm_out_sel" value="1st_order Retrieval info: --
</ "<generic name="gui_use_locked" value="true Retrieval info: --
</ "<generic name="gui_en_adv_params" value="false Retrieval info: --
</ "<generic name="gui_number_of_clocks" value="1 Retrieval info: --
</ "<generic name="gui_multiply_factor" value="1 Retrieval info: --
</ "<generic name="gui_frac_multiply_factor" value="1 Retrieval info: --
</ "<generic name="gui_divide_factor_n" value="1 Retrieval info: --
</ "<generic name="gui_cascade_counter0" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency0" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c0" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency0" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units0" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift0" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg0" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift0" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle0" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter1" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency1" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c1" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency1" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units1" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift1" value="0 Retrieval info: --

</ "<generic name="gui_phase_shift_deg1" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift1" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle1" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter2" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency2" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c2" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency2" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units2" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift2" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg2" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift2" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle2" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter3" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency3" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c3" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency3" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units3" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift3" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg3" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift3" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle3" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter4" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency4" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c4" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency4" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units4" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift4" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg4" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift4" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle4" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter5" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency5" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c5" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency5" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units5" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift5" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg5" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift5" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle5" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter6" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency6" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c6" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency6" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units6" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift6" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg6" value="0.0 Retrieval info: --

</ "<generic name="gui_actual_phase_shift6" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle6" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter7" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency7" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c7" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency7" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units7" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift7" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg7" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift7" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle7" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter8" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency8" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c8" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency8" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units8" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift8" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg8" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift8" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle8" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter9" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency9" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c9" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency9" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units9" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift9" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg9" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift9" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle9" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter10" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency10" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c10" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency10" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units10" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift10" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg10" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift10" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle10" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter11" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency11" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c11" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency11" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units11" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift11" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg11" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift11" value="0 Retrieval info: --

</ "<generic name="gui_duty_cycle11" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter12" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency12" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c12" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency12" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units12" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift12" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg12" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift12" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle12" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter13" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency13" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c13" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency13" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units13" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift13" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg13" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift13" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle13" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter14" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency14" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c14" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency14" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units14" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift14" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg14" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift14" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle14" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter15" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency15" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c15" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency15" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units15" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift15" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg15" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift15" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle15" value="50 Retrieval info: --
</ "<generic name="gui_cascade_counter16" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency16" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c16" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency16" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units16" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift16" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg16" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift16" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle16" value="50 Retrieval info: --

</ "<generic name="gui_cascade_counter17" value="false Retrieval info: --
</ "<generic name="gui_output_clock_frequency17" value="100.0 Retrieval info: --
</ "<generic name="gui_divide_factor_c17" value="1 Retrieval info: --
<generic name="gui_actual_output_clock_frequency17" value="0 Retrieval info: --
</ "MHz
</ "<generic name="gui_ps_units17" value="ps Retrieval info: --
</ "<generic name="gui_phase_shift17" value="0 Retrieval info: --
</ "<generic name="gui_phase_shift_deg17" value="0.0 Retrieval info: --
</ "<generic name="gui_actual_phase_shift17" value="0 Retrieval info: --
</ "<generic name="gui_duty_cycle17" value="50 Retrieval info: --
</ "<generic name="gui_pll_auto_reset" value="Off Retrieval info: --
</ "<generic name="gui_pll_bandwidth_preset" value="Auto Retrieval info: --
</ "<generic name="gui_en_reconf" value="false Retrieval info: --
</ "<generic name="gui_en_dps_ports" value="false Retrieval info: --
</ "<generic name="gui_en_phout_ports" value="false Retrieval info: --
</ "<generic name="gui_phout_division" value="1 Retrieval info: --
</ "<generic name="gui_mif_generate" value="false Retrieval info: --
</ "<generic name="gui_enable_mif_dps" value="false Retrieval info: --
</ "<generic name="gui_dps_cntr" value="C0 Retrieval info: --
</ "<generic name="gui_dps_num" value="1 Retrieval info: --
</ "<generic name="gui_dps_dir" value="Positive Retrieval info: --
</ "<generic name="gui_refclk_switch" value="false Retrieval info: --
</ "<generic name="gui_refclk1_frequency" value="100.0 Retrieval info: --
<generic name="gui_switchover_mode" value="Automatic Retrieval info: --
</ "Switchover
</ "<generic name="gui_switchover_delay" value="0 Retrieval info: --
</ "<generic name="gui_active_clk" value="false Retrieval info: --
</ "<generic name="gui_clk_bad" value="false Retrieval info: --
</ "<generic name="gui_enable_cascade_out" value="false Retrieval info: --
</ "<generic name="gui_cascade_outclk_index" value="0 Retrieval info: --
</ "<generic name="gui_enable_cascade_in" value="false Retrieval info: --
<generic name="gui_pll_cascading_mode" value="Create an Retrieval info: --
</ "adjpllin signal to connect with an upstream PLL
<Retrieval info: </instance --
IPFS_FILES : PLL_27_to_100Mhz_2.vho --
RELATED_FILES: PLL_27_to_100Mhz_2.vhd, PLL_27_to_100Mhz_2_0002.v --