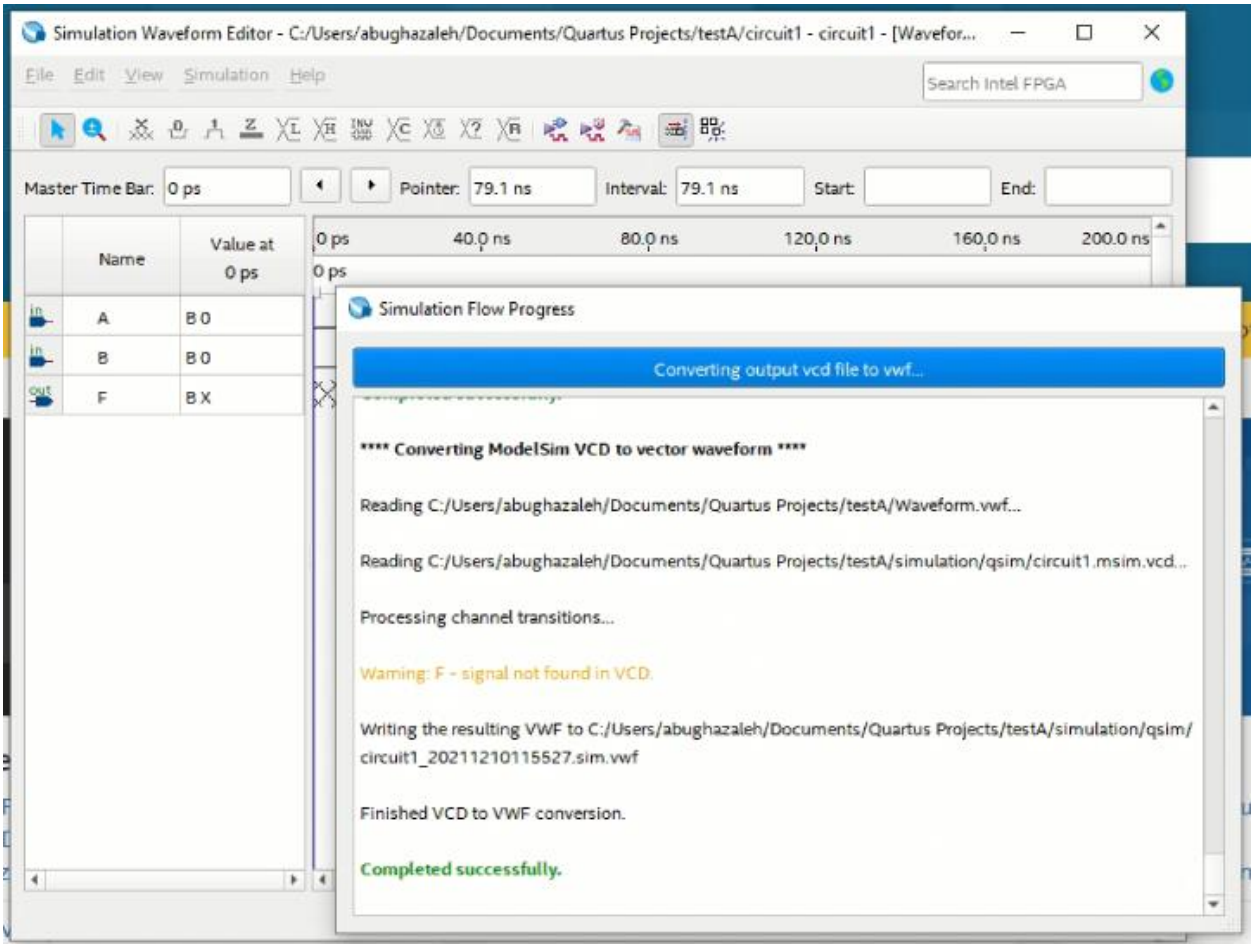
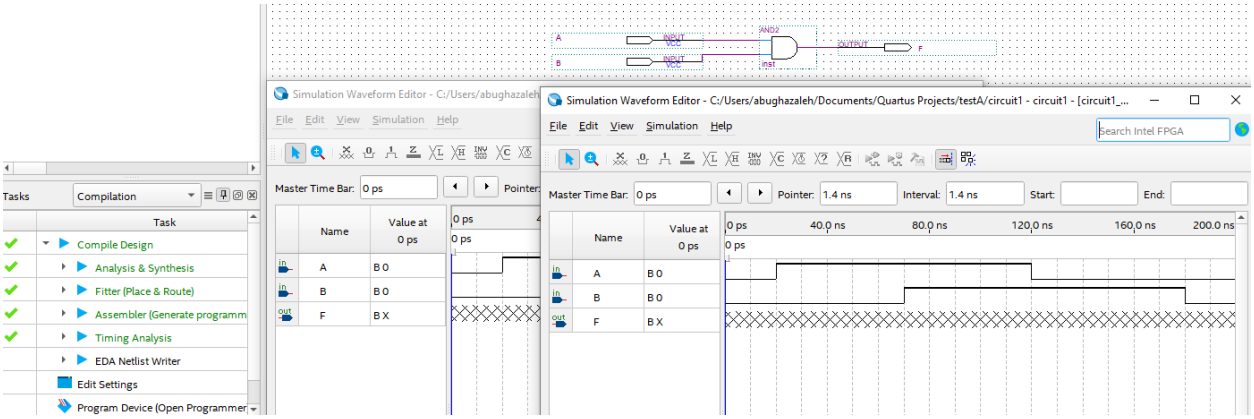

Simulation Waveform Editor - C:/Users/abughazaleh/Documents/Quartus Projects/testA/circuit1 - circuit1 - [Wavefor...
File Edit View Simulation Help
Search Intel FPGA
Master Time Bar: 0 ps
Pointer: 79.1 ns
Interval: 79.1 ns
Start:
End:
Name
Value at 0 ps
A
B 0
B
B 0
F
B X
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
Simulation Flow Progress
Converting output vcd file to vwf...
**** Converting ModelSim VCD to vector waveform ****
Reading C:/Users/abughazaleh/Documents/Quartus Projects/testA/Waveform.vwf...
Reading C:/Users/abughazaleh/Documents/Quartus Projects/testA/simulation/qsim/circuit1.msim.vcd...
Processing channel transitions...
Warning: F - signal not found in VCD.
Writing the resulting VWF to C:/Users/abughazaleh/Documents/Quartus Projects/testA/simulation/qsim/circuit1_20211210115527.sim.vwf
Finished VCD to VWF conversion.
Completed successfully.


Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer
Simulation Waveform Editor - C:/Users/abughazaleh/Documents/Quartus Projects/testA/circuit1 - circuit1 - [circuit1_...
Master Time Bar: 0 ps
Pointer: 1.4 ns
Interval: 1.4 ns
Start:
End:
Name
Value at 0 ps
A
B 0
B
B 0
F
B X
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns