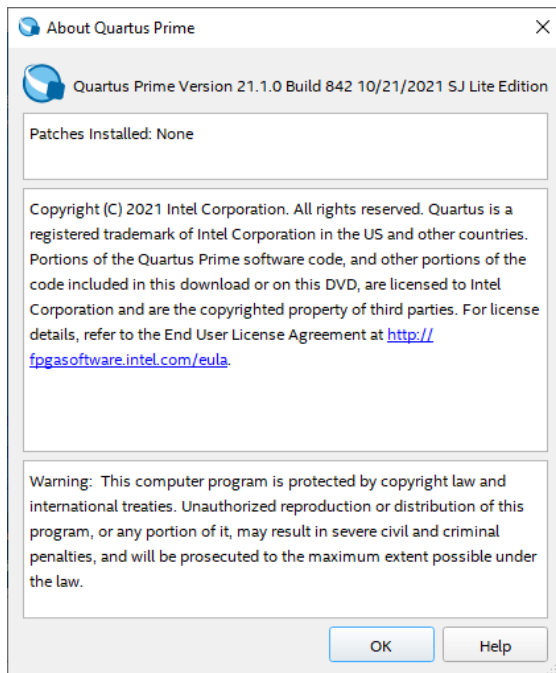
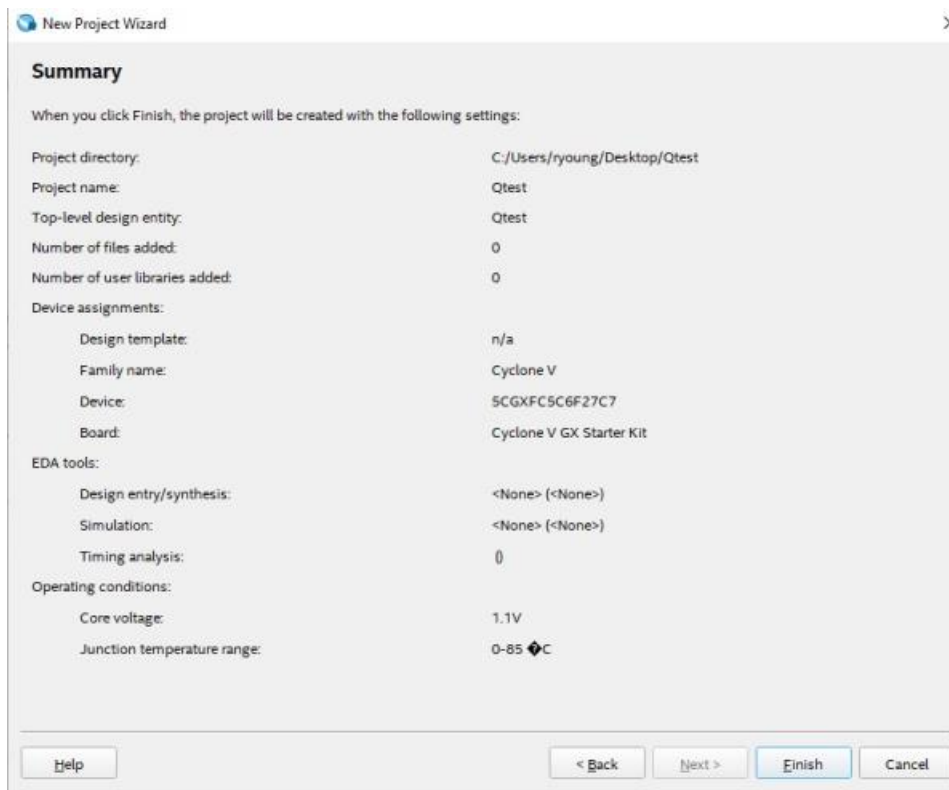


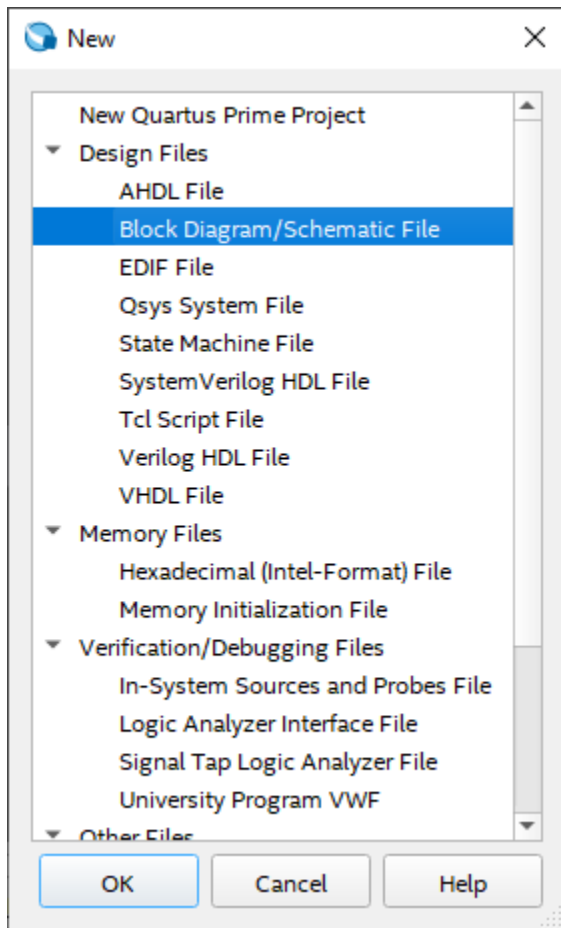
Quartus information:



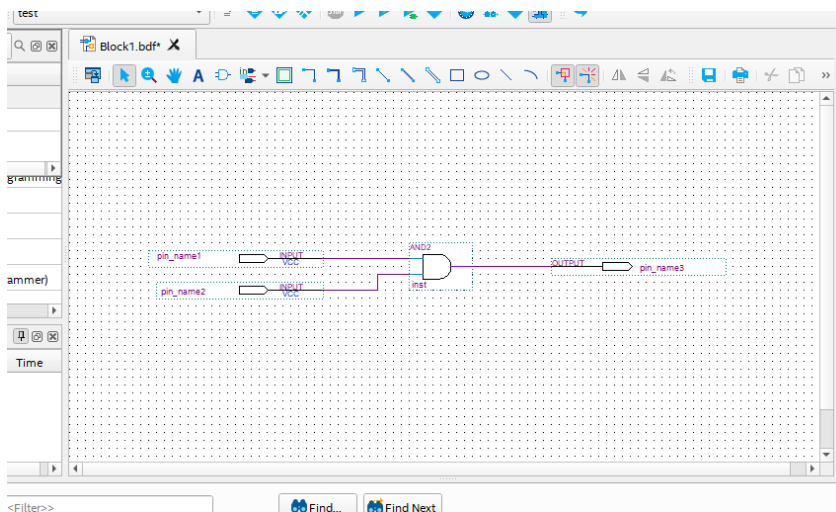
Set up information:



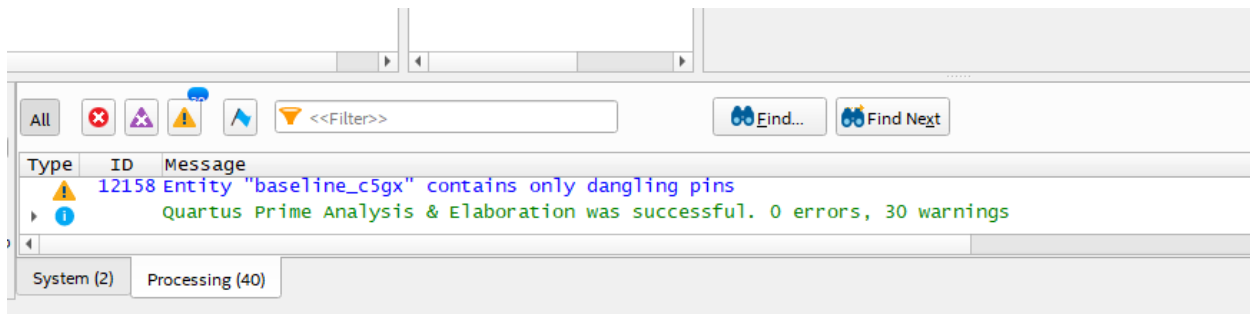
Select ok



Built circuit



Processing -> Start -> Start Analysis & Elaboration (Normally I don't do this, instead I just use Processing -> Start Compilation)



Assignments -> Pin Planner (This is where the problem is, I can't see the two inputs or the output.)

The screenshot shows the Pin Planner tool for a Cyclone V device (5CGXFC5C6F27C7). The interface includes a Groups panel on the left, a central Top View of the chip, a Pin Legend on the right, and a detailed pin assignment table at the bottom.

Pin Legend:

- User I/O (white circle)
- User assigned I/O (red circle)
- Fitter assigned I/O (green circle)
- Unbonded pad (grey circle)
- Reserved pin (purple circle)
- DEV_OE (E in a circle)
- DIFF_n (n in a circle)
- DIFF_p (p in a circle)
- DIFF_n output (n in a circle with a line)
- DIFF_p output (p in a circle with a line)
- DQ (Q in a circle)
- DQS (S in a circle)
- DOSB (B in a circle)

Pin Assignment Table:

| Node Name | Direction | Location | I/O Bank | VREF Group | I/O Standard | Reserved | Current Strength |
|-------------|-----------|----------|----------|------------|--------------|----------|------------------|
| ADC_CONVST | Output | PIN_AB22 | 4A | B4A_NO | 1.2 V | | 8mA (default) |
| ADC_SCK | Output | PIN_AA21 | 4A | B4A_NO | 1.2 V | | 8mA (default) |
| ADC_SDI | Output | PIN_Y10 | 3B | B3B_NO | 1.2 V | | 8mA (default) |
| ADC_SDO | Input | PIN_W10 | 3B | B3B_NO | 1.2 V | | 8mA (default) |
| AUD_ADCDAT | Input | PIN_D7 | 8A | B8A_NO | 2.5 V | | 12mA (default) |
| AUD_ADCLRCK | Bidir | PIN_C7 | 8A | B8A_NO | 2.5 V | | 12mA (default) |
| AUD_BCLK | Bidir | PIN_F6 | 8A | B8A_NO | 2.5 V | | 12mA (default) |

Processing -> Start Compilation (I thought I'd give this a try since this is what was used in QuartusII which worked in the past.)

Quartus Prime Lite Edition - C:/Users/ryoung/Desktop/Cyclone V/test - test

File Edit View Project Assignments Processing Tools Window Help

test

Project Navigator Hierarchy

Entity/Instance

Cyclone V: 5CGXFC5C6F27C7

baseline_c5gx

view report

Analysis & Elaboration

Partition Merge

Netlist Viewers

Design Assistant (Post-Mapping)

Status

| Module | % | Progress |
|----------------------|------|----------|
| Full Compilation | 100% | 00:01:03 |
| Analysis & Synthesis | 100% | 00:00:00 |
| Fitter | 100% | 00:00:00 |
| Assembler | 100% | 00:00:00 |

Table of Contents

Flow Summary

Flow Status: Successful - Tue May 17 15:08:39 2022

Quartus Prime Version: 21.1.0 Build 842 10/21/2021 SJ Lite Edition

Revision Name: test

Top-level Entity Name: baseline_c5gx

Family: Cyclone V

Device: 5CGXFC5C6F27C7

Timing Models: Final

Logic utilization (in ALMs): 1 / 29,080 (< 1 %)

Total registers: 0

Total pins: 237 / 364 (65 %)

Total virtual pins: 0

Total block memory bits: 0 / 4,567,040 (0 %)

Total DSP Blocks: 0 / 150 (0 %)

Total HSSI RX PCs: 0 / 6 (0 %)

Total HSSI PMA RX Deserializers: 0 / 6 (0 %)

Total HSSI TX PCs: 0 / 6 (0 %)

Total HSSI PMA TX Serializers: 0 / 6 (0 %)

Total PLLs: 0 / 12 (0 %)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

- Basic Functions
- DSP
- Interface Protocols
- Memory Interfaces and Controllers
- Processors and Peripherals
- University Program

Search for Partner IP

Messages

Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings

293000 Quartus Prime Full compilation was successful. 0 errors, 393 warnings

System (3) Processing (164)

3,76 100% 00:01:03

Assignments -> Pin Planner

Pin Planner - C:/Users/ryoung/Desktop/Cyclone V/test - test

File Edit View Processing Tools Window Help

Search Intel FPGA

Groups

Named: *

| Node Name | Direction |
|------------------|--------------|
| HDMI_TX_D[23..0] | Output Group |
| HEX0[6..0] | Output Group |
| HEX1[6..0] | Output Group |
| HEX2[6..0] | Output Group |

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...

Top View - Wire Bond

Cyclone V - 5CGXFC5C6F27C7

Pin Legend

| Symbol | Pin Type |
|--------|---------------------|
| ○ | User I/O |
| ● | User assigned I/O |
| ● | Fitter assigned I/O |
| ○ | Unbonded pad |
| ● | Reserved pin |
| E | DEV_OE |
| n | DIFF_n |
| p | DIFF_p |
| n | DIFF_n output |
| p | DIFF_p output |
| Q | DQ |
| S | DQS |
| DSB | DOSB |

| Node Name | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard | Reserved |
|-------------|-----------|----------|----------|------------|-----------------|--------------|----------|
| ADC_CONVST | Output | PIN_AB22 | 4A | B4A_NO | PIN_AB22 | 1.2 V | 8i |
| ADC_SCK | Output | PIN_AA21 | 4A | B4A_NO | PIN_AA21 | 1.2 V | 8i |
| ADC_SDI | Output | PIN_Y10 | 3B | B3B_NO | PIN_Y10 | 1.2 V | 8i |
| ADC_SDO | Input | PIN_W10 | 3B | B3B_NO | PIN_W10 | 1.2 V | 8i |
| AUD_ADCDAT | Input | PIN_D7 | 8A | B8A_NO | PIN_D7 | 2.5 V | 1i |
| AUD_ADCLRCK | Bidir | PIN_C7 | 8A | B8A_NO | PIN_C7 | 2.5 V | 1i |
| AUD_BCLK | Bidir | PIN_F6 | 8A | B8A_NO | PIN_F6 | 2.5 V | 1i |

Filter: Pins: all

0% 00:00:00

I scrolled throught the Node Name list and did not find the inputs or output listed.